

SNx4HC166 8 ビット、パラレルロード・シフト・レジスタ

1 特長

- 幅広い動作電圧範囲: 2V~6V
- 出力は最大 10 個の LSTTL 負荷を駆動可能
- 低消費電力、 I_{CC} : 80 μ A 以下
- $t_{pd} = 13$ ns (標準値)
- 5V で ± 4 mA の出力駆動能力
- 低い入力電流: 最大 1 μ A
- 同期ロード
- ダイレクト・オーバーライドのクリア
- パラレルからシリアルへの変換

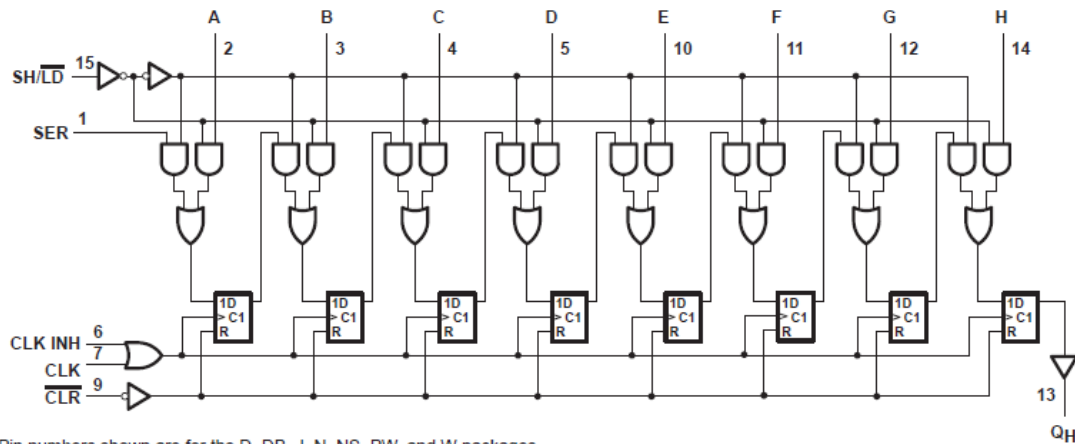
2 概要

SNx4HC166 デバイスは、1 つのシリアル入力と 8 つのパラレルロード入力を備えた 8 ビット・シフト・レジスタを内蔵しています。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
SN74HC166D	SOIC (16)	9.90mm × 3.90mm
SN74HC166DB	SSOP (16)	6.20mm × 5.30mm
SN74HC166N	PDIP (16)	19.31mm × 6.35mm
SN74HC166NS	SO (16)	6.20mm × 5.30mm
SN74HC166PW	TSSOP (16)	5.00mm × 4.40mm
SN54HC166J	CDIP (16)	24.38mm × 6.92mm
SNJ54HC166FK	LCCC (20)	8.89mm × 8.45mm
SNJ54HC166J	CFP (16)	10.16mm × 6.73mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

機能ブロック図



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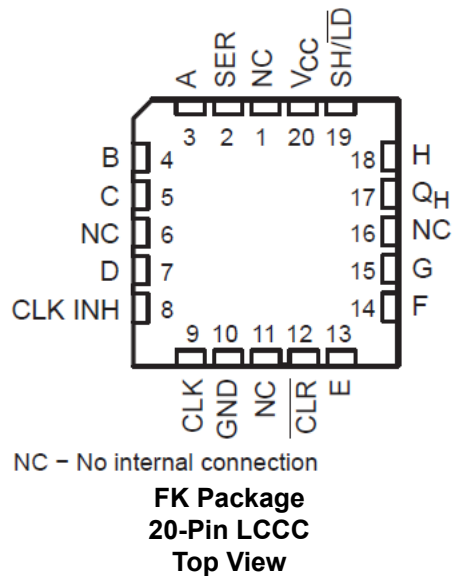
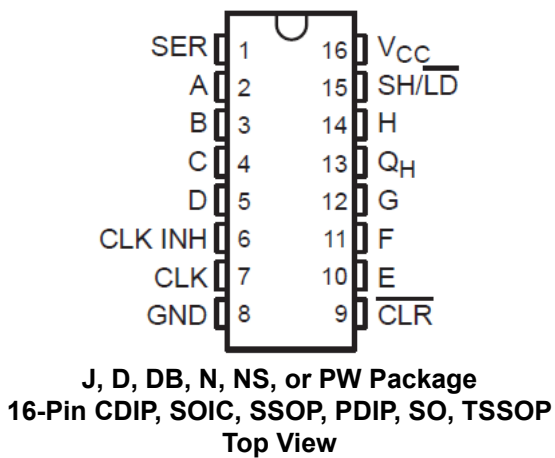
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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (December 1982) to Revision E (February 2022)	Page
• 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新.....	1

4 Pin Configuration and Functions



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		–0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0 or V _I > V _{CC}		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0 or V _O > V _{CC}		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under セクション 5.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			SN54HC166			SN74HC166			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5			1.5			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 6 V	4.2			4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.5			0.5	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 6 V			1.8			1.8	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv ⁽²⁾	Input transition rise/fall time	V _{CC} = 2 V			1000			1000	ns
		V _{CC} = 4.5 V			500			500	
		V _{CC} = 6 V			400			400	
T _A	Operating free-air temperature		–55		125	–40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) If this device is used in the threshold region (from V_{IL} max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_I = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

5.3 Thermal Information

		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
THERMAL METRIC		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	73	82	67	64	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	T _A = 25°C			SN54HC166		SN74HC166		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -20 µA	2	1.9	1.998		1.9		1.9		V
		4.5	4.4	4.499		4.4		4.4		
		6	5.9	5.999		5.9		5.9		
	I _{OH} = -4 mA	4.5	3.98	4.3		3.7		3.84		
	I _{OH} = -5.2 mA	6	5.48	5.8		5.2		5.34		
V _{OL}	I _{OL} = 20 µA	2		0.002	0.1		0.1		0.1	V
		4.5		0.001	0.1		0.1		0.1	
		6		0.001	0.1		0.1		0.1	
	I _{OL} = 4 mA	4.5		0.17	0.26		0.4		0.33	
	I _{OL} = 5.2 mA	6		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0	6		±0.1	±100		±1000		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6			8		160		80	µA
C _i		2 to 6		3	10		10		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC} (V)	T _A = 25°C		SN54HC166		SN74HC166		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		2	6		4.2		5		MHz
			4.5	31		21		25		
			6	36		25		29		
t _w	Pulse duration	CLR low	2	100		150		125		ns
			4.5	20		30		25		
			6	17		26		21		
		CLK high or low	2	80		120		100		
			4.5	16		24		20		
			6	14		20		17		
t _{su}	Setup time	SH/LD high before CLK ↑	2	145		220		180		ns
			4.5	29		44		36		
			6	25		38		31		
		SER before CLK ↑	2	80		120		100		
			4.5	16		24		20		
			6	14		20		17		
		CLK INH low before CLK- ↑	2	100		150		125		
			4.5	20		30		25		
			6	17		26		21		
		Data before CLK ↑	2	80		120		100		
			4.5	16		24		20		
			6	14		20		17		
		CLR inactive before CLK ↑	2	40		60		50		
			4.5	8		12		10		
			6	7		10		9		
t _h	Hold time	SH/LD high after CLK ↑	2	0		0		0		ns
			4.5	0		0		0		
			6	0		0		0		
		SER after CLK ↑	2	5		5		5		
			4.5	5		5		5		
			6	5		5		5		
		CLK INH high after CLK ↑	2	0		0		0		
			4.5	0		0		0		
			6	0		0		0		
		Data after CLK ↑	2	5		5		5		
			4.5	5		5		5		
			6	5		5		5		

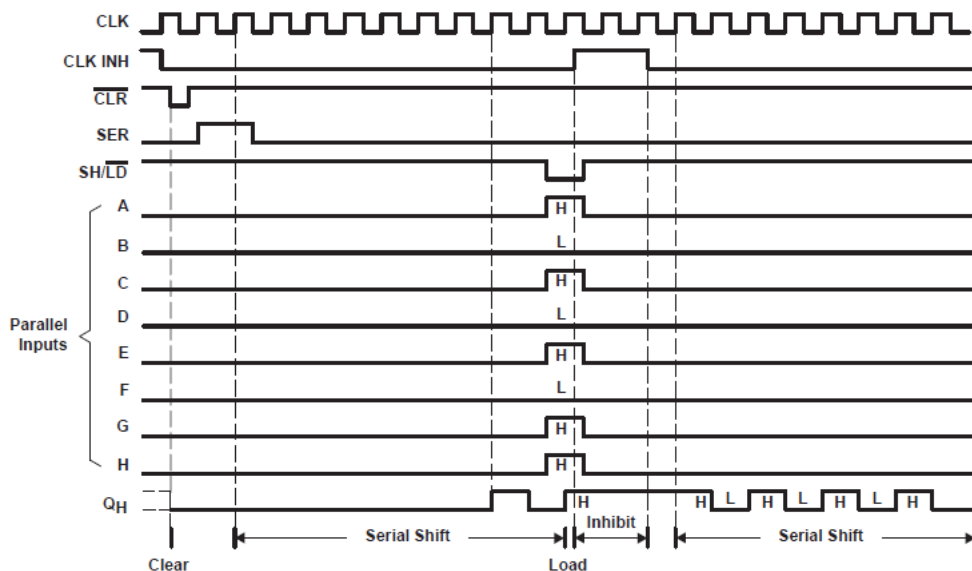


FIG 5-1. Typical Clear, Shift, Load, Inhibit, and Shift Sequence

5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	$T_A = 25^\circ\text{C}$			SN54HC166		SN74HC166		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			2	6	11		4.2		5		MHz
			4.5	31	36		21		25		
			6	36	45		25		29		
t_{PHL}	$\overline{\text{CLR}}$	Q_H	2		62	120		180		150	ns
			4.5		18	24		36		30	
			6		13	20		31		26	
t_{pd}	CLK	Q_H	2		75	150		225		190	ns
			4.5		15	30		45		38	
			6		13	26		38		32	
t_t		Any	2		38	75		110		95	ns
			4.5		8	15		22		19	
			6		6	13		19		16	

5.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

6 Parameter Measurement Information

t_{pd} is the maximum between t_{PLH} and t_{PHL}

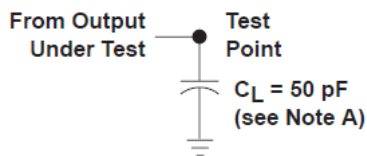


FIG 6-1. Load Circuit

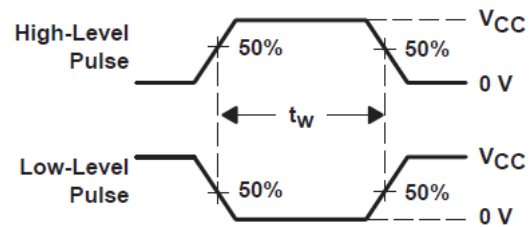


FIG 6-2. Voltage Waveforms Pulse Durations

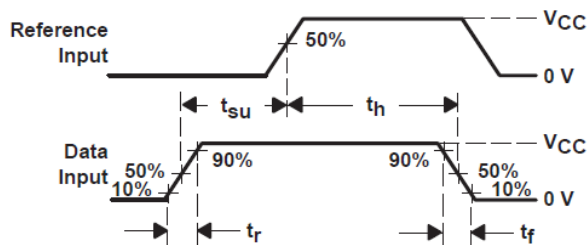


FIG 6-3. Voltage Waveforms Setup and Hold and Input Rise and Fall Times

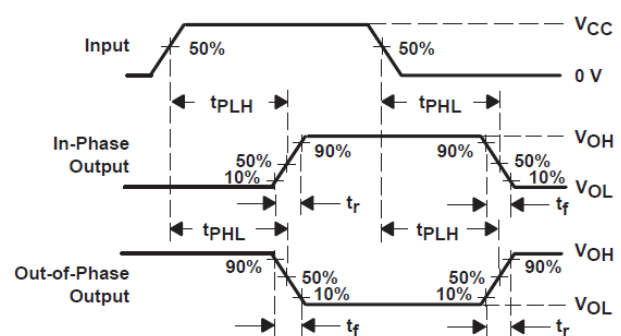


FIG 6-4. Voltage Waveforms Propagation Delay and Output Transition Times

A. C_L includes probe and jig capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.

C. For clock inputs, f_{max} is measured when the input duty cycle is 50%

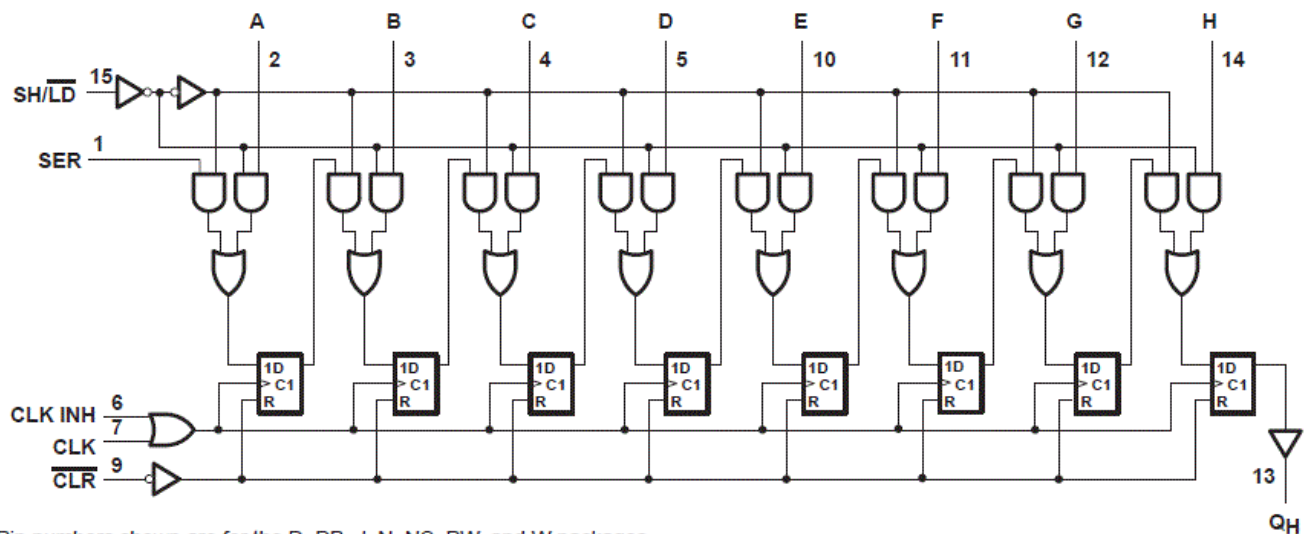
D. The outputs are measured one at a time with one input transition per measurement.

7 Detailed Description

7.1 Overview

These parallel-in or serial-in, serial-out registers feature gated clock (CLK, CLK INH) inputs and an overriding clear ($\overline{\text{CLR}}$) input. The parallel-in or serial-in modes are established by the shift/load ($\text{SH}/\overline{\text{LD}}$) input. When high, $\text{SH}/\overline{\text{LD}}$ enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of CLK through a 2-input positive-NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. CLK INH should be changed to the high level only when CLK is high. $\overline{\text{CLR}}$ overrides all other inputs, including CLK, and resets all flip-flops to zero.

7.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

7.3 Device Functional Modes

表 7-1. Function Table

INPUTS						OUTPUTS		
$\overline{\text{CLR}}$	$\text{SH}/\overline{\text{LD}}$	CLK INH	CLK	SER	PARALLEL A...H	INTERNAL		Q_H
						Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	$\uparrow$	X	a...h	a	b	h
H	H	L	$\uparrow$	H	X	H	Q_{An}	Q_{Gn}
H	H	L	$\uparrow$	L	X	L	Q_{An}	Q_{Gn}
H	X	H	$\uparrow$	X	X	Q_{A0}	Q_{B0}	Q_{H0}

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9050101Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9050101Q2A SNJ54HC 166FK
5962-9050101QEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101QE A SNJ54HC166J
5962-9050101VEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101VE A SNV54HC166J
5962-9050101VEA.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101VE A SNV54HC166J
SN54HC166J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC166J
SN54HC166J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC166J
SN74HC166D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	HC166
SN74HC166DBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC166
SN74HC166DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC166
SN74HC166DRE4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DRG4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC166
SN74HC166N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC166N
SN74HC166N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74HC166N
SN74HC166NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC166
SN74HC166PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	HC166
SN74HC166PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC166
SN74HC166PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC166PWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC166
SN74HC166PWT	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	HC166
SN74HCS166DYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS166
SN74HCS166DYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS166
SNJ54HC166FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9050101Q2A SNJ54HC 166FK
SNJ54HC166FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9050101Q2A SNJ54HC 166FK
SNJ54HC166J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101QE A SNJ54HC166J
SNJ54HC166J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101QE A SNJ54HC166J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

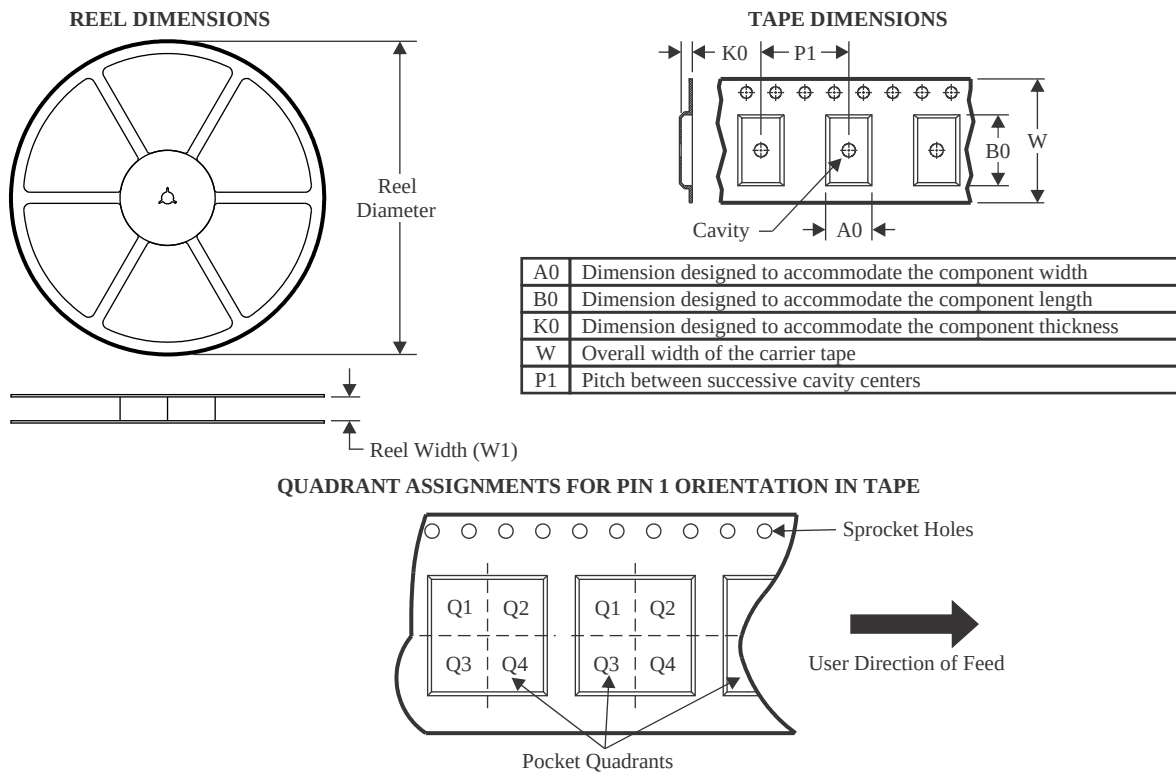
OTHER QUALIFIED VERSIONS OF SN54HC166, SN54HC166-SP, SN74HC166 :

- Catalog : [SN74HC166](#), [SN54HC166](#)
- Military : [SN54HC166](#)
- Space : [SN54HC166-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

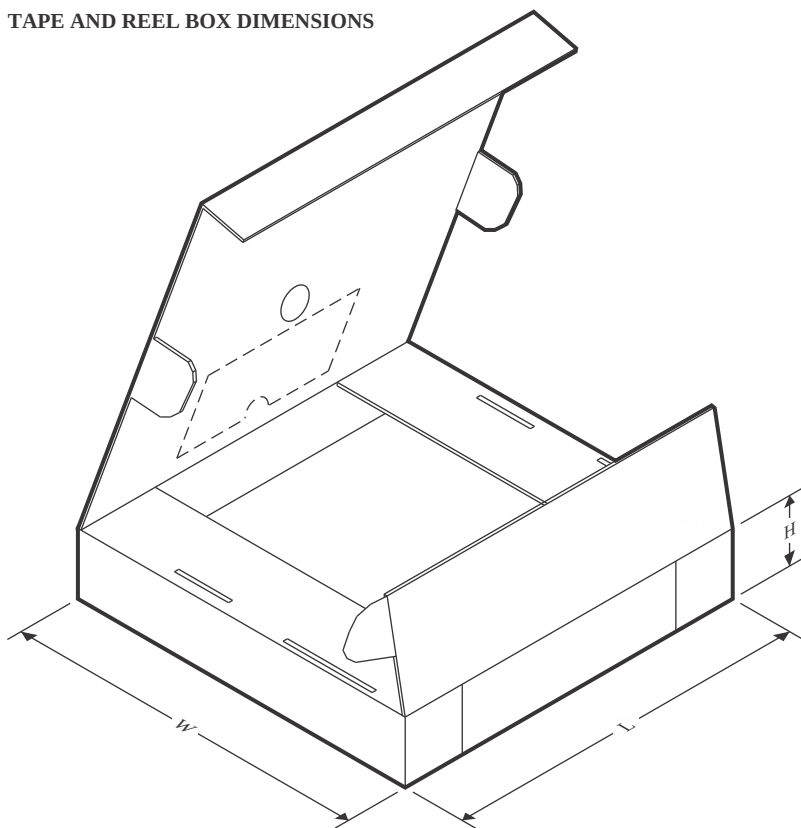
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC166DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC166DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC166DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC166DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC166NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC166NSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC166PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC166PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS166DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



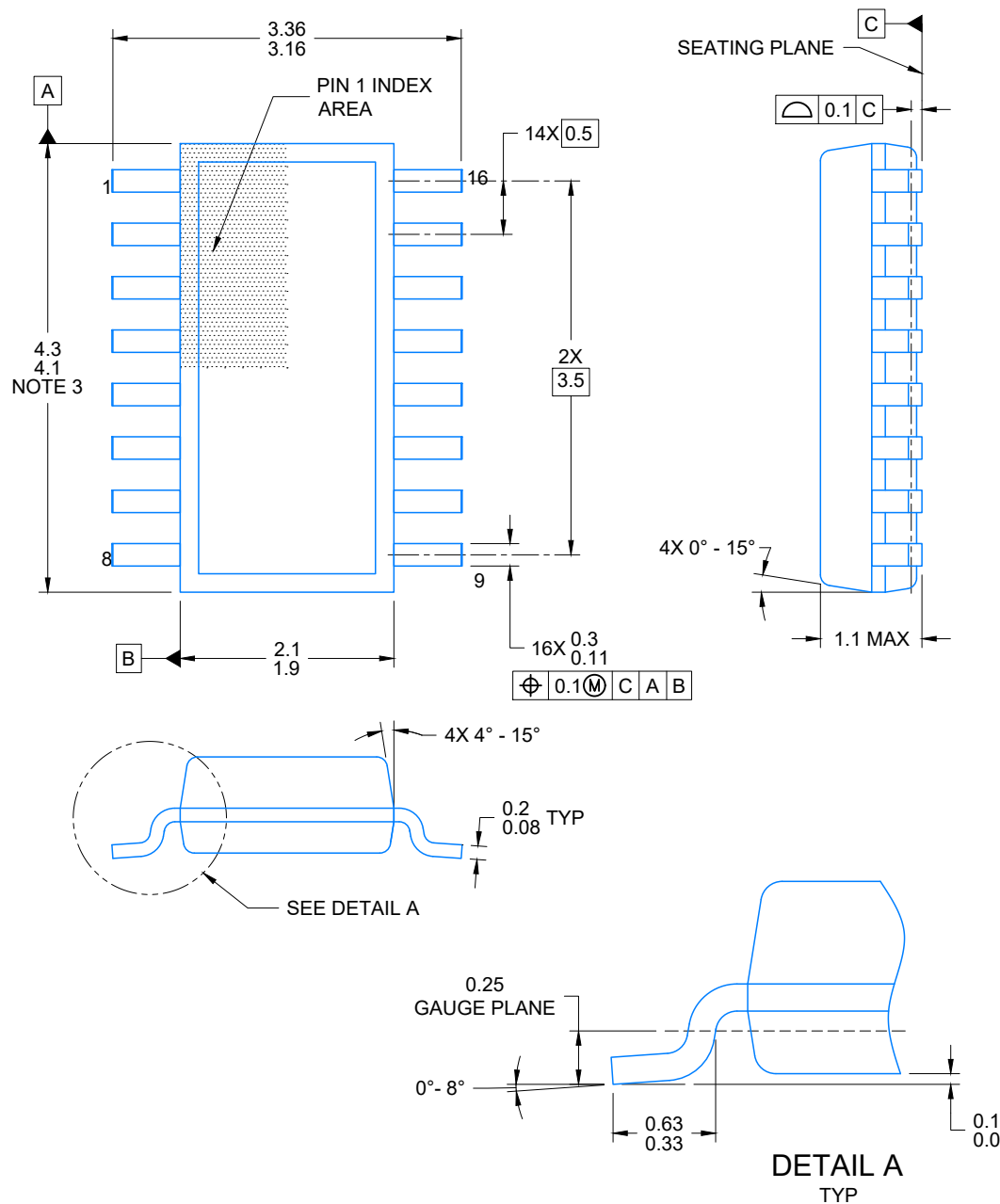
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC166DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HC166DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC166DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC166DRG4	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC166NSR	SOP	NS	16	2000	367.0	367.0	38.0
SN74HC166NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74HC166PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC166PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HCS166DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8

TUBE


*All dimensions are nominal

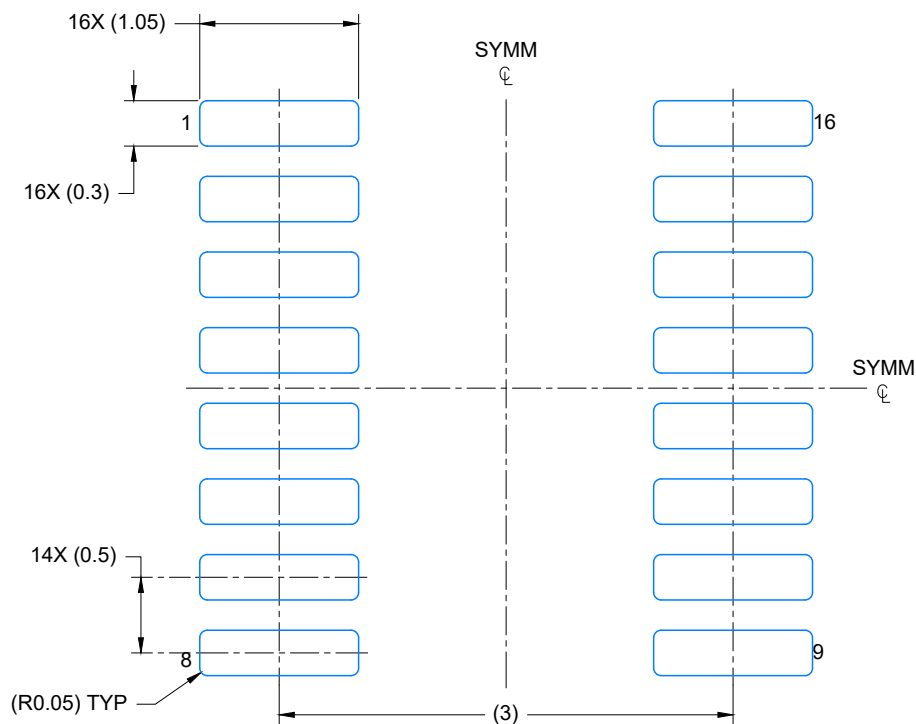
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9050101Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC166N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC166N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC166N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC166N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC166FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC166FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA



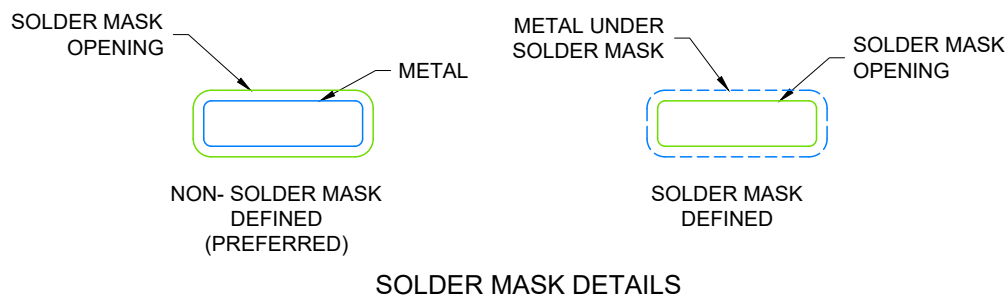
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



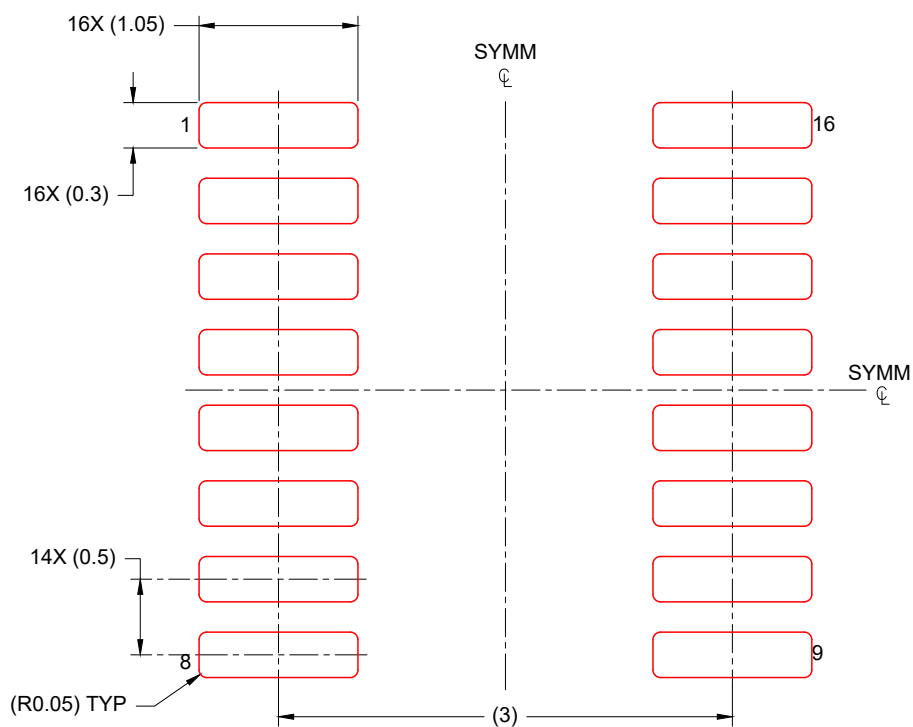
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

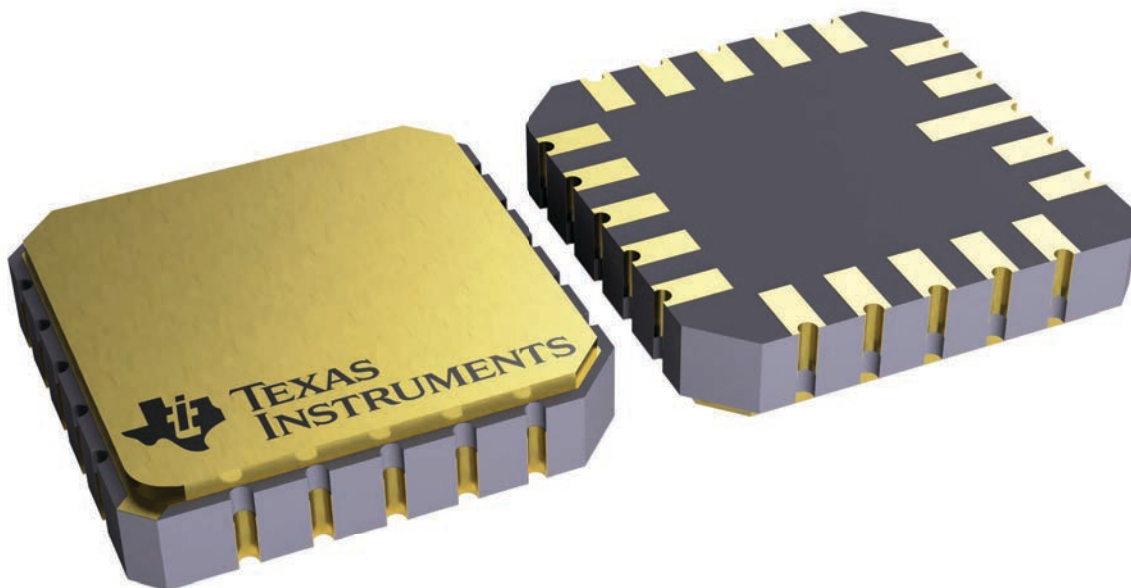
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

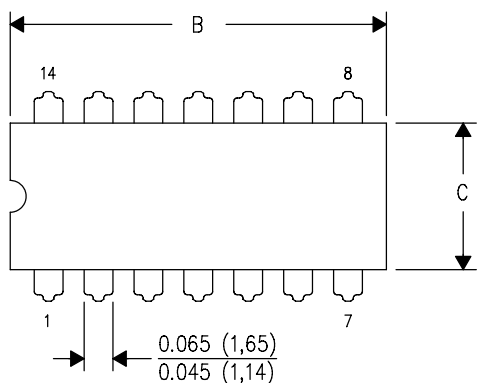


4229370VA\

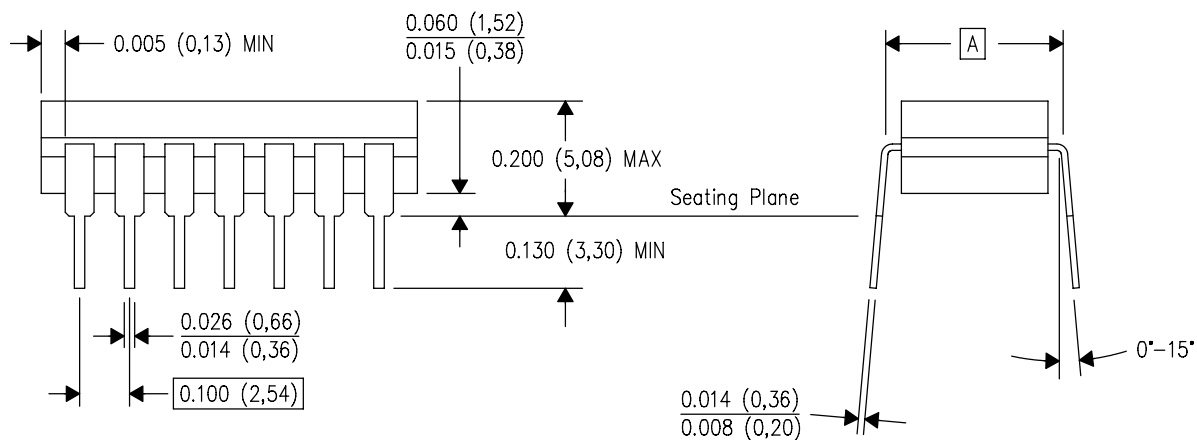
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



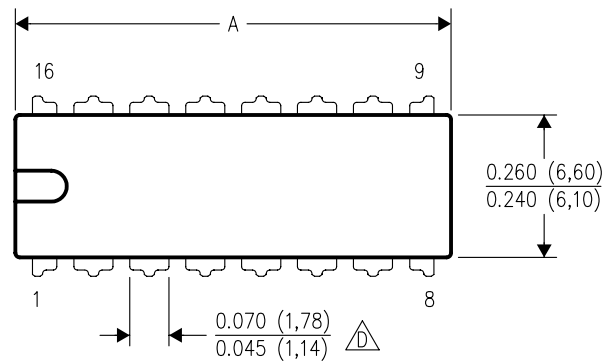
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

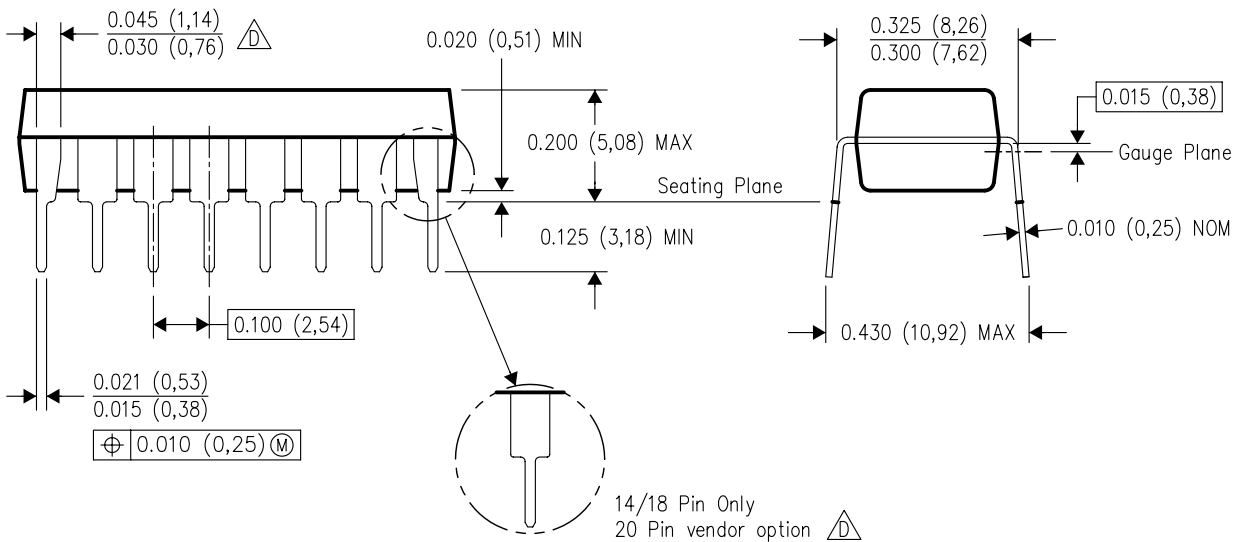
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

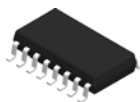


PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

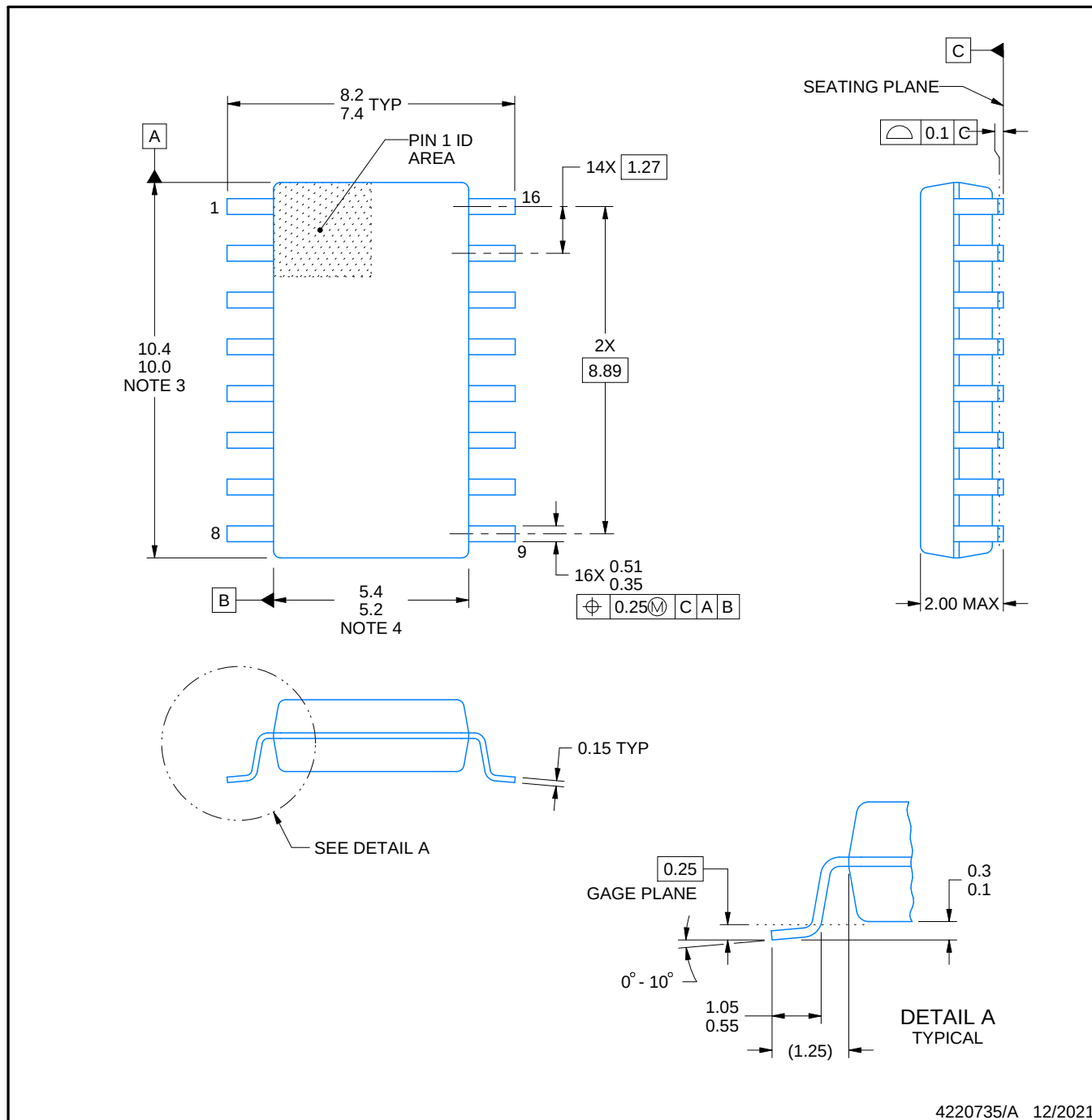


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

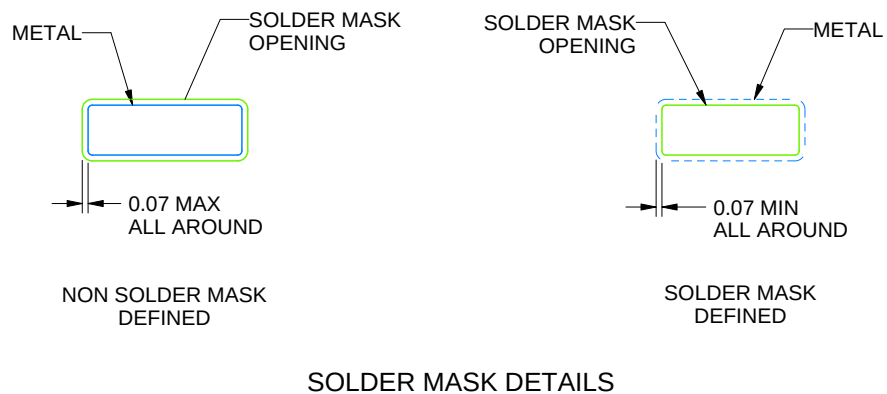
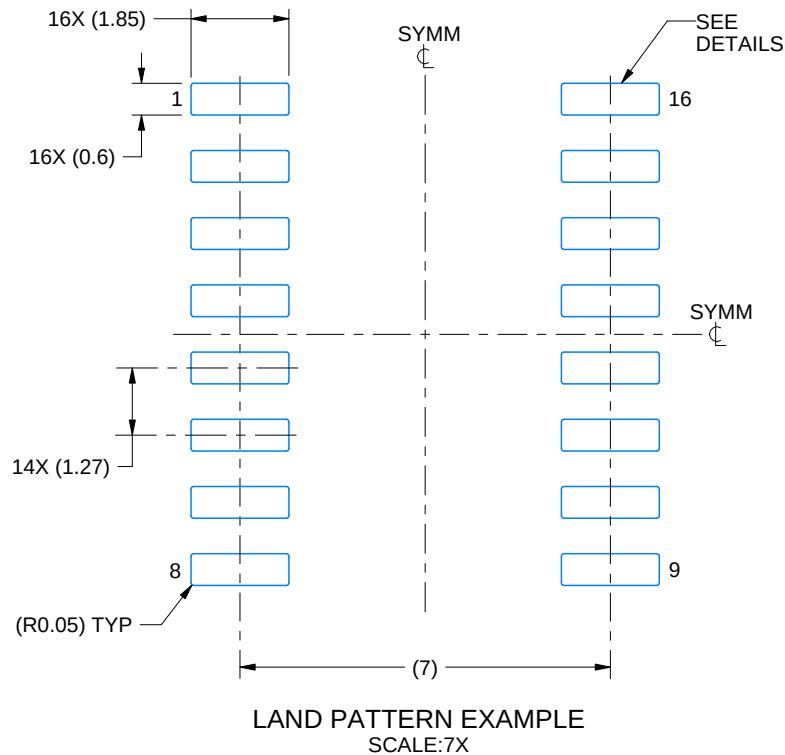
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP

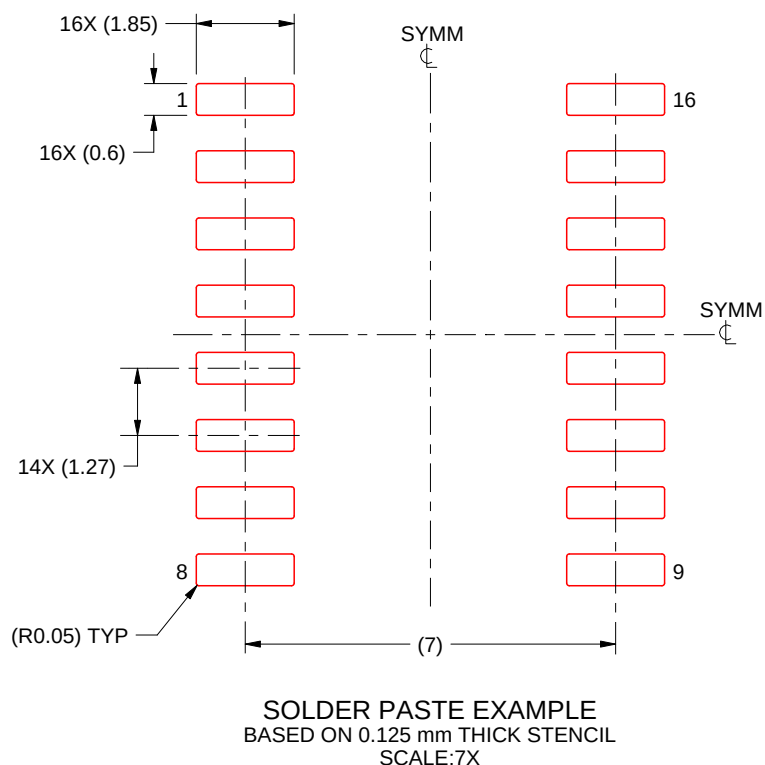


4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



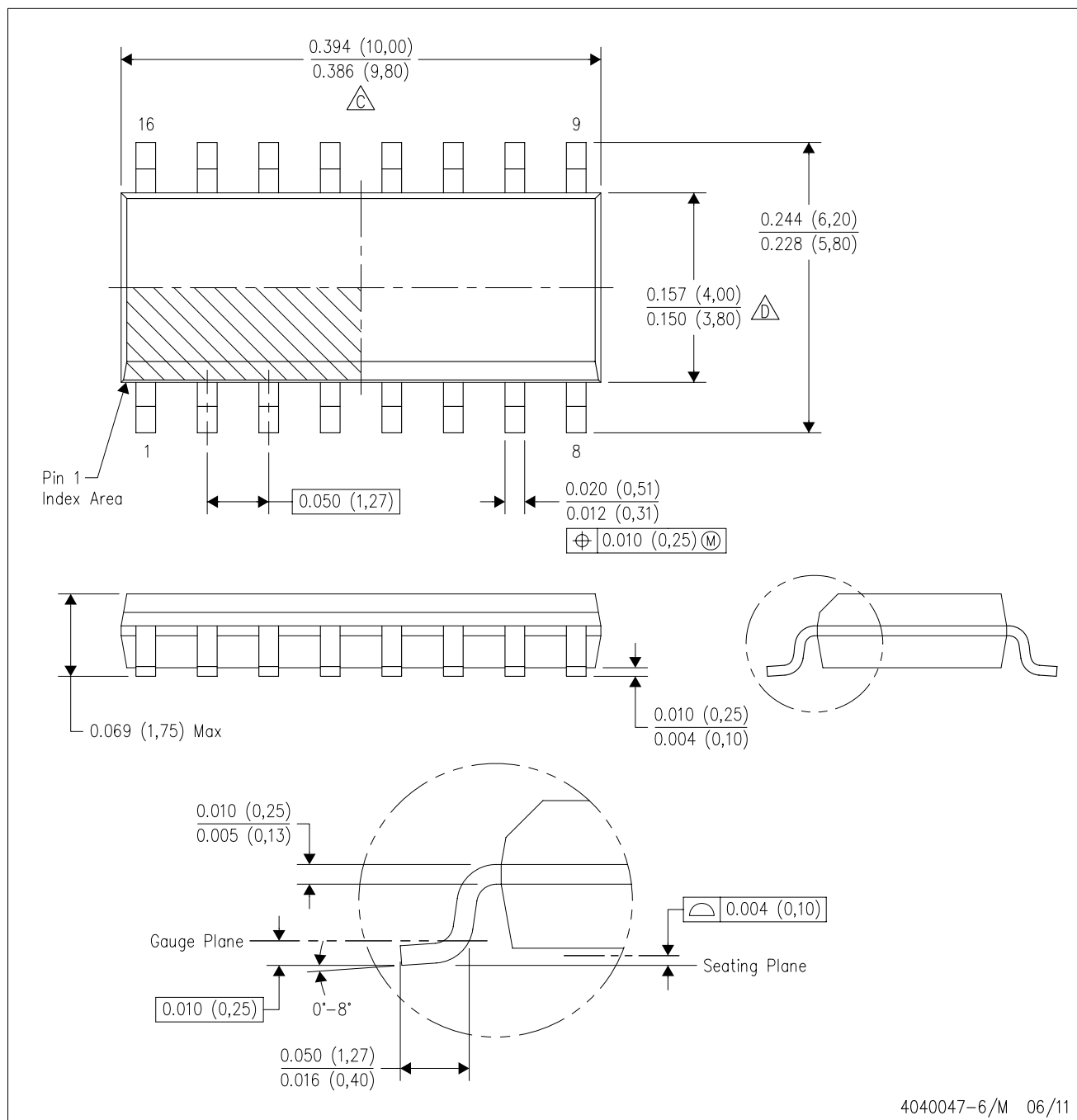
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



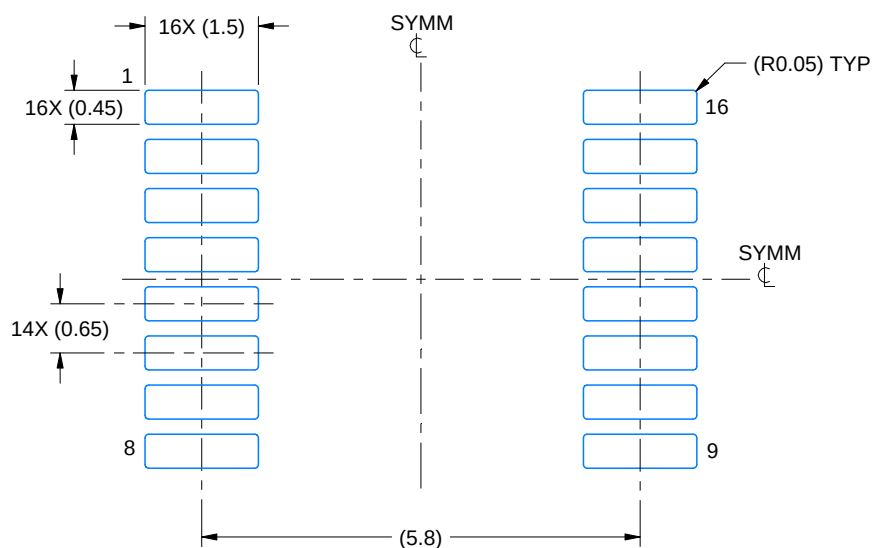
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

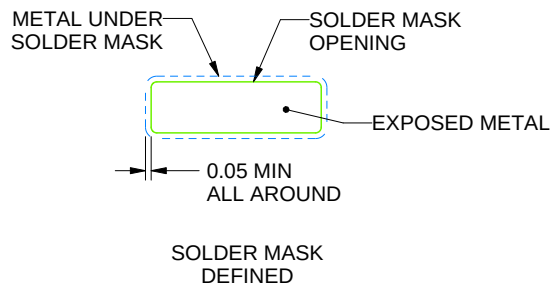
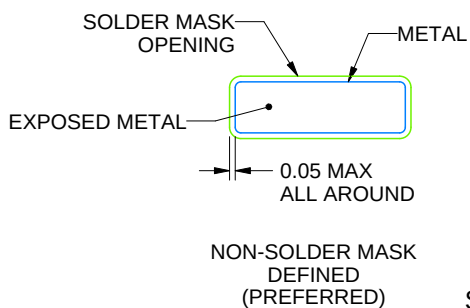
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

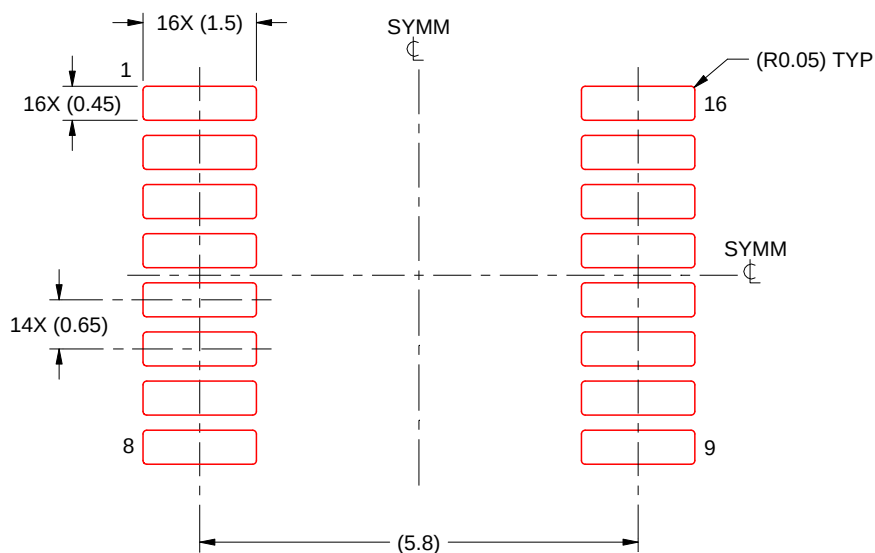
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

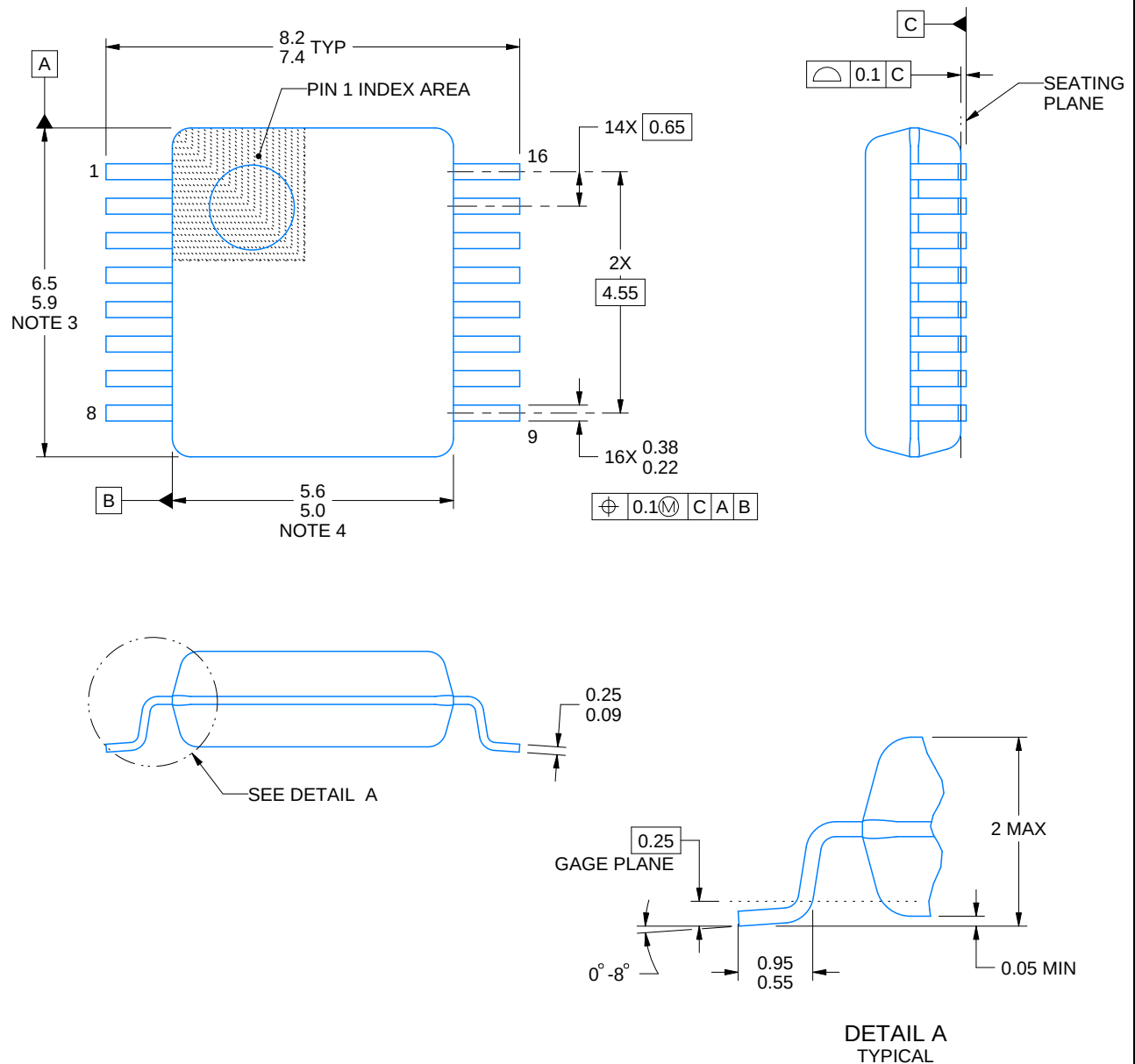


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220763/A 05/2022

NOTES:

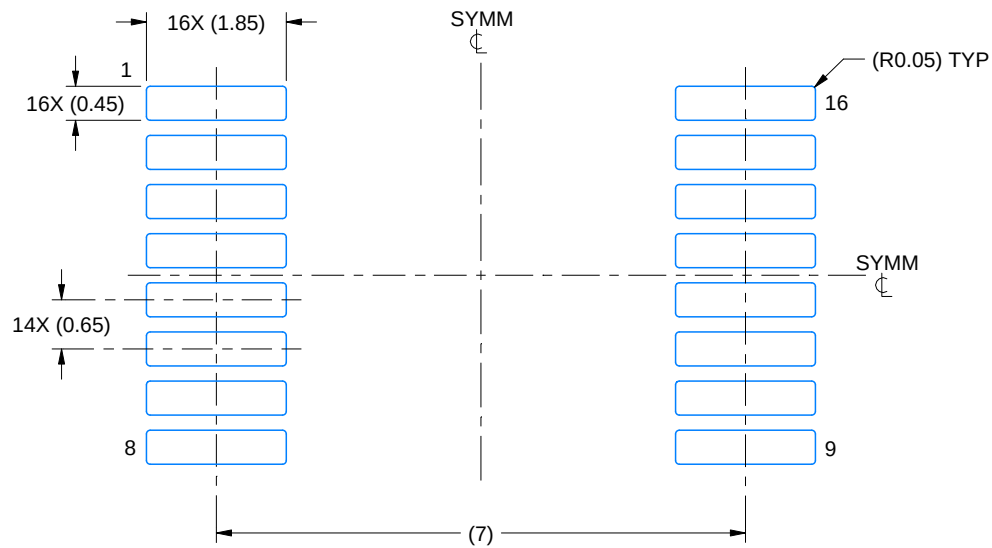
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

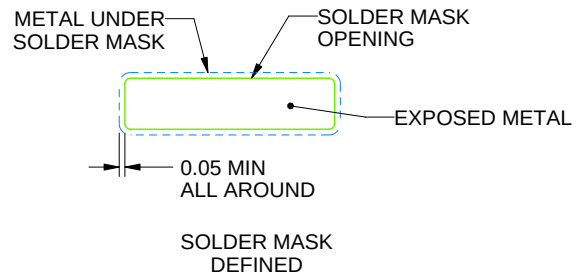
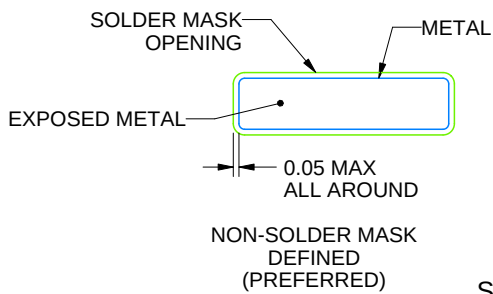
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

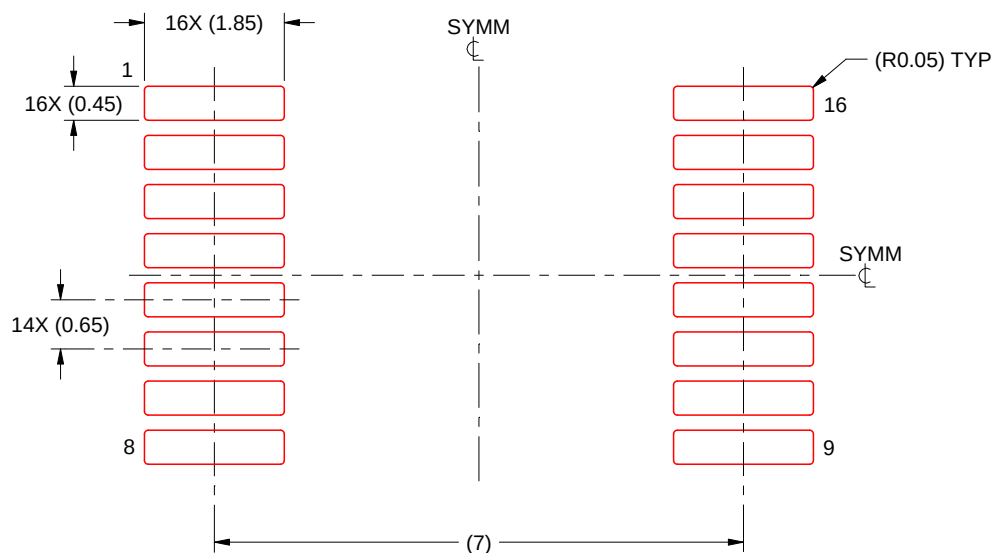
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

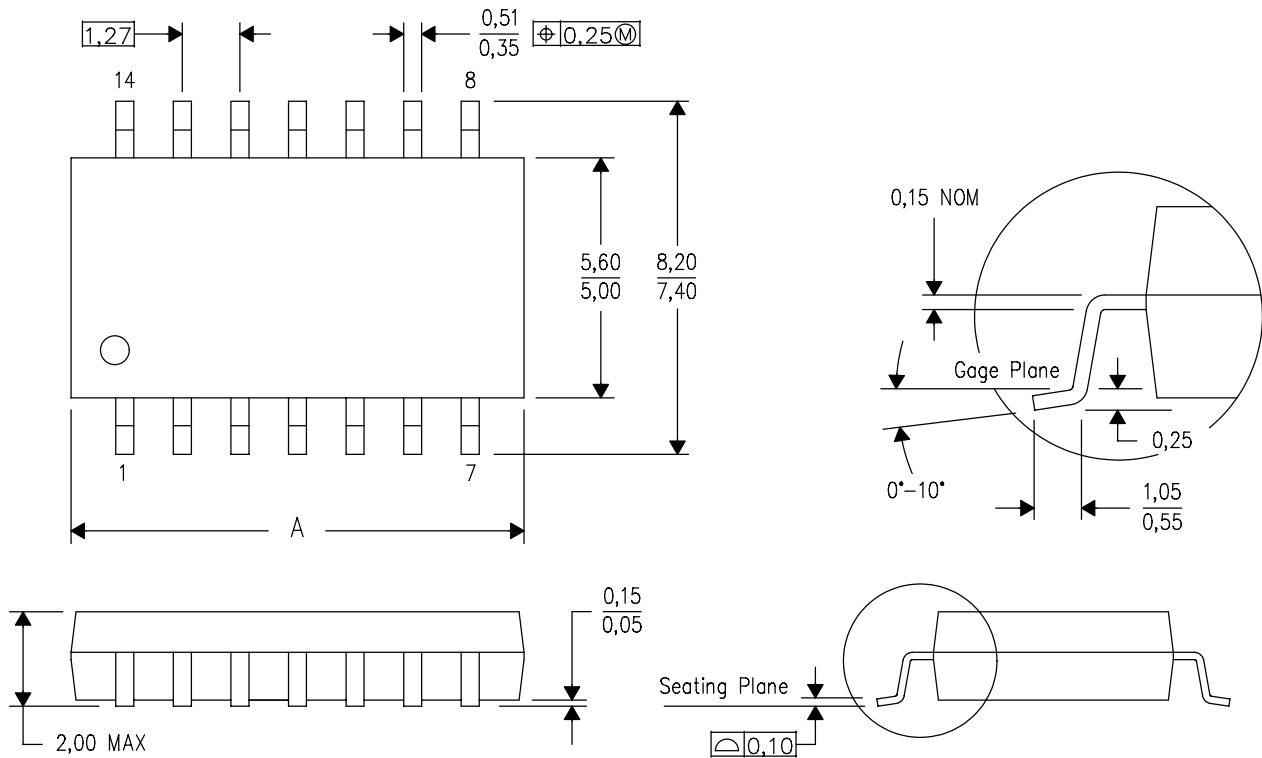
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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