

FEATURES

- Member of Texas Instruments Widebus™ Family
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- D-Type Flip-Flops With Qualified Storage Enable
- Translates Between GTL/GTL+ Signal Levels and LVTTL Logic Levels
- Supports Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port
- Distributed V_{CC} and GND Pins Minimize High-Speed Noise
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

The SN74GTL16622A is an 18-bit registered bus transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. This device is partitioned as two separate 9-bit transceivers with individual clock-enable controls and contains D-type flip-flops for temporary storage of data flowing in either direction. This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry.

The user has the flexibility of using this device at either GTL ($V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V) or the preferred higher noise margin GTL+ ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

Data flow in each direction is controlled by the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock (CLKAB and CLKBA) inputs. The clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs control each 9-bit transceiver independently, which makes the device more versatile.

DGG PACKAGE
(TOP VIEW)

$\overline{OEAB}$	1	64	CLKAB
1A1	2	63	$\overline{1CEAB}$
GND	3	62	$\overline{1CEBA}$
1A2	4	61	1B1
1A3	5	60	GND
GND	6	59	1B2
V_{CC}	7	58	1B3
1A4	8	57	V_{CC}
GND	9	56	1B4
1A5	10	55	1B5
1A6	11	54	1B6
GND	12	53	GND
1A7	13	52	1B7
1A8	14	51	1B8
GND	15	50	GND
1A9	16	49	1B9
2A1	17	48	2B1
GND	18	47	GND
2A2	19	46	2B2
2A3	20	45	2B3
GND	21	44	GND
2A4	22	43	2B4
2A5	23	42	2B5
GND	24	41	2B6
2A6	25	40	V_{REF}
V_{CC}	26	39	2B7
GND	27	38	2B8
2A7	28	37	GND
2A8	29	36	2B9
GND	30	35	$\overline{2CEBA}$
2A9	31	34	$\overline{2CEAB}$
$\overline{OEBA}$	32	33	CLKBA



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SN74GTL16622A

18-BIT LVTTTL-TO-GTL/GTL+ BUS TRANSCEIVER

SCBS673F–AUGUST 1996–REVISED APRIL 2005



DESCRIPTION/ORDERING INFORMATION (CONTINUED)

For A-to-B data flow, the device operates on the low-to-high transition of CLKAB if $\overline{CEAB}$ is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTL16622ADGGR	GTL16622A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE⁽¹⁾

INPUTS				OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	CLKAB	A		
X	H	X	X	Z	Isolation
H	L	X	X	$B_0^{(2)}$	Latched storage of A data
X	L	H or L	X	$B_0^{(2)}$	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

(1) A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

(2) Output level before the indicated steady-state input conditions are established

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range ⁽²⁾	A-port and control inputs	–0.5	6.5	V
		B port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high or power-off state ⁽²⁾	A port	–0.5	6.5	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		48	mA
		B port		100	
I_O	Current into any A-port output in the high state ⁽³⁾			48	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾			55	°C/W
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The current flows only when the output is in the high state and $V_O > V_{CC}$.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3.15	3.3	3.45	V
V _{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V _{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V _I	Input voltage	B port			V _{TT}	V
		Except B port			5.5	
V _{IH}	High-level input voltage	B port	V _{REF} + 50 mV			V
		Except B port	2			
V _{IL}	Low-level input voltage	B port	V _{REF} – 50 mV			V
		Except B port	0.8			
I _{IK}	Input clamp current				–18	mA
I _{OH}	High-level output current	A port			–24	mA
I _{OL}	Low-level output current	A port			24	mA
		B port			50	
T _A	Operating free-air temperature		–40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Normal connection sequence is GND first and $V_{CC} = 3.3$ V, I/O, control inputs, V_{TT} and V_{REF} (any order) last.
- (3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
- (4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} .

Electrical Characteristics

over recommended operating free-air temperature range for GTL/GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3.15\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	A port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$,	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$			V
		$V_{CC} = 3.15\text{ V}$	$I_{OH} = -12\text{ mA}$	2.4			
			$I_{OH} = -24\text{ mA}$	2			
V_{OL}	A port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$,	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 12\text{ mA}$			0.4	
			$I_{OL} = 24\text{ mA}$			0.5	
	B port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$,	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 10\text{ mA}$			0.2	
			$I_{OL} = 40\text{ mA}$			0.4	
			$I_{OL} = 50\text{ mA}$			0.55	
I_I	B port	$V_{CC} = 3.45\text{ V}$,	$V_I = V_{TT}\text{ or GND}$			± 5	μA
	A-port and control inputs	$V_{CC} = 3.45\text{ V}$	$V_I = V_{CC}\text{ or GND}$			± 5	
			$V_I = 5.5\text{ V or GND}$			± 20	
I_{off}		$V_{CC} = 0$,	$V_I\text{ or } V_O = 0\text{ to } 5.5\text{ V}$			100	μA
$I_{I(hold)}$	A port	$V_{CC} = 3.15\text{ V}$	$V_I = 0.8\text{ V}$	75			μA
			$V_I = 2\text{ V}$	-75			
		$V_{CC} = 3.45\text{ V}^{(2)}$,	$V_I = 0.8\text{ V to } 2\text{ V}$			± 500	
$I_{OZ}^{(3)}$	A port	$V_{CC} = 3.45\text{ V}$,	$V_O = V_{CC}\text{ or GND}$			± 10	μA
I_{OZH}	B port	$V_{CC} = 3.45\text{ V}$,	$V_O = 1.5\text{ V}$			10	μA
I_{CC}	A or B port	$V_{CC} = 3.45\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high			60	mA
			Outputs low			60	
			Outputs disabled			60	
$\Delta I_{CC}^{(4)}$		$V_{CC} = 3.45\text{ V}$, A-port or control inputs at $V_{CC}\text{ or GND}$, One input at $V_{CC} - 0.6\text{ V}$				500	μA
C_i	Control inputs	$V_I = 3.15\text{ V or } 0$			2.5	3	pF
C_{io}	A port	$V_O = 3.15\text{ V or } 0$			6	8	pF
	B port				6.5	8.5	

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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18-BIT LVTTTL-TO-GTL/GTL+ BUS TRANSCEIVER

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Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature for GTL (unless otherwise noted)

		MIN	MAX	UNIT
f_{clock}	Clock frequency		200	MHz
t_w	Pulse duration, CLK high or low	2.5		ns
t_{su}	Setup time	Data before CLK $\uparrow$	2.1	ns
		$\overline{\text{CE}}$ before CLK $\uparrow$	3.3	
t_h	Hold time	Data after CLK $\uparrow$	0.3	ns
		$\overline{\text{CE}}$ after CLK $\uparrow$	0	

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
f _{max}			200			MHz
t _{PLH}	CLKAB	B	2.5		5.5	ns
t _{PHL}			2.2		5.5	
t _{dis}	$\overline{\text{OEAB}}$	B	1.7		4.8	ns
t _{en}			2.2		5.2	
Slew rate	Both transitions (B port)		0.5			V/ns
t _r	Transition time, B outputs (0.6 V to 1 V)		0.6		2.2	ns
t _f	Transition time, B outputs (1 V to 0.6 V)		0.4		1.5	ns
t _{PLH}	CLKBA	A	2.1		5.3	ns
t _{PHL}			2.1		5	
t _{en}	$\overline{\text{OEBA}}$	A	1.7		5	ns
t _{dis}			2.3		5.5	

(1) All typical values are at $V_{\text{CC}} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature for GTL+ (unless otherwise noted)

		MIN	MAX	UNIT
f_{clock}	Clock frequency		200	MHz
t_w	Pulse duration, CLK high or low	2.5		ns
t_{su}	Setup time	Data before CLK↑	2.4	ns
		$\overline{\text{CE}}$ before CLK↑	3.2	
t_h	Hold time	Data after CLK↑	0.2	ns
		$\overline{\text{CE}}$ after CLK↑	0	

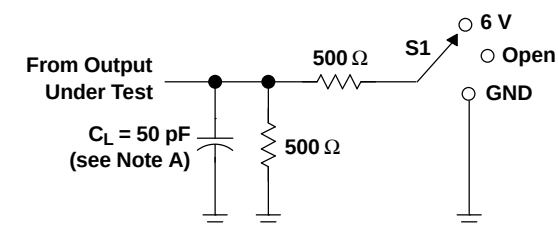
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
f _{max}			200			MHz
t _{PLH}	CLKAB	B	2.6	4	5.6	ns
t _{PHL}			2.3	4	5.7	
t _{PLH}	$\overline{\text{OEAB}}$	B	2.4	3.8	5.2	ns
t _{PHL}			1.8	3.4	5	
Slew rate	Both transitions (B port)		0.5			V/ns
t _r	Transition time, B outputs (0.6 V to 1.3 V)		1	1.6	2.7	ns
t _f	Transition time, B outputs (1.3 V to 0.6 V)		0.5	1.1	3.2	ns
t _{PLH}	CLKBA	A	2	3.8	5.3	ns
t _{PHL}			1.9	3.6	5	
t _{en}	$\overline{\text{OEBA}}$	A	1.9	3.6	5	ns
t _{dis}			2.1	4	5.5	

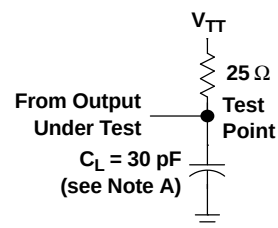
(1) All typical values are at $V_{\text{CC}} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

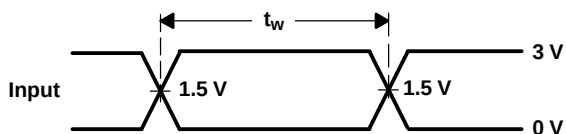


LOAD CIRCUIT FOR A OUTPUTS

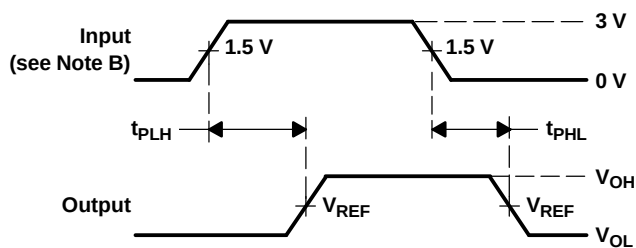
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



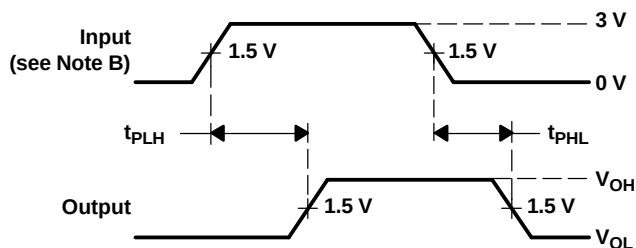
LOAD CIRCUIT FOR B OUTPUTS



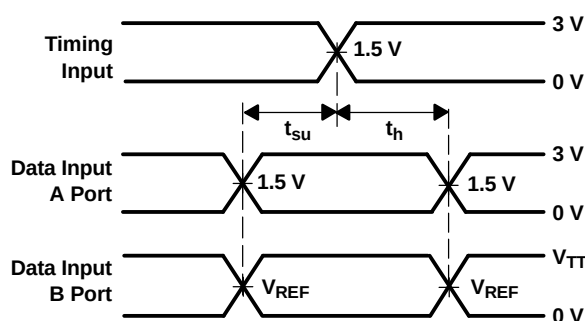
VOLTAGE WAVEFORMS
PULSE DURATION



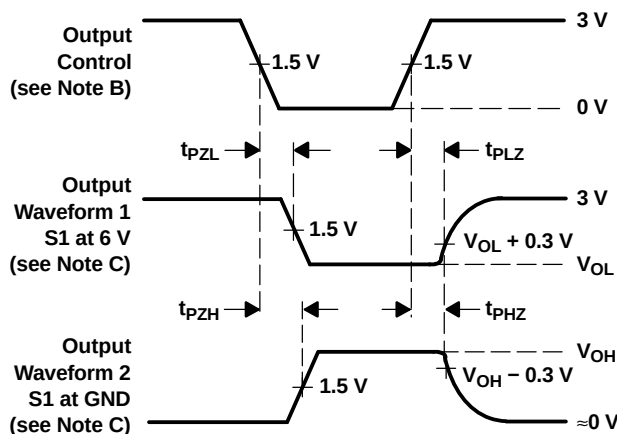
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKAB to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKBA to A port)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(OEBA to A port)

- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74GTL16622ADGGR	Active	Production	TSSOP (DGG) 64	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTL16622A
SN74GTL16622ADGGR.B	Active	Production	TSSOP (DGG) 64	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTL16622A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

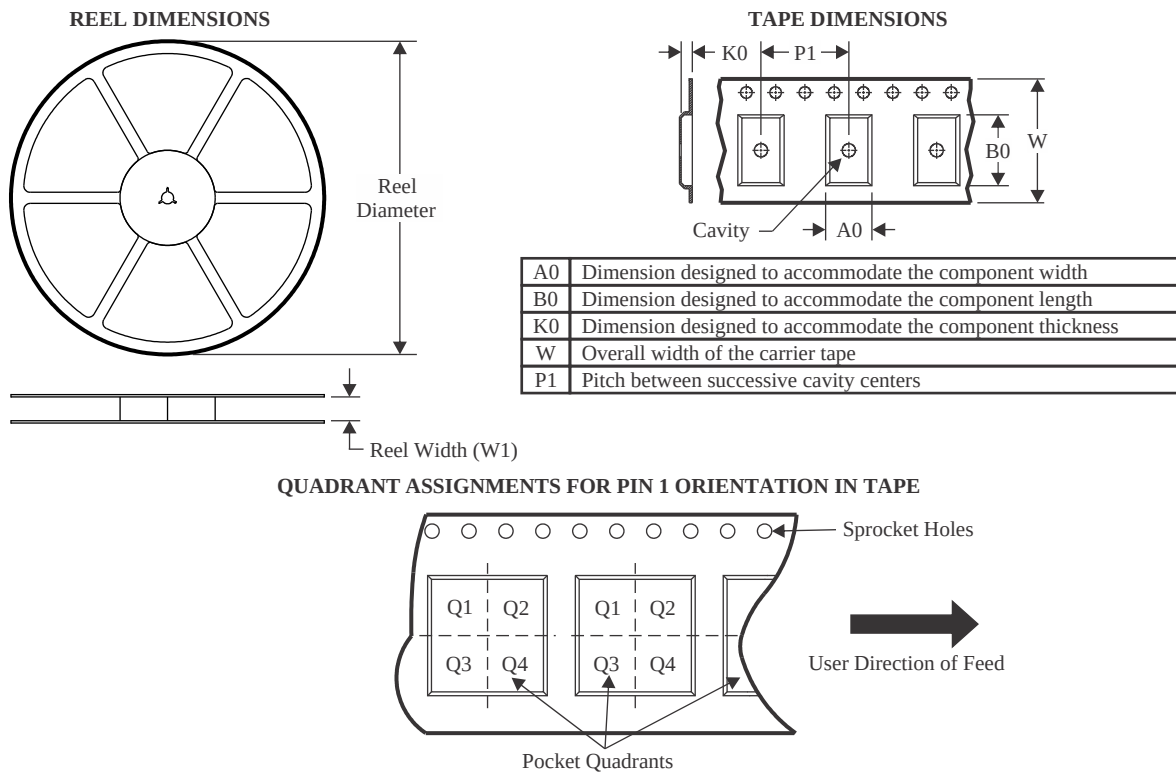
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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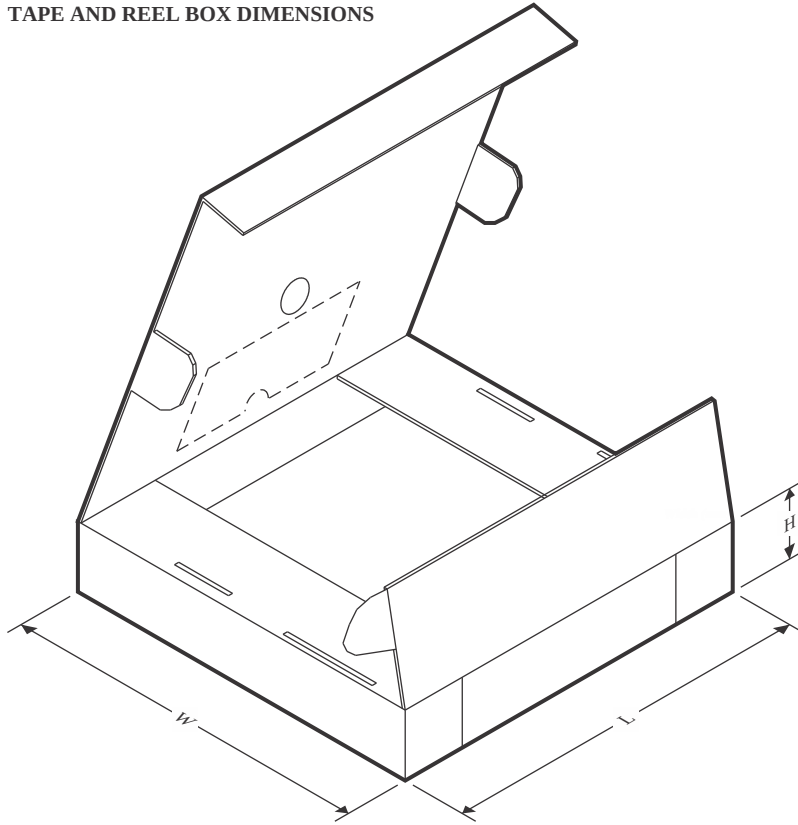
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL16622ADGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



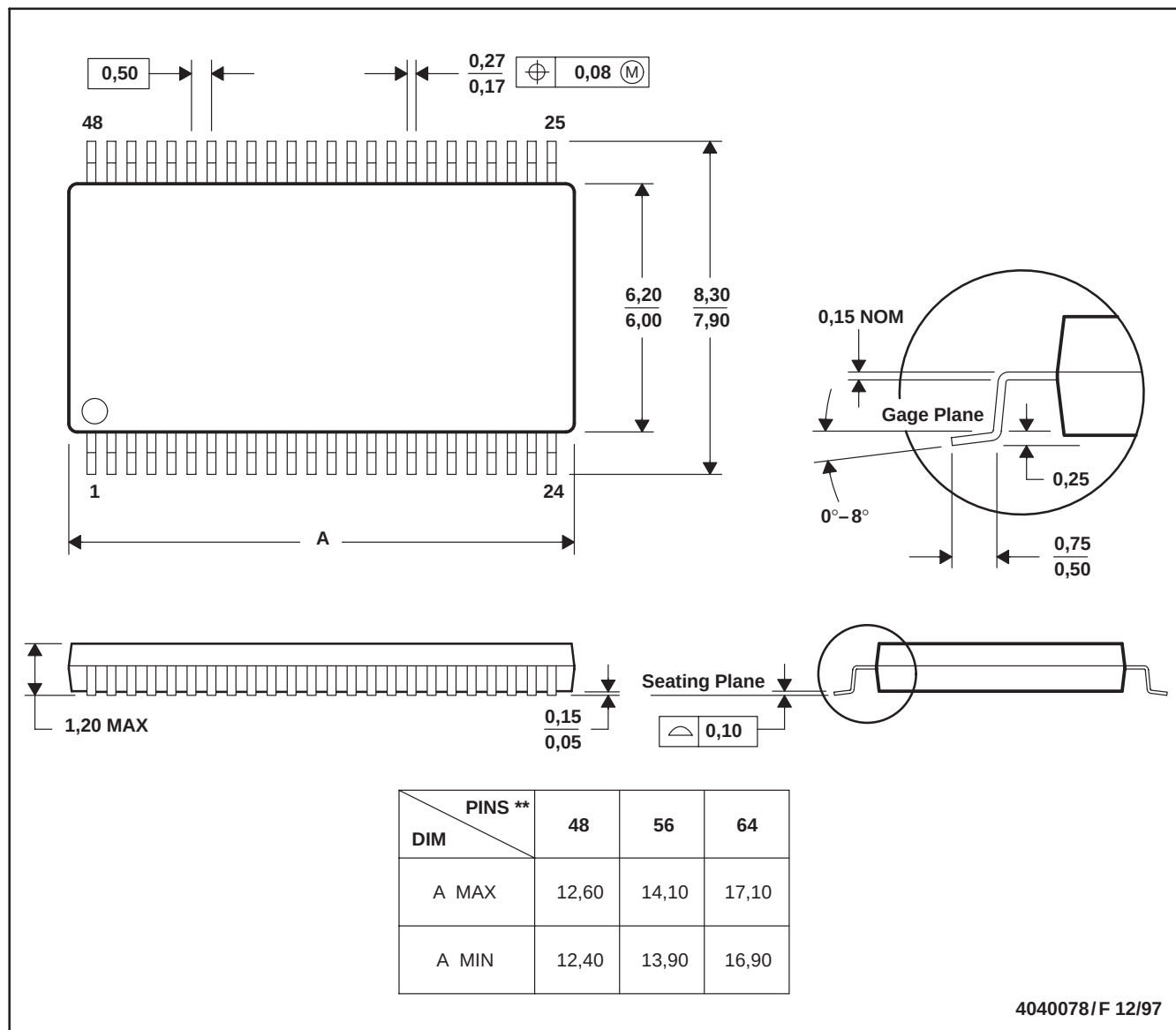
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL16622ADGGR	TSSOP	DGG	64	2000	356.0	356.0	45.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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