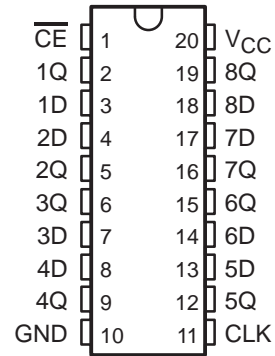


# SN74F377A OCTAL D-TYPE FLIP-FLOP WITH CLOCK ENABLE

SDFS018D – D2932, MARCH 1987 – REVISED OCTOBER 1993

- Contains Eight D-Type Flip-Flops With Single-Rail Outputs
- Clock Enable Latched to Avoid False Clocking
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Buffered Common Enable Input
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR N PACKAGE  
(TOP VIEW)



## description

The SN74F377A is a monolithic, positive-edge-triggered, octal, D-type flip-flop with clock enable inputs. The SN74F377A features a latched clock enable ( $\overline{CE}$ ) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if  $\overline{CE}$  is low. Clock triggering occurs at a particular voltage level and is not directly related to the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the  $\overline{CE}$  input.

The SN74F377A is characterized for operation from 0°C to 70°C.

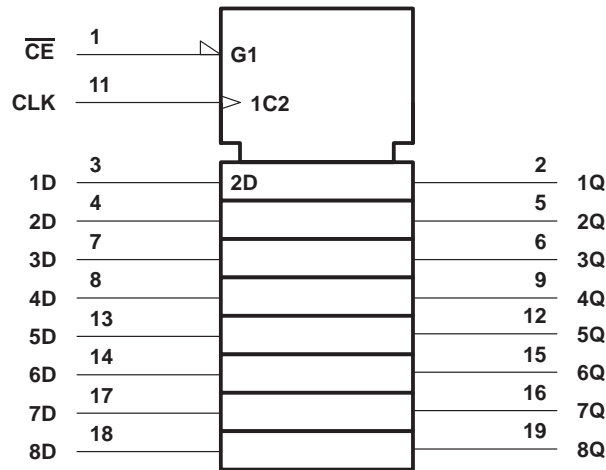
FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{CE}$	CLK	D	Q
H	X	X	$Q_0$
L	↑	H	H
L	↑	L	L
X	L	X	$Q_0$

# SN74F377A OCTAL D-TYPE FLIP-FLOP WITH CLOCK ENABLE

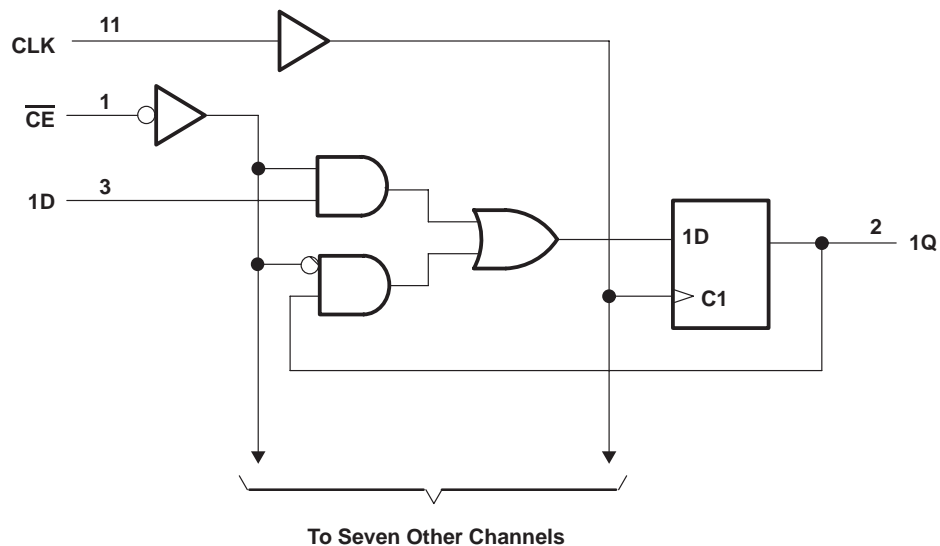
SDFS018D – D2932, MARCH 1987 – REVISED OCTOBER 1993

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-1.2 V to 7 V
Input current range .....	-30 mA to 5 mA
Voltage range applied to any output in the high state .....	-0.5 V to $V_{CC}$
Current into any output in the low state .....	40 mA
Operating free-air temperature range .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.



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# SN74F377A OCTAL D-TYPE FLIP-FLOP WITH CLOCK ENABLE

SDFS018D – D2932, MARCH 1987 – REVISED OCTOBER 1993

## recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-1	mA
$I_{OL}$	Low-level output current			20	mA
$T_A$	Operating free-air temperature	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	UNIT
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -1\text{ mA}$	2.5	3.4		V
	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -1\text{ mA}$	2.7			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 20\text{ mA}$		0.3	0.5	V
$I_I$	$V_{CC} = 0$ ,	$V_I = 7\text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	μA
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			-0.6	mA
$I_{OS}^{\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-60		-150	mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$ ,	See Note 2		55	72	mA
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ ,	See Note 3		70	90	mA

<sup>†</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTES: 2.  $I_{CCH}$  is measured after applying a momentary ground, then 4.5 V, to the clock input with all data inputs at 4.5 V and the enable input at GND.

3.  $I_{CCL}$  is measured after applying a momentary ground, then 4.5 V, to the clock input with all data and enable inputs at GND.

## timing requirements

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $T_A = \text{MIN to MAX}^{\S}$		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	110	0	110	MHz
$t_w$	Pulse duration	4		5		ns
$t_{\text{su}}$	Setup time before $\text{CLK}\uparrow$	Data high or low	2	2		ns
		$\overline{\text{CE}}$ high	2.5	2.5		
		$\overline{\text{CE}}$ low	4	4.5		
$t_h$	Hold time after $\text{CLK}\uparrow$	Data high or low	1	1		ns
		$\overline{\text{CE}}$ high or low	0	0		

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN74F377A

## OCTAL D-TYPE FLIP-FLOP WITH CLOCK ENABLE

SDFS018D – D2932, MARCH 1987 – REVISED OCTOBER 1993

### switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX †		UNIT
			MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			110	125		110		MHz
t <sub>PLH</sub>	CLK	Any Q	4	6.5	8.5	4	10	ns
t <sub>PHL</sub>			4	7	9	4	10.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 4: Load circuit and waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74F377ADW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	F377A
<a href="#">SN74F377ADWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F377A
SN74F377ADWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F377A
<a href="#">SN74F377AN</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F377AN
SN74F377AN.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F377AN

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F377ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F377ADWR	SOIC	DW	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74F377AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74F377AN.A	N	PDIP	20	20	506	13.97	11230	4.32



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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