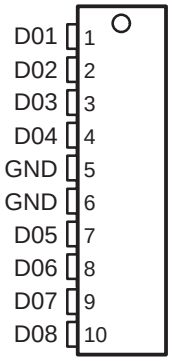
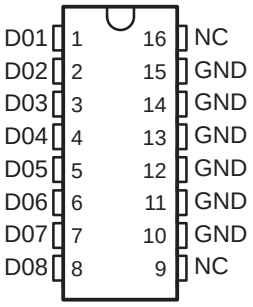
- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current 300 mA**
- **8-Bit Array Structure Suited for Bus-Oriented Systems**

SC PACKAGE
(TOP VIEW)



D PACKAGE
(TOP VIEW)



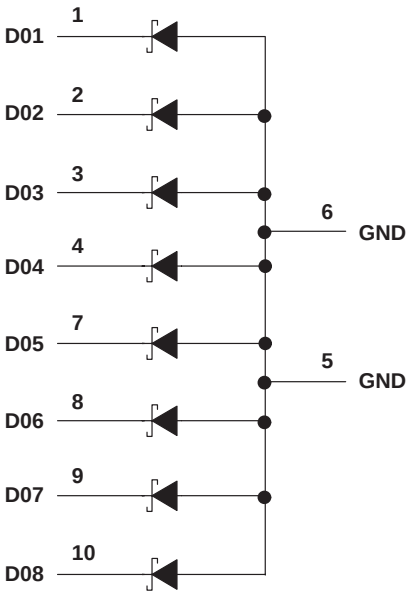
description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of an 8-bit high-speed Schottky diode array suitable for a clamp to GND.

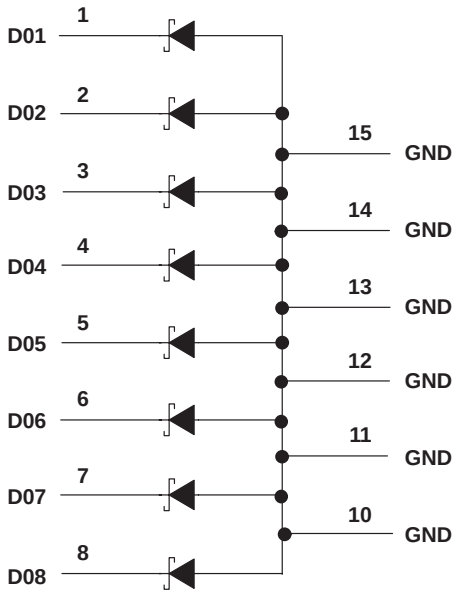
The SN74F1056 is characterized for operation from 0°C to 70°C.

schematic diagrams

SC Package



D Package



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R . . . . . 7 V
Continuous forward current, I_F: Any D terminal from GND . . . . . 50 mA
Total through all GND terminals . . . . . 170 mA
Repetitive peak forward current, I_{FRM} (see Note 1): Any D terminal from GND . . . . . 300 mA
Total through all GND terminals . . . . . 1.2 A
Continuous total power dissipation at (or below) 25°C free-air temperature . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These values apply for $t_w \leq 100$ µs, duty cycle ≤ 20%.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_R	Static reverse current	V_R = 7 V				2	µA
V_F	Static forward voltage	I_F = 18 mA			0.8	1	V
		I_F = 50 mA			1	1.2	
V_{FM}	Peak forward voltage	I_F = 200 mA			1.23		V
C_t	Total capacitance	V_R = 0,	f = 1 MHz		3	3.75	pF
		V_R = 2 V,	f = 1 MHz		2.5	3	

‡ All typical values are at T_A = 25°C.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_X	Internal crosstalk current	Total GND current = 1.2 A,	See Note 3		10	50	µA

‡ All typical values are at T_A = 25°C.

NOTE 3: I_X is measured under the following conditions with one diode static, all others switching:
Switching diodes: t_w = 100 µs, duty cycle = 20%
Static diode: V_R = 5 V
The static diode input current is the internal crosstalk current I_X.

switching characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	I_F = 10 mA, $I_{RM(REC)}$ = 10 mA, $I_{R(REC)}$ = 1 mA, R_L = 100 Ω		5	7	ns

undershoot characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{US}	Undershoot voltage	t_f = 2 ns, t_w = 50 ns, V_{IH} = 5 V, V_{IL} = 0, Z_S = 25 Ω, Z_O = 50 Ω, L = 36-inch coax		0.6	0.7	V

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74F1056 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current versus voltage plot for the SN74F1056 is shown in Figure 1.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 2(a) was evaluated. The resulting waveforms with and without the diode are shown in Figure 2(b).

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes also can be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

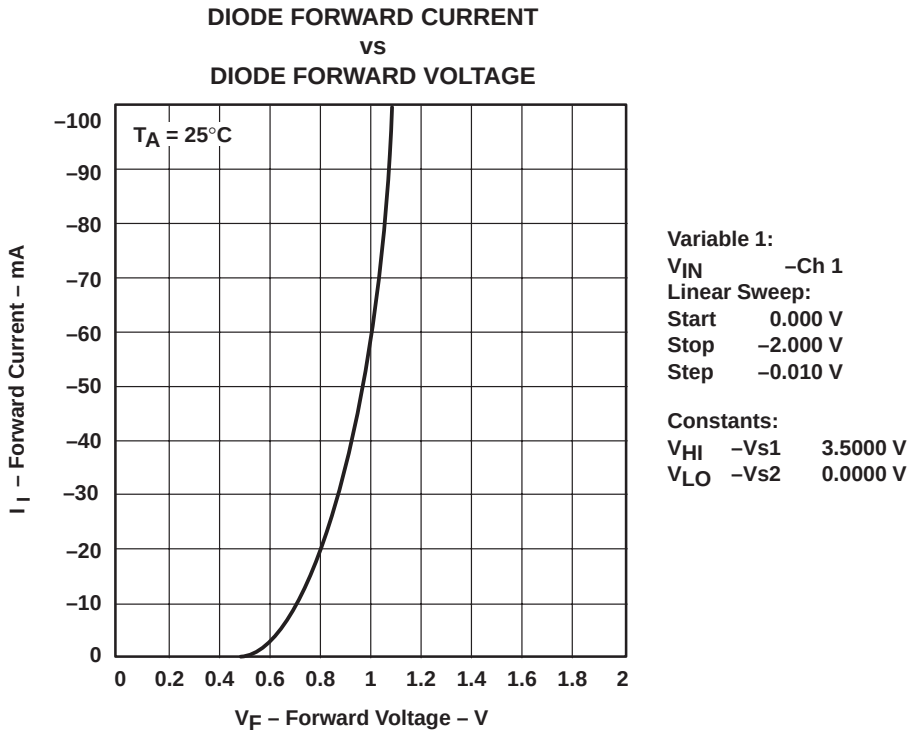
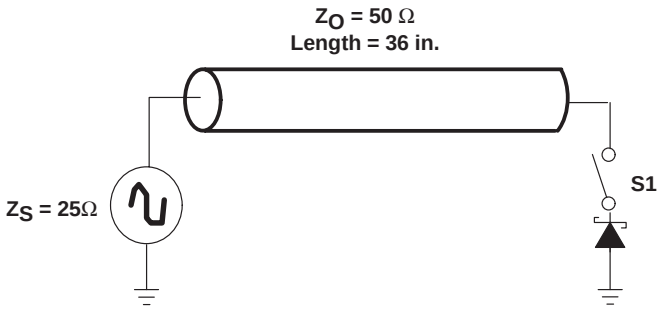
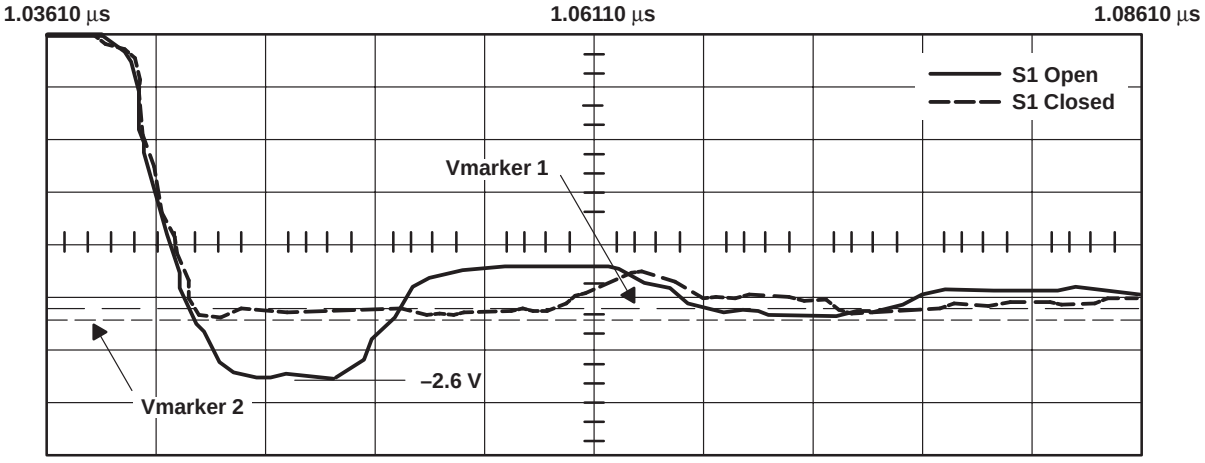


Figure 1. Current Versus Voltage for the SN74F1056

APPLICATION INFORMATION



(a) UNDERSHOOT TEST SETUP



Ch 1 = 2.000 V/div
Timebase = 5.00 ns/div
Vmarker 1 = 0.0000 V
Vmarker 2 = –600.00 mV

Offset = 2.340 V
Delay = 1.06110 μs
Delta V = –600.0 mV

(b) OSCILLOSCOPE DISPLAY

Figure 2. Undershoot Test Setup and Oscilloscope Display

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74F1056D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	F1056
SN74F1056DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F1056
SN74F1056DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F1056

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

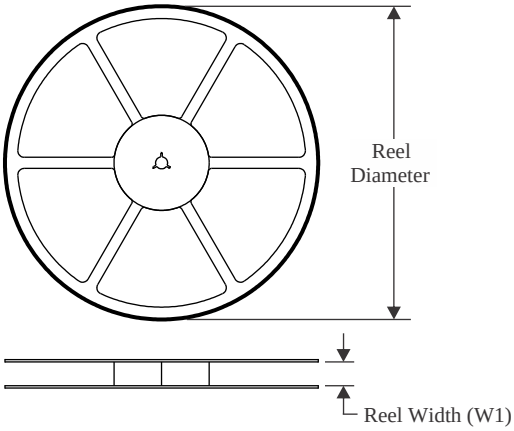
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

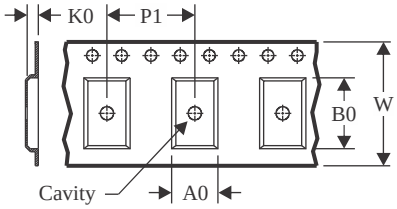
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

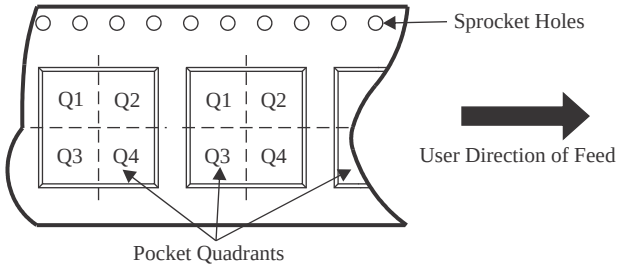


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

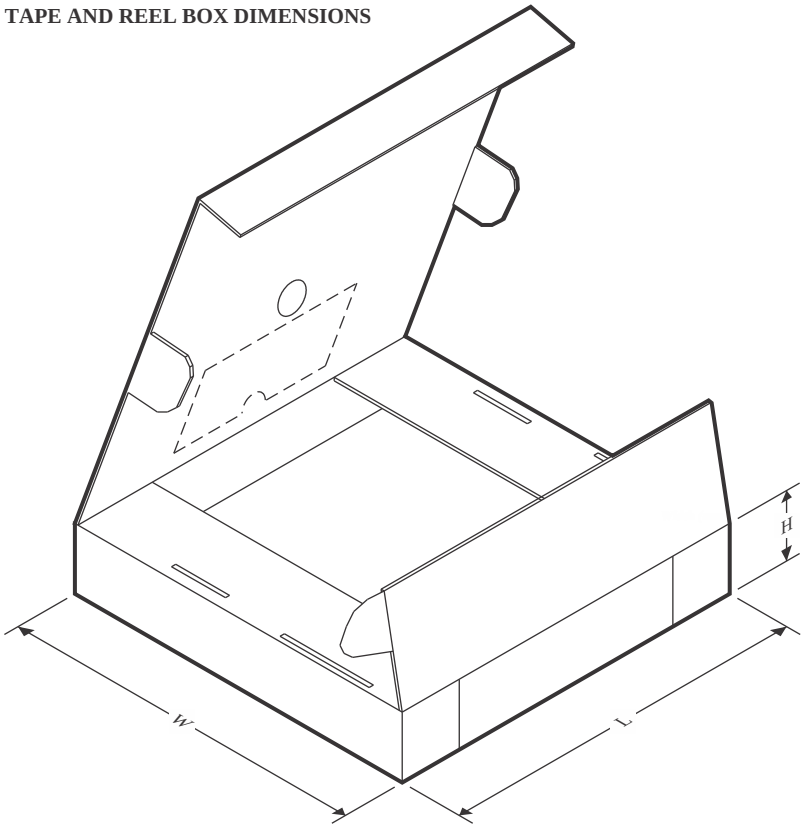
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F1056DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

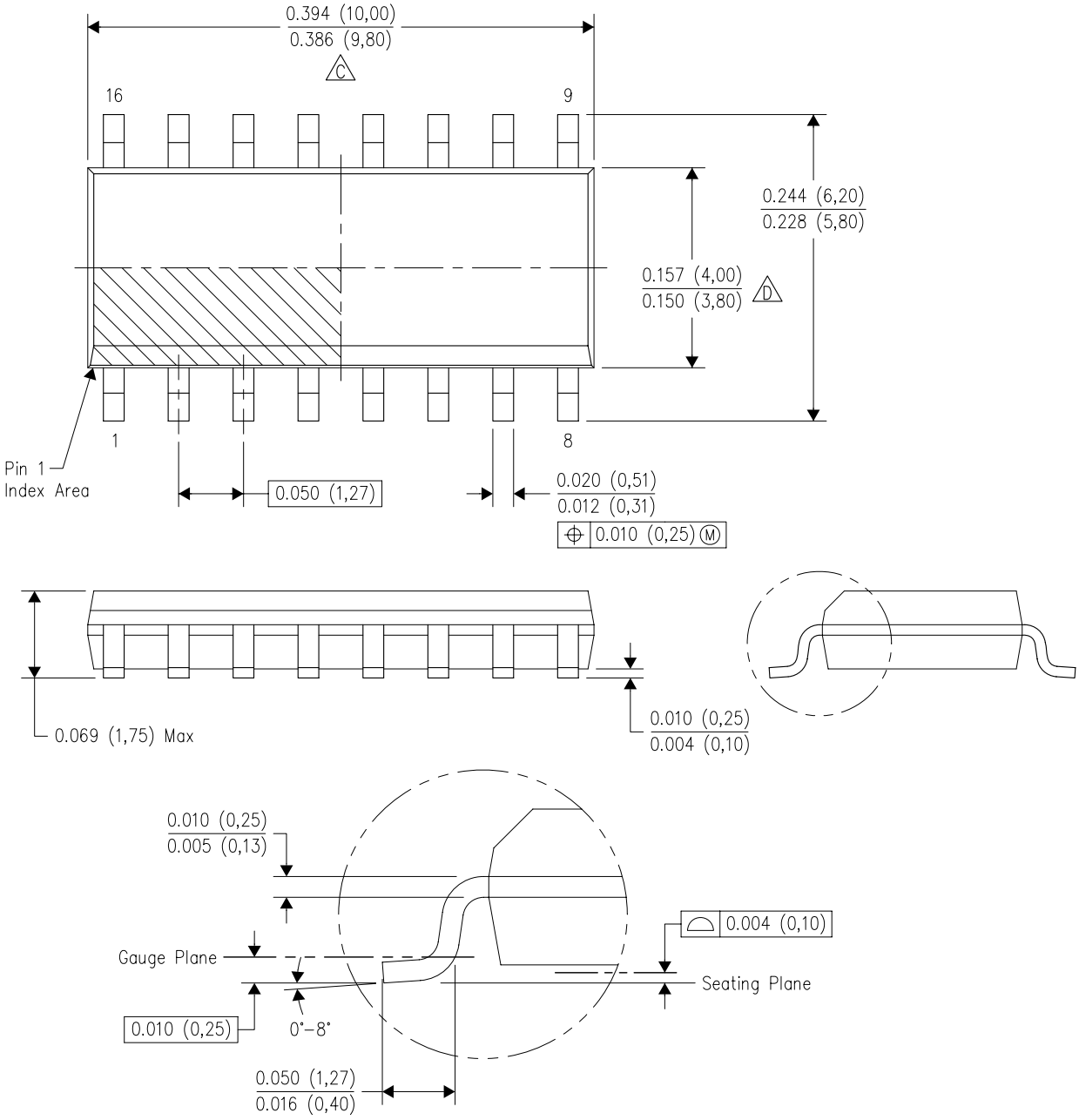
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F1056DR	SOIC	D	16	2500	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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