SN74CBTU4411 11 ビット 1:4 マルチプレクサ / デマルチプレクサ 1.8V DDR-II スイッチ、チャージ・ポンプ / プリチャージ出力付き

1 特長

- SSTL_18 信号レベルをサポート
- DDR-II アプリケーションに最適
- バイアス電圧 (V_{BIAS}) により D ポート出力をプリチャージ
- 制御入力を内部で終端
- 広帯域 (最小 400MHz)
- 低く平坦なオン抵抗 (r_{on}) 特性 (r_{on} ＝最大 17Ω)
- 400Ω プルダウン抵抗を内蔵
- 差動および立ち上がり/立ち下がりエッジ・スキューが小さい
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- ATCA ソリューション
- 自動体外式除細動器
- 適応型照明
- 血液ガス分析器:ポータブル
- Bluetooth 対応ヘッドセット
- CT スキャナ
- カメラ:監視アナログ
- 化学およびガス・センサ
- DLP 3D マシン・ビジョンおよび光ネットワーク

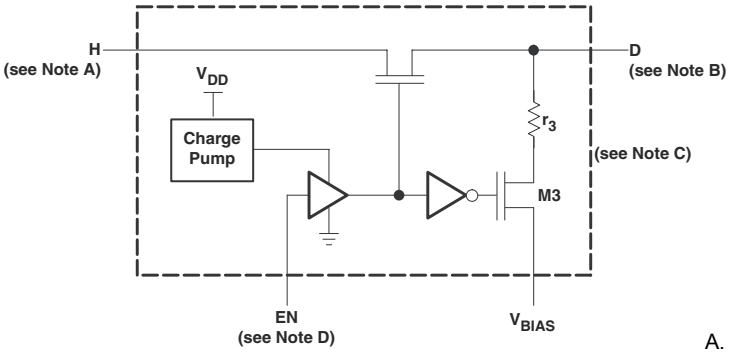
3 概要

SN74CBTU4411 は、広帯域、SSTL_18 準拠、オン抵抗 (r_{on}) の低い FET マルチプレクサ / デマルチプレクサです。内蔵されたチャージ・ポンプを使用してパス・トランジスタのゲート電圧を上げることにより、低く平坦な r_{on} を実現します。R_{on} が低く平坦であるため、伝搬遅延を最小限に抑えることができ、データ入出力 (I/O) ポートでのレール・ツー・レール信号処理をサポートします。また、データ I/O 容量が非常に小さいことから、容量性負荷およびデータバスでの信号歪みも最小限に抑えることができます。オン抵抗および I/O 容量のマッチングにより、差動および立ち上がり / 立ち下がりエッジのスキューは極めて小さくなります。このため、このデバイスは DDR-II アプリケーションで優れた性能を発揮します。

製品情報(1)

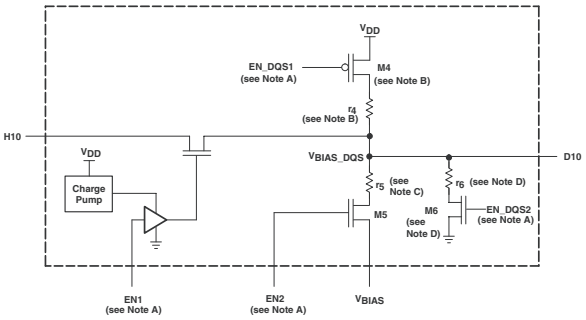
部品番号	パッケージ	本体サイズ
SN74CBTU4411ZST	NFBGA (72)	7.00mm × 7.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



A. ポート H0～H9 に該当
B. ポート D0～D9 に該当
C. r_3 + r_{on} (M3)＝ 400Ω (標準値)
D. EN はスイッチに印加される内部イネーブル信号

概略回路図、各 FET スイッチ(SW1)



A. EN_DQS1、EN_DQS2、EN1、EN2 はスイッチに印加される内部イネーブル信号
B. r_4 + r_{on} (M4)＝ 1kΩ (標準値)
C. r_5 + r_{on} (M5)＝ 400Ω (標準値)
D. r_6 + r_{on} (M6) ＝ 2.3kΩ (標準値)

概略回路図、各 FET スイッチ(SW2)

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (April 2018) to Revision C (September 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- データシートを包括的用語に更新 ... 1

Changes from Revision A (February 2016) to Revision B (April 2018) — **Page**

- Changed the V_{BIAS} MAX value From: 0.33 × V_{DD} To: V_{DD} in the *Recommended Operating Conditions* table ... 6

Changes from Revision * (April 2005) to Revision A (February 2016) — **Page**

- 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。 ... 1
- Removed *Pin Assignments* table due to updated *Pin Out Drawing* ... 3

5 Pin Configuration and Functions

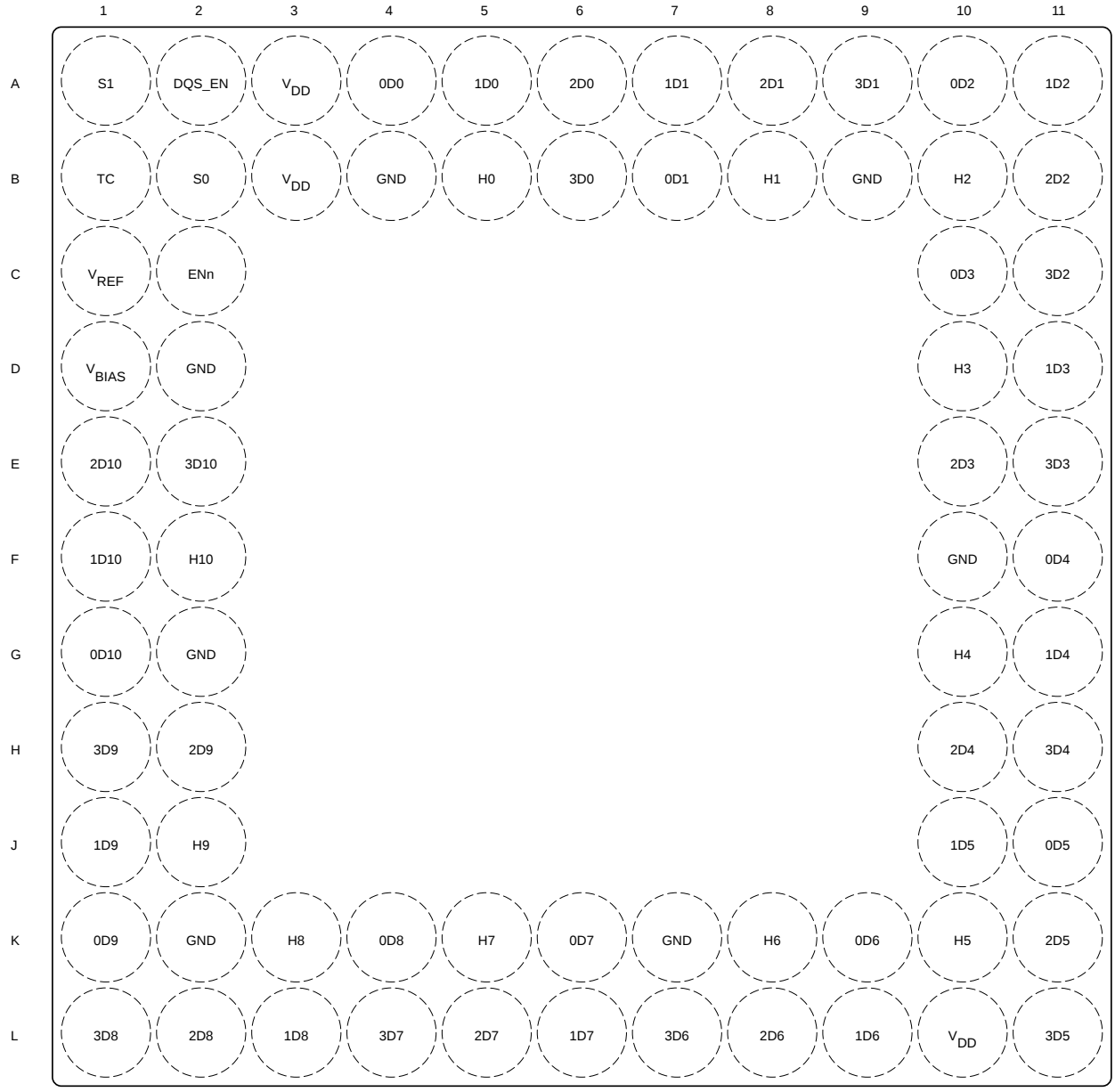


図 5-1. ZST Package
72-Pin NFBGA
Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
0D0	A4	I/O	D0 port0
0D1	B7	I/O	D1 port0
0D2	A10	I/O	D2 port0
0D3	C10	I/O	D3 port0
0D4	F11	I/O	D4 port0

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
0D5	J11	I/O	D5 port0
0D6	K9	I/O	D6 port0
0D7	K6	I/O	D7 port0
0D8	K4	I/O	D8 port0
0D9	K1	I/O	D9 port0
0D10	G1	I/O	D10 port0
1D0	A5	I/O	D0 port1
1D1	A7	I/O	D1 port1
1D2	A11	I/O	D2 port1
1D3	D11	I/O	D3 port1
1D4	G11	I/O	D4 port1
1D5	J10	I/O	D5 port1
1D6	L9	I/O	D6 port1
1D7	L6	I/O	D7 port1
1D8	L3	I/O	D8 port1
1D9	J1	I/O	D9 port1
1D10	F1	I/O	D10 port1
2D0	A6	I/O	D0 port2
2D1	A8	I/O	D1 port2
2D2	B11	I/O	D2 port2
2D3	E10	I/O	D3 port2
2D4	H10	I/O	D4 port2
2D5	K11	I/O	D5 port2
2D6	L8	I/O	D6 port2
2D7	L5	I/O	D7 port2
2D8	L2	I/O	D8 port2
2D9	H2	I/O	D9 port2
2D10	E1	I/O	D10 port2
3D0	B6	I/O	D0 port3
3D1	A9	I/O	D1 port3
3D2	C11	I/O	D2 port3
3D3	E11	I/O	D3 port3
3D4	H11	I/O	D4 port3
3D5	L11	I/O	D5 port3
3D6	L7	I/O	D6 port3
3D7	L4	I/O	D7 port3
3D8	L1	I/O	D8 port3
3D9	H1	I/O	D9 port3
3D10	E2	I/O	D10 port3
DQS_EN	A2	I	D10 port output voltage control
ENn	C2	I	Active low enable input
GND	B4, B9, F10, K7, K2, G2, D2	P	Ground
H0	B5	I/O	H port0
H1	B8	I/O	H port1

表 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
H2	B10	I/O	H port2
H3	D10	I/O	H port3
H4	G10	I/O	H port4
H5	K10	I/O	H port5
H6	K8	I/O	H port6
H7	K5	I/O	H port7
H8	K3	I/O	H port8
H9	J2	I/O	H port9
H10	F2	I/O	H port10
S0	B2	I	Select input control
S1	A1	I	Select input control
TC	B1	I	Termination control input
V_{BIAS}	D1	P	Bias voltage
V_{DD}	A3, B3, L10	P	Power supply
V_{REF}	C1	P	Reference voltage

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	2.5	V
V_{IN}	Control input voltage(2) (3)		–0.5	2.5	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	2.5	V
I_{IK}	Control input clamp current	$V_{IN} < 0$ or $V_{IN} > 0$		±50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$ or $V_{I/O} > 0$		±50	mA
$I_{I/O}$	ON-state switch current(5)			±100	mA
	Continuous current through V_{DD} or GND pins			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under セクション 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HGM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		1.7	1.8	1.9	V
V_{REF}	Reference supply voltage		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V
V_{BIAS}	BIAS supply voltage		0	0.3 × V_{DD}	V_{DD}	V
V_{IH}	High-level control input voltage	S	V_{REF} + 250 mV			V
		$\overline{EN}$, TX, DQS_EN	0.65 × V_{DD}			
V_{IL}	Low-level control input voltage	S			V_{REF} – 250 mV	V
		$\overline{EN}$, TX, DQS_EN			0.35 × V_{DD}	
$V_{I/O}$	Data input/output voltage		0		V_{DD}	V
T_A	Operating free-air temperature		0		85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC[1]		SN74CBTU4411 ZST (NFBGA) 72 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Minimum and maximum limits apply for T_A = 0°C to 85°C (unless otherwise noted). Typical limits apply for V_{DD} = 1.8 V and T_A = 25°C (unless otherwise noted).[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK} [2]	Control inputs[3]	V_{DD} = 1.7 V, I_{IN} = –18 mA				–1.8	V
V_{BIAS_DQS}	D10	V_{DD} = 1.7 V, DQS_EN = V_{DD}		1.1		1.275	V
V_{OH}	D10	V_{DD} = 1.7 V, DQS_EN = V_{DD}, $\overline{EN}$ = V_{DD}, I_O = 100 µA			1.6	1.8	V
I_{IN}	Control inputs[3]	V_{DD} = 1.9 V, V_{IN} = V_{DD} or GND				±1	µA
I_{OZ} [4]		V_{DD} = 1.9 V, V_O = 0 to 1.9 V, V_I = 0, Switch OFF, V_{BIAS} open				±10	µA
I_{CC}		V_{DD} = 1.9 V, TC = GND, $\overline{EN}$ = GND, $I_{I/O}$ = 0, S0 or S1 input switching at 50% duty cycles, Data I/O are open			0.7	2.5	mA
		$\overline{EN}$ = V_{DD}				500	µA
I_{CCD}		V_{DD} = 1.9 V, TC = GND, $\overline{EN}$ = GND, $I_{I/O}$ = 0, S0 or S1 input switching at 50% duty cycle, Data I/O are open				0.5	mA/ MHz[5]
C_{in}	S port	V_{DD} = 1.9 V, TC = GND, $\overline{EN}$ = GND, V_{IN} = V_{REF} ± 250 mV		2.5		3.5	pF
	$\overline{EN}$, TC, DQS_EN inputs	V_{DD} = 1.9 V, V_{IN} = 0 or 1.9 V			2.5		
$C_{io(OFF)}$	H port	$V_{I/O}$ = 0.5 × V_{DD} ± 0.4 V, Switch OFF, V_{BIAS} open				2.5	pF
$C_{io(ON)}$		$V_{I/O}$ = 0.5 × V_{DD} ± 0.4 V, Switch ON, V_{BIAS} = GND				4.6	pF
r_{on} [6]		V_{DD} = 1.7 V, V_I = 0.5 × V_{DD} ± 0.5 V, I_O = 10 mA		6	10	17	Ω
$\Delta r_{on(flat)}$ [7]		V_{DD} = 1.7 V, DQS_EN = V_{DD}, I_O = 10 mA	V_I = 0.5 V_{DD} ± 0.25 V		1.5	3	Ω
			V_I = 0.5 V_{DD} ± 0.5 V		2.5	5	
r_{term}	S port	V_{DD} = 1.7 V		110	160	210	Ω
$r_{pulldown}$	D0–D10	V_{DD} = 1.7 V	DQS_EN = GND	280	400	520	Ω
	D10		DQS_EN = V_{DD}, $\overline{EN}$ = GND	1600	2300	3000	
r_{pullup}	D10	V_{DD} = 1.7 V, DQS_EN = V_{DD}, $\overline{EN}$ = GND		700	1000	1300	Ω

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) V_{IK} refers to the clamp voltage due to the internal diode, which is connected from each control input to GND.
(3) For the leakage current test on S0 and S1, $\overline{EN}$ and TC inputs are set to low.
(4) For I/O ports, the parameter I_{OZ} includes the input leakage current. I_{OZ} applies only to the H port.
(5) This frequency of S0 and S1 inputs, for example, for a data I/O rate of 533 Mbit/s, with a burst of 4, the required frequency is for S0 or S1 input is ≅ 66 MHz (533/8). The total I_{CC} due to switching S0, S1 will be approximately 27 mA (66 MHz × 0.4 mA/MHz).
(6) Measured by the voltage drop between the D and H pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (D or H) pins.
(7) $\Delta r_{on(flat)}$ is the difference of maximum r_{on} and minimum r_{on} for a specific channel in a specific device.

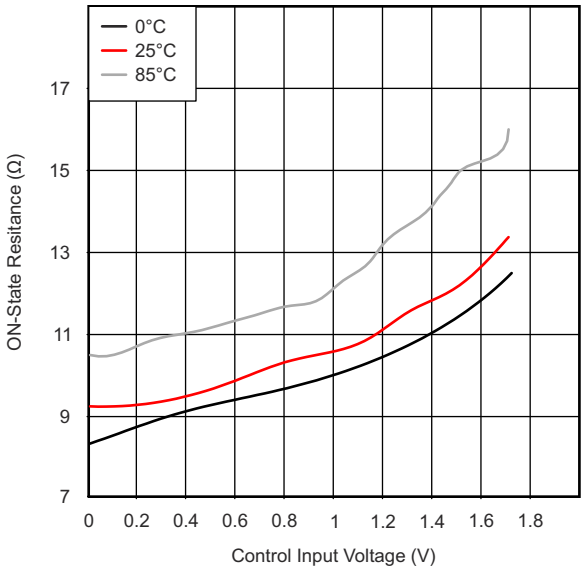
6.6 Switching Characteristics

T_A = 0°C to 85°C (unless otherwise noted) (see 図 7-1 and 図 7-2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	D or H port		400			MHz
	S port[1]		84			
t_{pd}		From D or H (input) to D or H (output)		297		ps
t_{en}(t_{PZL}, t_{PZH})[2]		From S (input) to D (output)	750		2100	ps
t_{dis}(t_{PLZ}, t_{PHZ})[2]		From S (input) to D (output)	750		2100	ps
t_{osk}					85	ps
t_{esk}					40	ps
t_{start} [3]				20		µs

(1) $\overline{EN}$ = GND, TC = GND
(2) V_{BIAS} = open
(3) t_{start} is the time required for the charge-pump circuit output voltage to reach a steady state value after V_{DD} is applied.

6.7 Typical Characteristic

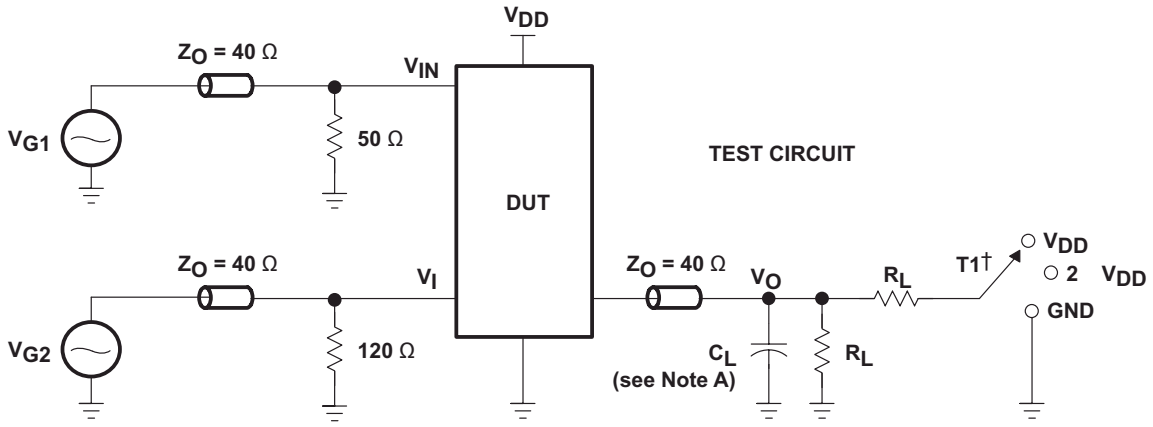


V_{IH} = 1.7 V V_{IL} = 0 V H0 to 0D0 at –10 mA

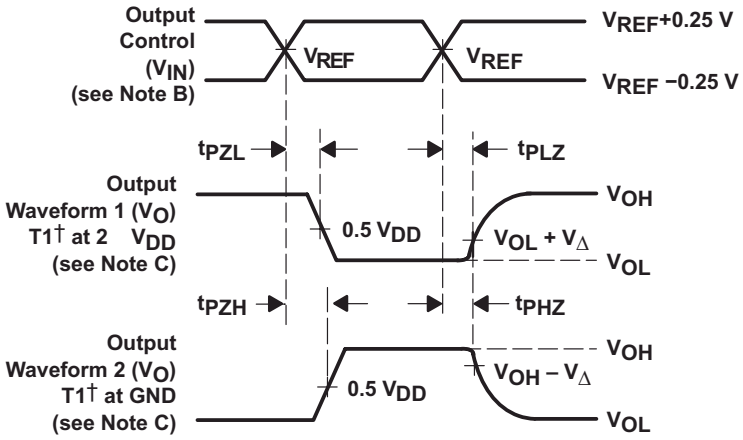
図 6-1. ON-State Resistance Across Temperature

7 Parameter Measurement Information

7.1 Enable and Disable Times



TEST	V_{DD}	T1†	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	1.8 V ± 0.1 V	2 × V_{DD}	1 kΩ	GND	6 pF	0.125 V
t_{PHZ}/t_{PZH}	1.8 V ± 0.1 V	GND	1 kΩ	V_{DD}	6 pF	0.125 V



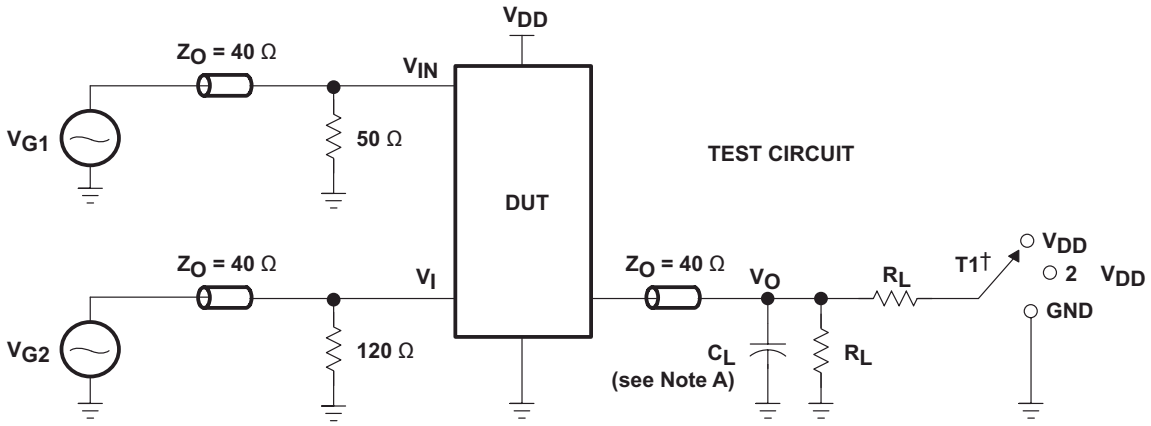
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

† T1 is an external terminal.

A. C_L includes probe and jig capacitance.
B. Output control applies to select (S0, S1) inputs.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. All input pulses are supplied by generators having the following characteristics: Z_{OS} = 50 Ω, rising and falling edge rate is 1 V/ns.
E. The outputs are measured one at a time, with one transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.

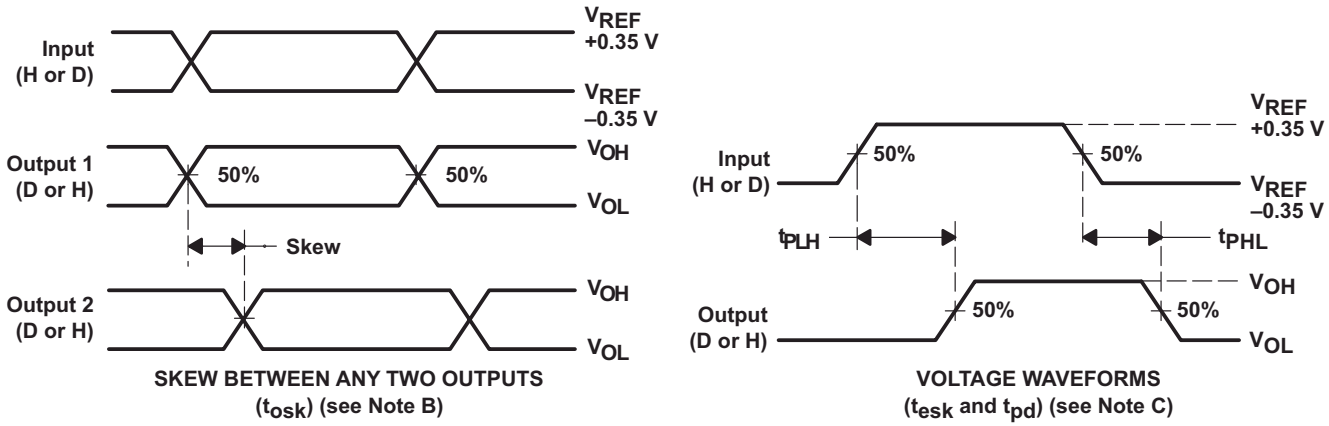
図 7-1. Test Circuit and Voltage Waveforms

7.2 Skew and Propagation Delay Times



TEST	V_{DD}	T1†	R_L	V_I	C_L
t_{pd}	1.8 V ± 0.1 V	V_{DD}	150 Ω	See waveform	6 pF
t_{osk}	1.8 V ± 0.1 V	V_{DD}	150 Ω	See waveform	6 pF
t_{esk}	1.8 V ± 0.1 V	V_{DD}	150 Ω	See waveform	6 pF

† T1 is an external terminal.



A. C_L includes probe and jig capacitance.
B. t_{osk} is the difference in output voltage from channel to channel in a specific device.
C. t_{PLH} and t_{PHL} are the same as t_{pd} and $t_{esk} = |t_{PLH} – t_{PHL}|$
D. All input pulses are supplied by generators having the following characteristics: Z_{OS} = 50 Ω, rising and falling edge rate is 1 V/ns.
E. The outputs are measured one at a time, with one transition per measurement.

図 7-2. Test Circuit and Voltage Waveforms

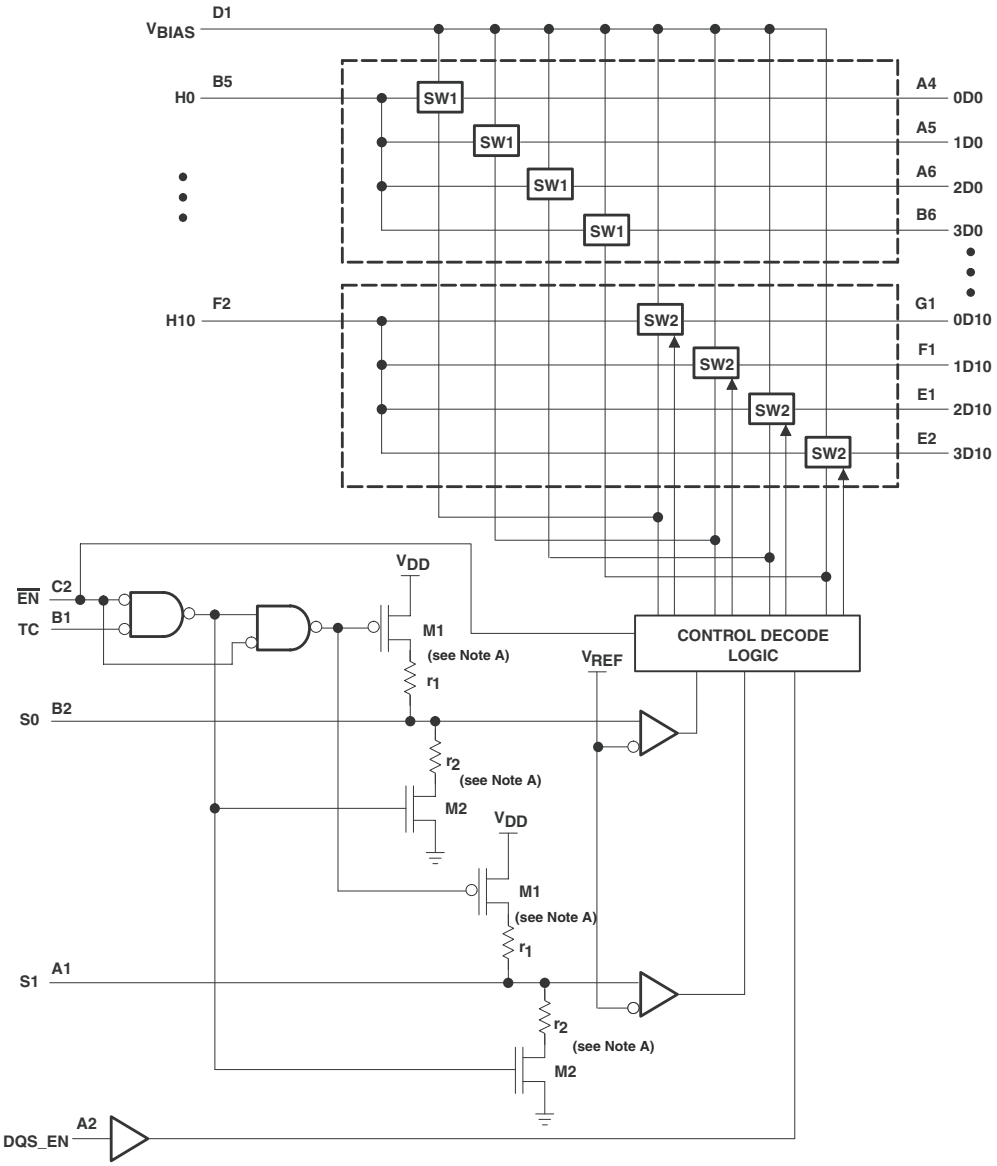
8 Detailed Description

8.1 Overview

The SN74CBTU4411 device is organized as an 11-bit 1-of-4 multiplexer or demultiplexer with a single switch-enable ($\overline{EN}$) input. When $\overline{EN}$ is low, the switch is enabled and the H port is connected to one of the D ports. Ports D0 to D9 for the disabled channels are connected to V_{BIAS} through a 400-Ω resistor. DQS_EN determines the output voltage for the disabled D10 ports. When DQS_EN is low, this voltage is V_{BIAS}. When DQS_EN is high, the disabled D10 ports are connected to an internal voltage (V_{BIAS_DQS}) source, which is approximately equal to 0.7 V_{DD}.

When $\overline{EN}$ is high, all the channels are disabled. Ports D0 to D9 are connected to V_{BIAS}. For the D10 port, the disabled output voltage is determined by the DQS_EN input. When DQS_EN is low, this voltage is V_{BIAS}. When DQS_EN is high, this voltage is V_{DD}.

8.2 Functional Block Diagram



A. $r_1 + r_{on}$ (M1), $r_2 + r_{on}$(M2) = 160 Ω typical

図 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. The $\overline{EN}$ and TC inputs determine the internal termination for S0 and S1 inputs. When $\overline{EN}$ is low, the termination is determined by the TC input. When both $\overline{EN}$ and TC are low, termination resistors are disconnected from the S inputs. When $\overline{EN}$ is low and TC is high, both pullup and pulldown resistors are connected to the S inputs. When $\overline{EN}$ is high, only the pulldown termination resistors are connected to the S inputs, regardless of the voltage level at the TC input.

8.4 Device Functional Modes

表 8-1 and 表 8-2 list the functional modes of the SN74CBTU4411.

表 8-1. Function Table

INPUTS				INPUT/OUTPUT Hn	FUNCTION
$\overline{EN}$	DQS_EN	S1	S0		
L	L	L	L	0Dn	Hn = 0Dn 1Dn, 2Dn, 3Dn connected to V_{BIAS}
L	L	L	H	1Dn	Hn = 1Dn 0Dn, 2Dn, 3Dn connected to V_{BIAS}
L	L	H	L	2Dn	Hn = 2Dn 0Dn, 1Dn, 3Dn connected to V_{BIAS}
L	L	H	H	3Dn	Hn = 3Dn 0Dn, 1Dn, 2Dn connected to V_{BIAS}
L	H	L	L	0Dn	H0–H9 = 0D0–0D9 1D0–1D9, 2D0–2D9, 3D0–3D9 connected to V_{BIAS} H10 = 0D10 1D10, 2D10, 3D10 connected to V_{BIAS_DQS} (1)
L	H	L	H	1Dn	H0–H9 = 1D0–1D9 0D0–0D9, 2D0–2D9, 3D0–3D9 connected to V_{BIAS} H10 = 1D10 0D10, 2D10, 3D10 connected to V_{BIAS_DQS} (1)
L	H	H	L	2Dn	H0–H9 = 2D0–2D9 0D0–0D9, 1D0–1D9, 3D0–3D9 connected to V_{BIAS} H10 = 2D10 0D10, 1D10, 3D10 connected to V_{BIAS_DQS} (1)
L	H	H	H	3Dn	H0–H9 = 3D0–3D9 0D0–0D9, 1D0–1D9, 2D0–2D9 connected to V_{BIAS} H10 = 3D10 0D10, 1D10, 2D10 connected to V_{BIAS_DQS} (1)
H	L	X	X	Z	0Dn, 1Dn, 2Dn, 3Dn connected to V_{BIAS}
H	H	X	X	Z	0D0–0D9, 1D0–1D9, 2D0–2D9, 3D0–3D9 connected to V_{BIAS} 0D10, 1D10, 2D10, 3D10 connected to V_{DD}

(1) V_{BIAS_DQS} is an internal voltage condition.

表 8-2. Function Table Continued

INPUTS		FUNCTION
$\overline{EN}$	TC	
L	L	Termination resistors disconnected from S inputs
L	H	Termination resistors connected with S inputs
H	X	Pulldown termination resistor connected and pullup termination resistor disconnected from the S inputs

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74CBTU4411 is suitable for DDR-II applications where high-bandwidth is required. This device has low and flat ON resistance and has internal termination control inputs. The D-ports are precharged by Bias voltage (V_{BIAS}).

9.2 Typical Application

SN74CBTU4411 is an 11 bit, 1:4 Mux and suitable for high-bandwidth applications.

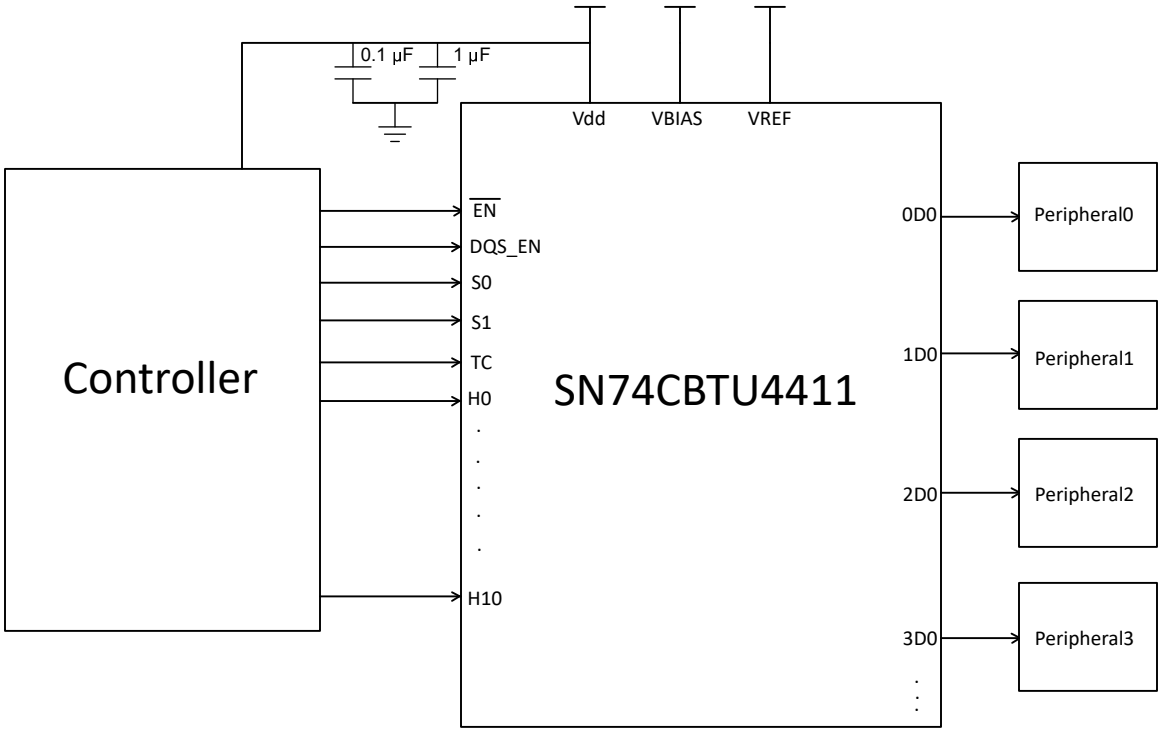


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

SN74CBTU4411 supports 400-MHz bandwidth on the D or H ports and 84 MHz on the S port. The Enable control from the controller must be activated and depending on the select pins, the data is transferred into one of the peripherals 0 to 3. The Enable control at high will tristate the input or output as per the functional table. See セクション 6.3 and セクション 6.1 for other voltage, current and handling parameters.

9.2.2 Detailed Design Procedure

The H port signal from the controller can go to one of the 4 peripheral ports depending on the select inputs S0 and S1. The V_{BIAS} and V_{REF} can be determined from セクション 6.3.

1. Recommended Input Conditions
   - For specified high and low levels for all the input control pins, see V_{IH} and V_{IL} in セクション 6.3.
   - Inputs are not overvoltage tolerant and should be below the valid V_{DD}.
2. Recommend Input/Output Conditions
   - The absolute maximum continuous on state switch current for any I/O should not exceed ±100 mA.
   - The I/O voltage range should not be above V_{DD} and below ground.

9.2.3 Application Curve

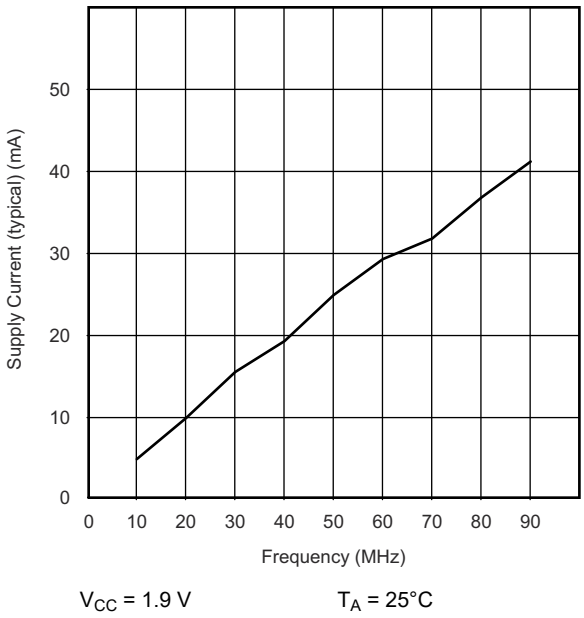


図 9-2. Supply Current (Typical) vs Frequency Data

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in セクション 6.3.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor. If there are multiple V_{CC} pins, TI recommends a 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

図 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the I/Os, so they also cannot float when disabled.

11.2 Layout Example

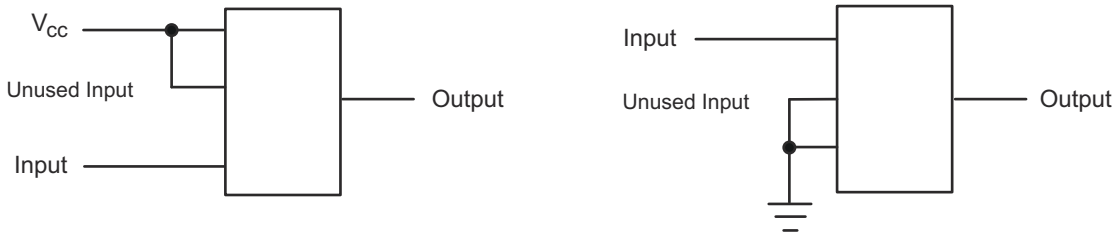


図 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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13 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBTU4411ZSTR	Active	Production	NFBGA (ZST) | 72	2000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	CTU4411
SN74CBTU4411ZSTR.A	Active	Production	NFBGA (ZST) | 72	2000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	CTU4411

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

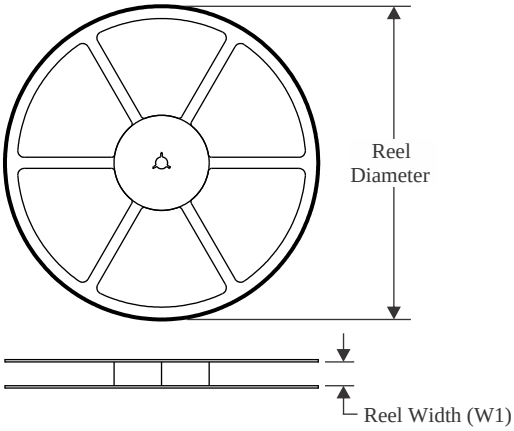
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

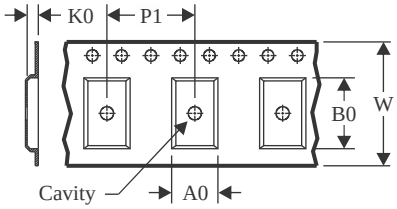
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

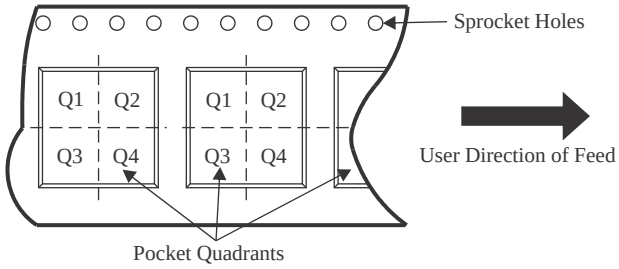


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

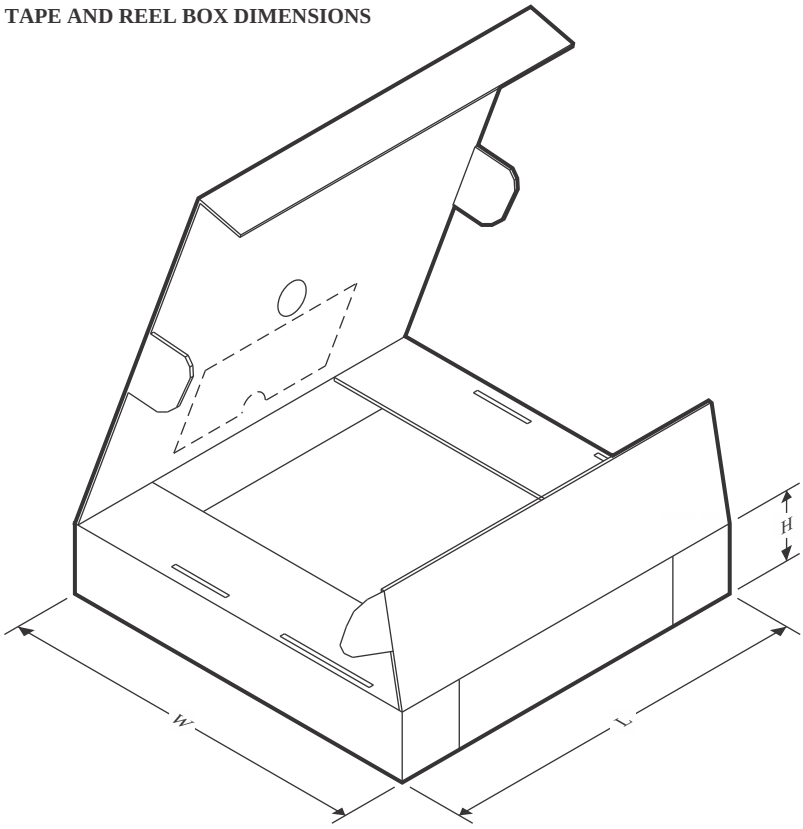
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTU4411ZSTR	NFBGA	ZST	72	2000	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

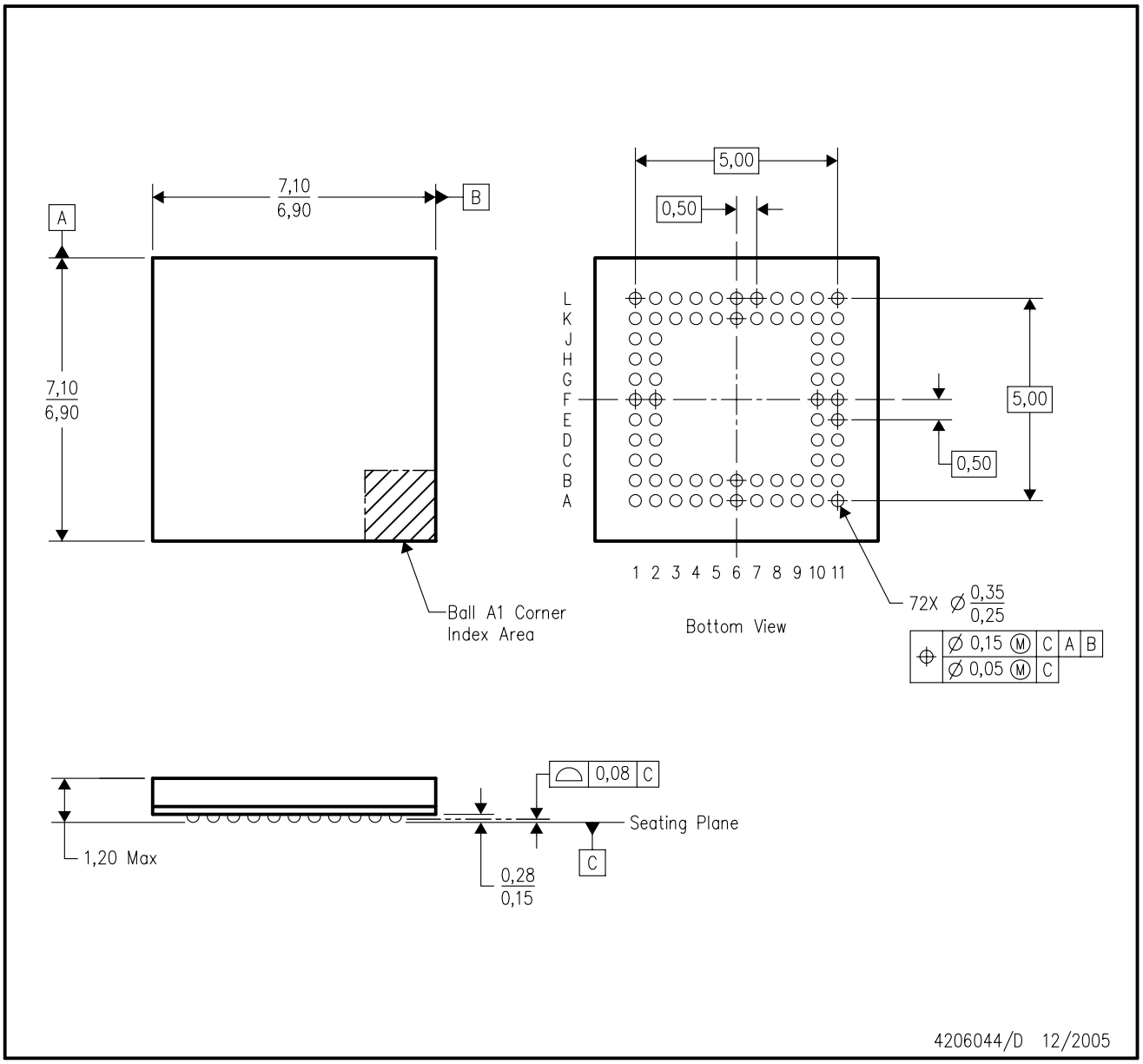
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTU4411ZSTR	NFBGA	ZST	72	2000	336.6	336.6	31.8

ZST (S–PBGA–N72) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Complies to JEDEC MO–195 variation AD (depopulated).
D. This package is lead–free. Refer to the 72 GST package (drawing 4206043) for tin–lead (SnPb).

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最終更新日：2025 年 10 月