

SN74CBT3383C 10 ビット FET バス交換スイッチ / 5V バス・スイッチ -2V アンダーシュート保護機能搭載

1 特長

- 最大 -2V の A および B ポートのオフ・アイソレーション用アンダーシュート保護
- 伝播遅延がゼロに近い双方向データ・フロー
- 低いオン抵抗 (r_{on}) 特性 ($r_{on} = 3\Omega$: 標準値)
- 低い入力および出力容量により負荷および信号歪みが最小化 ($C_{io}(OFF) = 8pF$: 標準値)
- データおよび制御入力にアンダーシュート・クランプ・ダイオードを搭載
- 低消費電力 ($ICC = 3\mu A$: 最大値)
- 4V~5.5V のデータ I/O で動作する V_{CC} は、0~5V の信号レベル (0.8V、1.2V、1.5V、1.8V、2.5V、3.3V、5V) をサポート
- 制御入力を TTL または 5V/3.3V CMOS 出力で駆動可能
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22-2000V 人体モデル (A114-B、Class II) – 1000V 荷電デバイス・モデル (C101) に準拠した ESD 性能テスト済み
- デジタルとアナログの両方のアプリケーションに対応: PCI インターフェイス、メモリ・インターリーブ、バス絶縁、低歪みの信号ゲーティング

2 アプリケーション

- エンタープライズ・サーバー
- イーサネット・スイッチ
- ルータ
- サーバー
- 産業用 PC

3 概要

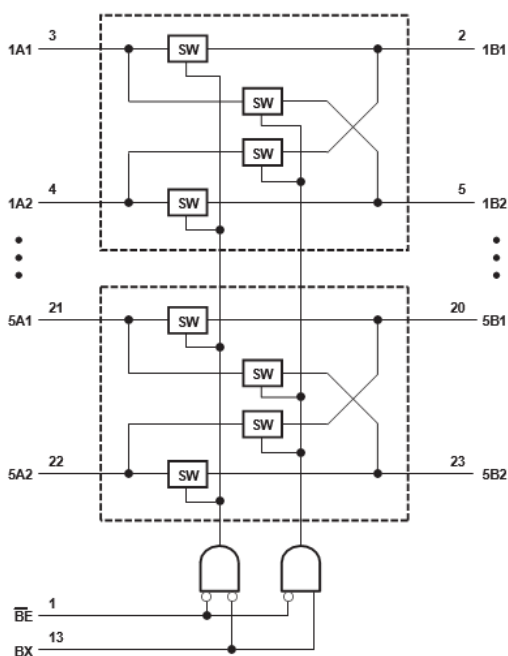
SN74CBT3383C は、オン抵抗 (r_{on}) が低い伝播遅延を最小限に低減できる高速 TTL 互換 FET バス・スイッチです。SN74CBT3383C の A および B ポートのアクティブ・アンダーシュート保護回路は、アンダーシュート・イベントを検出し、スイッチが適切なオフ状態に維持されるようにすることで、最大 -2V のアンダーシュートを保護します。

SN74CBT3383C は、10 ビットのバス・スイッチ、または単一の出力イネーブル ($\overline{BE}$) 入力を持つ 5 ビットのバス交換スイッチとして構成され、4 つの信号ポート間でデータを交換できます。セレクト (BX) 入力は、バス交換スイッチのデータ・パスを制御します。 $\overline{BE}$ が Low のとき、A ポートは B ポートに接続され、ポート間の双方向データ・フローが可能になります。 $\overline{BE}$ が High のとき、A ポートと B ポートの間に高インピーダンス状態が存在します。

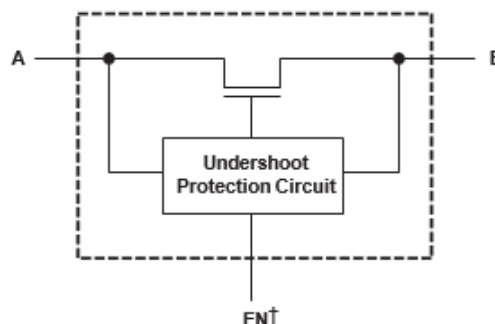
パッケージ情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
SN74CBT3383C	DBQ (SSOP, 24)	8.65mm × 3.90mm
	DW (SOIC, 24)	15.40mm × 7.50mm
	PW (TSSOP, 24)	7.80mm × 4.40mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)



概略回路図、各 FET スイッチ (SW)



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2004) to Revision A (December 2022)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• 「アプリケーション」、「ピン構成および機能」、「ESD 定格」、「熱に関する情報」、「詳細説明」、「アプリケーションと実装」、「電源に関する推奨事項」、「レイアウト」の各セクションを追加.....	1
• (RLOI) により、DGV および DB パッケージ情報をデータシートから削除.....	1
• Updated the <i>Design Requirements</i> section.....	11

5 概要 (続き)

このデバイスは、 I_{off} を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。 I_{off} 機能により、電源オフ時に損傷を引き起こすような電流がデバイスに逆流しないことが保証されます。デバイスは、電源オフ時は絶縁されています。

電源オンまたは電源オフ時に高インピーダンス状態を確保するため、 $\overline{BE}$ はプルアップ抵抗経路で V_{CC} に接続されます。この抵抗の最小値は、ドライバの電流シンク能力によって決定されます。

6 Pin Configuration and Functions

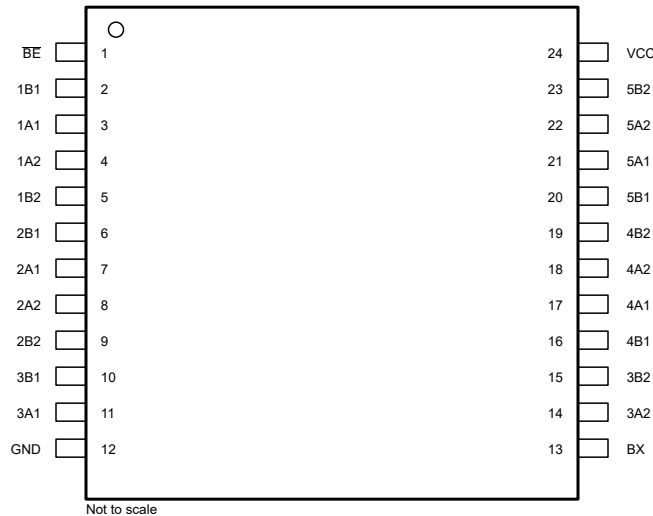


图 6-1. DBQ, DW, or PW Package, 24-Pin SSOP, SOIC, and TSSOP (Top View)

表 6-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
BE	1	I	Active-low input enable pin
1B1	2	I/O	I/O pin, can be input or output
1A1	3	I/O	I/O pin, can be input or output
1A2	4	I/O	I/O pin, can be input or output
1B2	5	I/O	I/O pin, can be input or output
2B1	6	I/O	I/O pin, can be input or output
2A1	7	I/O	I/O pin, can be input or output
2A2	8	I/O	I/O pin, can be input or output
2B2	9	I/O	I/O pin, can be input or output
3B1	10	I/O	I/O pin, can be input or output
3A1	11	I/O	I/O pin, can be input or output
GND	12	G	Ground
BX	13	I	Select pin. This controls the data path of the bus exchange. When BX is low xA1 = xB1 and xA2 port = xB2. When BX is high xA1 = xB2 and xA2 = xB1
3A2	14	I/O	I/O pin, can be input or output
3B2	15	I/O	I/O pin, can be input or output
4B1	16	I/O	I/O pin, can be input or output
4A1	17	I/O	I/O pin, can be input or output
4A2	18	I/O	I/O pin, can be input or output
4B2	19	I/O	I/O pin, can be input or output
5B1	20	I/O	I/O pin, can be input or output
5A1	21	I/O	I/O pin, can be input or output
5A2	22	I/O	I/O pin, can be input or output
5B2	23	I/O	I/O pin, can be input or output
V _{CC}	24	P	Power pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3) (4) (5) (6)}

		MIN	MAX	UNIT
Supply voltage range, V_{CC}		-0.5	7	V
Control input voltage range, V_{IN} (see notes 1 and 2)		-0.5	7	V
Switch I/O voltage range, $V_{I/O}$ (see notes 1, 2, and 3)		-0.5	7	V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		-50		mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		-50		mA
ON-state switch current, $I_{I/O}$ (see note 4)		128		mA
Continuous current through V_{CC} or GND terminals		100		mA
Package thermal impedance, θ_{JA} (see note 5):				
T_{stg}	DBQ package	61		°C /W
	DW package	46		°C /W
	PW package	88		°C /W
	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network ground terminal GND.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
- (5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused control input of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74CBT3383			UNIT
		DBQ (SSOP)	DW (SOIC)	PW (TSSOP)	
		24 PINS	24 PINS	24 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	61.0	46.0	88.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	22.1	19.9	26.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	—	19.33	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}	Control inputs	V _{CC} = 4.5 V,	I _{IN} = -18 mA				-1.8	V
V _{IKU}	Data inputs	V _{CC} = 5 V,	0 mA > I _I ≥ -50 mA, V _{IN} = V _{CC} or GND,	Switch OFF			-2	V
I _{IN}	Control inputs	V _{CC} = 5.5 V,	V _{IN} = V _{CC} or GND				±1	mA
I _{OZ} † ⁽³⁾		V _{CC} = 5.5 V,	V _O = 0 to 5.5 V, V _I = 0,	Switch OFF, V _{IN} = V _{CC} or GND			±10	mA
I _{off}		V _{CC} = 0,	V _O = 0 to 5.5 V, V _I = 0				10	mA
I _{CC}		V _{CC} = 5.5 V,	I _{I/O} = 0, V _{IN} = V _{CC} or GND,	Switch ON or OFF			3	mA
ΔI _{CC} ⁽⁴⁾	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
C _{in}	Control inputs	V _{IN} = 3 V or 0				3.5		pF
C _{io} (OFF)		V _{I/O} = 3 V or 0,	Switch OFF, V _{IN} = V _{CC} or GND			8		pF
C _{io} (ON)		V _{I/O} = 3 V or 0,	Switch ON, V _{IN} = V _{CC} or GND			18.5		pF
r _{on} ⁽⁵⁾		V _{CC} = 4 V, TYP at V _{CC} = 4 V	V _I = 2.4 V,	I _O = -15 mA		8	12	Ω
		V _{CC} = 4.5 V	V _I = 0	I _O = 64 mA		3	6	
				I _O = 30 mA		3	6	
			V _I = 2.4 V,	I _O = -15 mA		5	10	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

(2) All the typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. The lower of the voltages of the two (A or B) terminals determines the ON-state resistance.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4 V		VCC = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or B	B or A	0.24			0.15	ns
$t_{pd(s)}$	BX	A or B	5.8		1	5.3	ns
t_{en}	$\overline{BE}$	A or B	6.3		1	5.8	ns
t_{dis}	$\overline{BE}$	A or B	6		1	6	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

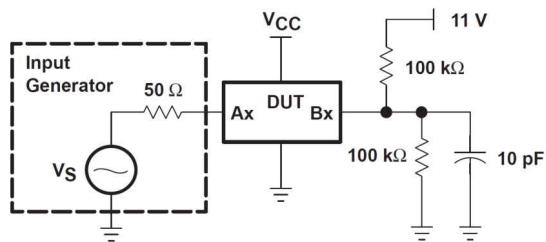
7.7 Undershoot Characteristics

over operating free-air temperature range (unless otherwise noted)

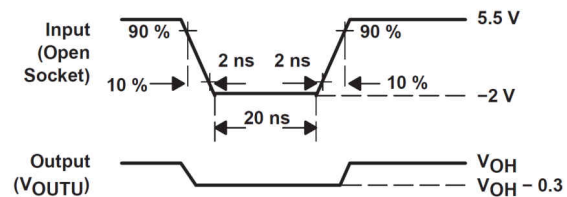
PARAMETER	TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OUTU}	$V_{CC} = 5.5 \text{ V}$,	Switch OFF,	$V_{IN} = V_{CC} \text{ or GND}$	2	$V_{OH} - 0.3$		V

(1) All typical values are at $V_{CC} = 5 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

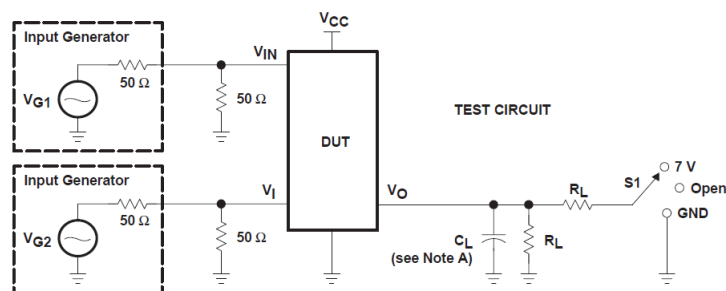
8 Parameter Measurement Information



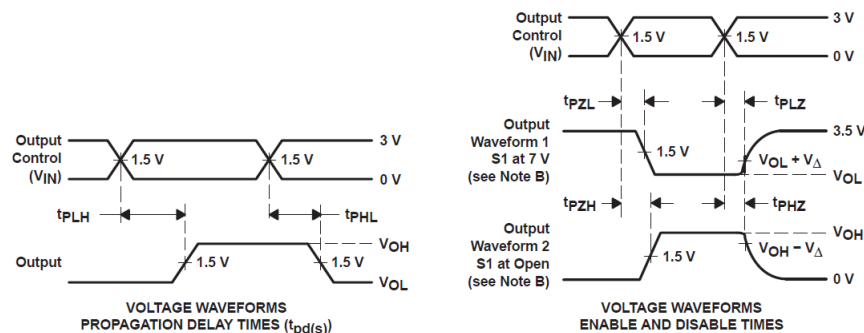
8-1. Device Test Setup



8-2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)



TEST	V_{CC}	S1	R_L	V_I	C_L	V_{Δ}
$t_{pd}(s)$	$5 V \pm 0.5 V$ 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	$5 V \pm 0.5 V$ 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	$5 V \pm 0.5 V$ 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V



- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as one or more t_{pds} . The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- All parameters and waveforms are not applicable to all devices.

8-3. Test Circuit and Voltage Waveforms

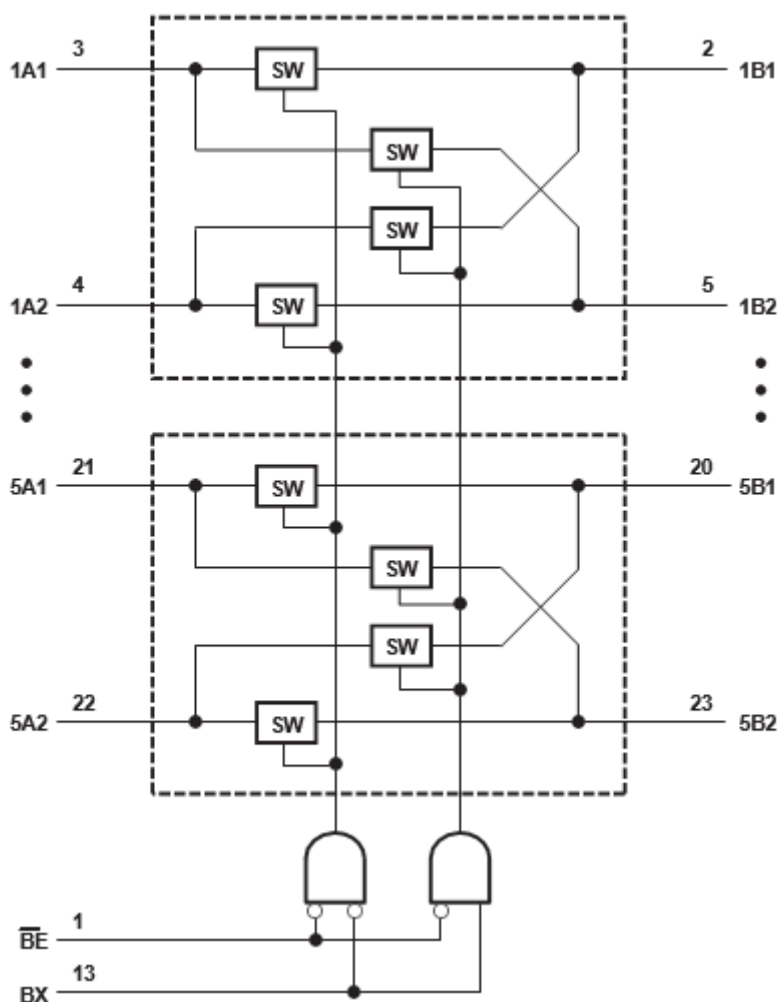
9 Detailed Description

9.1 Overview

The SN74CBT3383C provides ten high-speed CMOS TTL-compatible bus switches. The low ON-resistance of the SN74CBT3383C allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable ($\overline{BE}$) signal turns the switches on. The Bus Exchange (BX) signal provides nibble swap of the 1A and 1B pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a 5-wide, 2-to-1 multiplexer, to create low delay barrel shifters, and so forth.

Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3383C provides protection for undershoot up to -2 V by sensing and undershoot event and ensuring that the switch remains in the proper OFF state.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Bidirectional Data Flow With Near-Zero Propagation Delay

The SN74CBT3383C features a low propagation delay or t_{pd} that works great for multiple rail information transfer (for example, from 1A1 to 1B1 and 1A2 to 1B2). However, the SN74CBT3383C also features BUS exchange functionality, which allows for bidirectional data transfers from the inputs and outputs connected on the B side. By enabling the BX pin, the outputs are now crossed or exchanged. Data can now flow from 1A1 to 1B2 and 1A2 to 1B1 with little to no propagation delay. This can be used to enable byte swapping of buses within a system or to create a 5-wide, 2-to-1 multiplexer.

9.4 Device Functional Modes

**表 9-1. Function Table
(Each 5-Bit Bus-Exchange)**

INPUTS		INPUTS/OUTPUTS		FUNCTION
BE	BX	1A1 – 5A1	1A2 – 5A2	
L	L	1B1 – 5B1	1B2 – 5B2	A1 port = B1 port, A2 port = B2 port
L	H	1B2 – 5B2	1B1 – 5B1	A1 port = B2 port, A2 port = B1 port
H	X	Z	Z	Disconnect

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The SN74CBT3383C can be used to multiplex up to 5 channels simultaneously in a 2:1 configuration. 図 10-1 shows a 2-bit bus being multiplexed between two devices. The $\overline{BE}$ and BX pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires only one bit control or exchange, then remember to tie the unused bit to high or low. By using another bus controller, exchange can be enabled across A1 and A2 to B1 and B2, allowing for greater system communication.

10.2 Typical Application

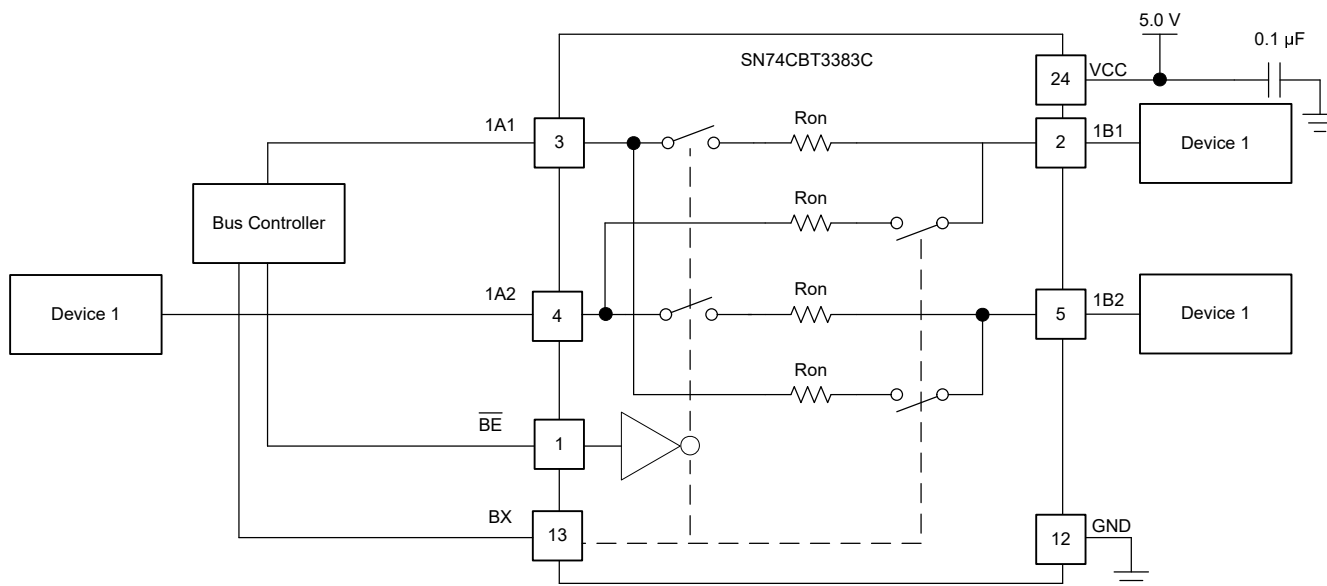


図 10-1. 1:2 Multiplexer or Bus and Selector Using 1 Bus Controller

10.2.1 Design Requirements

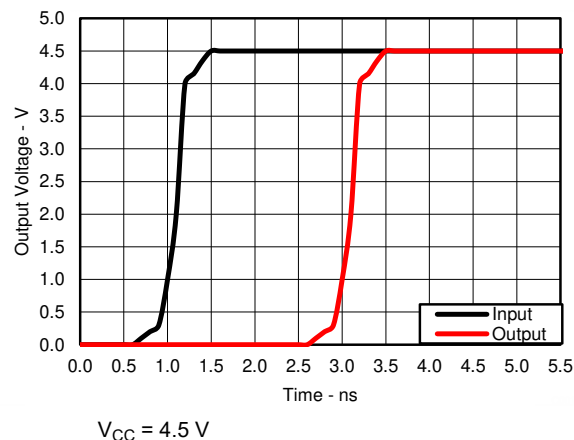
- Recommended input conditions:
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) section.
- Recommended output conditions:
 - Load currents must not exceed 128 mA per channel.
- Frequency selection criteria:
 - Added trace resistance and capacitance can reduce maximum frequency capability; use layout practices as directed in the [Layout](#) section.

10.2.2 Detailed Design Procedure

The 2-bit bus is connected directly to 1A1 and 1A2 on the SN74CBT3383C, which essentially combines in the bus controller to form a single input or split bus bits. When $\overline{BE}$ is low and BX is low, the selected bus uses 1A1 and 1B1 as inputs and outputs. This means that Device 1 is connected to the bus controller and Device 2 is connected to Device 3 when $\overline{BE}$ is low and BX is low. While keeping $\overline{BE}$ low and BX high, communication is enabled from the bus controller to Device 2 and from Device 1 to Device 3. This setup is especially useful when two controllers or devices need to share the same data from Device 1 and Device 2 and the bus addresses are limited or hard coded.

The 0.1- μ F capacitor on V_{CC} is a decoupling capacitor and should be placed as close to the device as possible.

10.2.3 Application Curve



10-2. Propagation Delay (t_{pd}) Simulation Results

11 Power Supply Recommendations

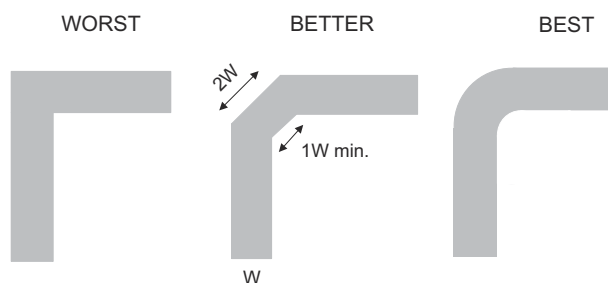
The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#) table. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of the trace width. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.  12-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

12.2 Layout Example



 12-1. Trace Example

13 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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13.3 Trademarks

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13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBT3383CDBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3383C
SN74CBT3383CDBQR.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3383C
SN74CBT3383CDW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C
SN74CBT3383CDW.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C
SN74CBT3383CDWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C
SN74CBT3383CDWR.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C
SN74CBT3383CPWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU383C
SN74CBT3383CPWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU383C

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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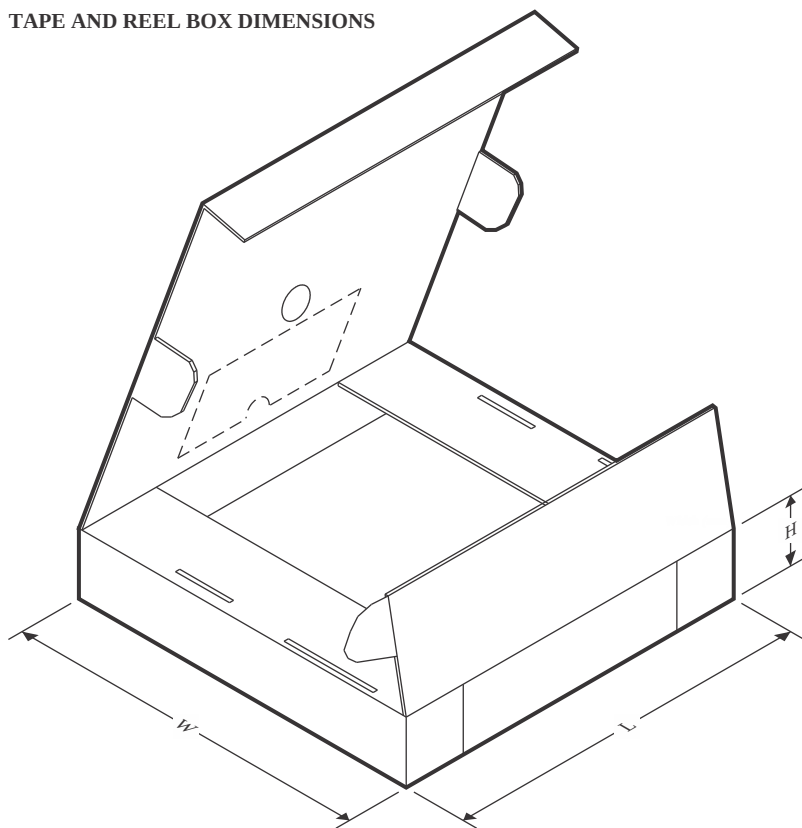
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3383CDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3383CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBT3383CPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3383CDBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
SN74CBT3383CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74CBT3383CPWR	TSSOP	PW	24	2000	367.0	367.0	38.0

TUBE

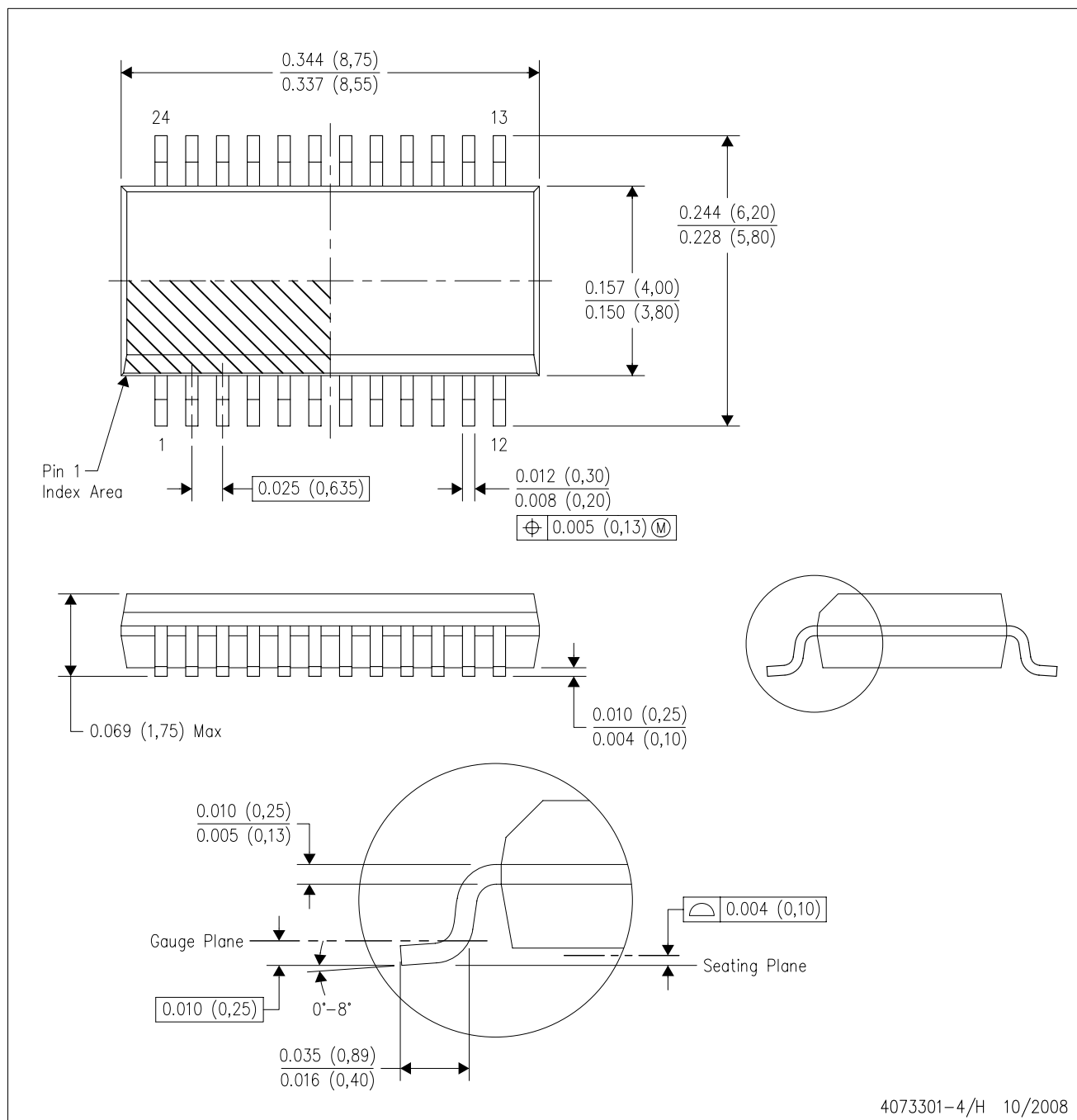


*All dimensions are nominal

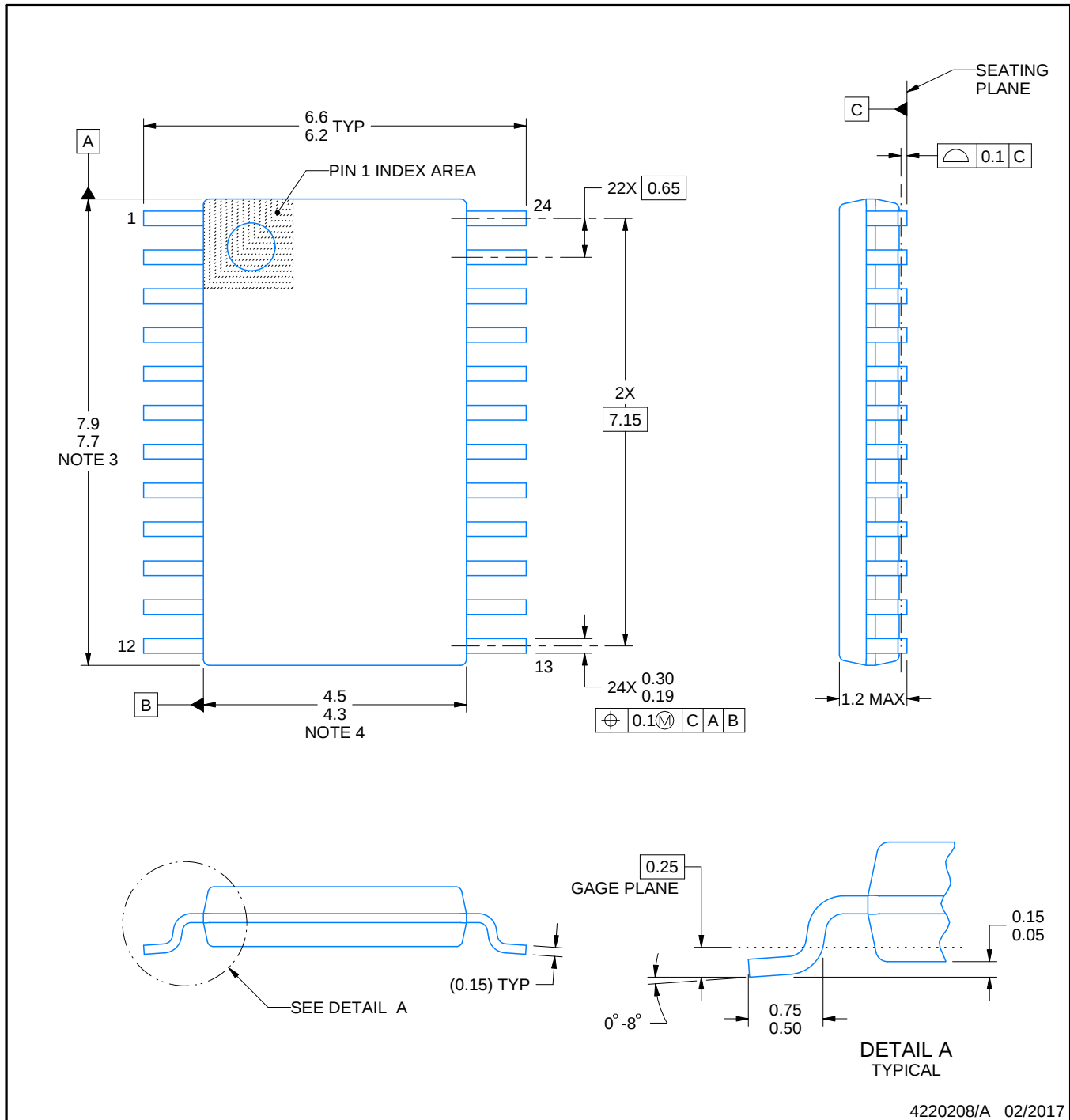
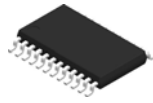
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT3383CDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CBT3383CDW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.



4220208/A 02/2017

NOTES:

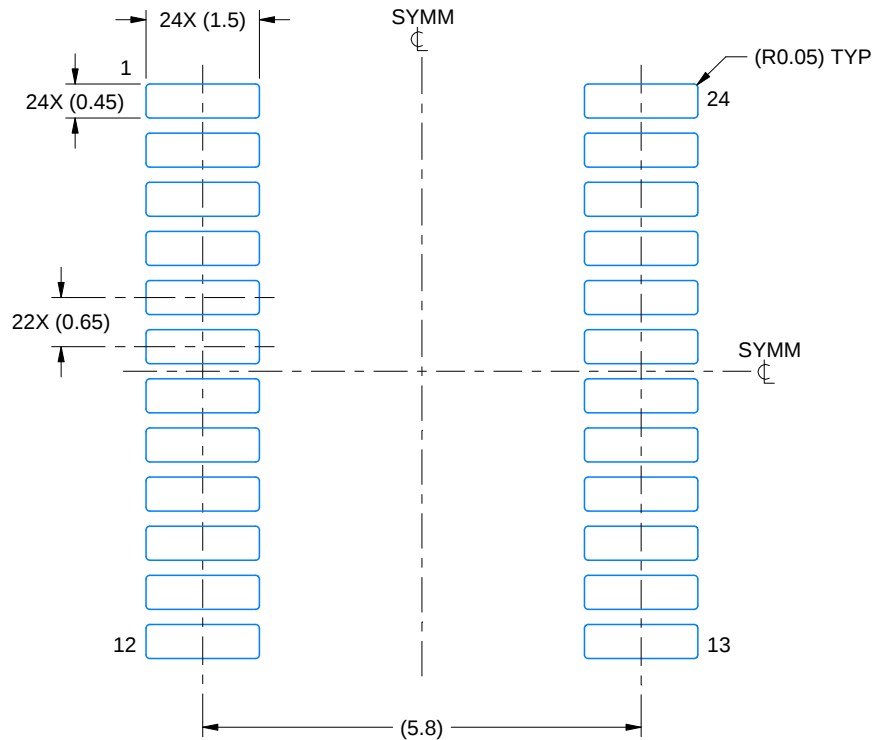
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

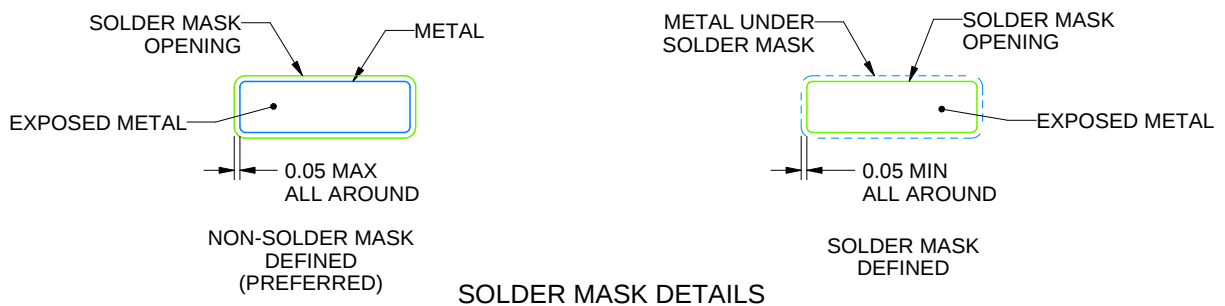
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

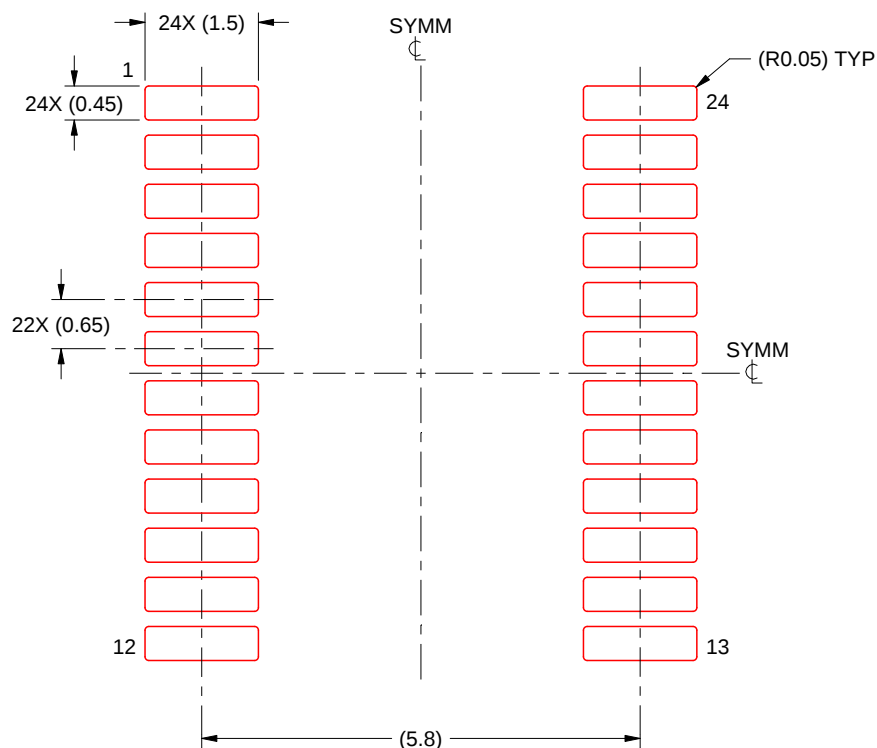
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

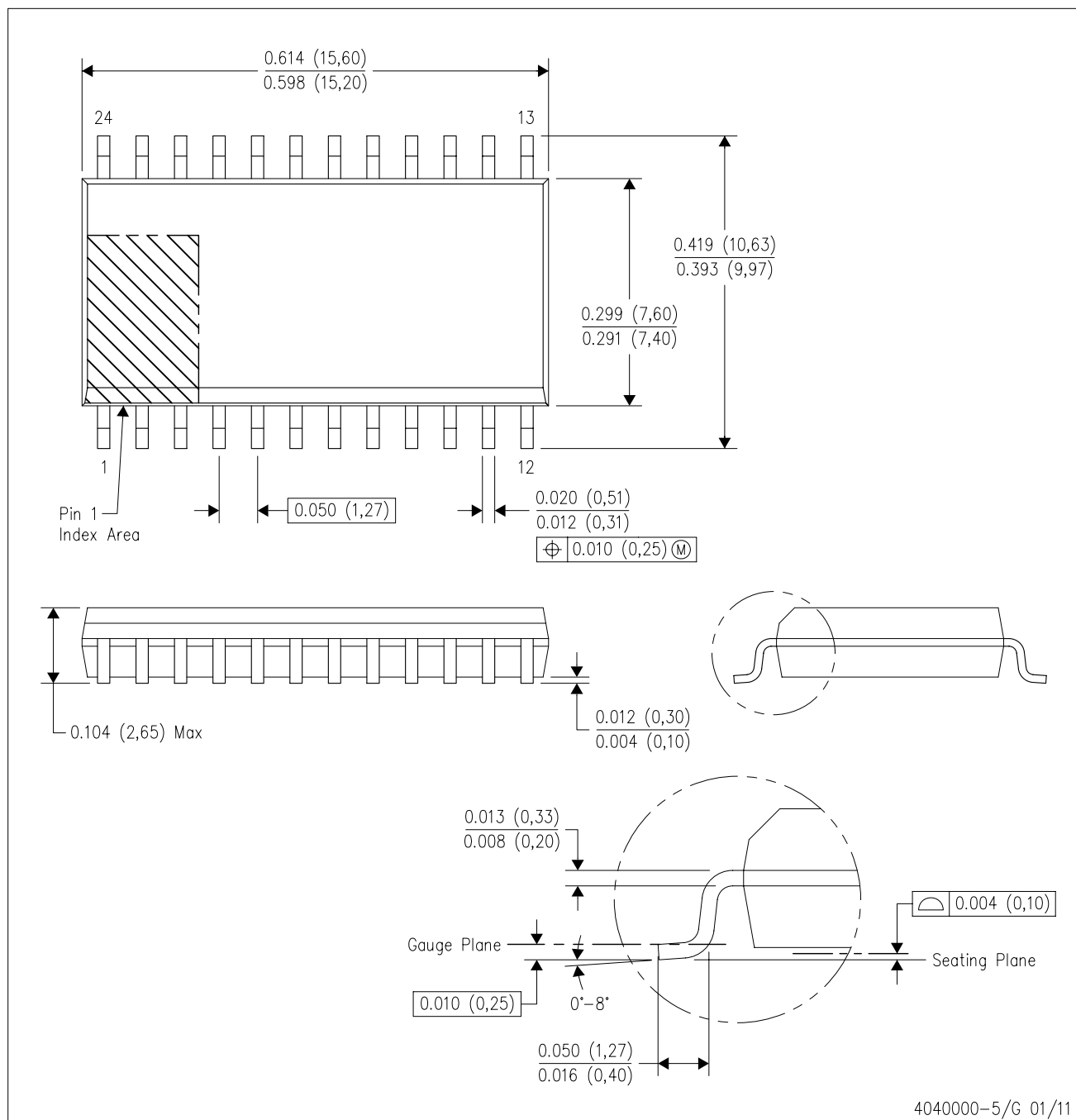
4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

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