SN74CBT3251 1-of-8 FET Multiplexer and Demultiplexer

1 Features

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Low Crosstalk Between Switches
- Fast Switching and Propagation Speeds
- Operating Temperature Range: –40°C to 85°C

2 Applications

- Digital Radio
- Signal Gating
- Factory Automation
- Televisions
- Appliances
- Programmable Logic Circuits
- Sensors

3 Description

The SN74CBT3251 is a 1-of-8 high-speed TTL-compatible FET multiplexer and demultiplexer. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

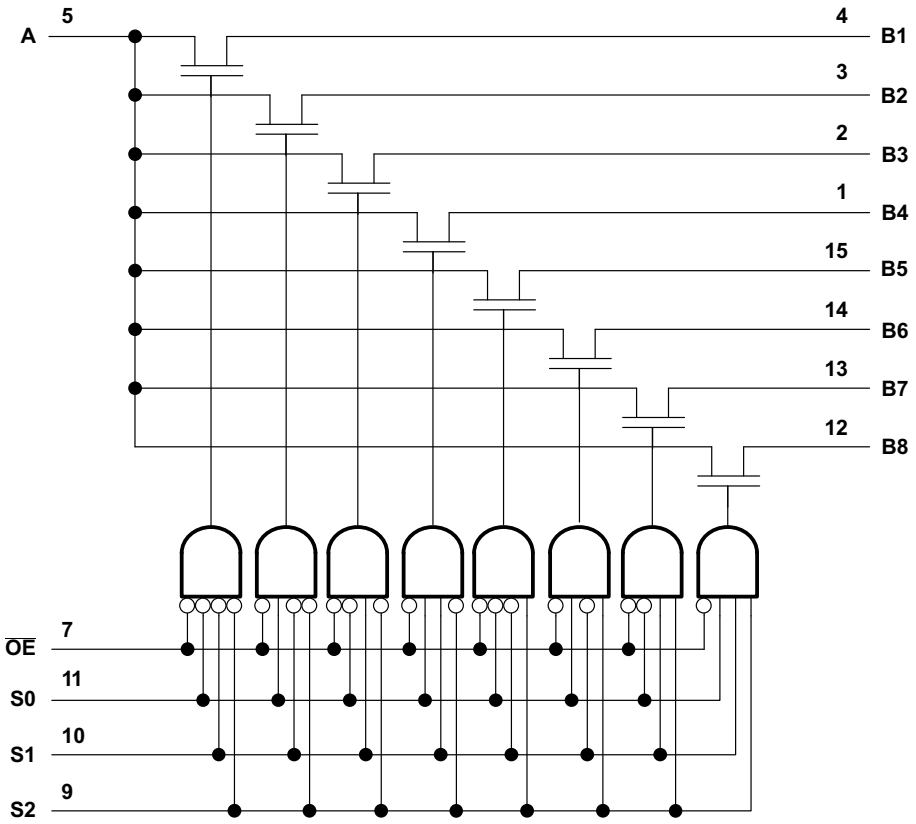
When output enable ($\overline{OE}$) is low, the SN74CBT3251 is enabled, and S0, S1, and S2 select one of the B outputs for the A-input data.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CBT3251RGY	VQFN (16)	3.50 mm × 4.00 mm
SN74CBT3251DBQ	SSOP (16)	3.90 mm × 4.90 mm
SN74CBT3251PW	TSSOP (16)	4.40 mm × 5.00 mm
SN74CBT3251DB	SSOP (16)	5.30 mm × 6.20 mm
SN74CBT3251D	SOIC (16)	3.91 mm × 9.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagram of the SN74CBT3251



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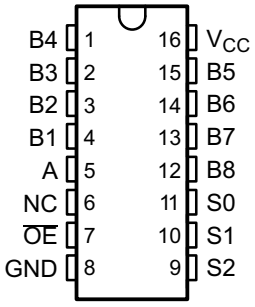
4 Revision History

Changes from Revision L (January 2004) to Revision M **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

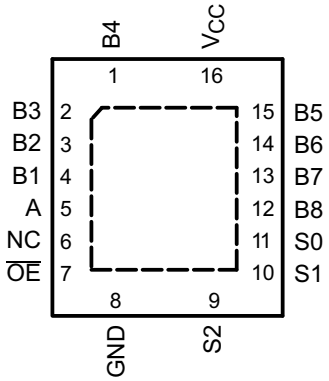
5 Pin Configuration and Functions

D, DB, DBQ, or PW Packages
16-Pin SOIC, SSOP, or TSSOP
Top View



NC − No internal connection

RGY Package
16-Pin VQFN
Top View



NC − No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	B4	I/O	Port B4
2	B3	I/O	Port B3
3	B2	I/O	Port B2
4	B1	I/O	Port B1
5	A	I/O	Common OUT/IN
6	NC	—	No Connect
7	$\overline{OE}$	I	Enable Ports (Active Low). See Table 1.
8	GND	—	Ground
9	S2	I	Select Pin 2. See Table 1.
10	S1	I	Select Pin 1. See Table 1.
11	S0	I	Select Pin 0. See Table 1.
12	B8	I/O	Port B8
13	B7	I/O	Port B7
14	B6	I/O	Port B6
15	B5	I/O	Port B5
16	V_{CC}	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.5	7	V
Input voltage, V_I(2)	–0.5	7	V
Continuous channel current		128	mA
Input clamp current, I_K ($V_{I/O}$ < 0)		–50	mA
Maximum junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN74CBT3251					UNIT
		D (SOIC)	DB (SSOP)	DBQ (SSOP)	PW (TSSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73(2)	82(2)	90(2)	108(2)	39(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.6	49.0	59.0	41.6	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.8	49.4	50.1	51.9	20.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.3	10.5	13.9	4.0	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.4	48.8	49.7	51.3	20.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	6.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) The package thermal impedance is calculated in accordance with JESD 51-5.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA					–1.2	V
I_I		V_{CC} = 5.5 V, V_I = 5.5 V or GND					±1	µA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = VCC or GND					3	µA
ΔI_{CC}(2)	Control inputs	V_{CC} = 5.5 V; One input at 3.4 V, other inputs at V_{CC} or GND					2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0, $\overline{OE}$ = V_{CC}				17.5		pF
	B port	V_O = 3 V or 0, $\overline{OE}$ = V_{CC}				4		
r_{on}(3)		V_{CC} = 4 V, TYP at V_{CC} = 4 V, V_I = 2.4 V, I_I = 15 mA				14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V, I_I = 15 mA			10	15	

(1) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
(2) This is the increase in supply current for each input at the specified TTL voltage level, rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over operating free-air temperature free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}(1)	A or B	B or A	V_{CC} = 4 V		0.35	ns
			V_{CC} = 5 V ±0.5 V		0.24	
t_{pd}	S	A	V_{CC} = 4 V		6	ns
			V_{CC} = 5 V ±0.5 V	2	5.5	
t_{en}	S	B	V_{CC} = 4 V		6.4	ns
			V_{CC} = 5 V ±0.5 V	1.5	5.6	
	$\overline{OE}$	A or B	V_{CC} = 4 V		6.4	
			V_{CC} = 5 V ±0.5 V	1.6	5.8	
t_{dis}	S	B	V_{CC} = 4 V		6.8	ns
			V_{CC} = 5 V ±0.5 V	1.9	6.4	
	$\overline{OE}$	A or B	V_{CC} = 4 V		6	
			V_{CC} = 5 V ±0.5 V	2.3	6.2	

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Typical Characteristic

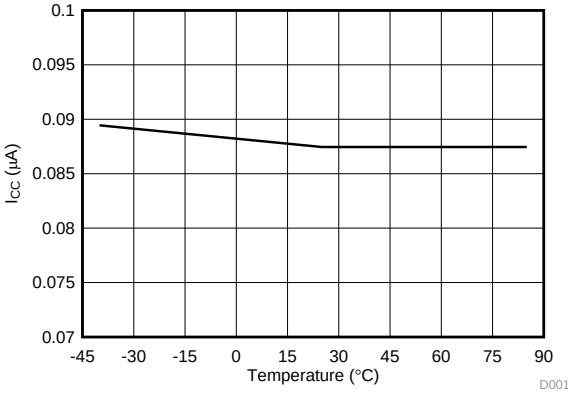
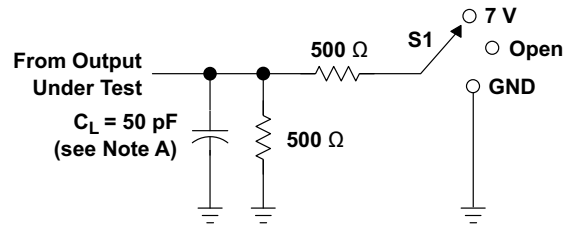


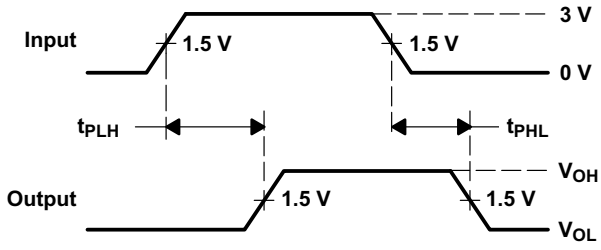
Figure 1. I_{CC} Variation With Temperature

7 Parameter Measurement Information

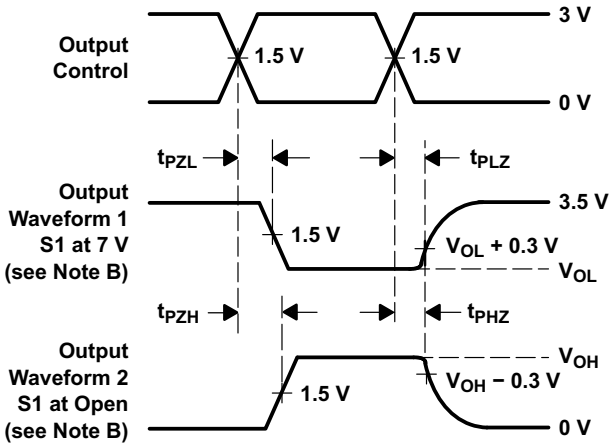


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CBT3251 device is a single 8-channel multiplexer with three binary control inputs, S_0, S_1, and S_2 and an $\overline{OE}$ (output enable, active low) input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

When they are used as demultiplexers, the CHANNEL IN/OUT terminals (B) are the outputs and the COMMON OUT/IN terminal (A) is the input.

8.2 Functional Block Diagram

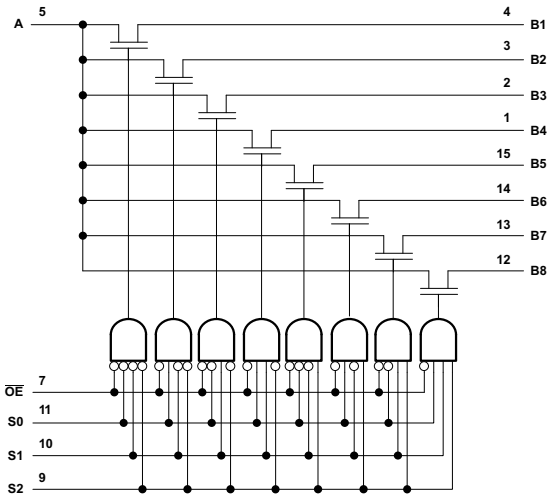


Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

The SN74CBT3251 1-of-8 FET multiplexers and demultiplexers can accept a wide range of analog signal levels from 0 V to 5 V. It has low Ron resistance, typically 5-Ω for V_{CC} = 5 V which allows very little signal loss through the switch. Binary address decoding on chip makes channel selection easy.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74CBT3251.

Table 1. Function Table (Each Multiplexer and Demultiplexer)

INPUTS				FUNCTION
$\overline{OE}$	S2	S1	S0	
L	L	L	L	A port = B1 port
L	L	L	H	A port = B2 port
L	L	H	L	A port = B3 port
L	L	H	H	A port = B4 port
L	H	L	L	A port = B5 port
L	H	L	H	A port = B6 port
L	H	H	L	A port = B7 port
L	H	H	H	A port = B8 port
H	X	X	X	Disconnect

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CBT351 device can be used for a wide variety of applications, including expanding MCU GPIOs.

9.2 Typical Application

One application of the SN74CBT3251 device is to use in conjunction with a microcontroller to poll a keypad. Figure 4 shows the basic schematic for such a polling system. The microcontroller uses the channel-select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This is a very robust setup that allows for simultaneous key presses with very little power consumption. It also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must frequently scan the keys for a press.

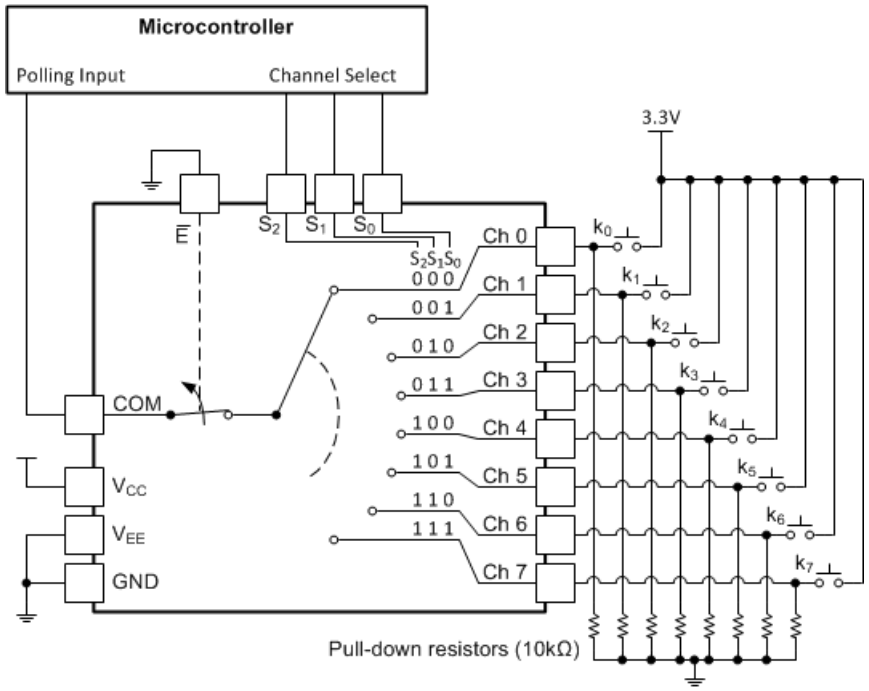


Figure 4. Keypad Polling Application

9.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For switch time specifications, see propagation delay times in *Recommended Operating Conditions*.
   - Inputs must not be pulled below ground.
   - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.

Typical Application (continued)

2. Input and output current consideration:
   – Load currents must not exceed per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.

9.2.3 Application Curve

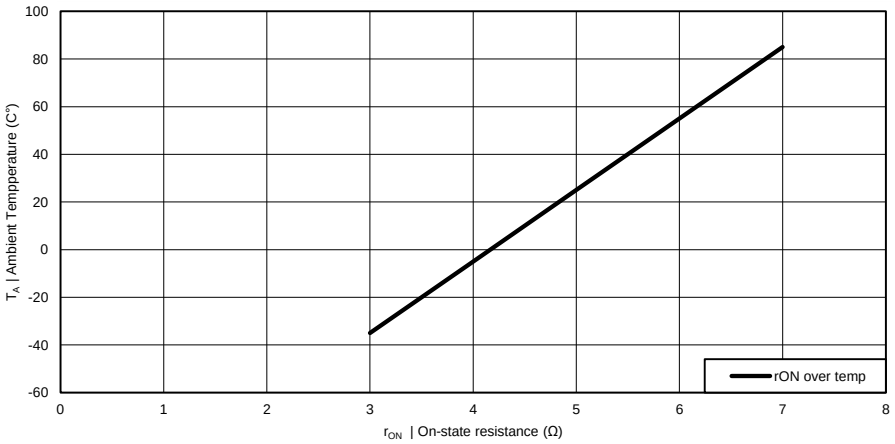


Figure 5. r_{ON} Over Temperature

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

11.2 Layout Example

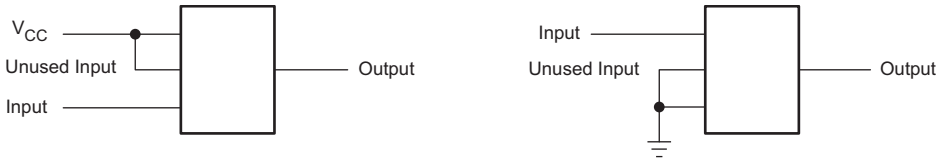


Figure 6. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBT3251D	NRND	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3251
SN74CBT3251D.A	NRND	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3251
SN74CBT3251DBQR	NRND	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU251
SN74CBT3251DBQR.A	NRND	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU251
SN74CBT3251DBR	NRND	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251
SN74CBT3251DBR.A	NRND	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251
SN74CBT3251DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3251
SN74CBT3251DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3251
SN74CBT3251PW	NRND	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251
SN74CBT3251PW.A	NRND	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251
SN74CBT3251PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251
SN74CBT3251PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251
SN74CBT3251RGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU251
SN74CBT3251RGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU251

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

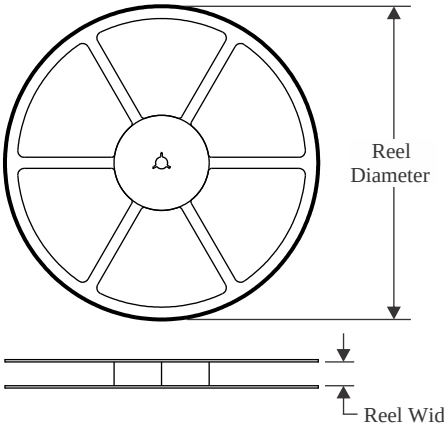
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

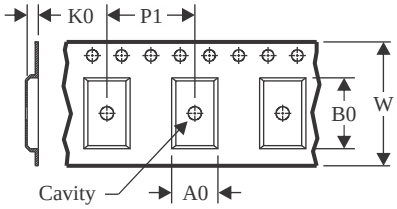
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

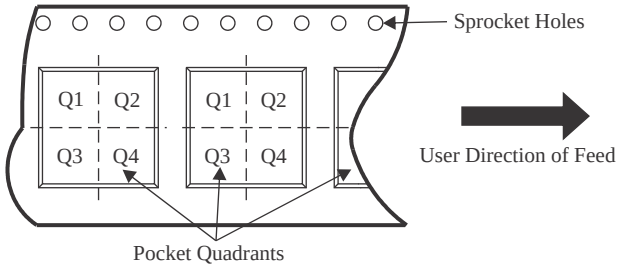


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

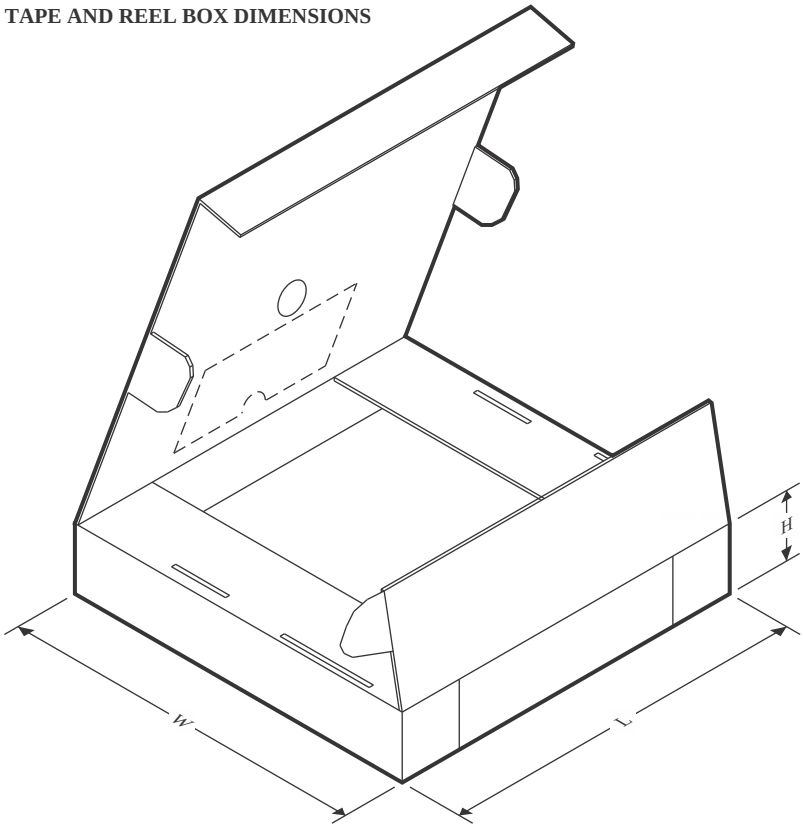
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3251DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3251DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74CBT3251DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CBT3251PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3251RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

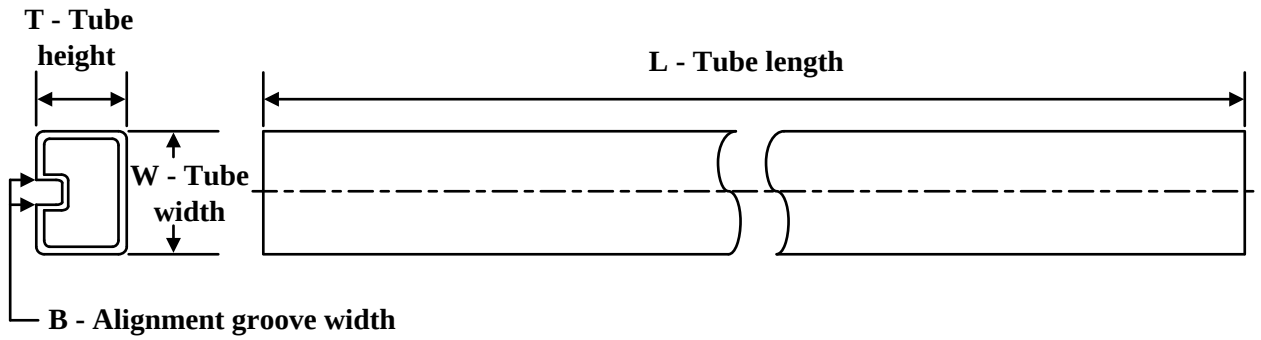
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3251DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBT3251DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74CBT3251DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74CBT3251PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74CBT3251RGYR	VQFN	RGY	16	3000	353.0	353.0	32.0

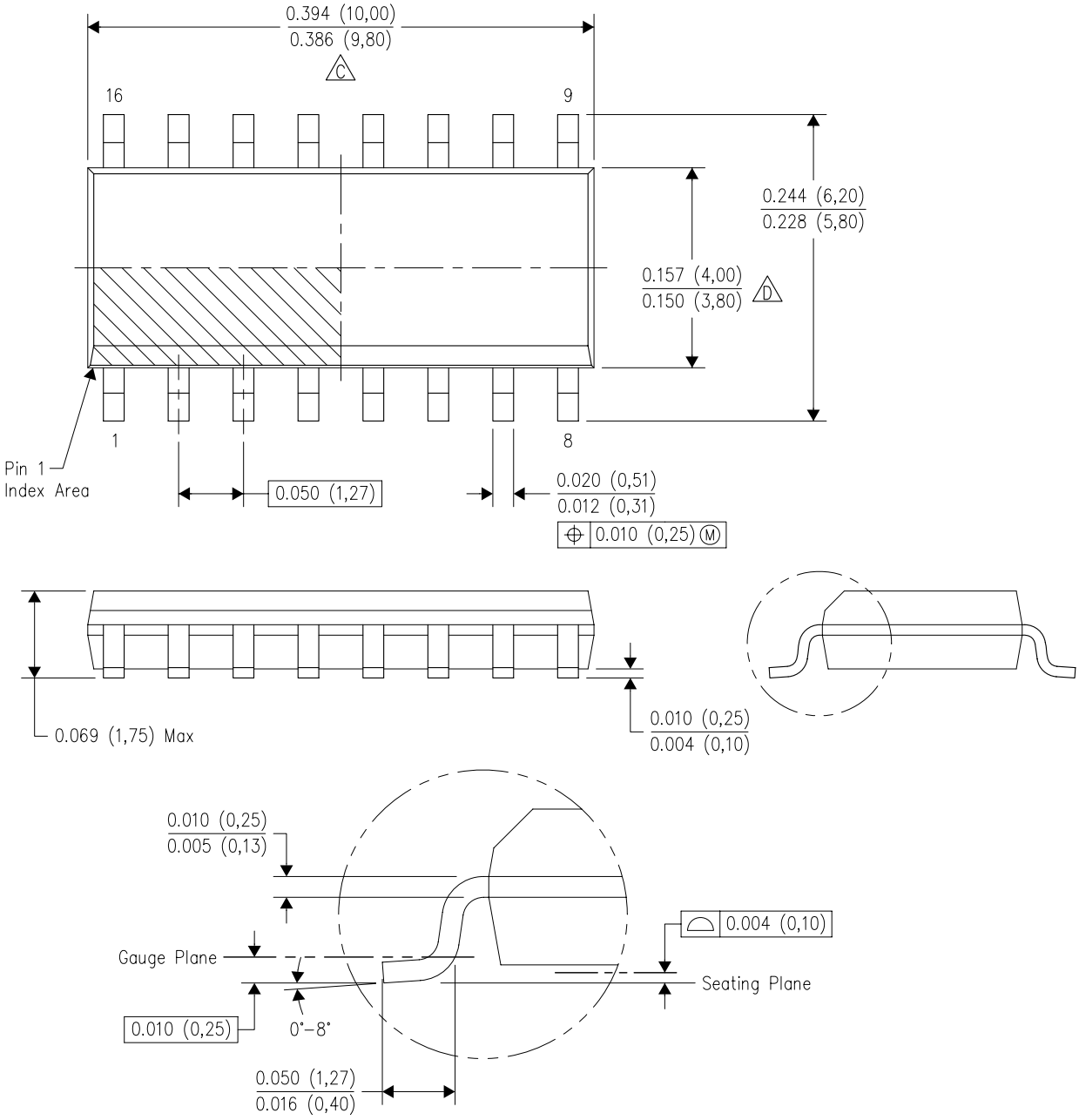
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT3251D	D	SOIC	16	40	507	8	3940	4.32
SN74CBT3251D.A	D	SOIC	16	40	507	8	3940	4.32
SN74CBT3251PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74CBT3251PW.A	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



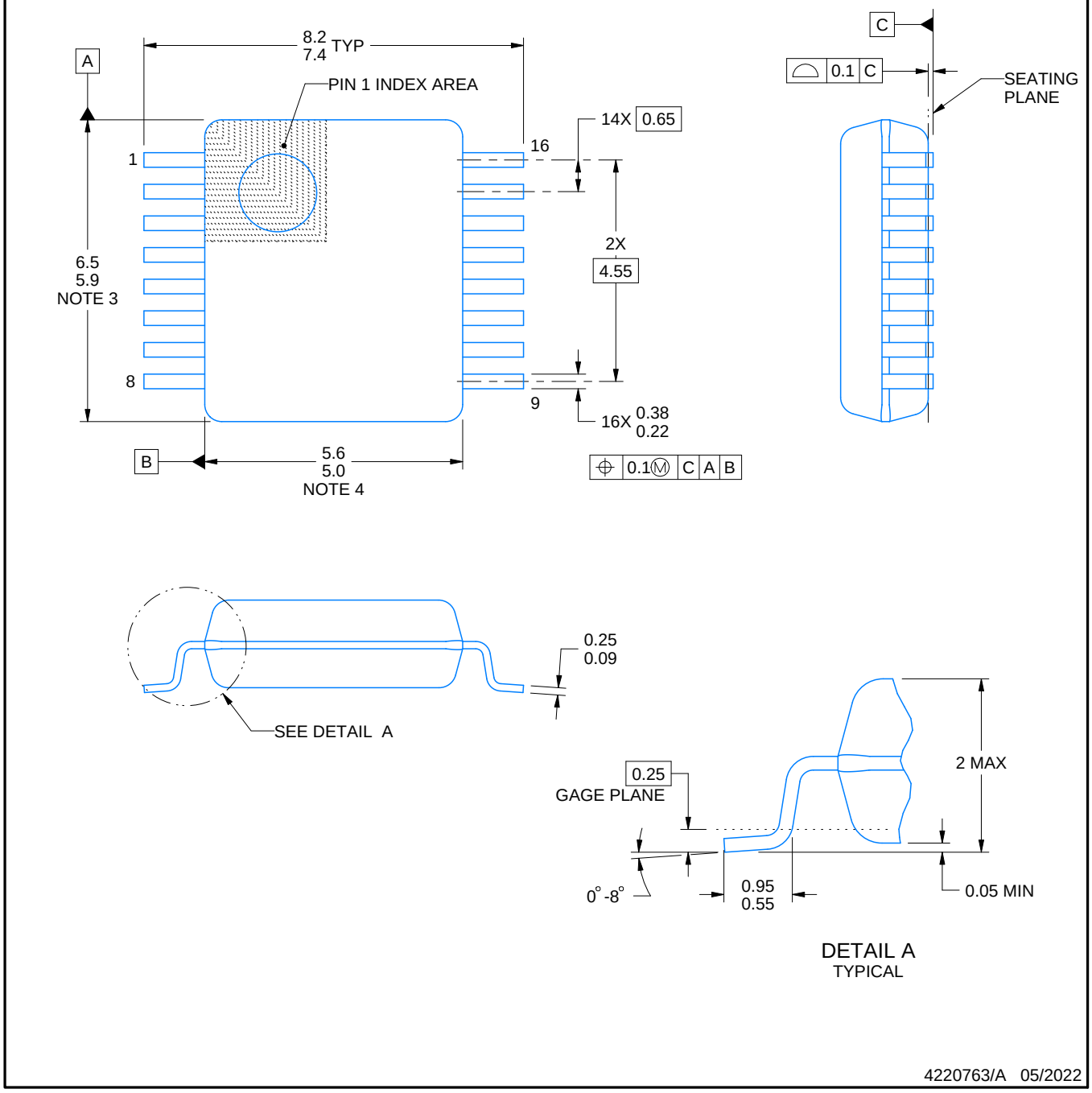
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DB0016A

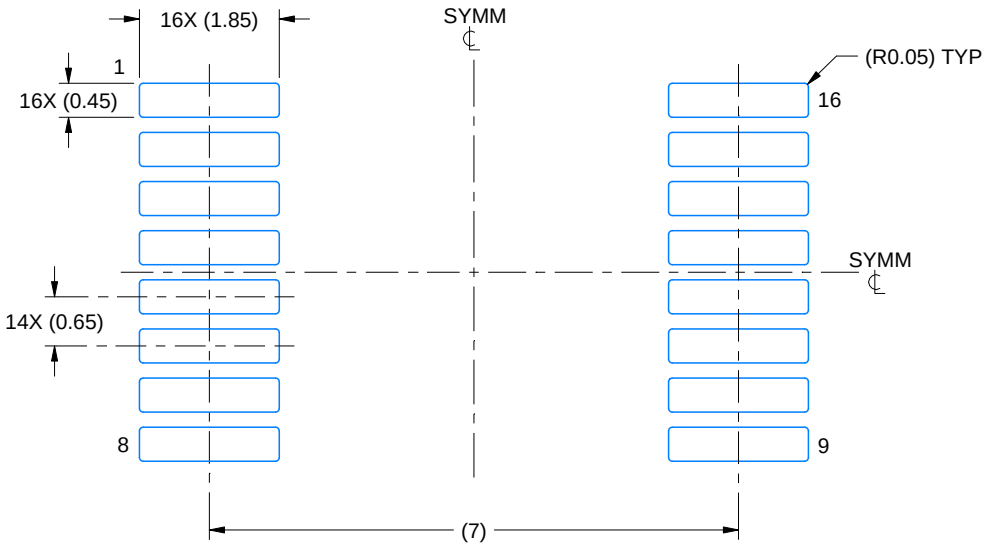
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

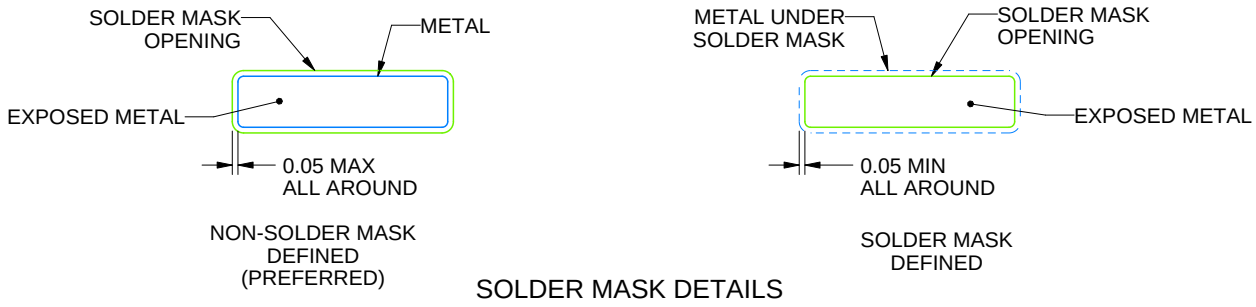


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

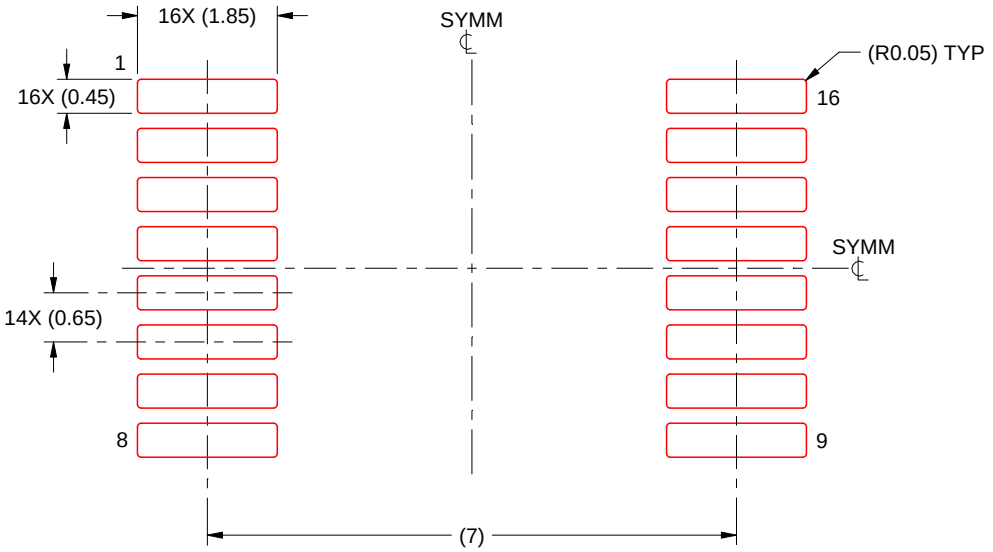


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

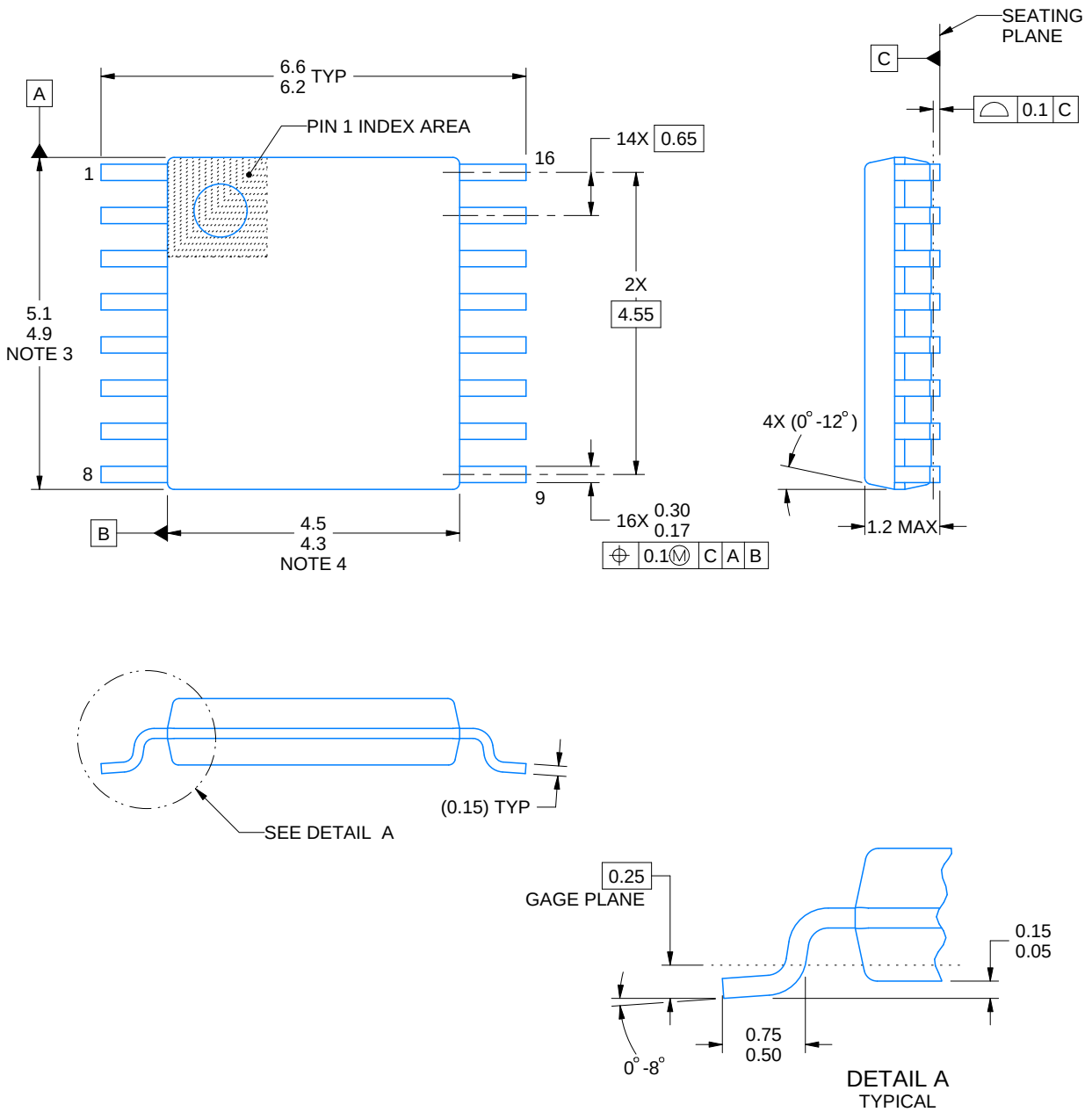
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

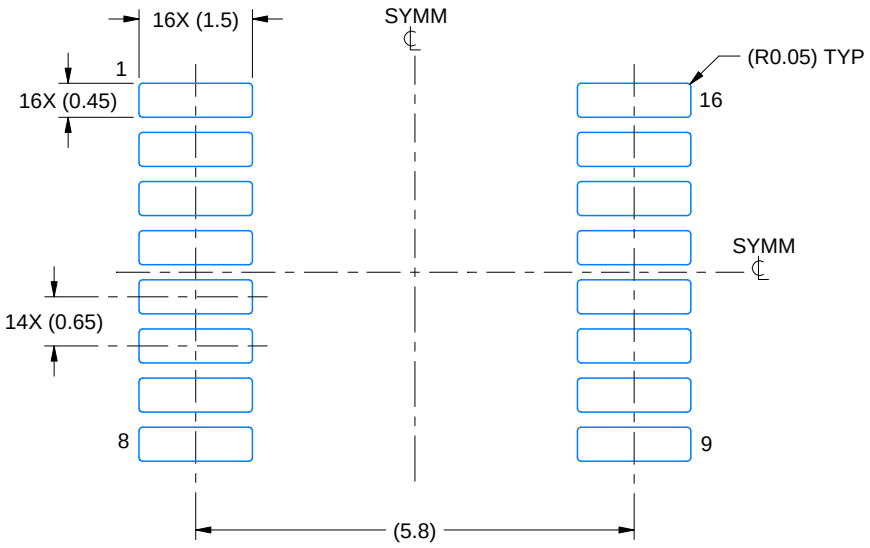
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



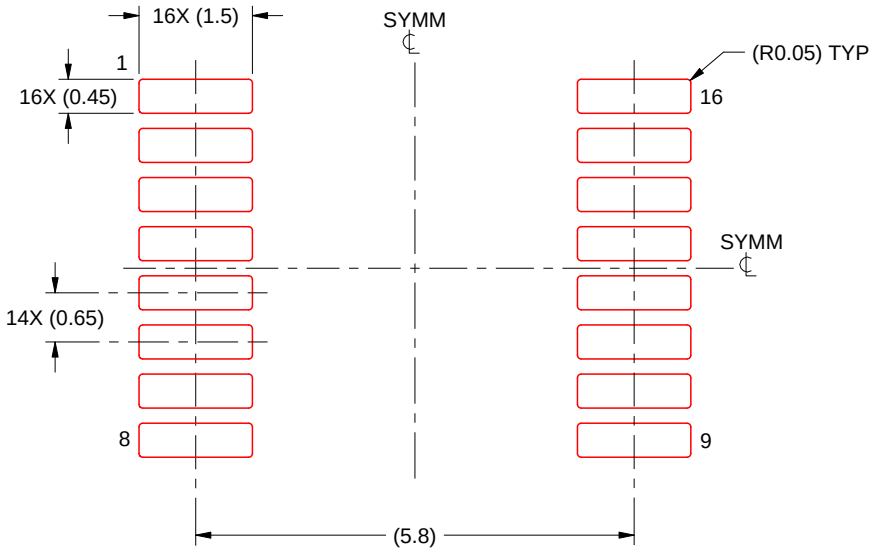
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

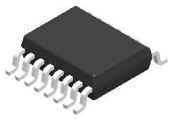


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

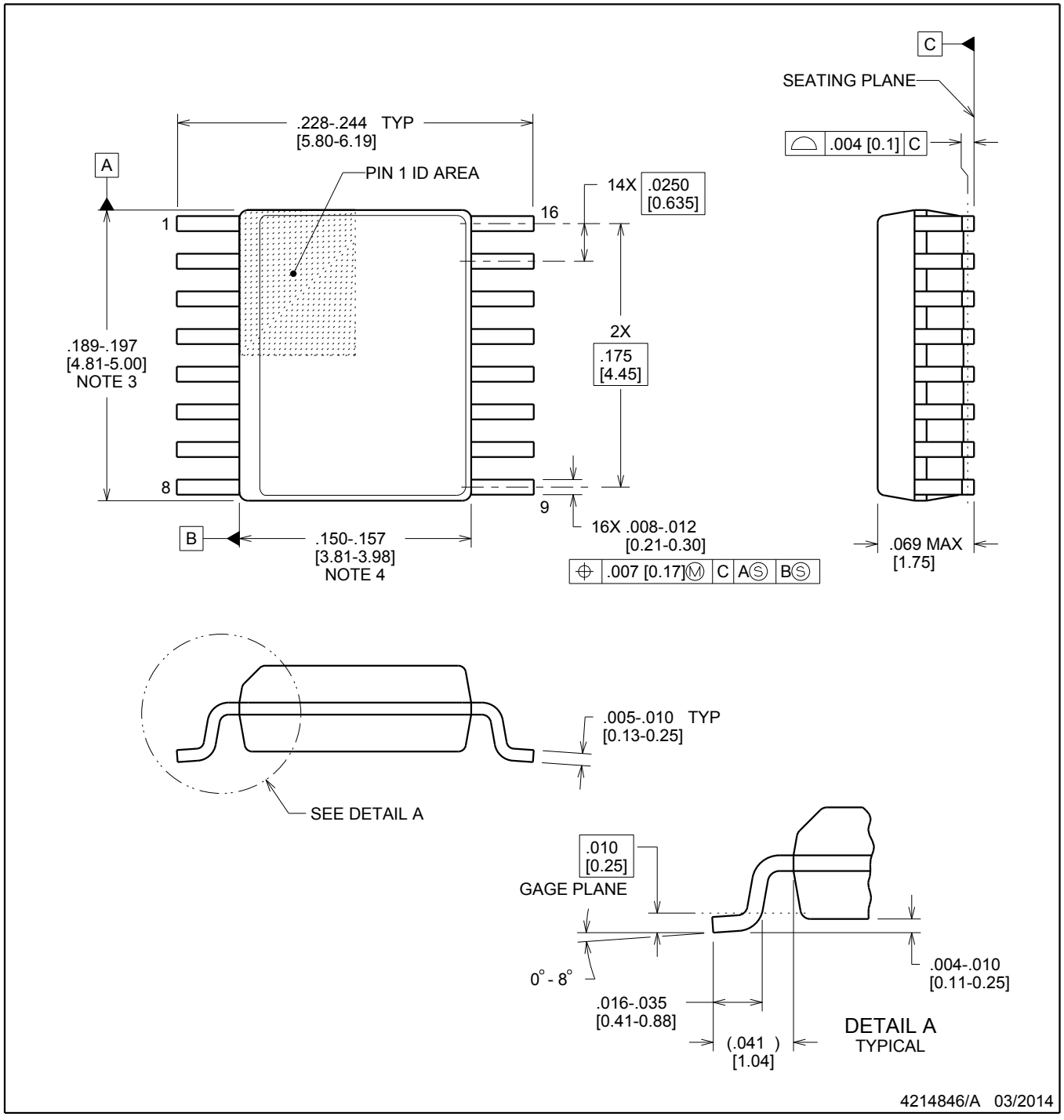


PACKAGE OUTLINE

DBQ0016A

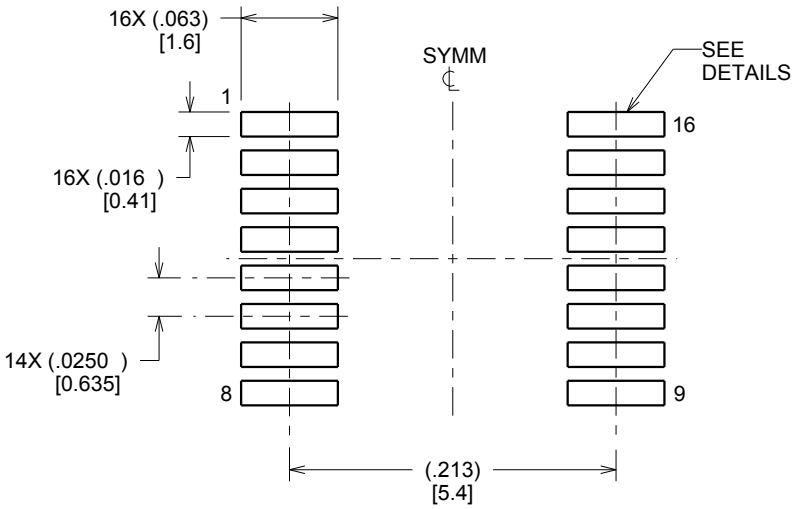
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

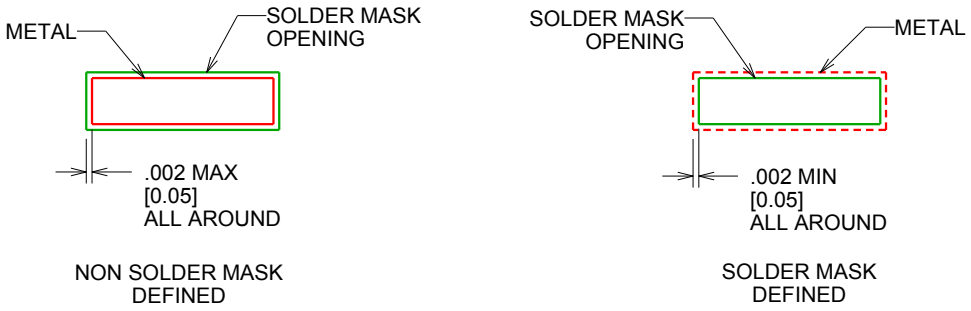


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

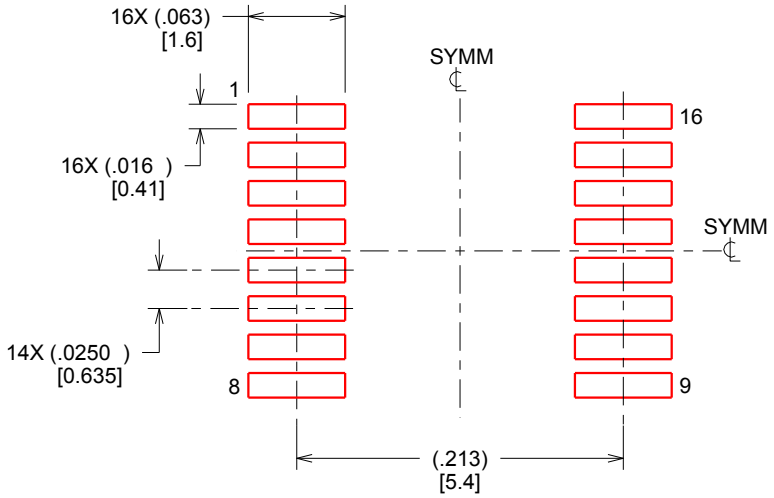
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



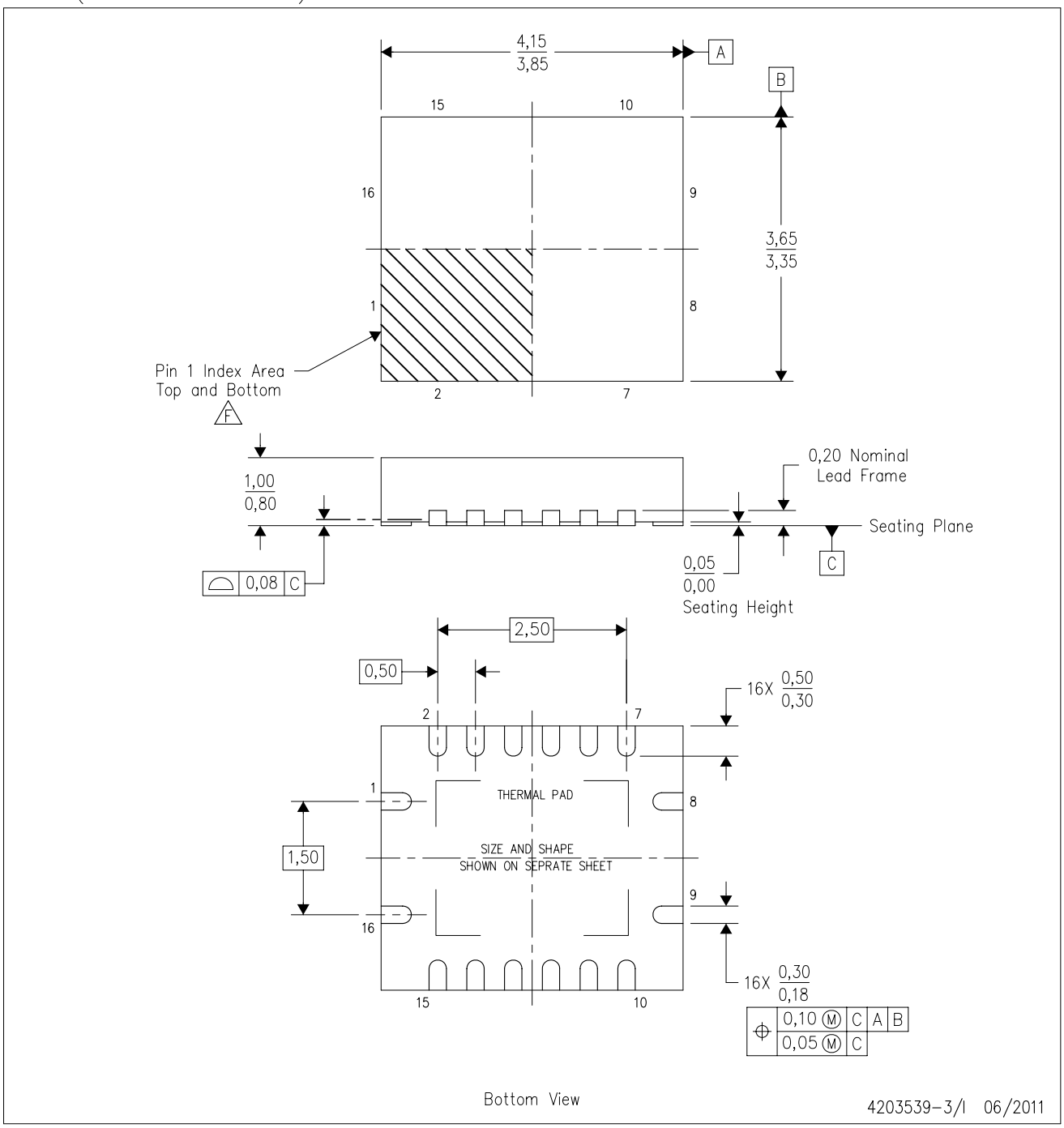
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

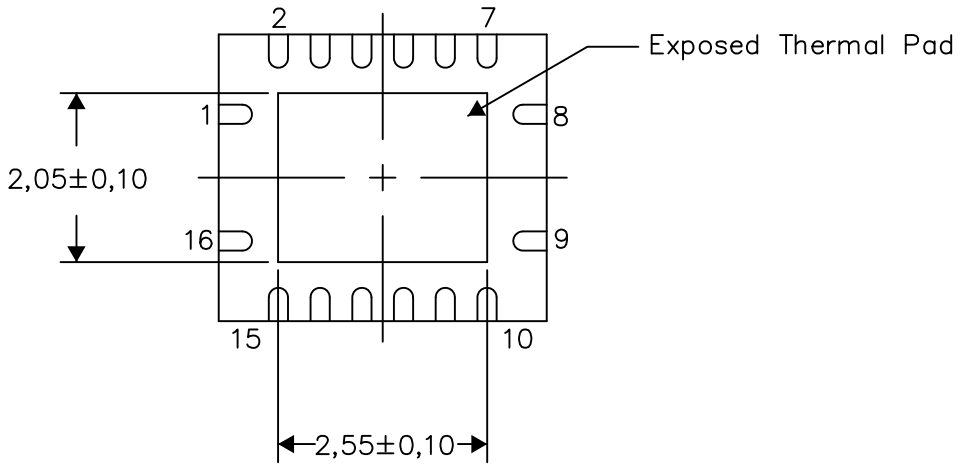
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



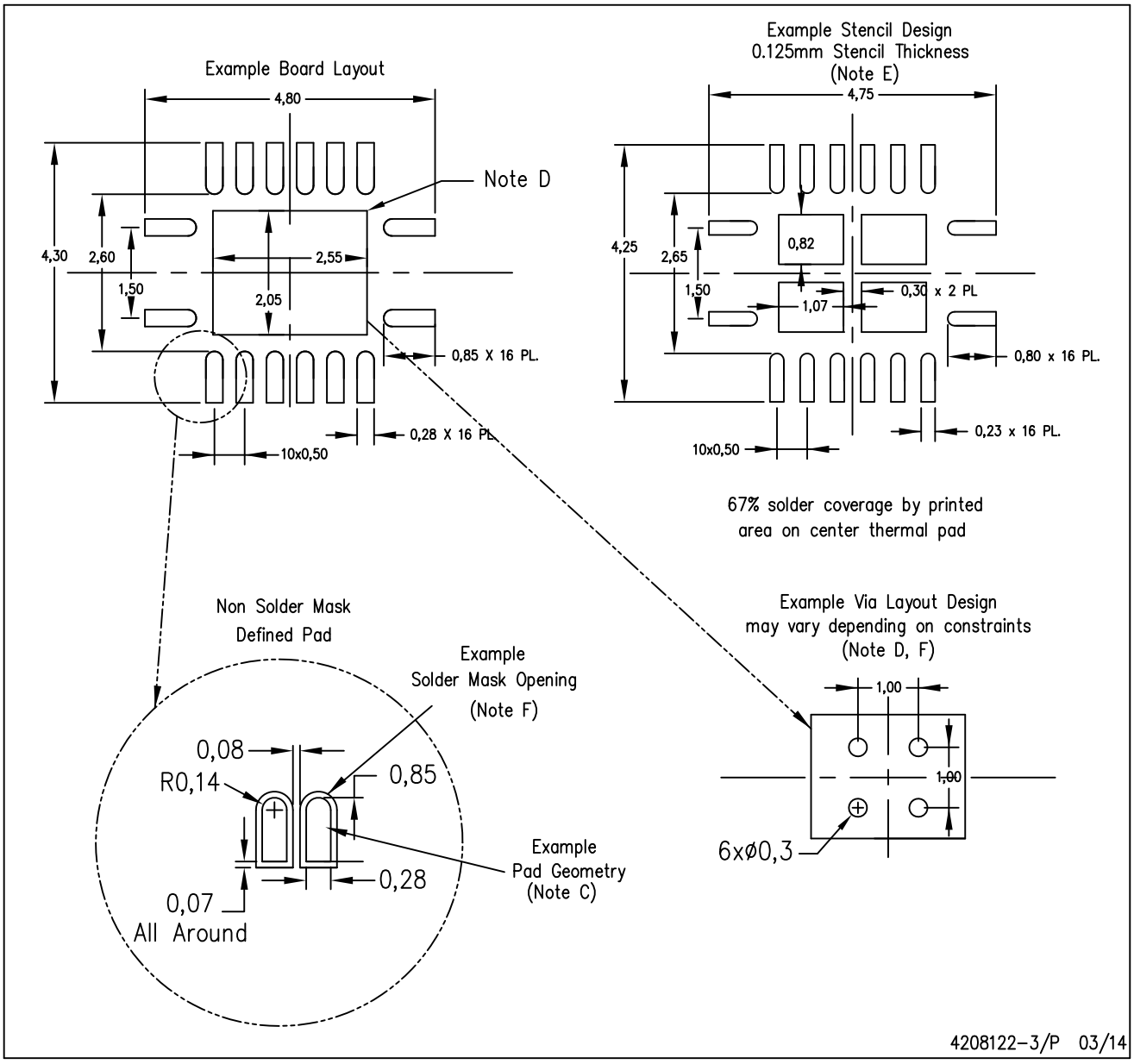
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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