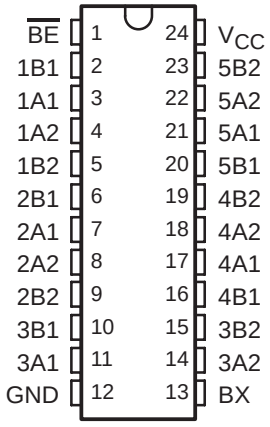
SN74CB3T3383
10-BIT FET BUS-EXCHANGE SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS158A − OCTOBER 2003 − REVISED DECEMBER 2004

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V-Tolerant I/Os With Device Powered Up or Powered Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 8 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 20 μA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, Memory Interleaving, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

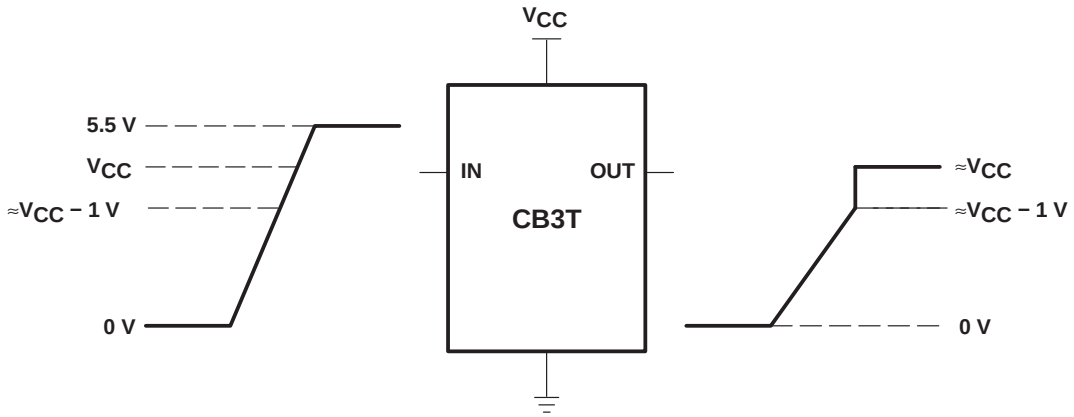
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CB3T3383DW	CB3T3383
		Tape and reel	SN74CB3T3383DWR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3T3383DBQR	CB3T3383
	TSSOP − PW	Tube	SN74CB3T3383PW	KS383
		Tape and reel	SN74CB3T3383PWR	
	TVSOP − DGV	Tape and reel	SN74CB3T3383DGVR	KS383

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description/ordering information (continued)

The SN74CB3T3383 is a high-speed TTL-compatible FET bus-exchange switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3383 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T3383 is organized as a 10-bit bus switch or as a 5-bit bus-exchange with enable ($\overline{BE}$) input. When used as a 5-bit bus-exchange, the device provides data exchanging between four signal ports. When $\overline{BE}$ is low, the bus-exchange switch is ON, and the select input (BX) controls the data path. When $\overline{BE}$ is high, the bus-exchange switch is OFF, and a high-impedance state exists between the A and B ports.

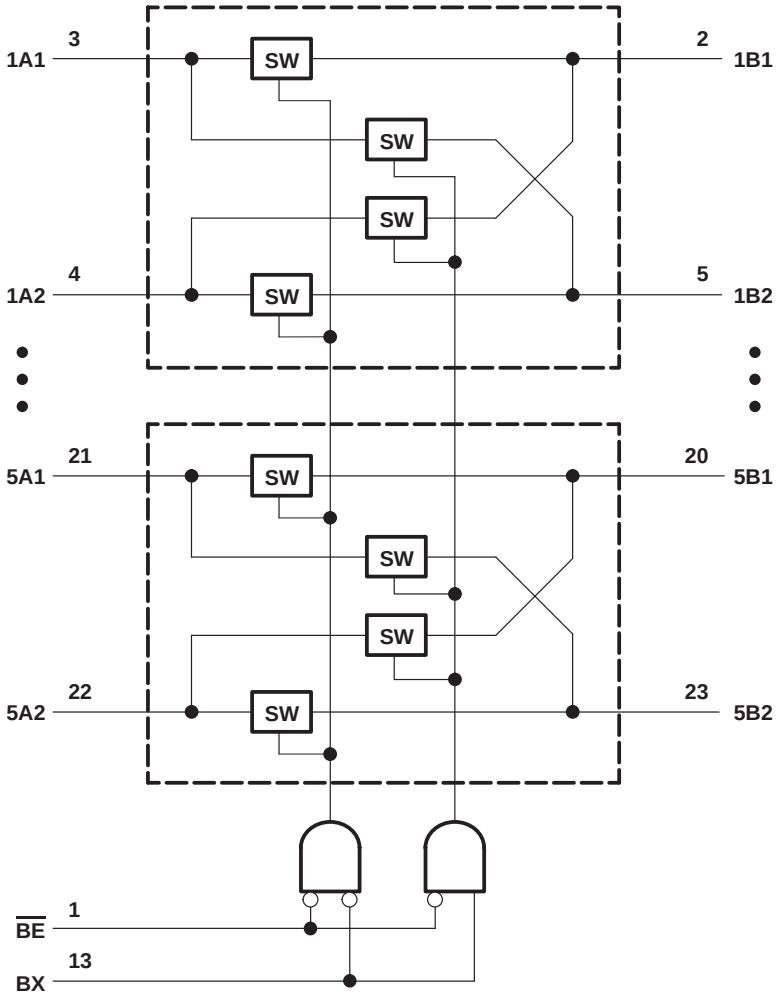
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{BE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

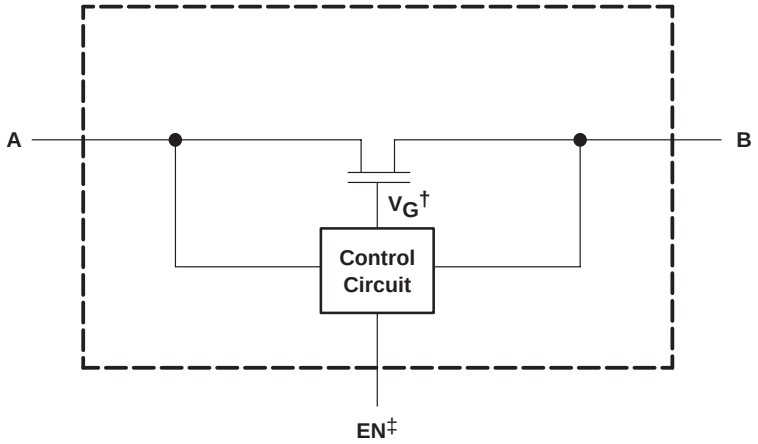
FUNCTION TABLE
(each 5-bit switch)

INPUTS		INPUTS/OUTPUTS		FUNCTION
$\overline{BE}$	BX	A1	A2	
L	L	B1	B2	A1 port = B1 port A2 port = B2 port
L	H	B2	B1	A1 port = B2 port A2 port = B1 port
H	X	Z	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$) . . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package . . . . . 61°C/W
DGV package . . . . . 86°C/W
DW package . . . . . 46°C/W
PW package . . . . . 88°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See Figures 3 and 4					
I_{IN}‡	Control inputs	V_{CC} = 3.6 V, V_{IN}‡ = 3.6 V to 5.5 V or GND				±10	µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	µA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}§		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			20	µA
			V_I = 5.5 V			20	
ΔI_{CC}¶	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			4		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			8		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		7		pF
			$V_{I/O}$ = GND		21		
r_{on}#		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	9	Ω
			I_O = 16 mA		5	9	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	8	
			I_O = 32 mA		5	8	

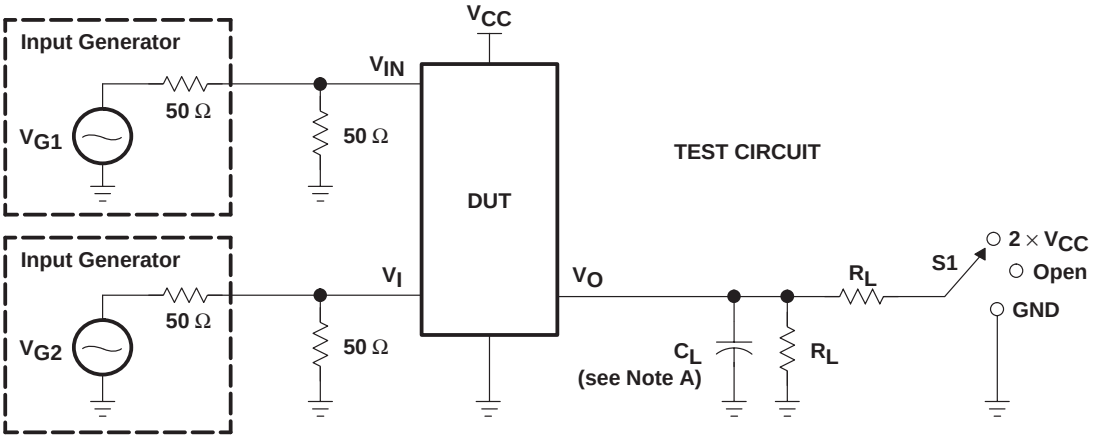
† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
‡ V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
# Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

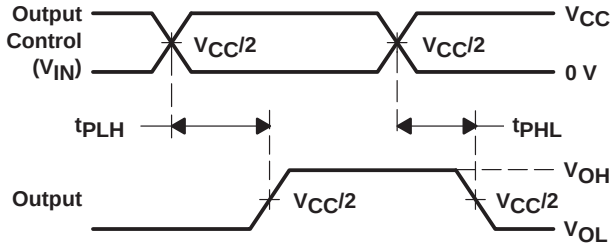
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		0.15		0.25	ns
$t_{pd(s)}$	BX	A or B	1	15	1	10	
t_{en}	$\overline{BE}$	A or B	1	13.5	1	9	ns
t_{dis}	$\overline{BE}$	A or B	1	7	1	8.5	ns

† The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

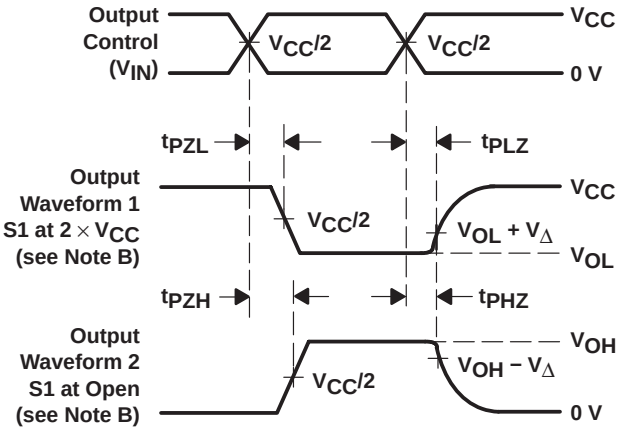
PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

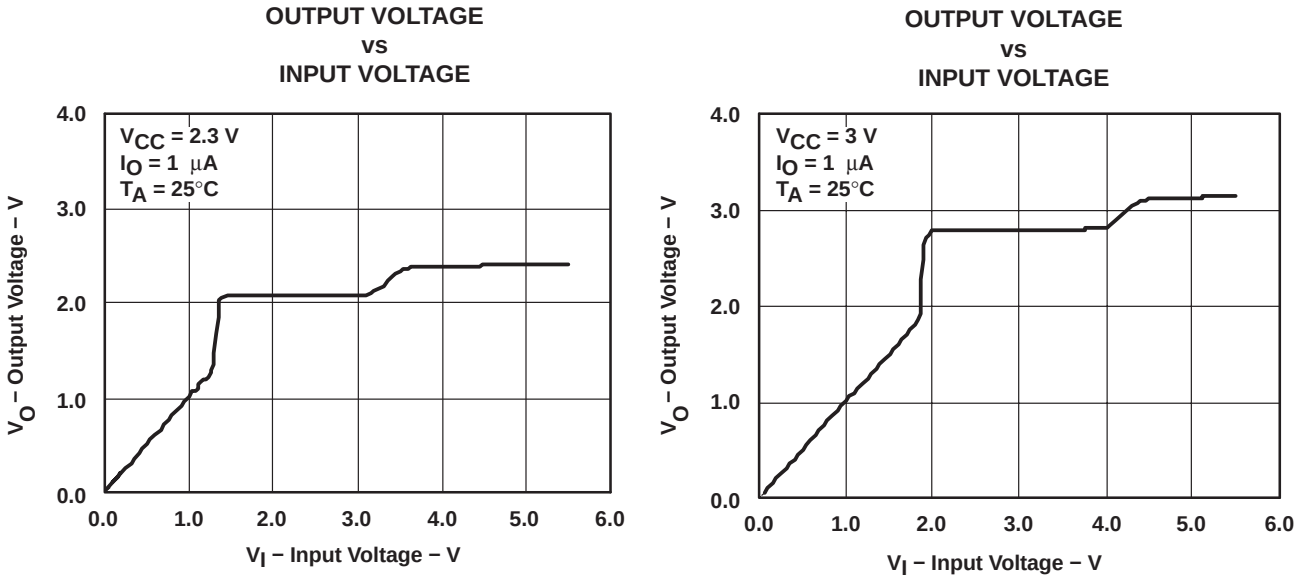


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)

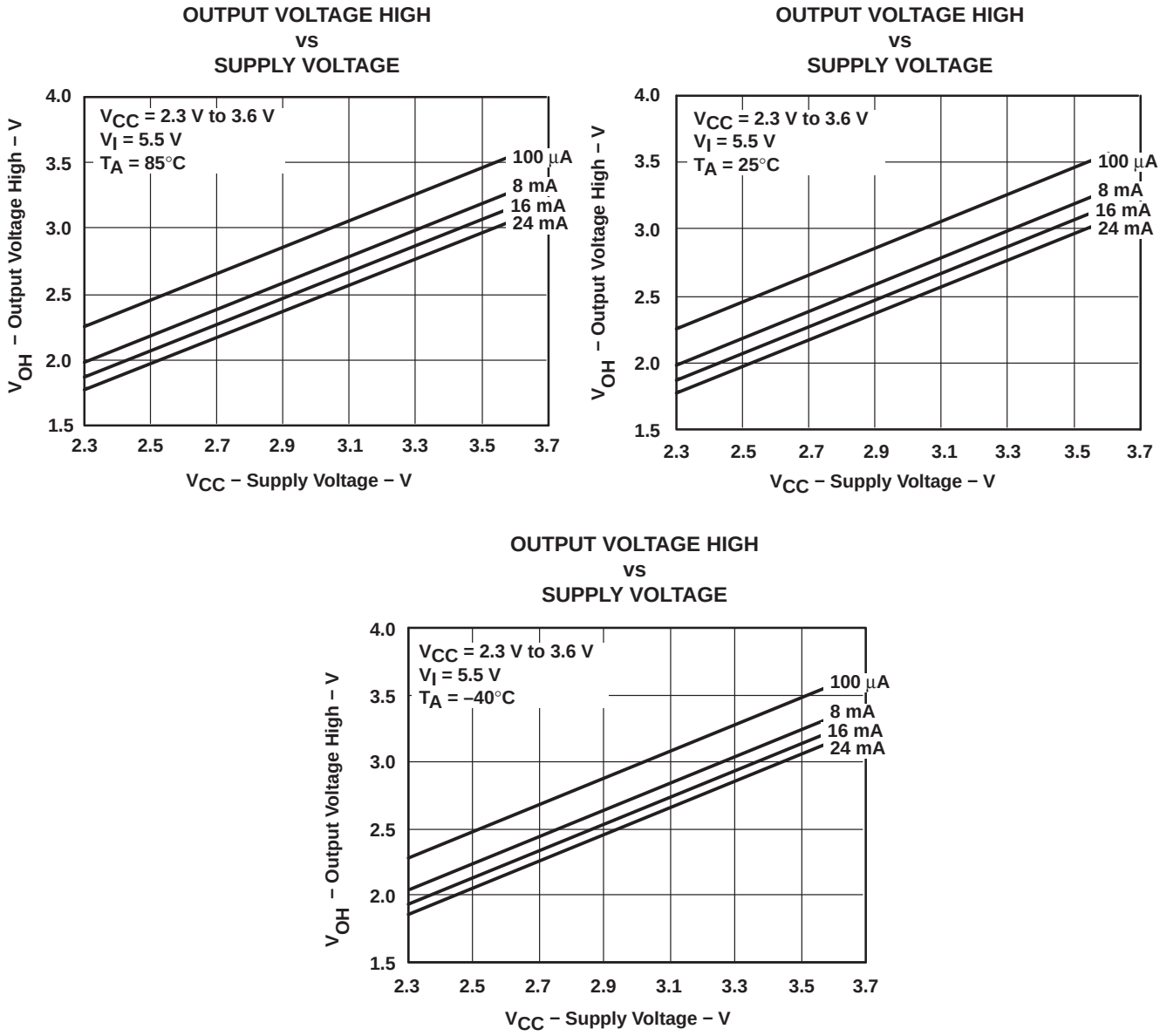


Figure 4. V_{OH} Values

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CB3T3383DGVR	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS383
SN74CB3T3383DGVR.B	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS383
SN74CB3T3383DWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3383
SN74CB3T3383DWR.B	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3383
SN74CB3T3383PW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS383
SN74CB3T3383PW.B	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS383
SN74CB3T3383PWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS383
SN74CB3T3383PWR.B	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS383
SN74CB3T3383PWRG4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS383
SN74CB3T3383PWRG4.B	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS383

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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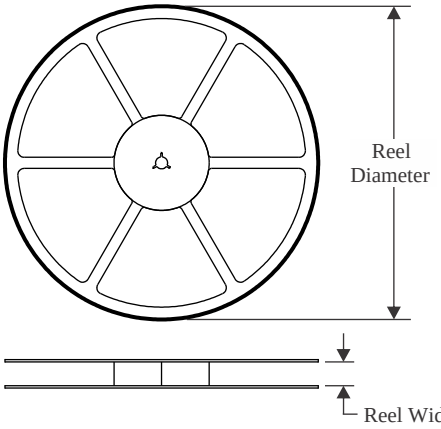
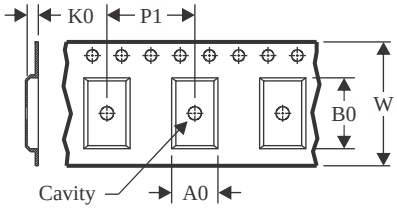
TAPE AND REEL INFORMATION

REEL DIMENSIONS

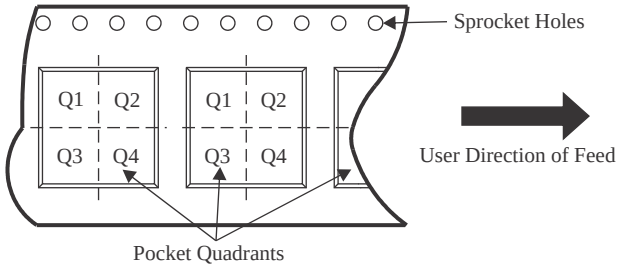


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

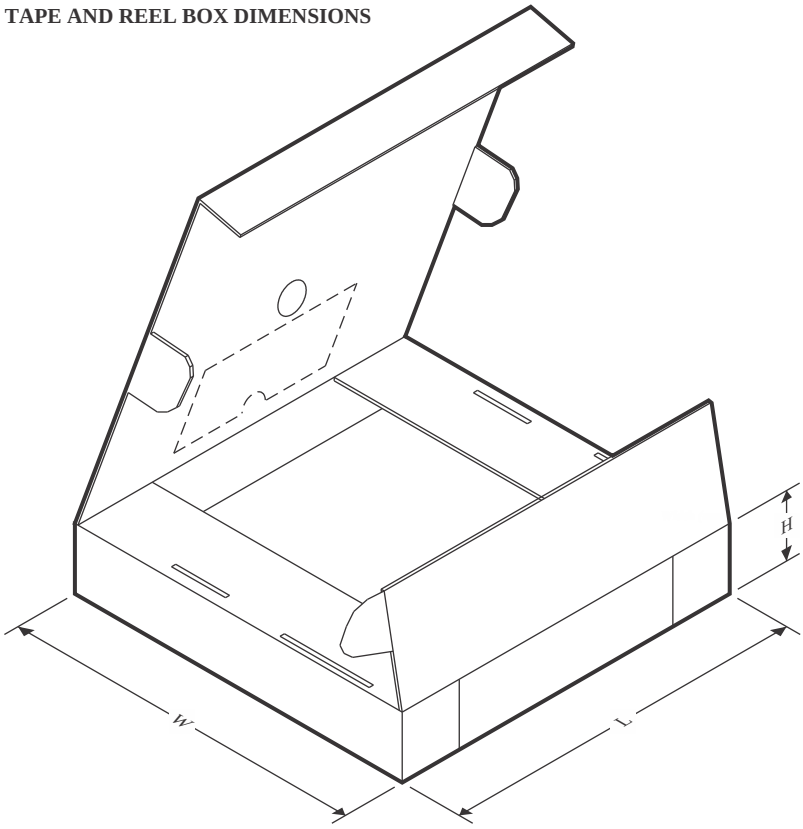
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3383DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3T3383DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

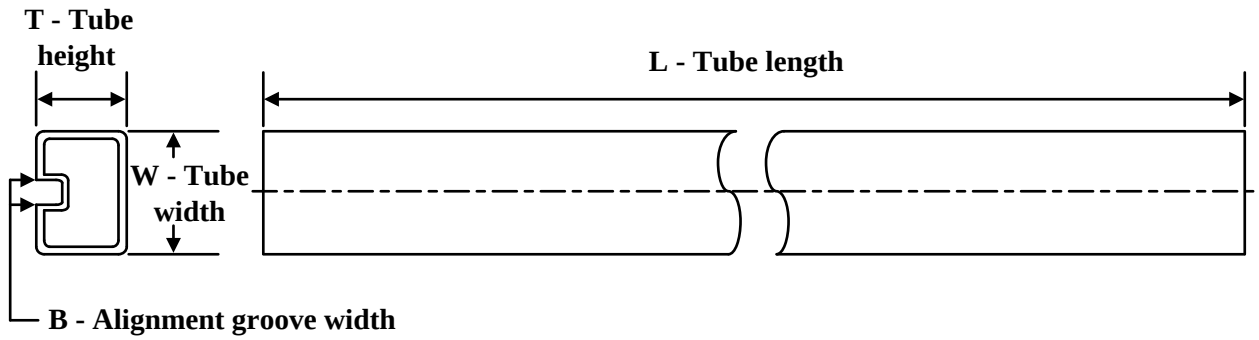
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3383DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
SN74CB3T3383DWR	SOIC	DW	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

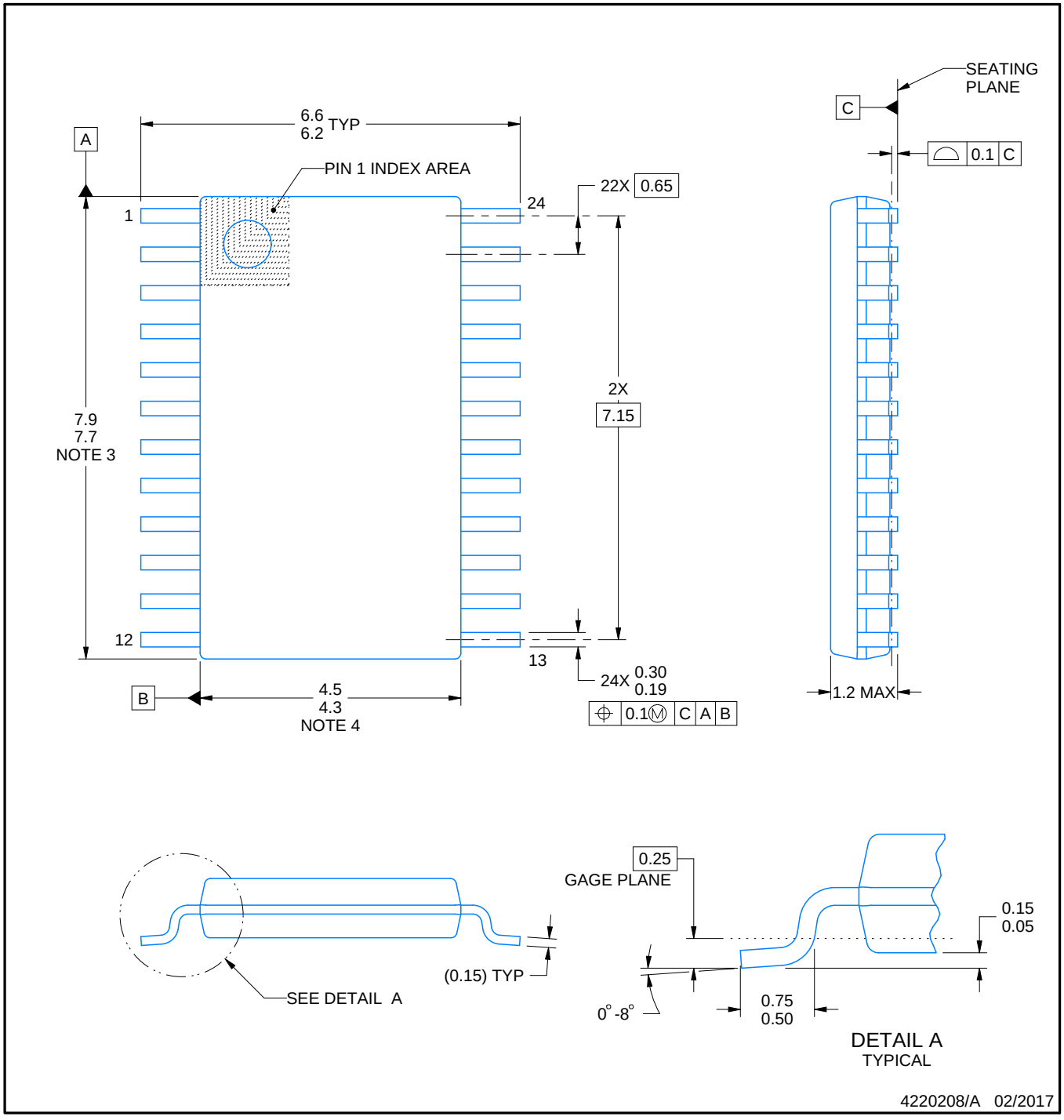
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CB3T3383PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74CB3T3383PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

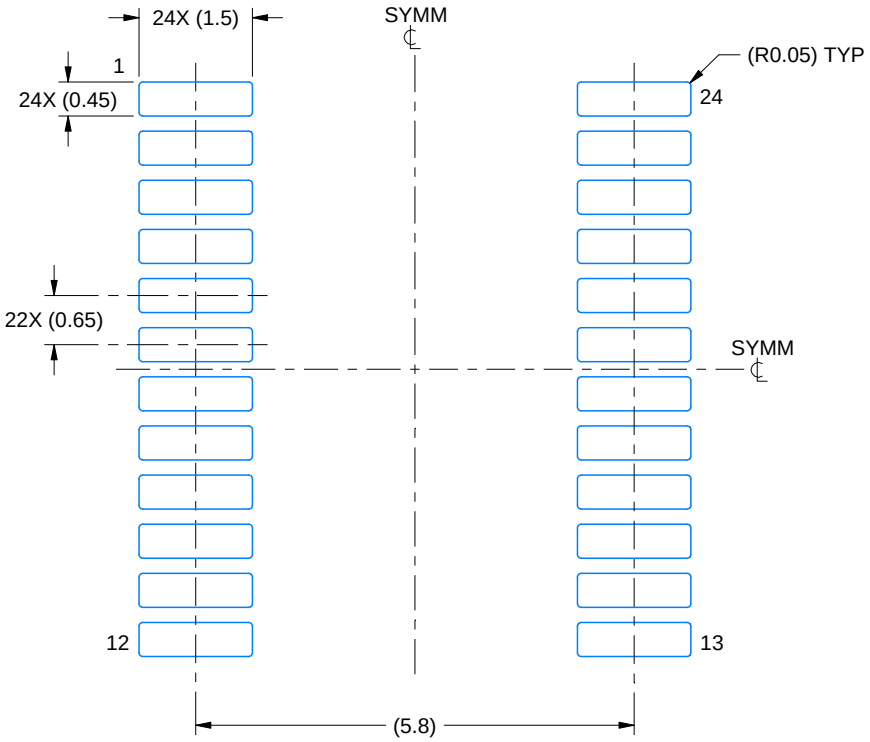
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

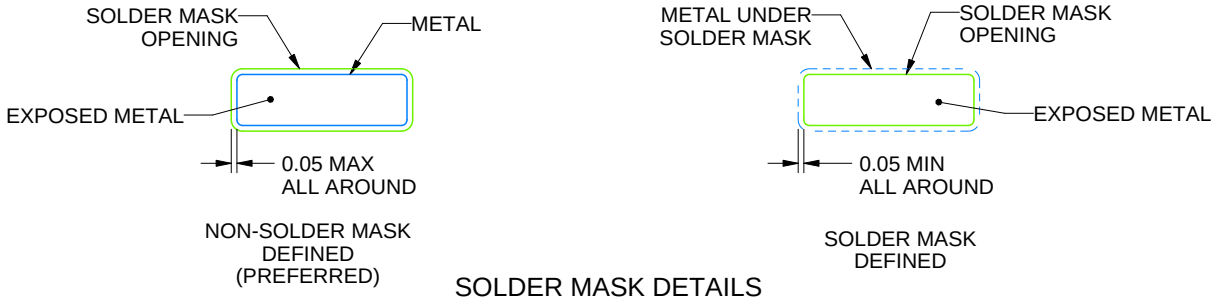


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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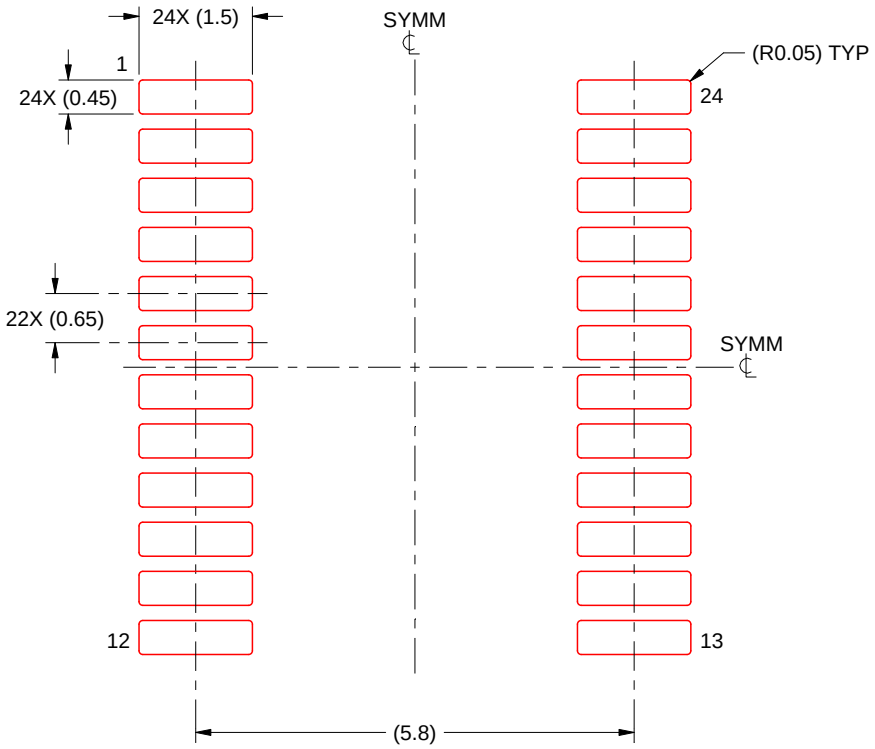
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



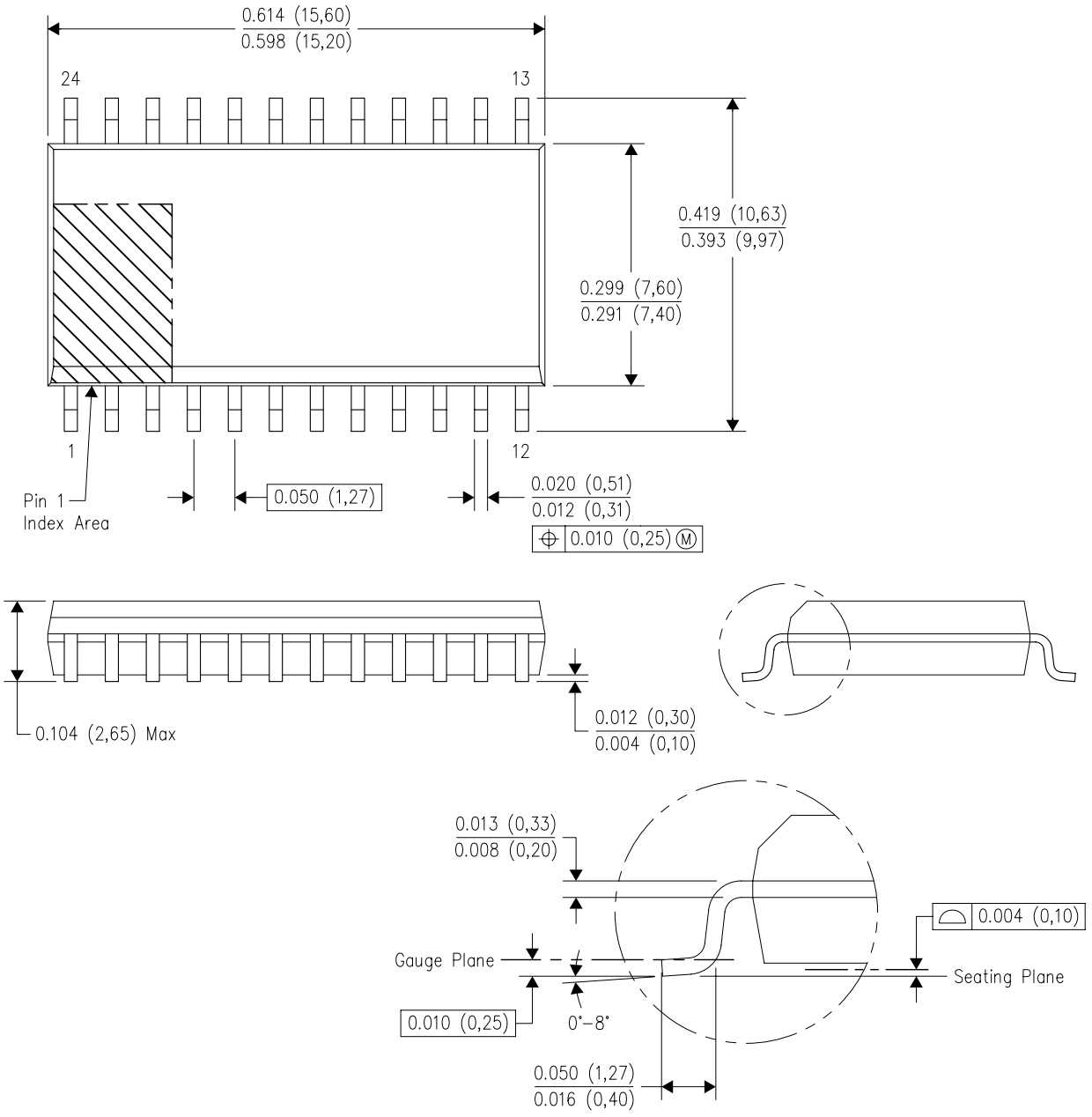
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



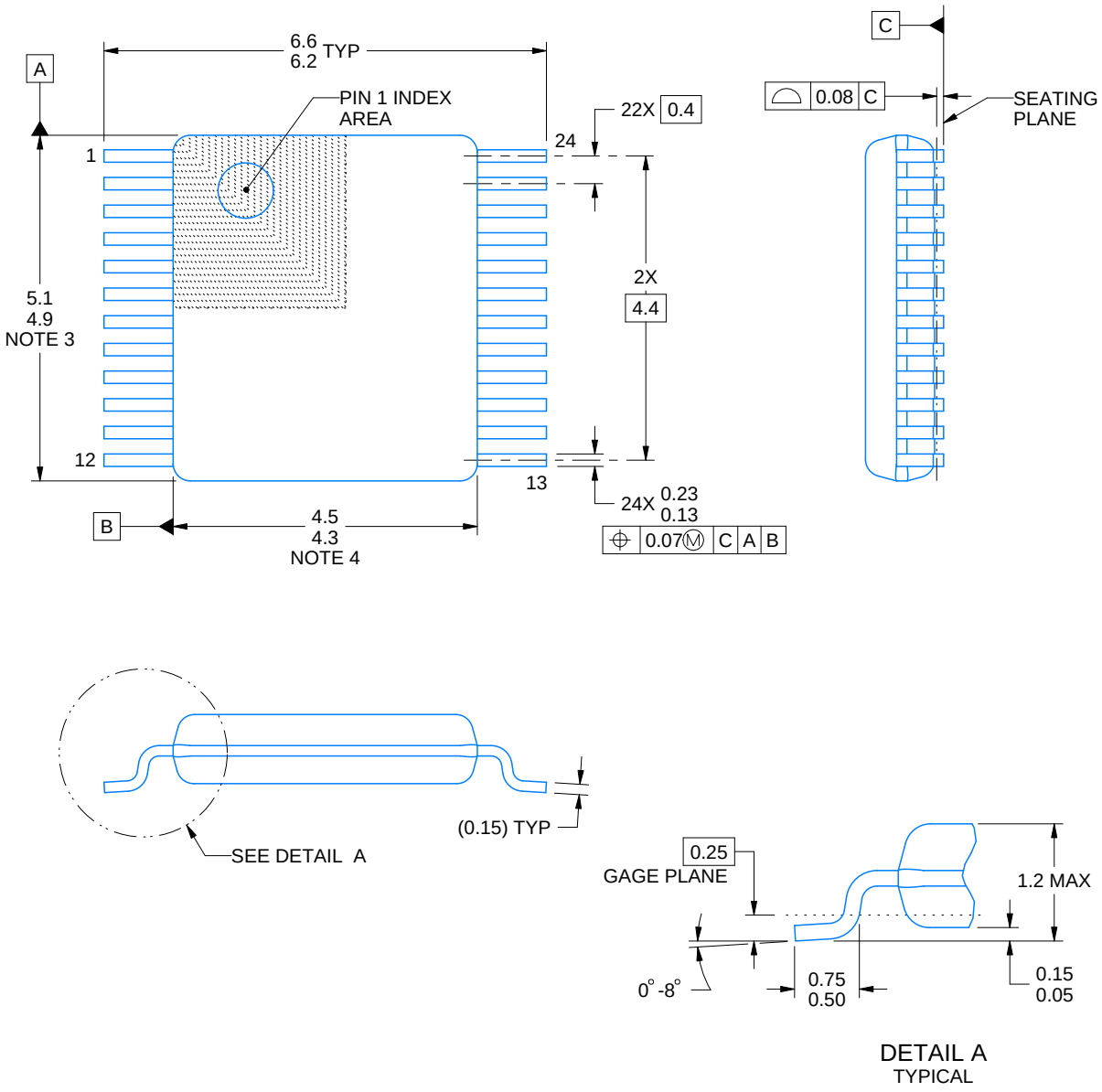
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

PACKAGE OUTLINE

DGV0024A

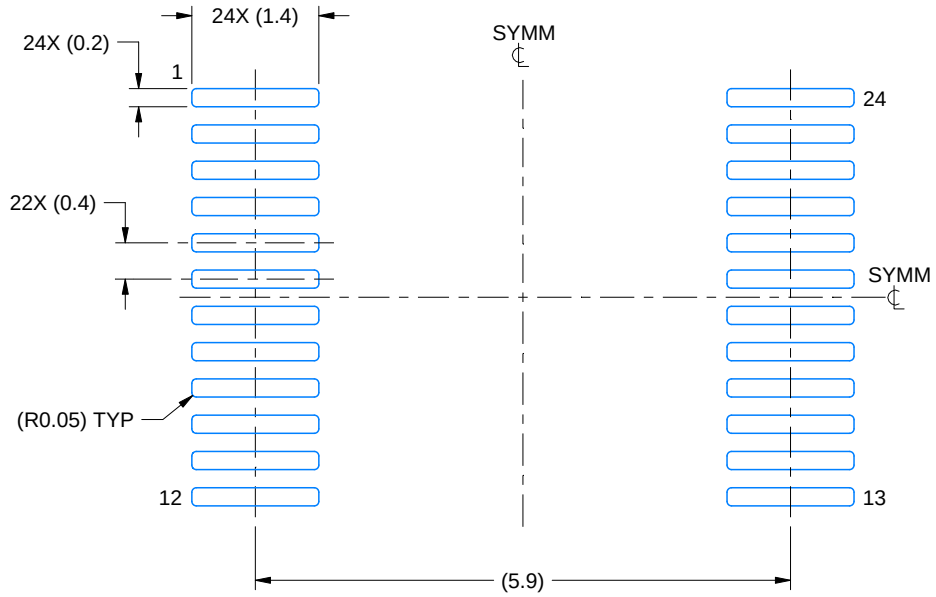
TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

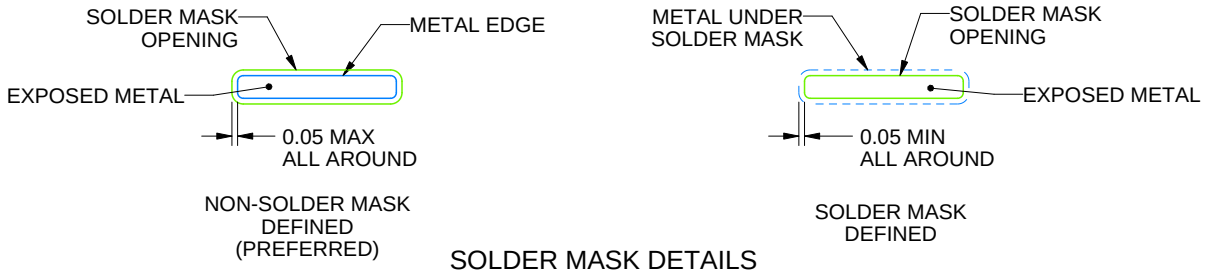


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

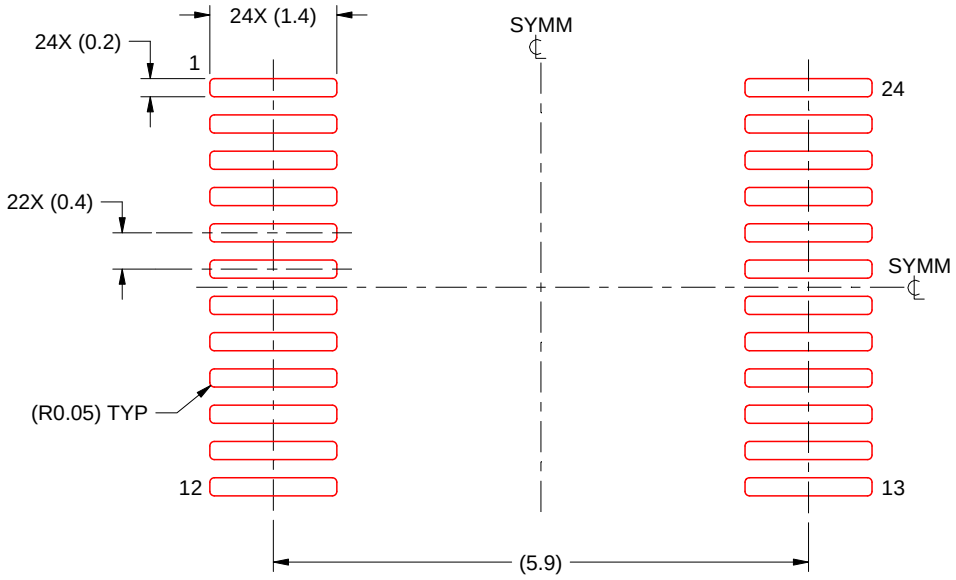


SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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