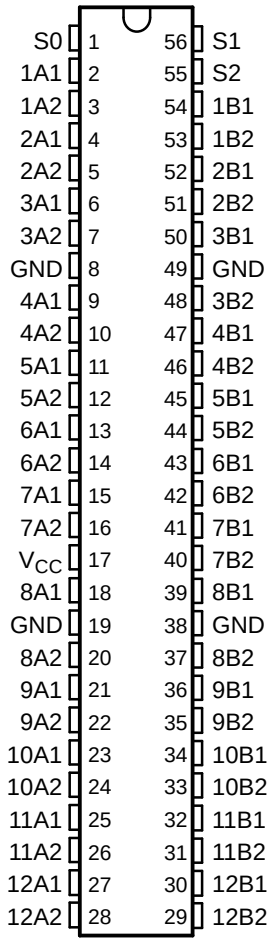
# SN74CB3T16212
# 24-BIT FET BUS-EXCHANGE SWITCH, 2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS157A–OCTOBER 2003–REVISED FEBRUARY 2005

## FEATURES

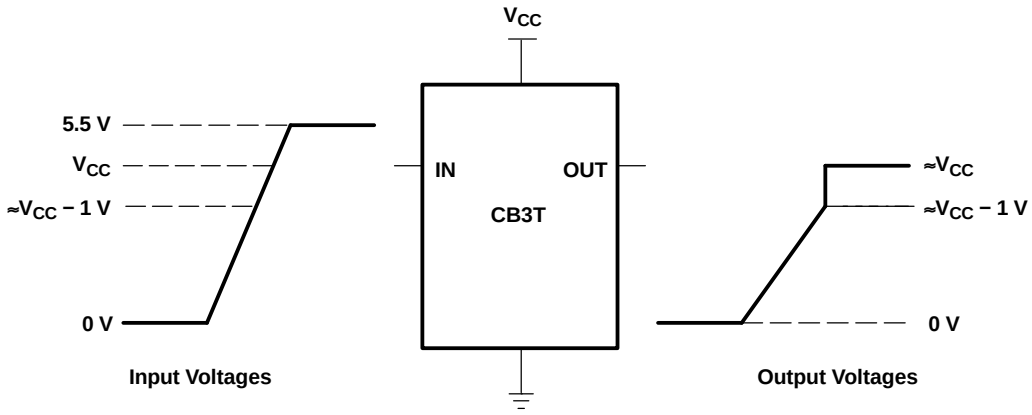
- Member of the Texas Instruments Widebus™ Family
- Output Voltage Translation Tracks $V_{CC}$
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
  - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V $V_{CC}$
  - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V $V_{CC}$
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ($r_{on}$) Characteristics ($r_{on}$ = 5 Ω Typ)
- Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 9 pF Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC}$ = 70 μA Max)
- $V_{CC}$ Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0-V to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model(A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, PCI Interface, USB Interface, Memory Interleaving, and Bus Isolation
- Ideal for Low-Power Portable Equipment

**DGG OR DGV PACKAGE**
**(TOP VIEW)**




## DESCRIPTION/ORDERING INFORMATION

The SN74CB3T16212 is a high-speed TTL-compatible FET bus-exchange switch, with low ON-state resistance ($r_{on}$), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks $V_{CC}$. The SN74CB3T16212 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).




NOTE: If the input high-voltage ($V_{IH}$) level is greater than or equal to $V_{CC}$ − 1 V and less than or equal to 5.5 V, the output high-voltage ($V_{OH}$) level is equal to approximately the $V_{CC}$ voltage level.

**Figure 1. Typical DC Voltage Translation Characteristics**

The SN74CB3T16212 operates as a 24-bit bus switch or as a 12-bit bus exchange that provides data exchanging between four signal ports. The select (S0, S1, S2) inputs control the data path of the bus-exchange switch. When the bus-exchange switch is ON, the A port is connected to the B port, allowing bidirectional data flow between ports. When the bus-exchange switch is OFF, a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

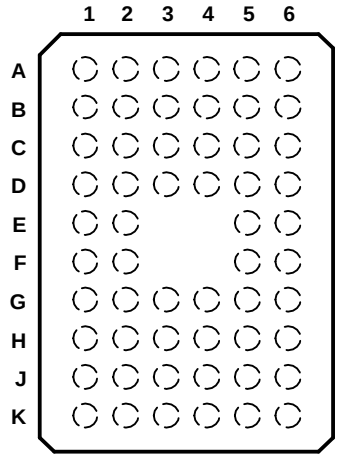
To ensure the high-impedance state during power up or power down, each select input should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

## ORDERING INFORMATION

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | TSSOP – DGG | Tape and reel | SN74CB3T16212DGGR | CB3T16212 |
| | TVSOP – DGV | Tape and reel | SN74CB3T16212DGVR | KR212 |
| | VFBGA – GQL | Tape and reel | SN74CB3T16212GQLR | KR212 |
| | VFBGA – ZQL (Pb-free) | Tape and reel | SN74CB3T16212ZQLR | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**GQL OR ZQL PACKAGE**
**(TOP VIEW)**



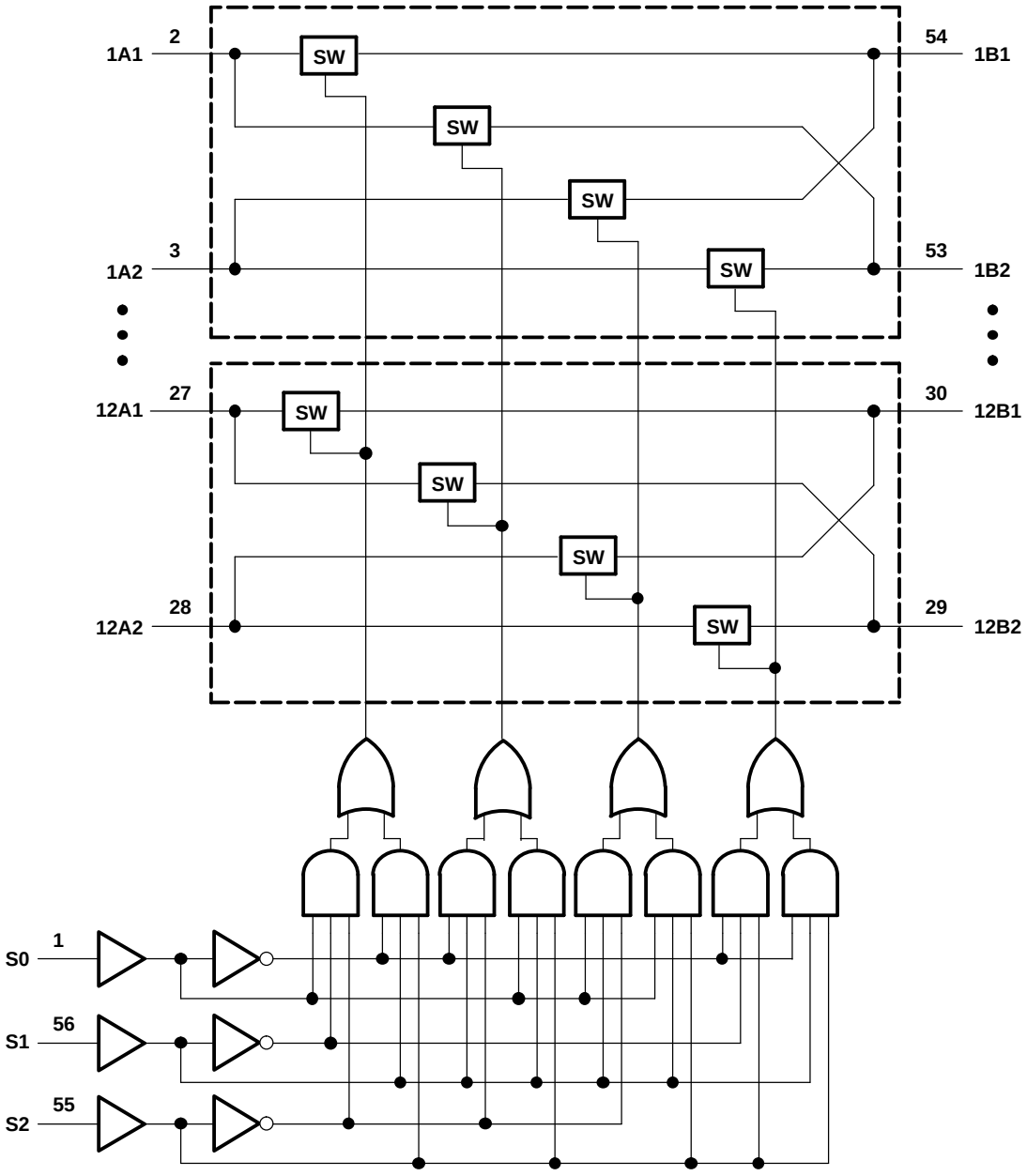

## TERMINAL ASSIGNMENTS

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | 1A2 | 1A1 | S0 | S1 | S2 | 1B1 |
| **B** | 3A1 | 2A2 | 2A1 | 1B2 | 2B1 | 2B2 |
| **C** | 4A1 | GND | 3A2 | 3B1 | GND | 3B2 |
| **D** | 5A2 | 4A2 | 5A1 | 4B2 | 4B1 | 5B1 |
| **E** | 6A2 | 6A1 | | | 5B2 | 6B1 |
| **F** | 7A1 | 7A2 | | | 7B1 | 6B2 |
| **G** | $V_{CC}$ | GND | 8A1 | 8B1 | GND | 7B2 |
| **H** | 8A2 | 9A1 | 9A2 | 9B2 | 9B1 | 8B2 |
| **J** | 10A1 | 10A2 | 11A1 | 11B1 | 10B2 | 10B1 |
| **K** | 11A2 | 12A1 | 12A2 | 12B2 | 12B1 | 11B2 |

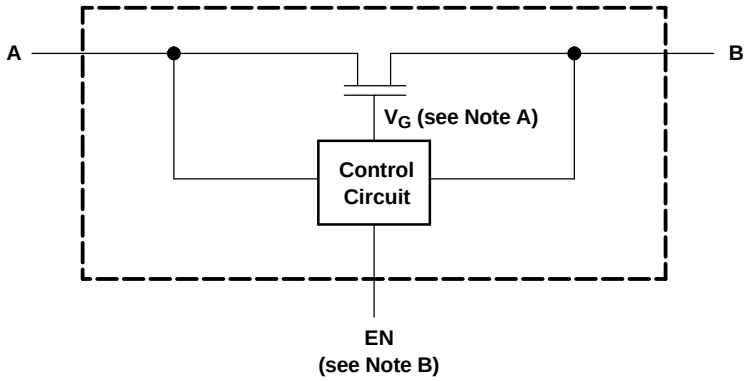
## FUNCTION TABLE

| INPUTS | | | INPUTS/OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|
| **S2** | **S1** | **S0** | **A1** | **A2** | |
| L | L | L | Z | Z | Disconnect |
| L | L | H | B1 port | Z | A1 port = B1 port |
| L | H | L | B2 port | Z | A1 port = B2 port |
| L | H | H | Z | B1 port | A2 port = B1 port |
| H | L | L | Z | B2 port | A2 port = B2 port |
| H | L | H | Z | Z | Disconnect |
| H | H | L | B1 port | B2 port | A1 port = B1 port<br>A2 port = B2 port |
| H | H | H | B2 port | B1 port | A1 port = B2 port<br>A2 port = B1 port |

## LOGIC DIAGRAM (POSITIVE LOGIC)



**SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)**




A. Gate voltage ($V_G$) is equal to approximately $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.

B. EN is the internal enable signal applied to the switch.

## ABSOLUTE MAXIMUM RATINGS(1)

over free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range(2) | | –0.5 | 7 | V |
| $V_{IN}$ | Control input voltage range(2)(3) | | –0.5 | 7 | V |
| $V_{I/O}$ | Switch I/O voltage range(2)(3)(4) | | –0.5 | 7 | V |
| $I_{IK}$ | Control input clamp current | $V_{IN} < 0$ | | –50 | mA |
| $I_{I/OK}$ | I/O port clamp current | $V_{I/O} < 0$ | | –50 | mA |
| $I_{I/O}$ | ON-state switch current(5) | | | ±128 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(6) | DGG package | | 64 | °C/W |
| | | DGV package | | 48 | |
| | | GQL/ZQL package | | 42 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output volrage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
(5) $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | 5.5 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | 5.5 | |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | 0.8 | |
| $V_{I/O}$ | Data input/output voltage | | 0 | 5.5 | V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS(1)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 3 V, $I_I$ = –18 mA | | | | –1.2 | V |
| $V_{OH}$ | | See Figures 3 and 4 | | | | | |
| $I_{IN}$ | Control inputs | $V_{CC}$ = 3.6 V, $V_{IN}$ = 3.6 V to 5.5 V or GND | | | | ±10 | µA |
| $I_I$ | | $V_{CC}$ = 3.6 V, $V_{IN}$ = $V_{CC}$ or GND, Switch ON | $V_I$ = $V_{CC}$ – 0.7 V to 5.5 V | | | ±20 | µA |
| | | | $V_I$ = 0.7 V to $V_{CC}$ – 0.7 V | | | –40 | |
| | | | $V_I$ = 0 to 0.7 V | | | ±5 | |
| $I_{OZ}$(3) | | $V_{CC}$ = 3.6 V, $V_I$ = 0, $V_{IN}$ = $V_{CC}$ or GND, $V_O$ = 0 to 5.5 V, Switch OFF | | | | ±10 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, $V_I$ = 0, $V_O$ = 0 to 5.5 V | | | | 10 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $V_{IN}$ = $V_{CC}$ or GND, $I_{I/O}$ = 0, Switch ON or OFF | $V_I$ = $V_{CC}$ or GND | | | 70 | µA |
| | | | $V_I$ = 5.5 V | | | 70 | |
| $\Delta I_{CC}$(4) | Control inputs | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 300 | µA |
| $C_{in}$ | Control inputs | $V_{CC}$ = 3.3 V, $V_{IN}$ = $V_{CC}$ or GND | | | 4 | | pF |
| $C_{io(OFF)}$ | | $V_{CC}$ = 3.3 V, $V_{IN}$ = $V_{CC}$ or GND, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF | | | 9 | | pF |
| $C_{io(ON)}$ | | $V_{CC}$ = 3.3 V, $V_{IN}$ = $V_{CC}$ or GND, Switch ON | $V_{I/O}$ = 5.5 V or 3.3 V | | 8 | | pF |
| | | | $V_{I/O}$ = GND | | 23 | | |
| $r_{ON}$(5) | | $V_{CC}$ = 2.3 V, TYP at $V_{CC}$ = 2.5 V, $V_I$ = 0 | $I_O$ = 24 mA | | 5 | 9.5 | Ω |
| | | | $I_O$ = 16 mA | | 5 | 9.5 | |
| | | $V_{CC}$ = 3 V, $V_I$ = 0 | $I_O$ = 64 mA | | 5 | 8.5 | |
| | | | $I_O$ = 32 mA | | 5 | 8.5 | |

(1) $V_{IN}$ and $I_{IN}$ refer to control inputs. $V_I$, $V_O$, $I_I$, and $I_O$ refer to data pins.
(2) All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
(5) Measured by the voltage drop between A and B terminals at the indicated current throught the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

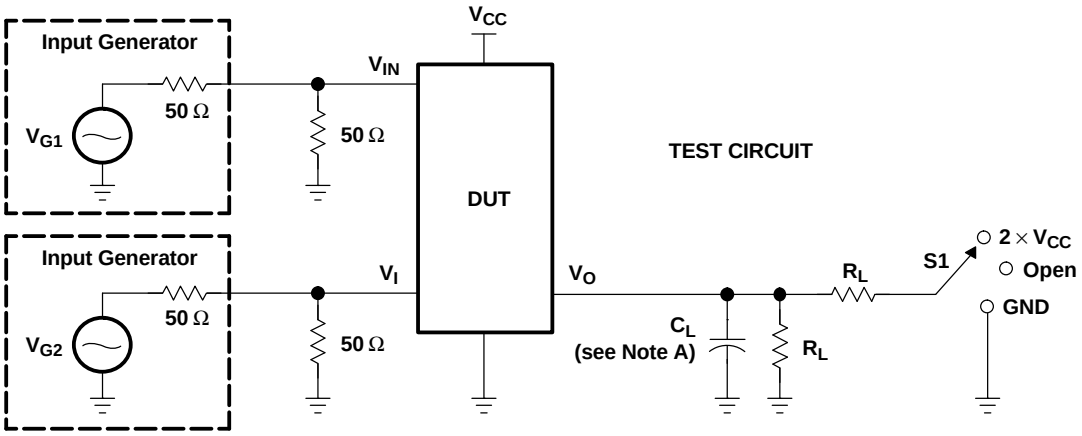
## SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) (see Figure 2)

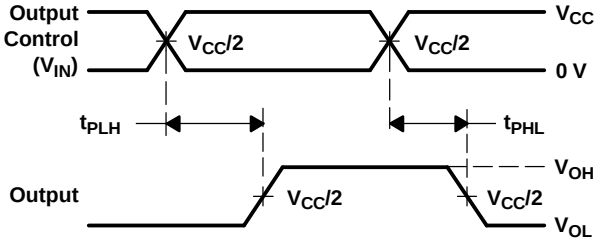
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$(1) | A or B | B or A | | 0.15 | | 0.25 | ns |
| $t_{pd(s)}$ | S | A | 1 | 15.5 | 1 | 11.5 | ns |
| $t_{en}$ | S | B | 1 | 15 | 1 | 12 | ns |
| $t_{dis}$ | S | B | 1 | 12 | 1 | 10.5 | ns |

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capaitance, when driven by an ideal voltage source (zero output impedance).

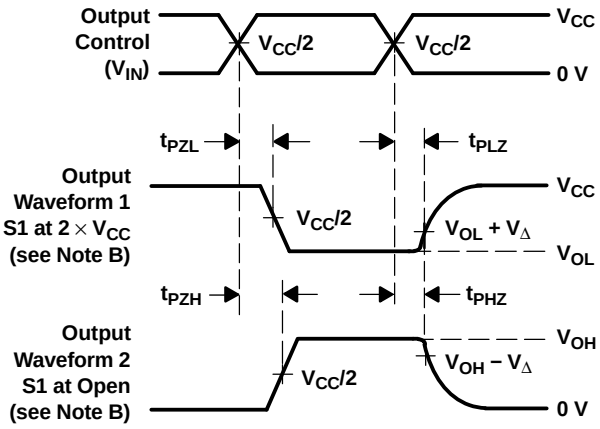
## PARAMETER MEASUREMENT INFORMATION




| TEST | $V_{CC}$ | S1 | $R_L$ | $V_I$ | $C_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|
| $t_{pd(s)}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | Open<br>Open | 500 Ω<br>500 Ω | 3.6 V or GND<br>5.5 V or GND | 30 pF<br>50 pF | |
| $t_{PLZ}/t_{PZL}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | 2 × $V_{CC}$<br>2 × $V_{CC}$ | 500 Ω<br>500 Ω | GND<br>GND | 30 pF<br>50 pF | 0.15 V<br>0.3 V |
| $t_{PHZ}/t_{PZH}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | Open<br>Open | 500 Ω<br>500 Ω | 3.6 V<br>5.5 V | 30 pF<br>50 pF | 0.15 V<br>0.3 V |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

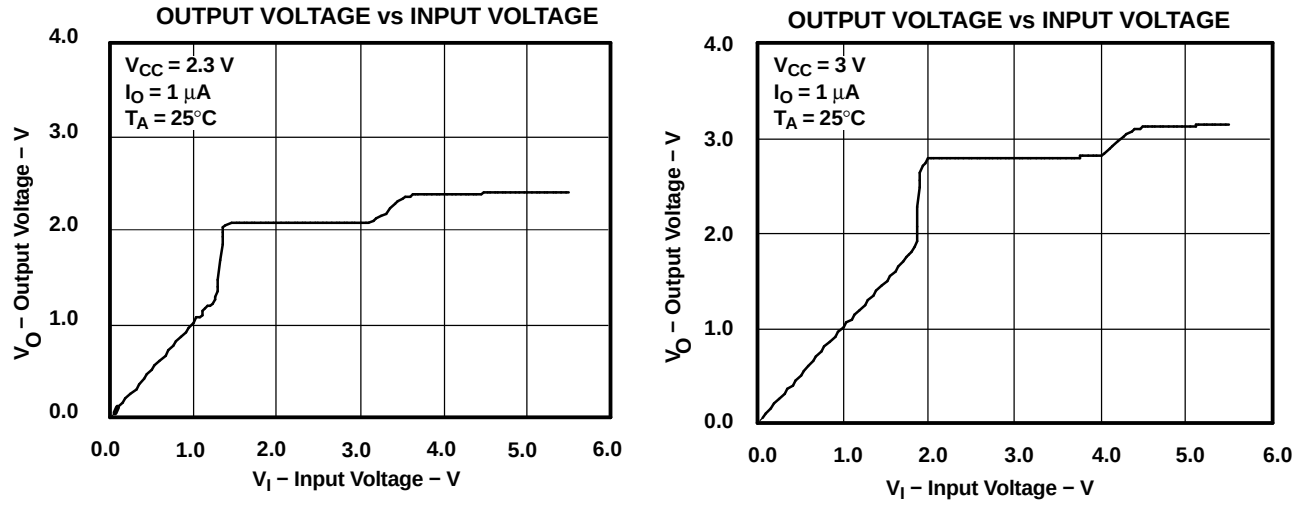
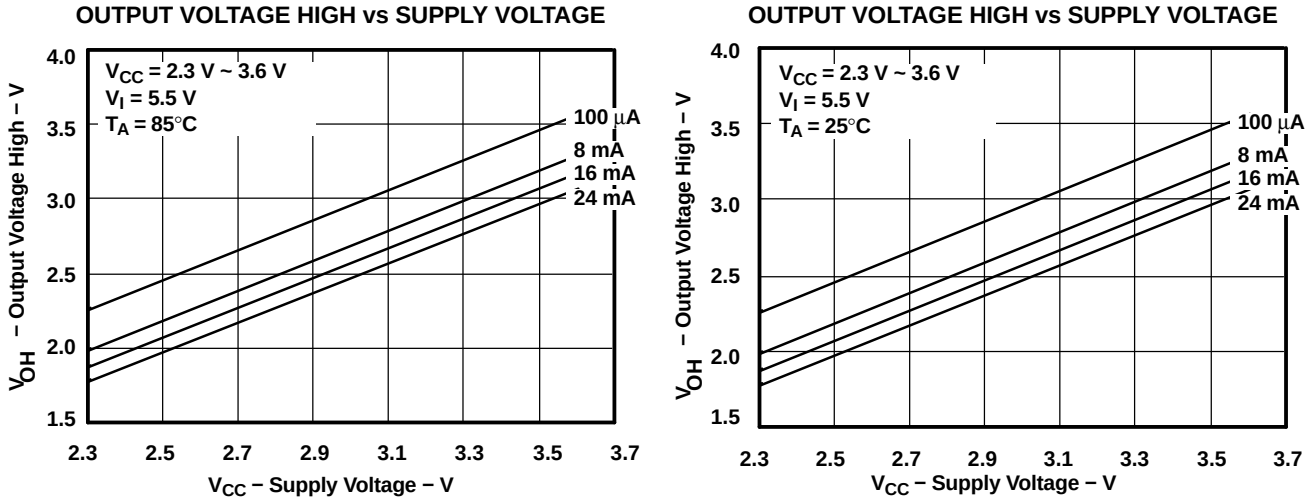



**Figure 3. Data Output Voltage vs Data Input Voltage**



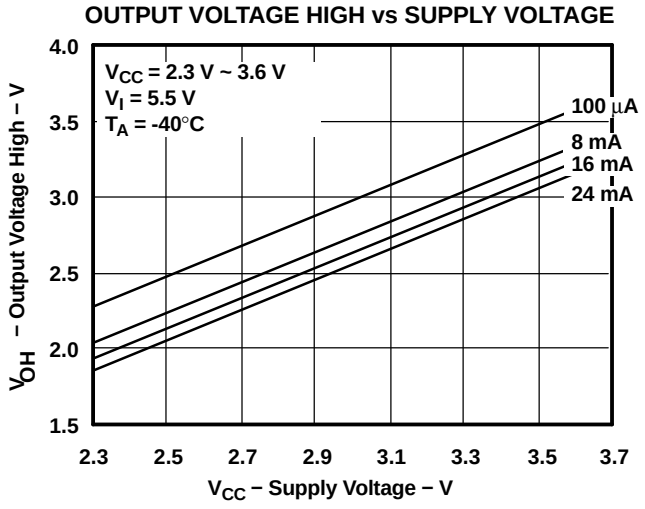




**Figure 4. $V_{OH}$ Values**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 74CB3T16212DGGRG4 | Active | Production | TSSOP (DGG) \| 56 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16212 |
| 74CB3T16212DGGRG4.B | Active | Production | TSSOP (DGG) \| 56 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16212 |
| SN74CB3T16212DGGR | Active | Production | TSSOP (DGG) \| 56 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16212 |
| SN74CB3T16212DGGR.B | Active | Production | TSSOP (DGG) \| 56 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16212 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

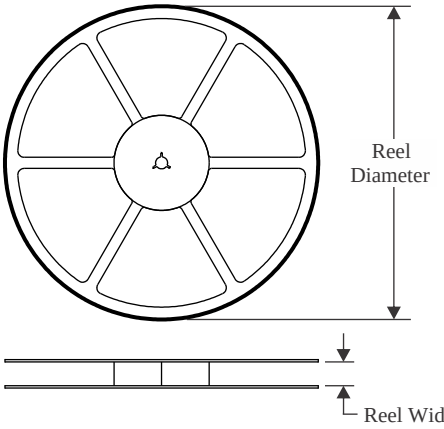
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

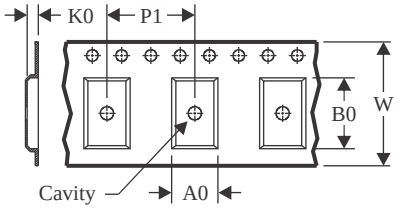
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

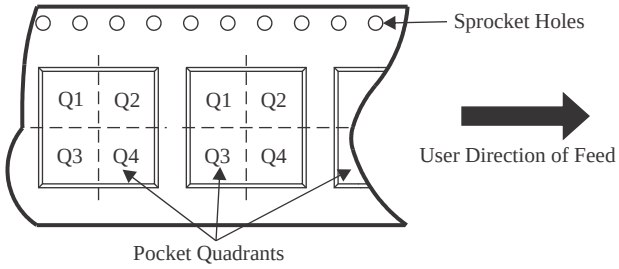



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

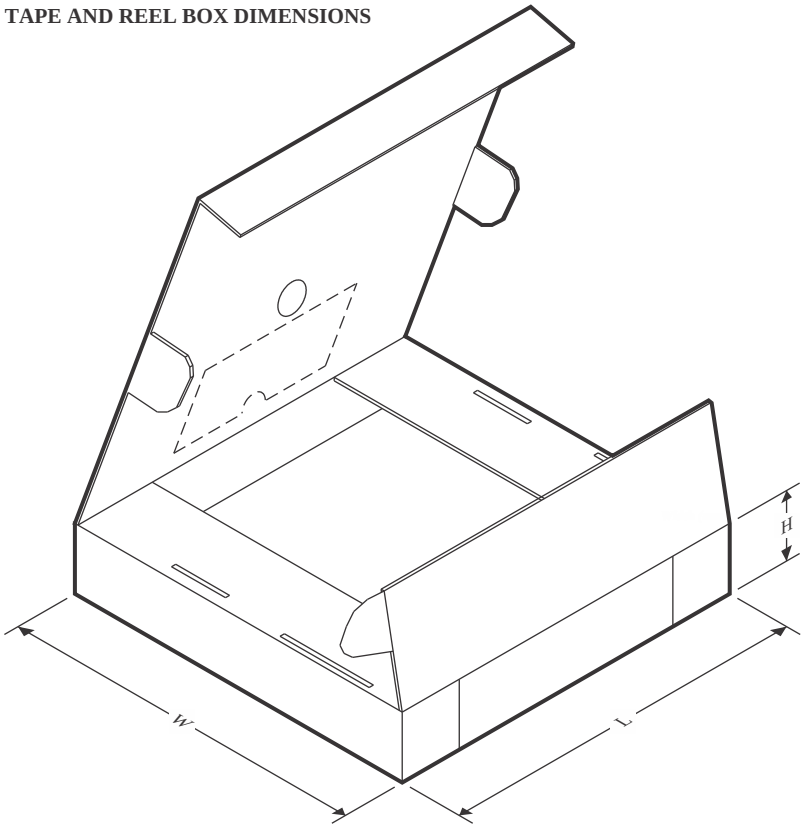
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74CB3T16212DGGRG4 | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.9 | 14.7 | 1.4 | 12.0 | 24.0 | Q1 |
| SN74CB3T16212DGGR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.9 | 14.7 | 1.4 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

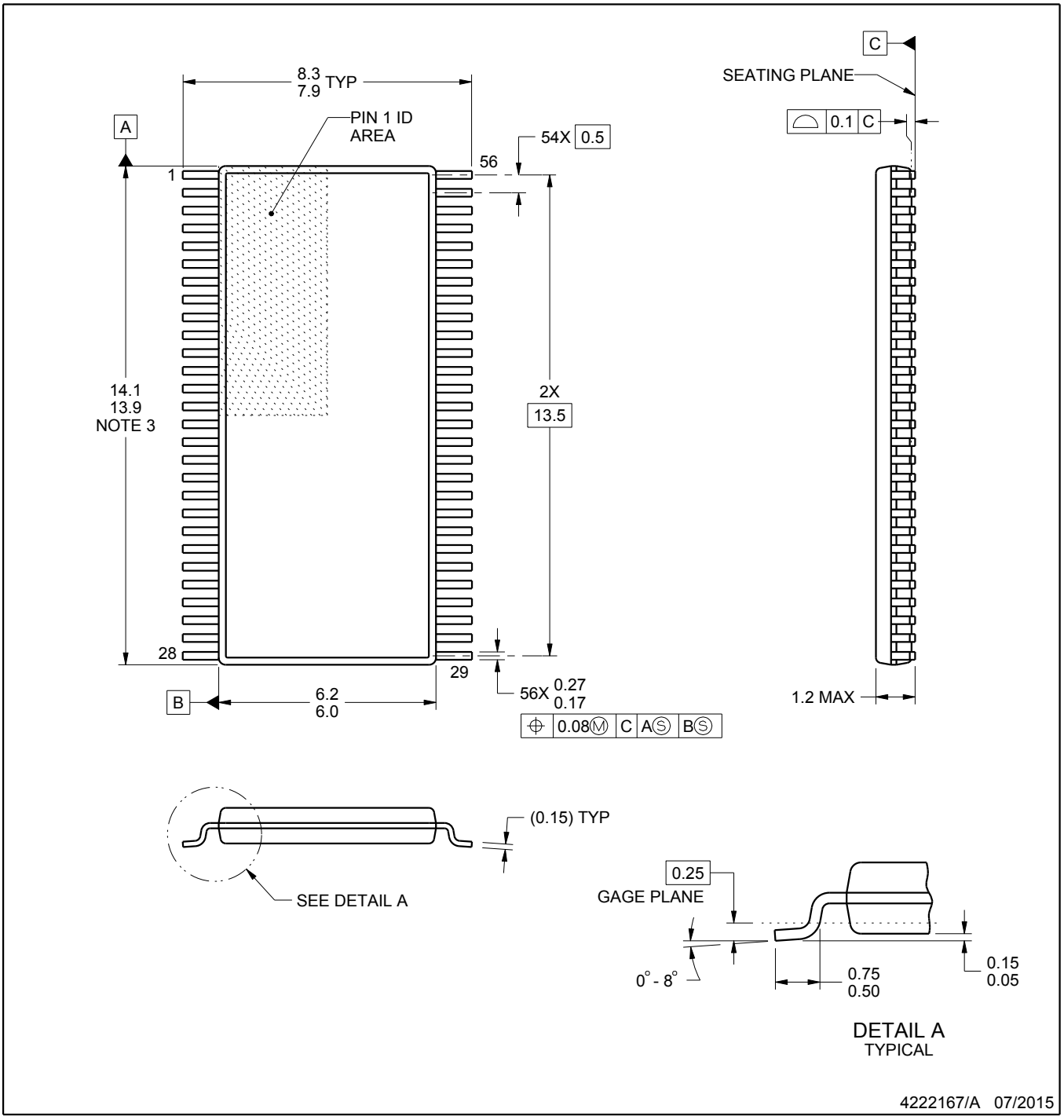
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74CB3T16212DGGRG4 | TSSOP | DGG | 56 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74CB3T16212DGGR | TSSOP | DGG | 56 | 2000 | 356.0 | 356.0 | 45.0 |

# PACKAGE OUTLINE

## DGG0056A

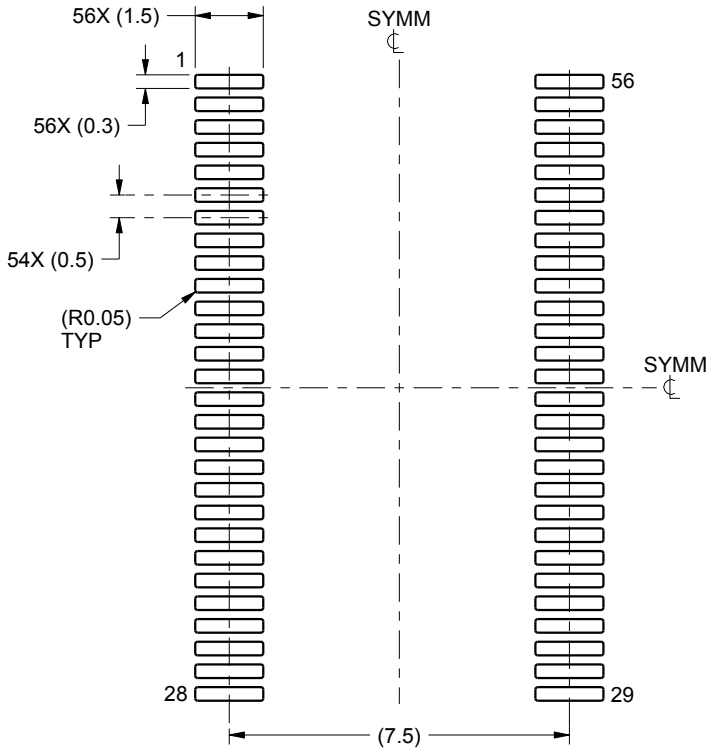
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

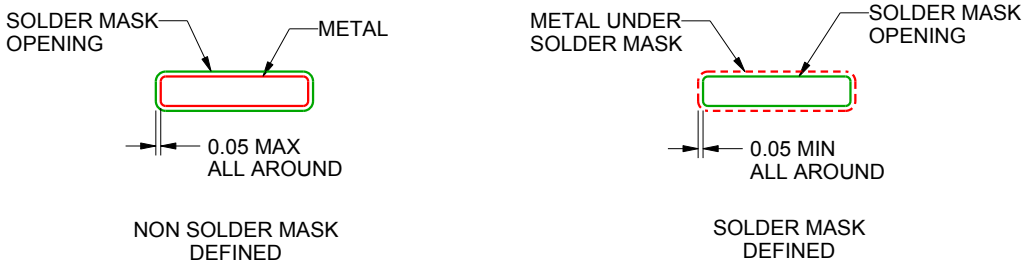



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
SCALE:6X

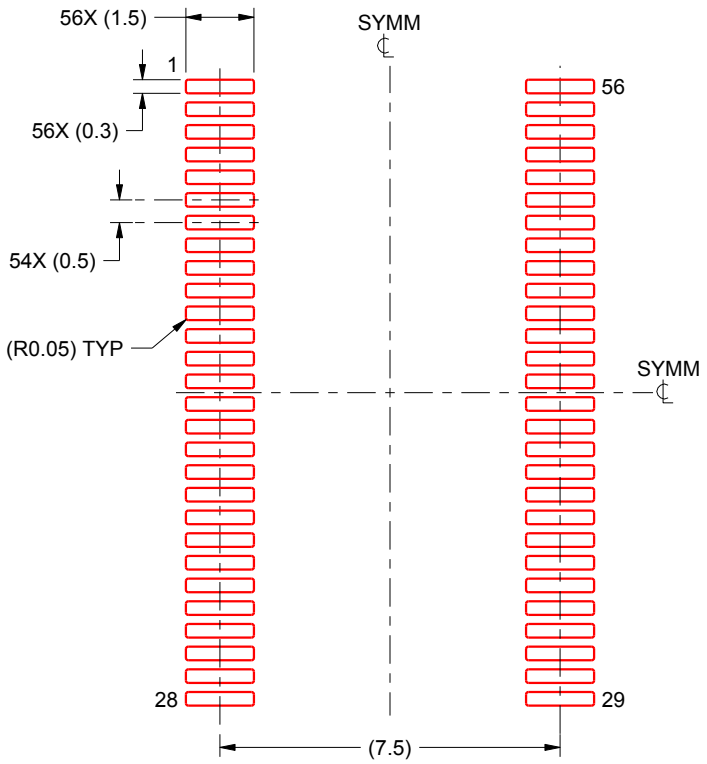



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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