

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
 - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V V_{CC}
 - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 5\ \Omega$ Typ)
- Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)} = 9\text{ pF}$ Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 70\ \mu\text{A}$ Max)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0-V to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model(A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, PCI Interface, USB Interface, Memory Interleaving, and Bus Isolation
- Ideal for Low-Power Portable Equipment

DGG OR DGV PACKAGE
(TOP VIEW)

S0	1	56	S1
1A1	2	55	S2
1A2	3	54	1B1
2A1	4	53	1B2
2A2	5	52	2B1
3A1	6	51	2B2
3A2	7	50	3B1
GND	8	49	GND
4A1	9	48	3B2
4A2	10	47	4B1
5A1	11	46	4B2
5A2	12	45	5B1
6A1	13	44	5B2
6A2	14	43	6B1
7A1	15	42	6B2
7A2	16	41	7B1
V_{CC}	17	40	7B2
8A1	18	39	8B1
GND	19	38	GND
8A2	20	37	8B2
9A1	21	36	9B1
9A2	22	35	9B2
10A1	23	34	10B1
10A2	24	33	10B2
11A1	25	32	11B1
11A2	26	31	11B2
12A1	27	30	12B1
12A2	28	29	12B2

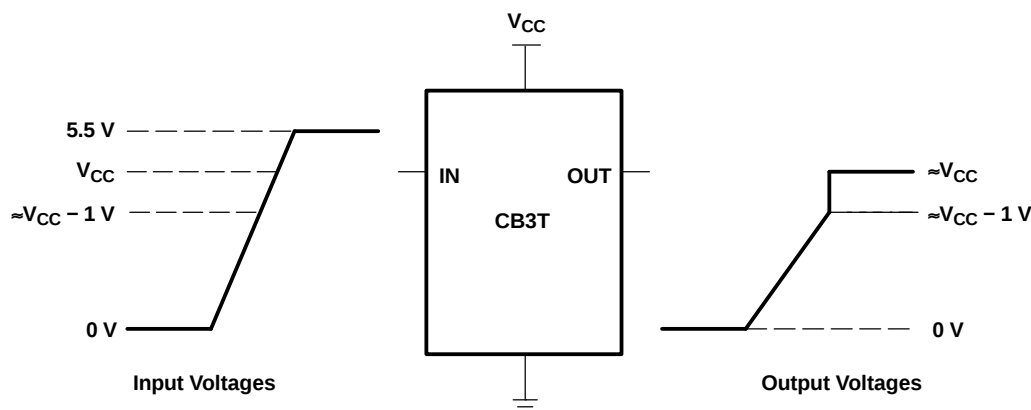
DESCRIPTION/ORDERING INFORMATION

The SN74CB3T16212 is a high-speed TTL-compatible FET bus-exchange switch, with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T16212 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).



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Widebus is a trademark of Texas Instruments.



NOTE: If the input high-voltage (V_{IH}) level is greater than or equal to $V_{CC} - 1\text{ V}$ and less than or equal to 5.5 V , the output high-voltage (V_{OH}) level is equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T16212 operates as a 24-bit bus switch or as a 12-bit bus exchange that provides data exchanging between four signal ports. The select (S_0 , S_1 , S_2) inputs control the data path of the bus-exchange switch. When the bus-exchange switch is ON, the A port is connected to the B port, allowing bidirectional data flow between ports. When the bus-exchange switch is OFF, a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

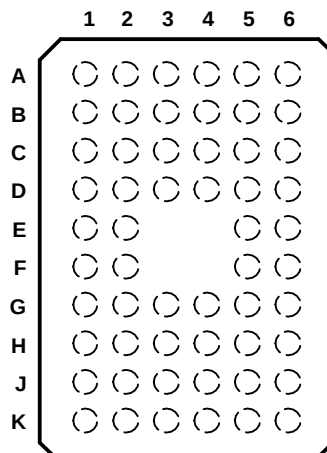
To ensure the high-impedance state during power up or power down, each select input should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74CB3T16212DGGR	CB3T16212
	TVSOP – DGV	Tape and reel	SN74CB3T16212DGVR	KR212
	VFBGA – GQL	Tape and reel	SN74CB3T16212GQLR	KR212
	VFBGA – ZQL (Pb-free)	Tape and reel	SN74CB3T16212ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**GQL OR ZQL PACKAGE
(TOP VIEW)**



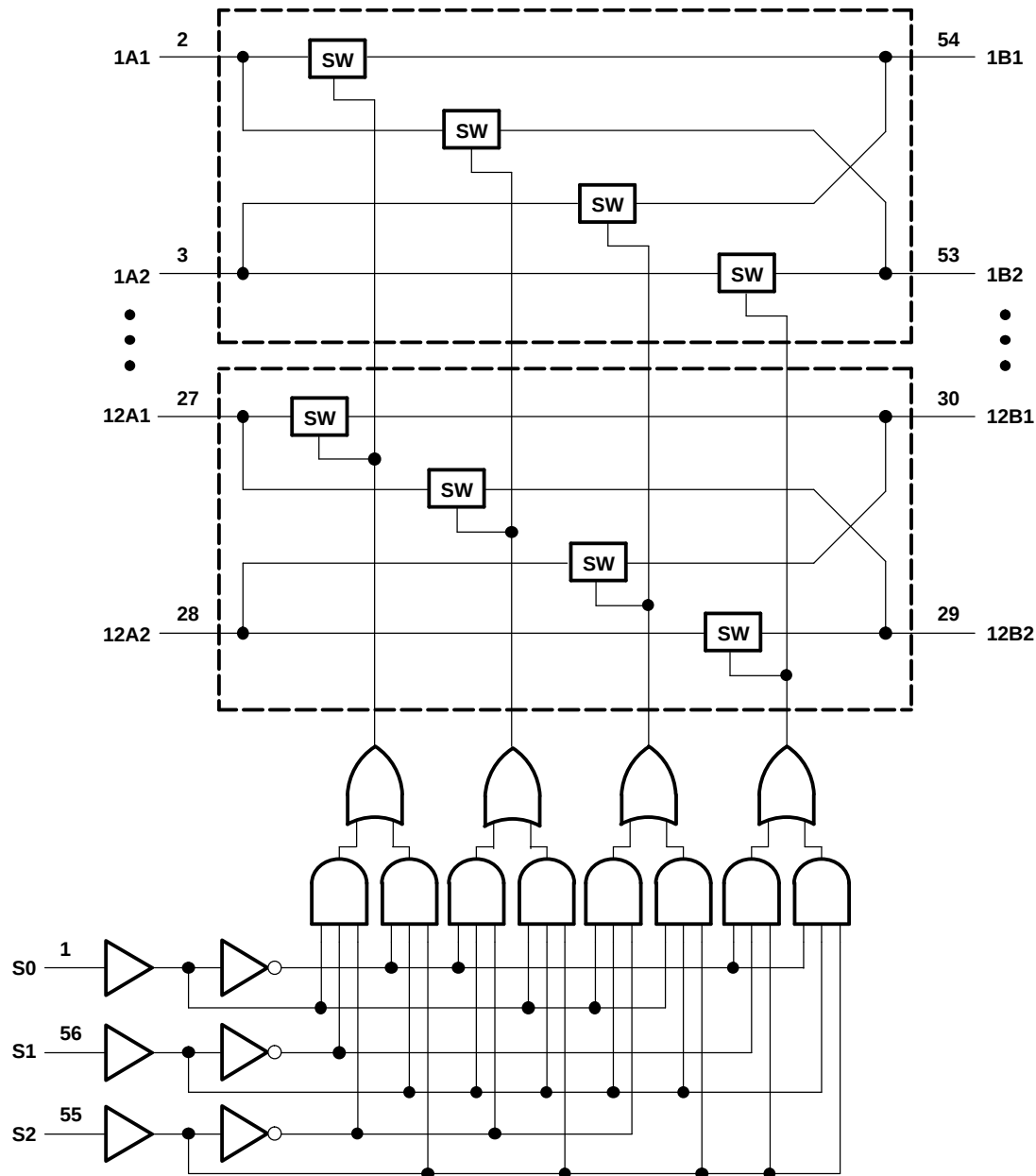
TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	1A2	1A1	S0	S1	S2	1B1
B	3A1	2A2	2A1	1B2	2B1	2B2
C	4A1	GND	3A2	3B1	GND	3B2
D	5A2	4A2	5A1	4B2	4B1	5B1
E	6A2	6A1			5B2	6B1
F	7A1	7A2			7B1	6B2
G	V _{CC}	GND	8A1	8B1	GND	7B2
H	8A2	9A1	9A2	9B2	9B1	8B2
J	10A1	10A2	11A1	11B1	10B2	10B1
K	11A2	12A1	12A2	12B2	12B1	11B2

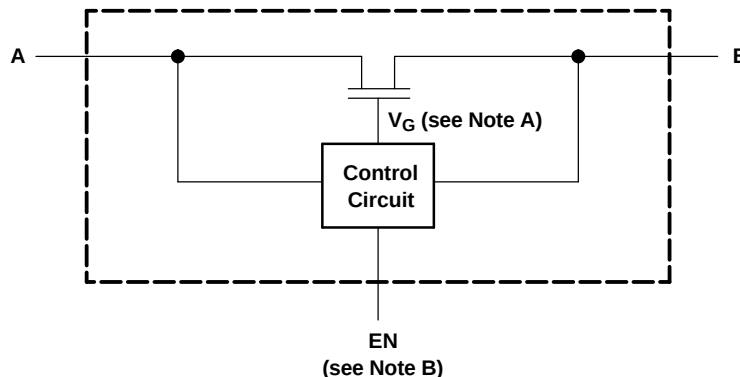
FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1 port	Z	A1 port = B1 port
L	H	L	B2 port	Z	A1 port = B2 port
L	H	H	Z	B1 port	A2 port = B1 port
H	L	L	Z	B2 port	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port
H	H	H	B2 port	B1 port	A1 port = B2 port A2 port = B1 port

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



- A. Gate voltage (V_G) is equal to approximately $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
B. EN is the internal enable signal applied to the switch.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		−0.5	7	V
V _{IN}	Control input voltage range ⁽²⁾⁽³⁾		−0.5	7	V
V _{I/O}	Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾		−0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0		−50	mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0		−50	mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±128	mA
Continuous current through V _{CC} or GND				±100	mA
θ _{JA}	Package thermal impedance ⁽⁶⁾	DGG package		64	°C/W
		DGV package		48	
		GQL/ZQL package		42	
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}		V _{CC} = 3 V, I _I = −18 mA				−1.2	V
V _{OH}		See Figures 3 and 4					
I _{IN}	Control inputs	V _{CC} = 3.6 V, V _{IN} = 3.6 V to 5.5 V or GND				±10	μA
I _I		V _{CC} = 3.6 V, V _{IN} = V _{CC} or GND, Switch ON	V _I = V _{CC} − 0.7 V to 5.5 V			±20	μA
			V _I = 0.7 V to V _{CC} − 0.7 V			−40	
			V _I = 0 to 0.7 V			±5	
I _{OZ} ⁽³⁾		V _{CC} = 3.6 V, V _I = 0, V _{IN} = V _{CC} or GND, V _O = 0 to 5.5 V, Switch OFF				±10	μA
I _{off}		V _{CC} = 0, V _I = 0, V _O = 0 to 5.5 V				10	μA
I _{CC}		V _{CC} = 3.6 V, V _{IN} = V _{CC} or GND, I _{I/O} = 0, Switch ON or OFF	V _I = V _{CC} or GND			70	μA
			V _I = 5.5 V			70	
ΔI _{CC} ⁽⁴⁾	Control inputs	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND				300	μA
C _{in}	Control inputs	V _{CC} = 3.3 V, V _{IN} = V _{CC} or GND			4		pF
C _{iO(OFF)}		V _{CC} = 3.3 V, V _{IN} = V _{CC} or GND, V _{I/O} = 5.5 V, 3.3 V, or GND, Switch OFF			9		pF
C _{iO(ON)}		V _{CC} = 3.3 V, V _{IN} = V _{CC} or GND, Switch ON	V _{I/O} = 5.5 V or 3.3 V		8		pF
			V _{I/O} = GND		23		
r _{ON} ⁽⁵⁾		V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V, V _I = 0	I _O = 24 mA		5	9.5	Ω
			I _O = 16 mA		5	9.5	
		V _{CC} = 3 V, V _I = 0	I _O = 64 mA		5	8.5	
			I _O = 32 mA		5	8.5	

(1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.(2) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

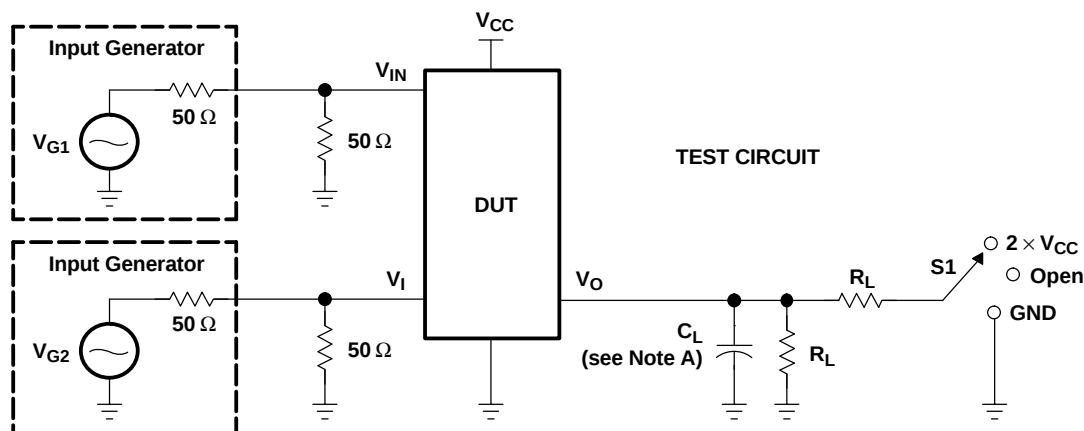
SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) (see Figure 2)

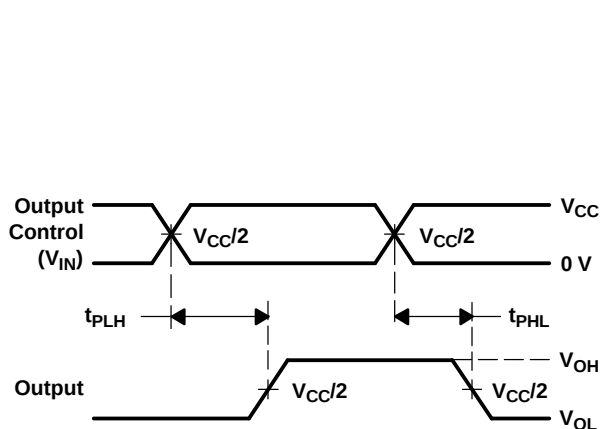
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or B	B or A		0.15		0.25	ns
$t_{pd(s)}$	S	A	1	15.5	1	11.5	ns
t_{en}	S	B	1	15	1	12	ns
t_{dis}	S	B	1	12	1	10.5	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

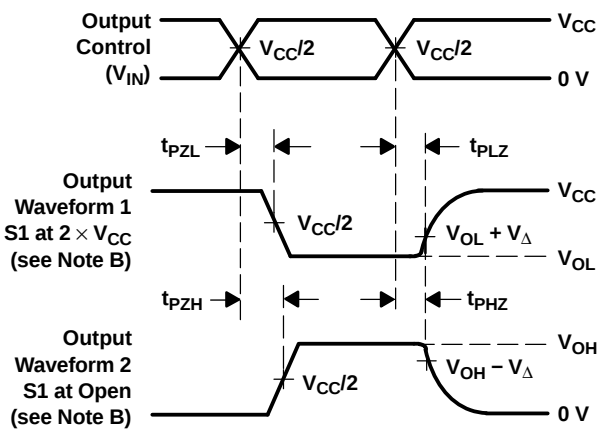
PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V _{CC} 2 × V _{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (t_{pd(s)})



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

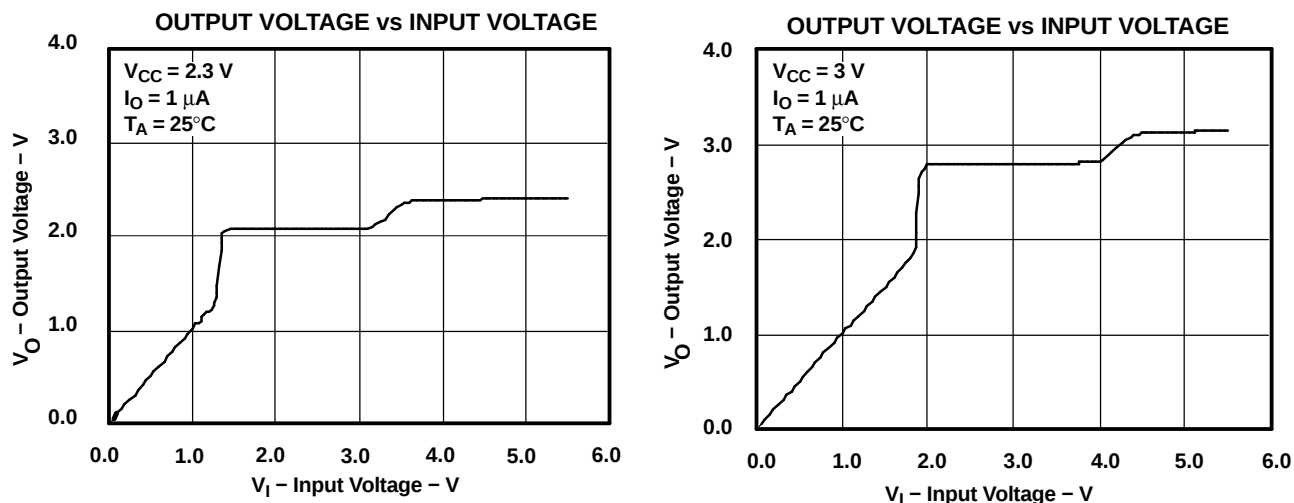
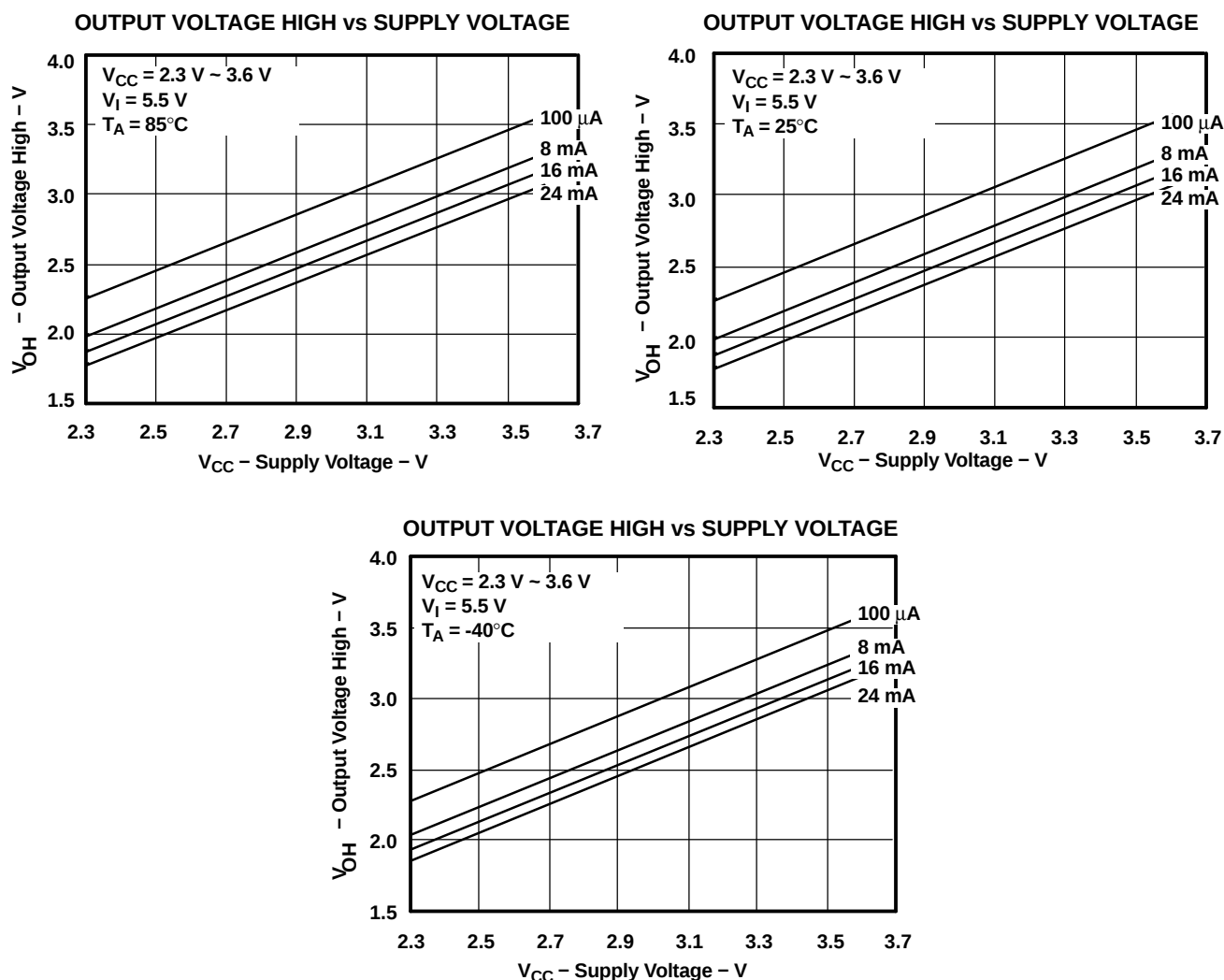


Figure 3. Data Output Voltage vs Data Input Voltage

Figure 4. V_{OH} Values

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CB3T16212DGGRG4	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16212
74CB3T16212DGGRG4.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16212
SN74CB3T16212DGGR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16212
SN74CB3T16212DGGR.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16212

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

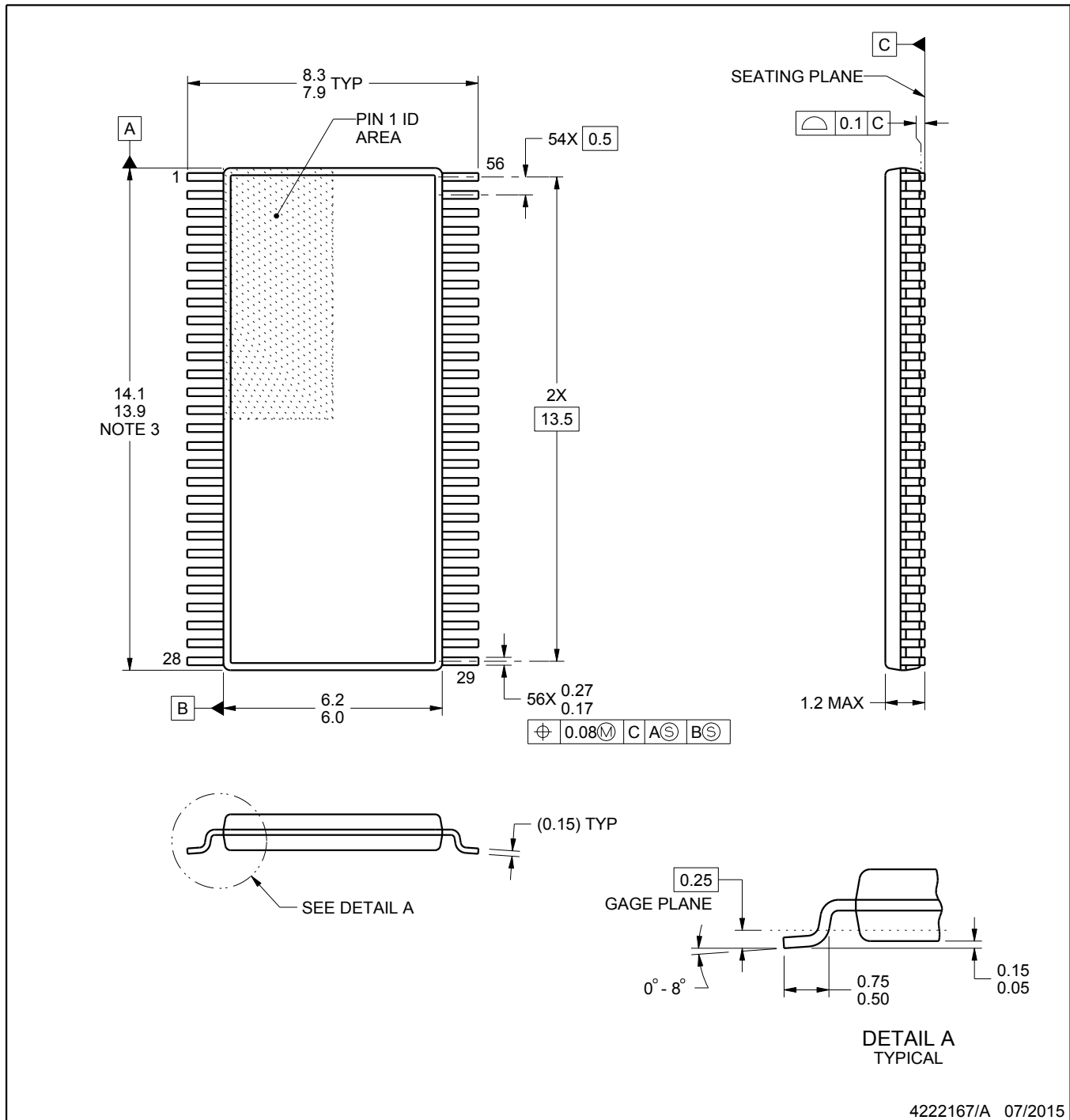
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CB3T16212DGGRG4	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74CB3T16212DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CB3T16212DGGRG4	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74CB3T16212DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0



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NOTES:

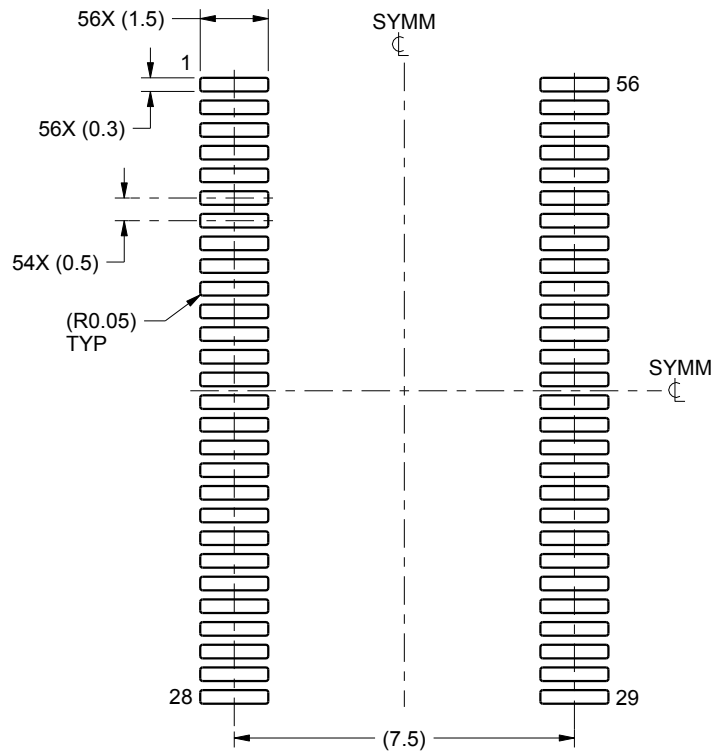
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

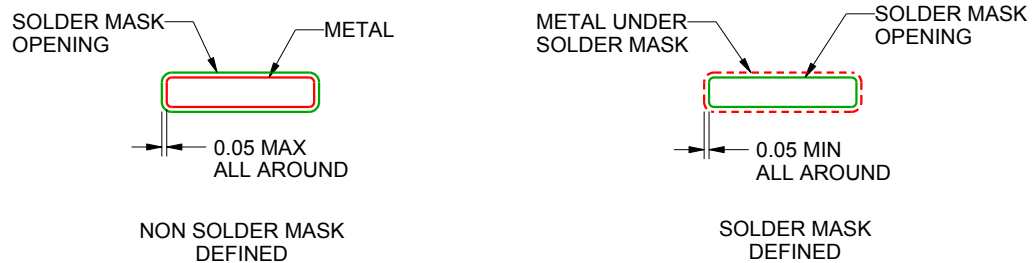
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

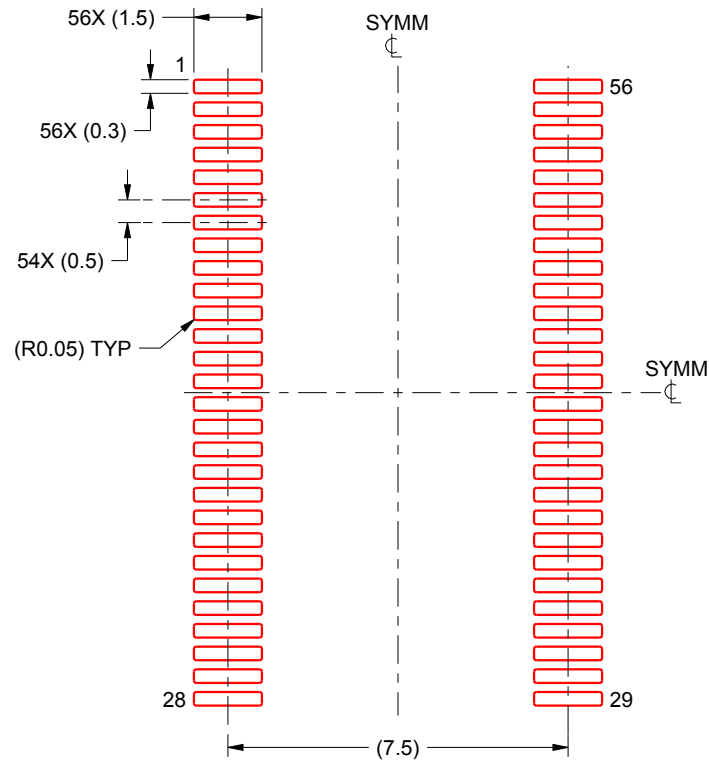
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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