SN74CB3Q3305 デュアル FET バス・スイッチ、2.5V/3.3V、低電圧、高帯域バス・スイッチ

1 特長

- 高帯域幅データ・パス (最大 500MHz)[1]
- デバイスの電源オン時とオフ時の両方で 5V 許容の I/O
- 動作範囲全体にわたって小さく平坦なオン抵抗 (r_{on}) 特性
  (r_{on} = 3Ω、標準値)
- データ I/O ポートの電源電圧を超える入力電圧をサポート
  - V_{CC} = 3.3V で 0～5V のスイッチング
  - V_{CC} = 2.5V で 0～3.3V のスイッチング
- 伝播遅延がゼロに近い双方向データ・フロー
- 低い入力および出力容量により負荷および信号歪みが最小化
  ($C_{io(OFF)}$ = 3.5pF、標準値)
- 高いスイッチング周波数 (f_{OE} = 20MHz、最大値)
- データおよび制御入力にアンダーシュート・クランプ・ダイオードを搭載
- 低消費電力 (I_{CC} = 0.25mA、標準値)
- 2.3V～3.6V の範囲の V_{CC} で動作
- データ I/O は 0～5V の信号レベルに対応 (0.8V、1.2V、1.5V、1.8V、2.5V、3.3V、5V)
- 制御入力は、TTL または 5V/3.3V CMOS 出力で駆動可能
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- IP 電話：有線および無線
- 光モジュール
- 光ネットワーク：Video Over Fiber および EPON
- 構内交換機 (PBX)
- WiMAX およびワイヤレス・インフラストラクチャ機器
- USB、差動信号インターフェイス
- バス絶縁

3 概要

SN74CB3Q3305 デバイスは高帯域の FET バス・スイッチで、チャージ・ポンプを使用してパス・トランジスタのゲート電圧を上昇させ、低い平坦なオン抵抗 (r_{on}) を実現します。オン抵抗が低く平坦であるため、伝搬遅延を最小限に抑えることができ、データ入出力 (I/O) ポートでの電源電圧を超える入力電圧のスイッチングをサポートします。本デバイスはデータ I/O の静電容量が小さいため、データ・バスの容量性負荷と信号歪みも最小限に抑えることができます。高帯域幅アプリケーションに対応するために特別に設計された SN74CB3Q3305 デバイスは、ブロードバンド通信、ネットワーク、データ集約型コンピューティング・システムに理想的な、最適化されたインターフェイス・ソリューションを提供します。

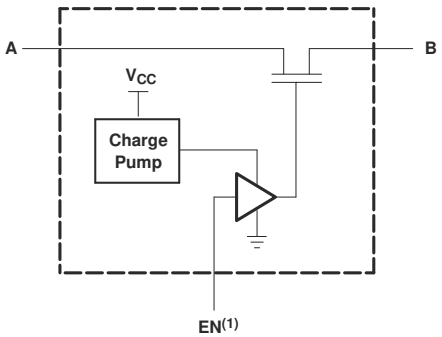
このデバイスは、I_{off} を使用する部分的パワーダウン・アプリケーション用の動作が完全に規定されています。電源切断時にデバイスに電流が逆流することによる損傷を I_{off} 回路が防止します。デバイスは、電源オフ時は絶縁されています。

電源オンまたは電源オフ時に高インピーダンス状態を確保するため、OE をプルダウン抵抗経由で GND に接続する必要があります。この抵抗の最小値は、ドライバの電流ソース能力によって決まります。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
SN74CB3Q3305	VSSOP (8)	2.00mm × 3.10mm
	TSSOP (8)	3.00mm × 6.10mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



(1) EN is the internal enable signal applied to the switch.

概略回路図、各 FET スイッチ (SW)

[1] CB3Q ファミリの性能特性の詳細情報については、TI のアプリケーション・レポート『*CBT-C、CB3T、CB3Q 信号スイッチ・ファミリ*』(SCDA008) を参照してください。

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2015) to Revision D (September 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 包括的な用語を使ってデータシートを更新。	1

Changes from Revision B (October 2009) to Revision C (October 2015)	Page
• 「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加	1

5 Pin Configuration and Functions

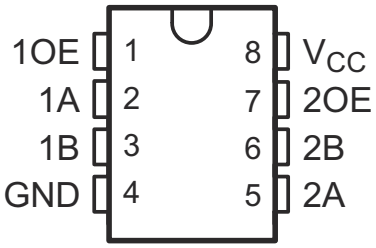


図 5-1. PW Package
8-Pin TSSOP
Top View

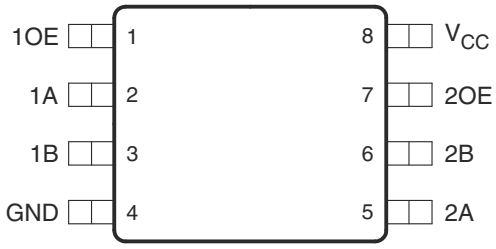


図 5-2. DCU Package
8-Pin VSSOP
Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	2	I/O	Channel 1 A port
1B	3	I/O	Channel 1 B port
1OE	1	I	Output Enable for switch 1
2A	5	I/O	Channel 2 A port
2B	6	I/O	Channel 2 B port
2OE	7	I	Output Enable for switch 2
GND	4	P	Ground
V_{cc}	8	P	Power supply

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)			88	°C/W
T_j	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		SN74CB3Q3305 DCU (VSSOP) 8 PINS	SN74CB3Q3305 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183	190.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.2	74.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.5	119.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	120.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.1	117.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = –18 mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ} [3]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.25	0.7	mA
ΔI_{CC} [4]	Control inputs	V_{CC} = 3.6 V, One input at 3 V, Other inputs at V_{CC} or GND					25	µA
I_{CCD} [5]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.040	0.045	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		8	10.5	pF
r_{on} [6]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0, I_O = 30 mA			3	8	Ω
			V_I = 1.7 V, I_O = –15 mA			3.5	9	
		V_{CC} = 3 V	V_I = 0, I_O = 30 mA			3	6	
			V_I = 2.4 V, I_O = –15 mA			3.5	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see 図 9-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{OE} (1)	OE	A or B	V_{CC} = 2.5 V ± 0.2 V		10	MHz
			V_{CC} = 3.3 V ± 0.3 V		20	
t_{pd} (2)	A or B	B or A	V_{CC} = 2.5 V ± 0.2 V		0.09	ns
			V_{CC} = 3.3 V ± 0.3 V		0.15	
t_{en}	OE	A or B	V_{CC} = 2.5 V ± 0.2 V	1	5	ns
			V_{CC} = 3.3 V ± 0.3 V	1	4.5	
t_{dis}	OE	A or B	V_{CC} = 2.5 V ± 0.2 V	1	4.5	ns
			V_{CC} = 3.3 V ± 0.3 V	1	5	

(1) Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0).
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Typical Characteristics

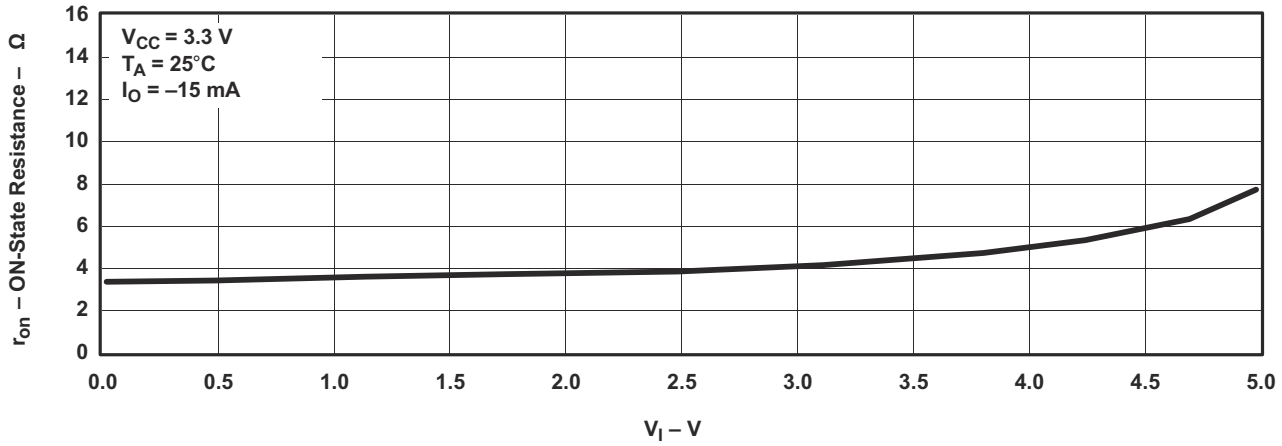
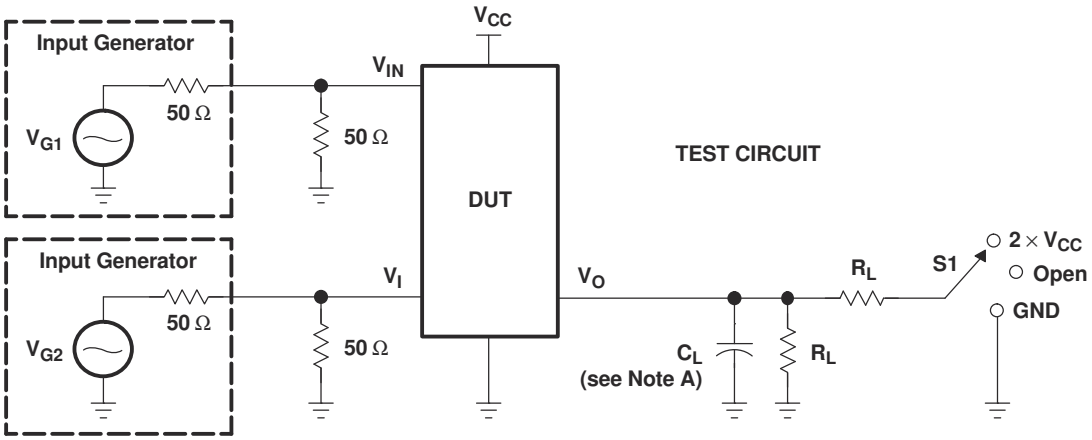
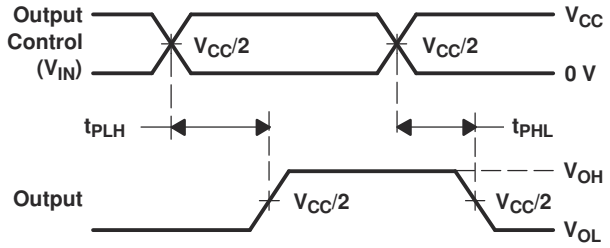


図 6-1. Typical r_{on} vs V_I

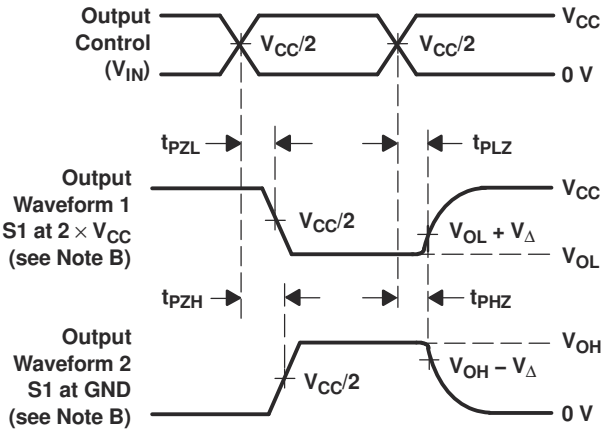
7 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

図 7-1. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CB3Q3305 device is organized as two 1-bit switches with separate output-enable (1OE and 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF and a high-impedance state exists between the A and B ports.

8.2 Functional Block Diagram

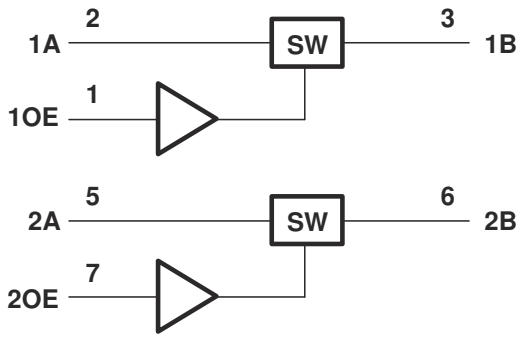


図 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The device supports High-Bandwidth data path up to 500 MHz. The I/O ports are 5 V tolerant when powered up or powered down due to I_{OFF}. The charge pump creates low and flat ON-state resistance characteristics over the whole operating temperature range.

Switching input voltage beyond the supply is supported on data I/O ports: 0 V to 5 V with 3.3 V V_{CC} or 0 V to 3.3 V with 2.5 V V_{CC}.

The data flow is bidirectional with near-zero propagation delay. Reduced input/output capacitance for higher speed applications. OE can be toggled at the high speeds of 20 MHz for fast switching applications.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74CB3Q3305.

表 8-1. Function Table (Each Bus Switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

図 9-1 shows that the SN74CB3Q3305 can be used as bidirectional switch. The controller operates at 5 V and the peripheral can accept 5 V. Even with a V_{CC} of 3 V on the SN74CB3Q3305, the two ports can be connected to pass the 5 V signal. The controller uses the OE pin control the switch. This is a very generic example and could apply to many situations. For applications that require only 1 bit (for example, one channel), tie the unused OE low and tie the unused ports A and B to either high or low (not shown).

9.2 Typical Application

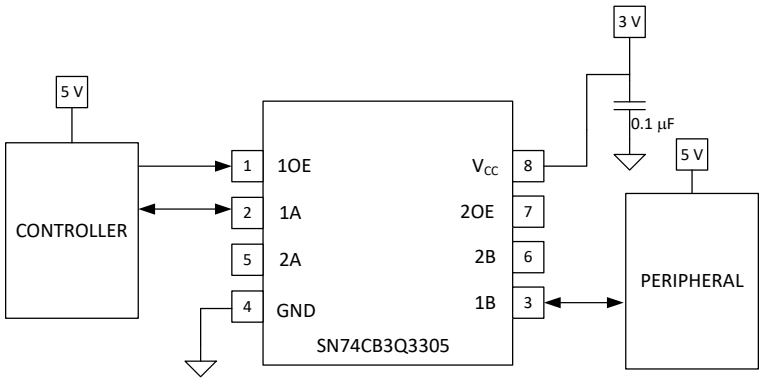


図 9-1. Typical Application of the SN74CB3Q3305

9.2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in セクション 6.3.
   - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Absolute Maximum Conditions:
   - I/O currents should not exceed ±64 mA per channel.
   - Continuos current through GND or V_{CC} should not exceed ±100 mA.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 500 MHz.
   - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in セクション 11.

9.2.2 Detailed Design Procedure

The 0.1 µF capacitor should be placed as close as possible to the device.

9.2.3 Application Curve

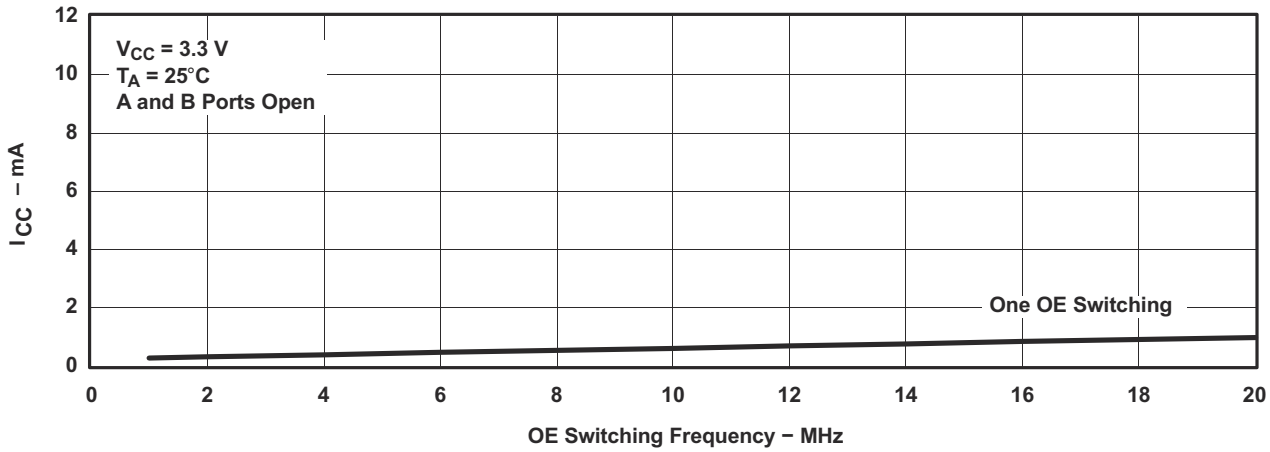


図 9-2. Typical I_{CC} vs OE Switching Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in セクション 6.1 table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01 µF or 0.022 µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1 µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 図 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

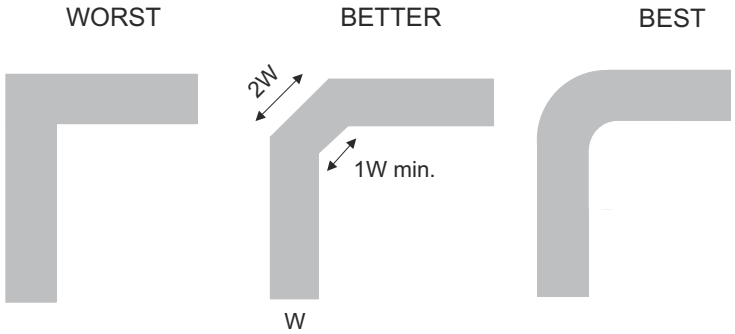


図 11-1. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *CBT-C, CB3T, and CB3Q Signal-Switch Families* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Selecting the Right Texas Instruments Signal Switch* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CB3Q3305DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GARR
74CB3Q3305DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GARR
SN74CB3Q3305DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(GARQ, GARR)
SN74CB3Q3305DCUR.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(GARQ, GARR)
SN74CB3Q3305DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(GARQ, GARR)
SN74CB3Q3305PW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	BU305
SN74CB3Q3305PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BU305
SN74CB3Q3305PWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305
SN74CB3Q3305PWR.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305
SN74CB3Q3305PWRE4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305
SN74CB3Q3305PWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305
SN74CB3Q3305PWRG4.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

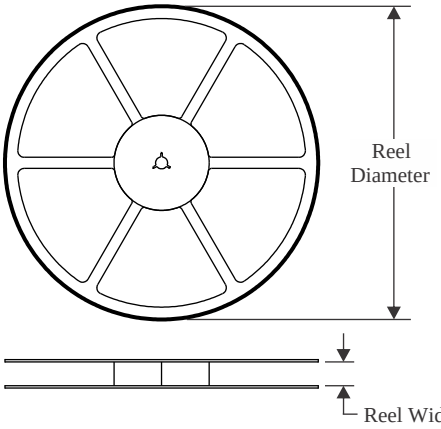
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

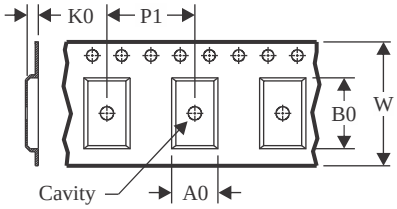
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

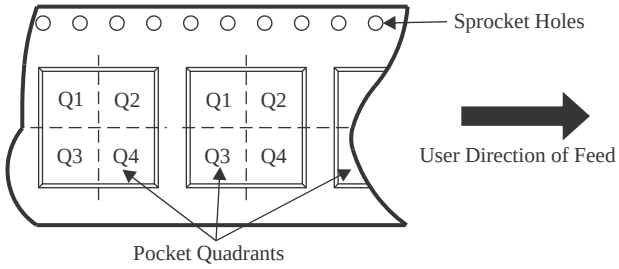


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

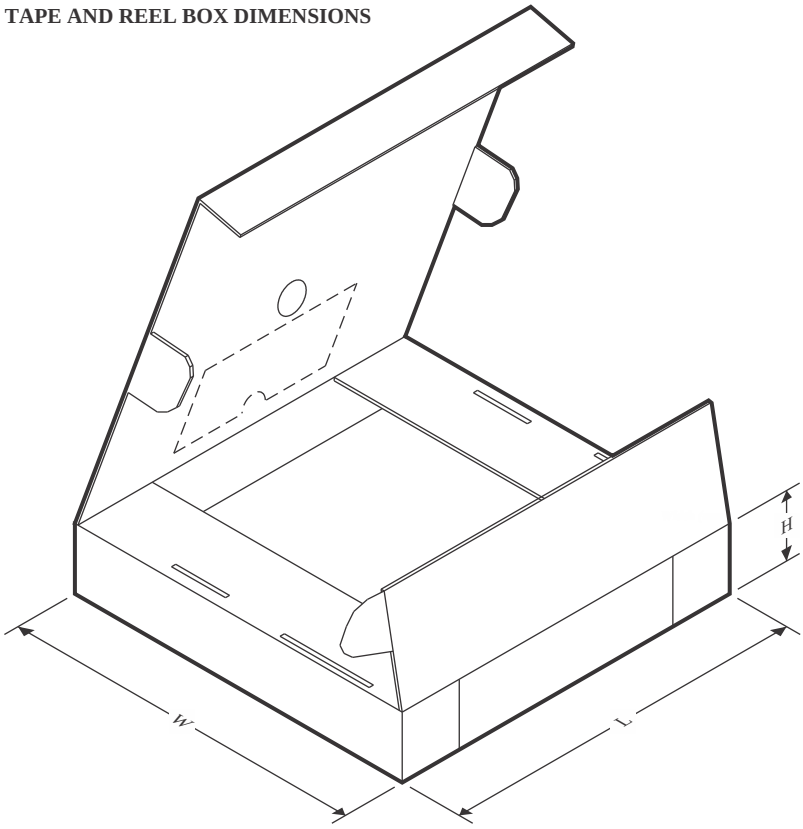
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

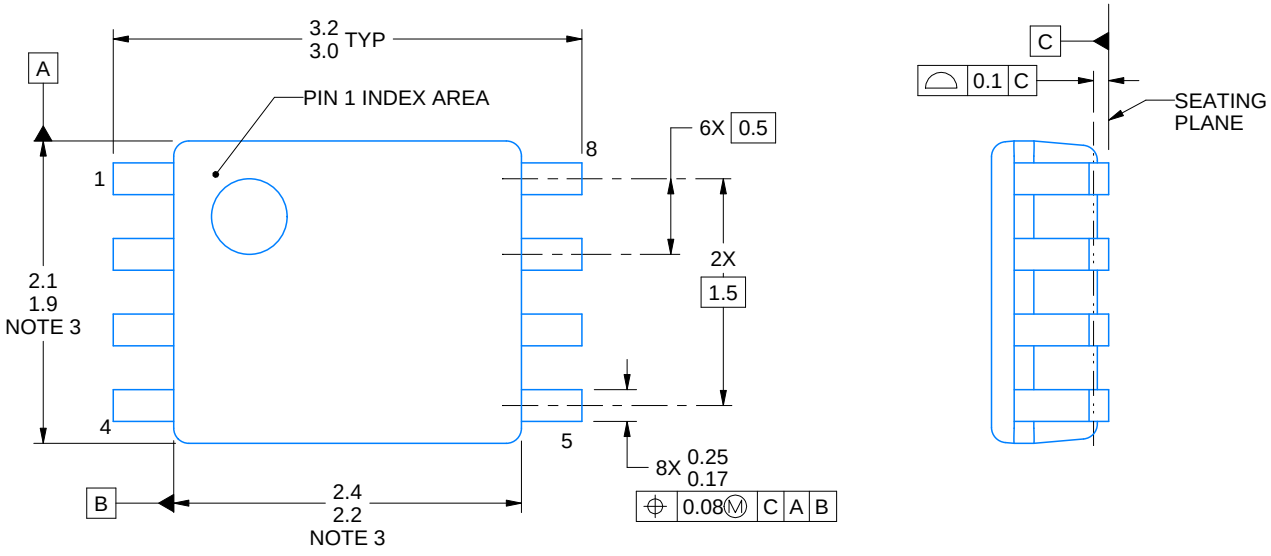
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74CB3Q3305PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0

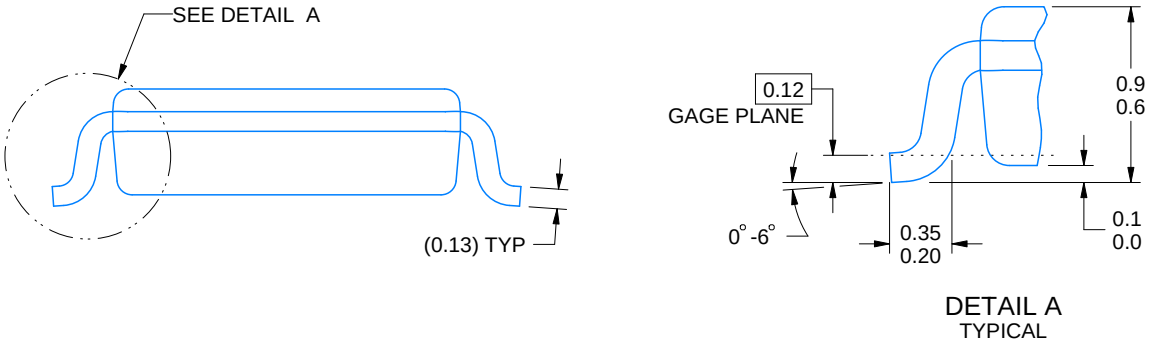
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

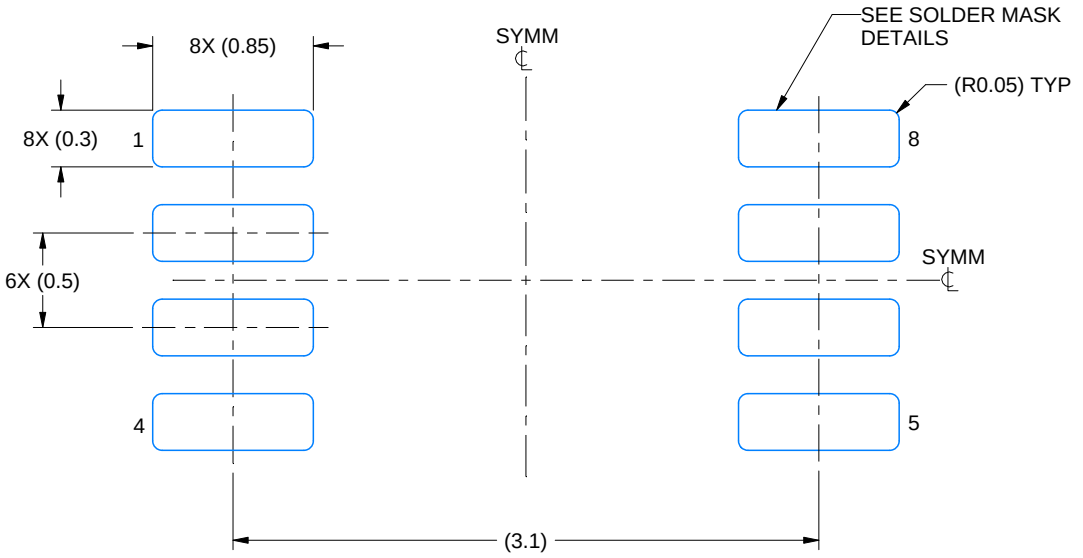




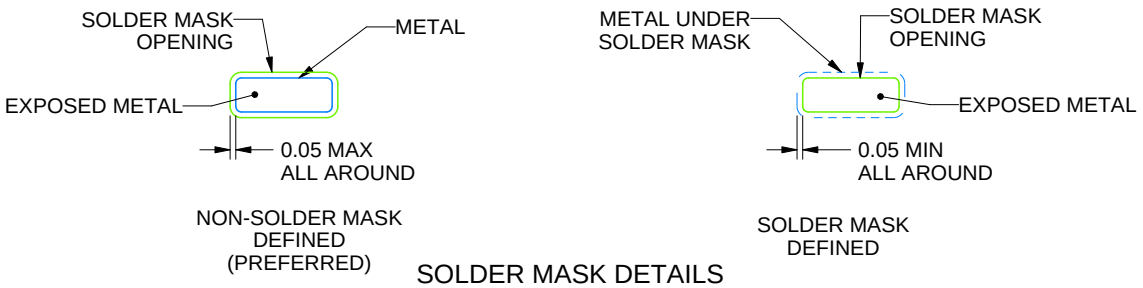
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

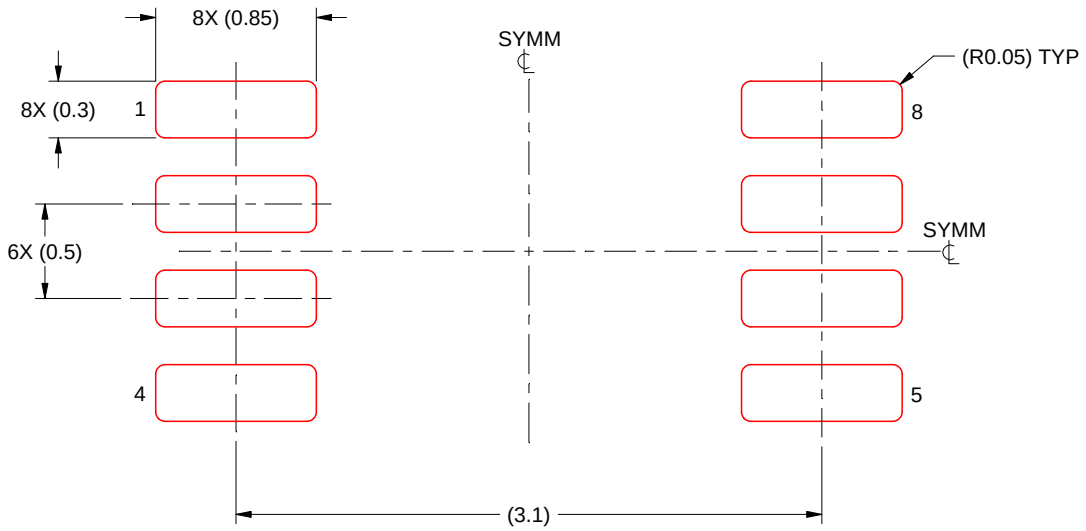


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

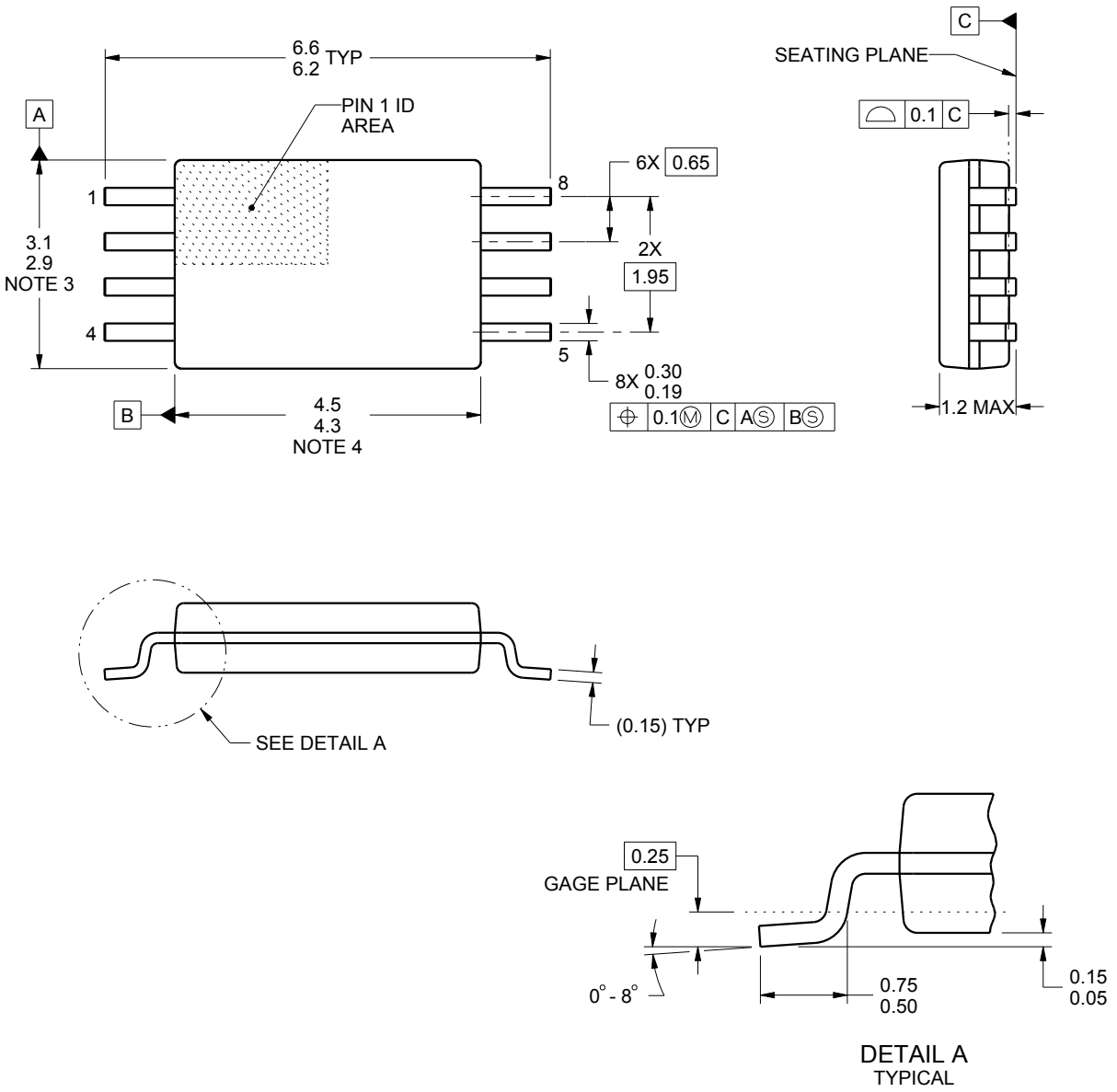
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

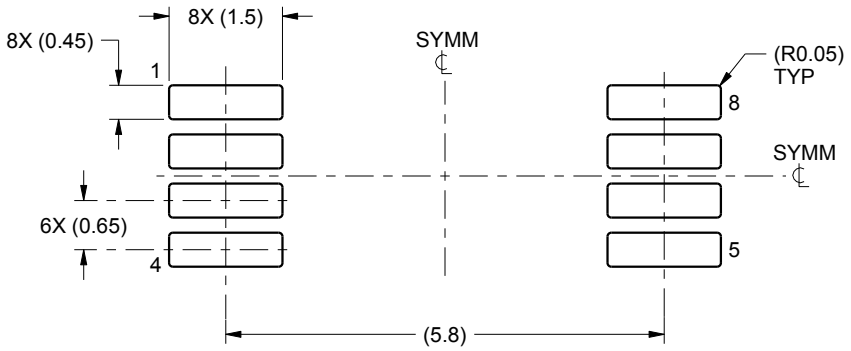
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

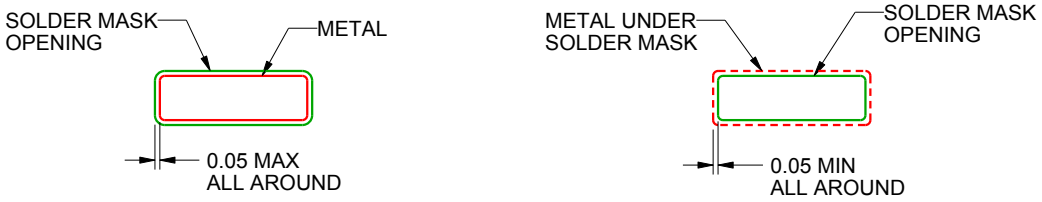


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

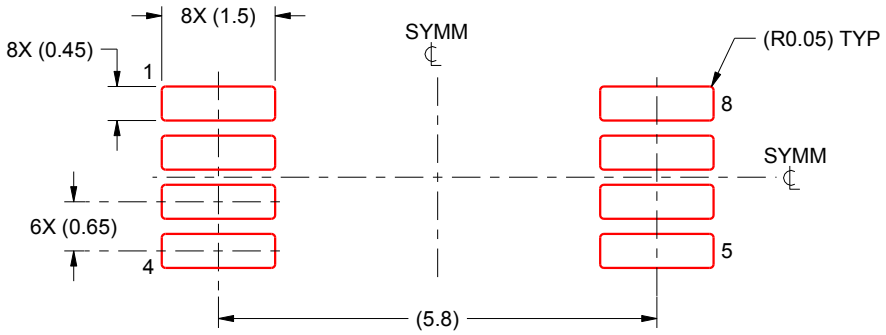


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月