

SCES802-APRIL 2010

LOW POWER, 1.8/2.5/3.3-V INPUT, 3.3-V CMOS OUTPUT, SINGLE SCHMITT-TRIGGER INVERTER GATE

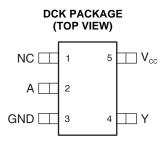
Check for Samples: SN74AUP1T14

FEATURES

- Single-Supply Voltage Translator
- Output Level Up to Supply V_{CC} CMOS Level
 - 1.8 V to 3.3 V (at V_{CC} = 3.3 V)
 - 2.5 V to 3.3 V (at V_{CC} = 3.3 V)
 - 1.8 V to 2.5 V (at V_{CC} = 2.5 V)
 - 3.3 V to 2.5 V (at V_{CC} = 2.5 V
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- I_{off} Supports Partial Power Down (V_{CC} = 0 V)
- Very Low Static Power Consumption: 0.1 μA
- Very Low Dynamic Power Consumption: 0.9 μA
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Pb-Free Packages Available: SC-70 (DCK) 2 x 2.1 x 0.65 mm (Height 1.1 mm)

DESCRIPTION/ORDERING INFORMATION

- More Gate Options Available at www.ti.com/littlelogic
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



The SN74AUP1T14 performs the Boolean function $Y = \overline{A}$ with designation for logic-level translation applications with output referenced to supply V_{CC} .

AUP technology is the industry's lowest-power logic technology designed for use in extending battery-life in operating. All input levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V V_{CC} supply. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).

The wide V_{CC} range of 2.3 V to 3.6 V allows the possibility of switching output level to connect to external controllers or processors.

Schmitt-trigger inputs ($\Delta V_T = 210 \text{ mV}$ between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

 I_{off} is a feature that allows for powered-down conditions ($V_{CC} = 0$ V) and is important in portable and mobile applications. When $V_{CC} = 0$ V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

The SN74AUP1T14 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74AUP1T14

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ORDERING INFORMATION⁽¹⁾

T _A	T _A PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
40%C to 95%C		Reel of 3000	SN74AUP1T14DCKR	¢۲
–40°C to 85°C	SOT (SC-70) – DCK	Reel of 250	SN74AUP1T14DCKT	6F_

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) The actual top-side marking has one additional character that designates the water fab/assembly site.

FUNCTION TABLE

INPUT (Lower Level Input)	OUTPUT (V _{CC} CMOS)
А	Y
Н	L
L	Н

Supply $V_{CC} = 2.3 \text{ V}$ to 2.7 V (2.5 V)

INP V _{T+} max V _{T-} min =	OUTPUT CMOS	
Α	В	Y
V _{IH} =	1.1 V	V _{OH} = 1.85 V
$V_{IL} = 0$	0.35 V	$V_{OL} = 0.45 V$

Supply $V_{CC} = 3 V$ to 3.6 V (3.3 V)

INP V _{T+} max V _{T-} min =	OUTPUT CMOS						
Α	В	Y					
V _{IH} =	1.19 V	V _{OH} = 2.55 V					
V _{IL} =	$V_{IL} = 0.5 V$						

LOGIC DIAGRAM (SCHMITT-TRIGGER INVERTER GATE)

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A <u>-</u>

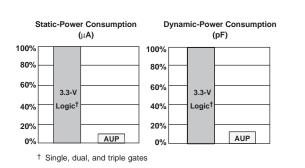
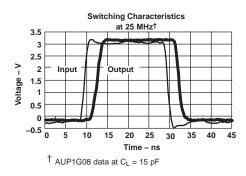


Figure 1. AUP – The Lowest-Power Family





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SN74AUP1T14

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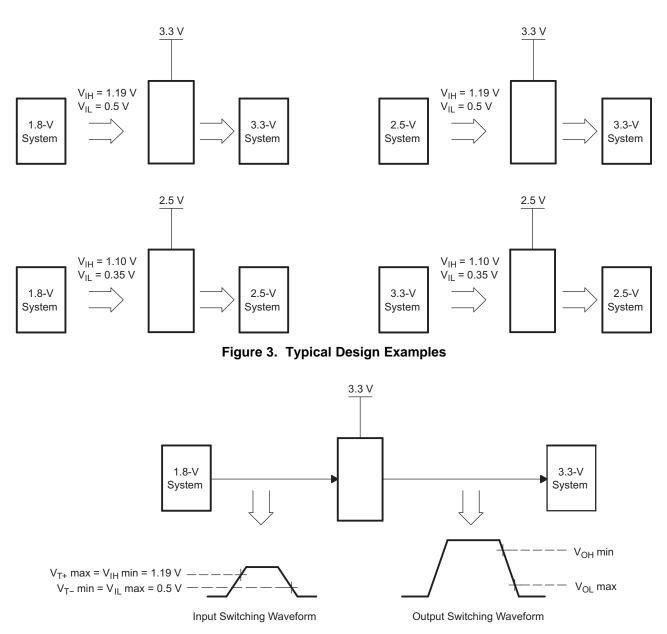


Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾		-0.5	4.6	V
Vo	Voltage range applied to any output in the high-impedance or power-off state	(2)	-0.5	4.6	V
Vo	Output voltage range in the high or low state ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
lo	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DCK package		259	°C/W
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
VI	Input voltage		0	3.6	V
Vo	Output voltage		0	V_{CC}	V
	Ligh lovel output ourgest	$V_{CC} = 2.3 V$		-3.1	~ ^
I _{OH}	High-level output current	$V_{CC} = 3 V$		-4	mA
		V_{CC} = 2.3 V		3.1	~ ^
OL	Low-level output current	$V_{CC} = 3 V$		3.6 3.6 V _{CC} -3.1 -4	mA
T _A	Operating free-air temperature		-40	85	°C

 All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications* of Slow or Floating CMOS Inputs, literature number SCBA004.



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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	V _{cc}	T _A =	= 25°C	T _A = -40 to 85°C		UNIT
				MIN	TYP MAX	MIN	MAX	
V_{T+}			2.3 V to 2.7 V	0.6	1.1	0.6	1.1	
	e-going input old voltage		3 V to 3.6 V	0.75	1.16	0.75	1.19	V
V _{T-}			2.3 V to 2.7 V	0.35	0.6	0.35	0.6	
Negative-going input threshold voltage			3 V to 3.6 V	0.5	0.85	0.5	0.85	V
ΔV_T			2.3 V to 2.7 V	0.23	0.6	0.1	0.6	
Hystere (V _{T+} -			3 V to 3.6 V	0.25	0.56	0.15	0.56	V
		I _{OH} = -20 μA	2.3 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1		
		I _{OH} = -2.3 mA	2.3 V	2.05		1.97		V
V _{OH}		I _{OH} = -3.1 mA	2.3 V	1.9		1.85		
		I _{OH} = -2.7 mA	3 V	2.72		2.67		
		$I_{OH} = -4 \text{ mA}$	3 V	2.6		2.55		
		I _{OL} = 20 μA	2.3 V to 3.6 V		0.1		0.1	
		I _{OL} = 2.3 mA	2.3 V		0.31		0.33	
V _{OL}		I _{OL} = 3.1 mA	2.3 V		0.44		0.45	V
		I _{OL} = 2.7 mA	3 V		0.31		0.33	
		I _{OL} = 4 mA	3 V		0.44		0.45	
l _l	All inputs	$V_I = 3.6 V \text{ or GND}$	0 V to 3.6 V		0.1		0.5	μΑ
I _{off}		V_{I} or $V_{O} = 0$ V to 3.6 V	0 V		0.1		0.5	μΑ
∆l _{off}		V_{I} or $V_{O} = 3.6 V$	0 V to 0.2 V		0.2		0.5	μΑ
I _{CC}		$V_{I} = 3.6 \text{ V or GND}, I_{O} = 0$	2.3 V to 3.6 V		0.5		0.9	μΑ
AL		One input at 0.3 V or 1.1 V, Other inputs at 0 or V _{CC} , $I_0 = 0$	2.3 V to 2.7 V				4	
ΔI _{CC}		One input at 0.45 V or 1.2 V, Other inputs at 0 or V _{CC} , $I_0 = 0$	3 V to 3.6 V				12	μA
Ci		$V_{I} = V_{CC}$ or GND	3.3 V		1.5			pF
Co		$V_{O} = V_{CC}$ or GND	3.3 V		3			pF

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $V_I = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted) (see Figure 5)

	PARAMETER	FROM (INPUT)		CL	Т	ק = 25°C		T _A = to 85	40°C 5°C	UNIT
		(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	
				5 pF	1.8	2.3	2.9	0.5	6.8	
	4	•	v	10 pF	2.3	2.8	3.4	1	7.9	
	t _{pd}	A	Y	15 pF	2.6	3.1	3.8	1	8.7	ns
				30 pF	3.8	4.4	5.1	1.5	10.8	



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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $V_1 = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 5)

PARAMETER	FROM	TO	TO UTPUT) CL	T _A = 25°C			T _A = to 85	UNIT	
	(INPUT)	(001P01)		MIN	TYP	MAX	MIN	MAX	
			5 pF	1.8	2.3	3.1	0.5	6	
	•	v	10 pF	2.2	2.8	3.5	1	7.1	
t _{pd}	A	Ť	15 pF	2.6	3.2	5.2	1	7.9	ns
			30 pF	3.7	4.4	5.2	1.5	10	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $V_I = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO	C _L	т,	λ = 25°C		T _A = to 85	40°C 5°C	UNIT
	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	
			5 pF	2	2.7	3.5	0.5	5.5	
	•	V	10 pF	2.4	3.1	3.9	1	6.5	
t _{pd}	A	ř	15 pF	2.8	3.5	4.3	1	7.4	ns
			30 pF	4	4.7	5.5	1.5	9.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_I = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted) (see Figure 5)

PARAMETER		TO (OUTPUT) C _L						T _A = to 85	UNIT
	(INPUT)			MIN	TYP	MAX	MIN	MAX	
		5 pF	1.6	2	2.5	0.5	8		
	•	V	10 pF	2	2.4	2.9	1	8.5	
t _{pd}	A	ř	15 pF	2.3	2.8	3.3	1	9.1	ns
			30 pF	3.4	3.9	4.4	1.5	9.8	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_1 = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO	CL	Т	ק = 25°C		T _A = to 85	40°C 5°C	UNIT
		(OUTPUT)		MIN	TYP	MAX	MIN	MAX	
	5 pF	1.6	1.9	2.4	0.5	5.3			
	٨	V	10 pF	2	2.3	2.7	1	6.1	
t _{pd}	A	Ť	15 pF	2.3	2.7	3.1	1	6.8	ns
			30 pF	3.4	3.8	4.2	1.5	8.5	



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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_I = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 5)

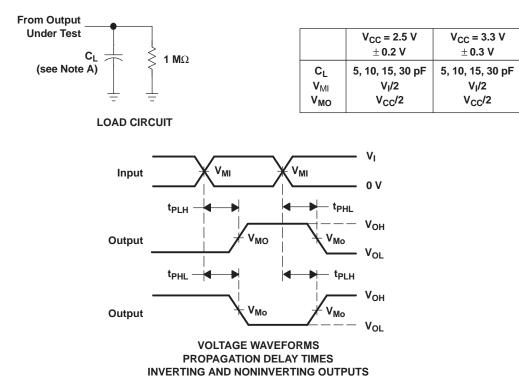
PARAMETER	FROM	TO			T _A = 25°C			T _A = -40°C to 85°C	
	(INPUT)	(OUTPUT)	_	MIN	TYP	MAX	MIN	MAX	
t _{pd}			5 pF	1.6	2.1	2.7	0.5	4.7	
	•	v	10 pF	10 pF 2 2.4 15 pF 2.3 2.7	3	1	5.7	~~	
	A	ř	15 pF		2.7	3.3	1	6.2	ns
			30 pF	3.4	3.8	4.4	1.5	7.8	

OPERATING CHARACTERISTICS

 $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
C _{pd}	Power dissipation capacitance	f = 10 MHz	4	5	pF	





PARAMETER MEASUREMENT INFORMATION

- NOTES: A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , slew rate \geq 1 V/ns.
 - C. The outputs are measured one at a time, with one transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AUP1T14DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	6FF
SN74AUP1T14DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	6FF
SN74AUP1T14DCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6FF
SN74AUP1T14DCKRG4.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6FF

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	-	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T14DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AUP1T14DCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3



PACKAGE MATERIALS INFORMATION

25-Jun-2025



*All dimensions are nominal

Device	Package Type Package Drawing Pins		SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74AUP1T14DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AUP1T14DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0

DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



DCK0005A

EXAMPLE BOARD LAYOUT

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

Publication IPC-7351 may have alternate designs.
Solder mask tolerances between and around signal pads can vary based on board fabrication site.



DCK0005A

EXAMPLE STENCIL DESIGN

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

10. Board assembly site may have different recommendations for stencil design.



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