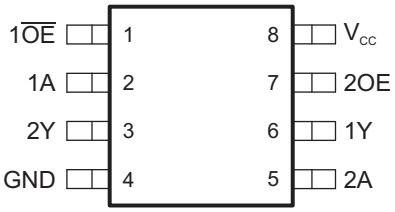
SN74AUC2G241
DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES535C – DECEMBER 2003 – REVISED JANUARY 2007

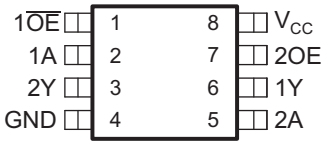
FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Sub-1-V Operable**
- **Max t_{pd} of 1.9 ns at 1.8 V**
- **Low Power Consumption, 10 μA at 1.8 V**
- **±8-mA Output Drive at 1.8 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

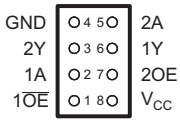
DCT PACKAGE
(TOP VIEW)



DCU PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This dual buffer/driver is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC2G241 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device is organized as two 1-bit line drivers with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. When $1\overline{OE}$ is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or 2OE is low, the outputs are in the high-impedance state.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G241YZPR	_ _ _U2_
	SSOP – DCT	Reel of 3000	SN74AUC2G241DCTR	U41_ _ _
	VSSOP – DCU	Reel of 3000	SN74AUC2G241DCUR	U2_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor, and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

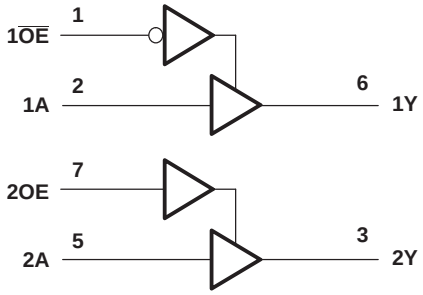
For more information about AUC Little Logic devices, please refer to the TI application report, *Applications of Texas Instruments AUC Sub-1-V Little Logic Devices,* literature number SCEA027.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	3.6	V
V_I	Input voltage range(2)		–0.5	3.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	3.6	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(3)	DCT package		220	°C/W
		DCU package		227	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
V_I	Input voltage		0	3.6	V
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	
I_{OH}	High-level output current	V_{CC} = 0.8 V		–0.7	mA
		V_{CC} = 1.1 V		–3	
		V_{CC} = 1.4 V		–5	
		V_{CC} = 1.65 V		–8	
		V_{CC} = 2.3 V		–9	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		0.7	mA
		V_{CC} = 1.1 V		3	
		V_{CC} = 1.4 V		5	
		V_{CC} = 1.65 V		8	
		V_{CC} = 2.3 V		9	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 0.8 V to 1.65 V[2]		20	ns/V
		V_{CC} = 1.65 V to 1.95 V[3]		20	
		V_{CC} = 2.3 V to 2.7 V[3]		20	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) The data was taken at C_L = 15 pF, R_L = 2 kΩ (see Figure 1).
(3) The data was taken at C_L = 30 pF, R_L = 500 Ω (see Figure 1).

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		0.8 V to 2.7 V	V_{CC} – 0.1			V
		I_{OH} = –0.7 mA		0.8 V		0.55		
		I_{OH} = –3 mA		1.1 V	0.8			
		I_{OH} = –5 mA		1.4 V	1			
		I_{OH} = –8 mA		1.65 V	1.2			
		I_{OH} = –9 mA		2.3 V	1.8			
V_{OL}		I_{OL} = 100 µA		0.8 V to 2.7 V			0.2	V
		I_{OL} = 0.7 mA		0.8 V		0.25		
		I_{OL} = 3 mA		1.1 V			0.3	
		I_{OL} = 5 mA		1.4 V			0.4	
		I_{OL} = 8 mA		1.65 V			0.45	
		I_{OL} = 9 mA		2.3 V			0.6	
I_I	All inputs	$V_I = V_{CC}$ or GND		0 to 2.7 V			±5	µA
I_{off}		V_I or V_O = 2.7 V		0			±10	µA
I_{OZ}		$V_O = V_{CC}$ or GND		2.7 V			±10	µA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	0.8 V to 2.7 V			10	µA
C_I		$V_I = V_{CC}$ or GND		2.5 V		2.5		pF
C_o		$V_O = V_{CC}$ or GND		2.5 V		5.5		pF

(1) All typical values are at T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	5.1	1	3.5	0.8	2.3	0.7	1.2	1.9	0.6	1.4	ns
t_{en}	$\overline{OE}$ or OE	Y	5.9	1.2	4.2	1	2.7	0.9	1.3	2	0.8	1.6	ns
t_{dis}	$\overline{OE}$ or OE	Y	6.2	2.2	4.8	2.5	4.4	1	2.9	4.2	1.6	3.3	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 1)

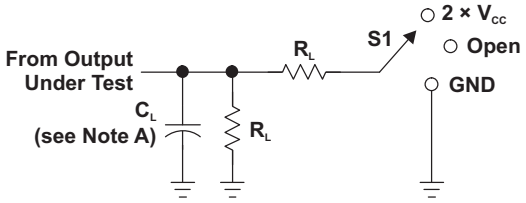
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.9	1.6	2.5	0.8	1.8	ns
t_{en}	$\overline{OE}$ or OE	Y	1.1	1.7	2.8	1	2	ns
t_{dis}	$\overline{OE}$ or OE	Y	1.9	2.3	3.6	0.9	2.1	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	16	16	16	17	18	pF

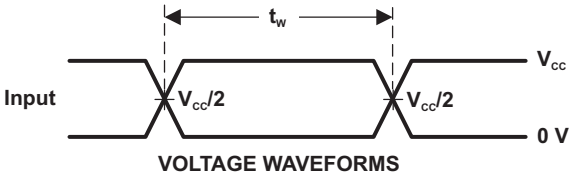
PARAMETER MEASUREMENT INFORMATION



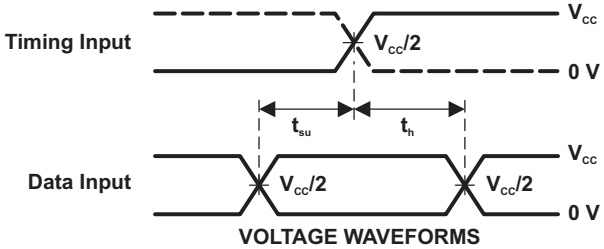
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

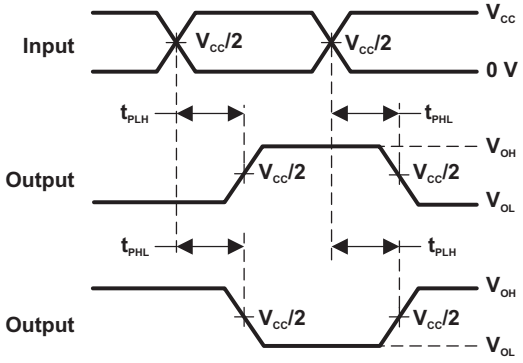
V_{CC}	C_L	R_L	V_Δ
0.8 V	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V



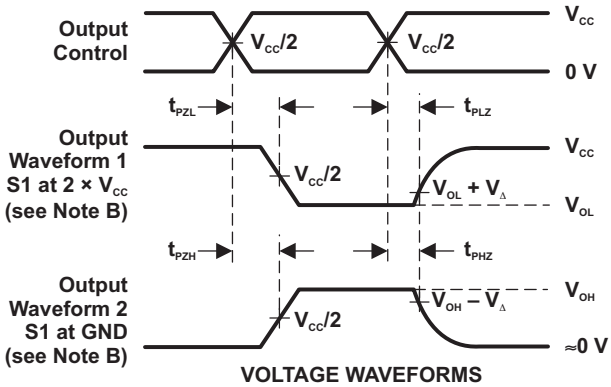
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUC2G241DCTR	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2XB5, U41) (R, Z)
SN74AUC2G241DCTR.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2XB5, U41) (R, Z)
SN74AUC2G241DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(U41Q, U41R)
SN74AUC2G241DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U41Q, U41R)
SN74AUC2G241DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
SN74AUC2G241YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U2N
SN74AUC2G241YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U2N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

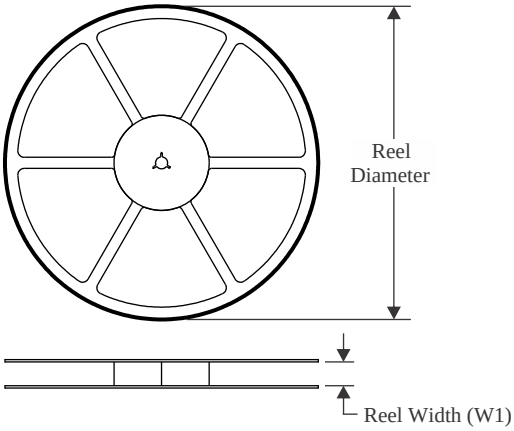
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

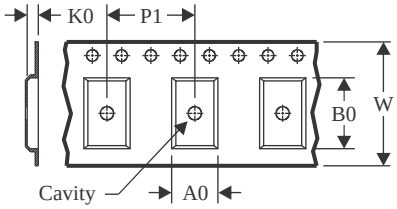
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

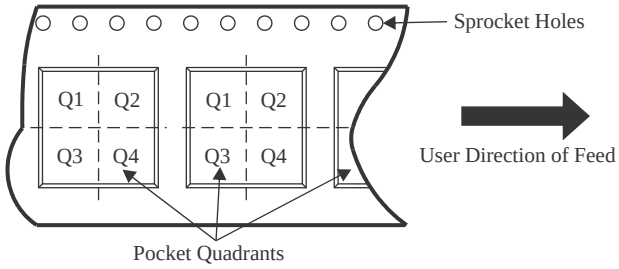


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

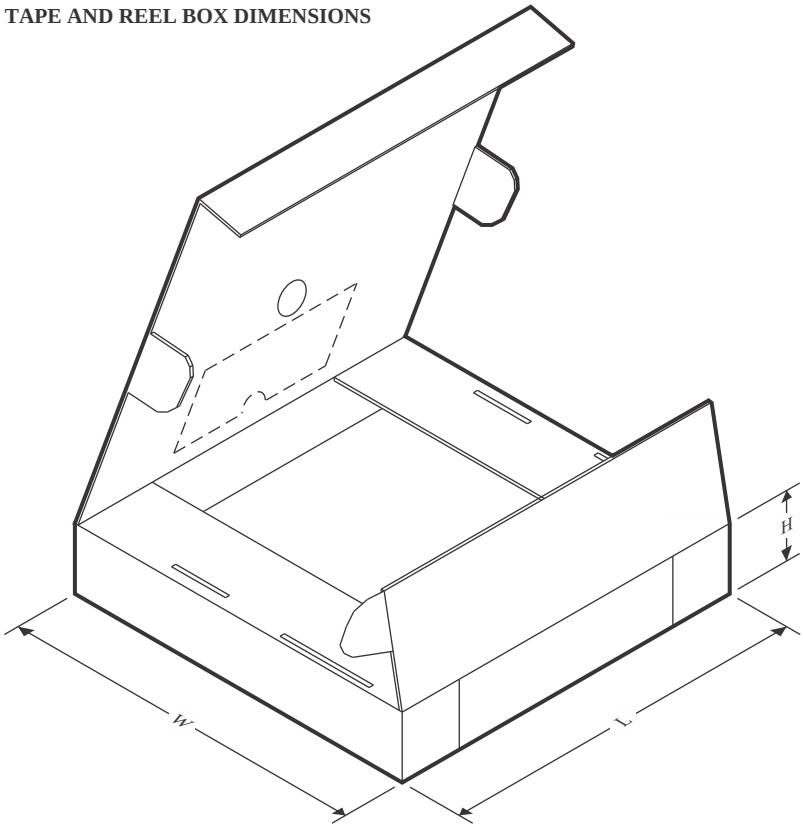
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G241DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC2G241DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G241DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G241YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

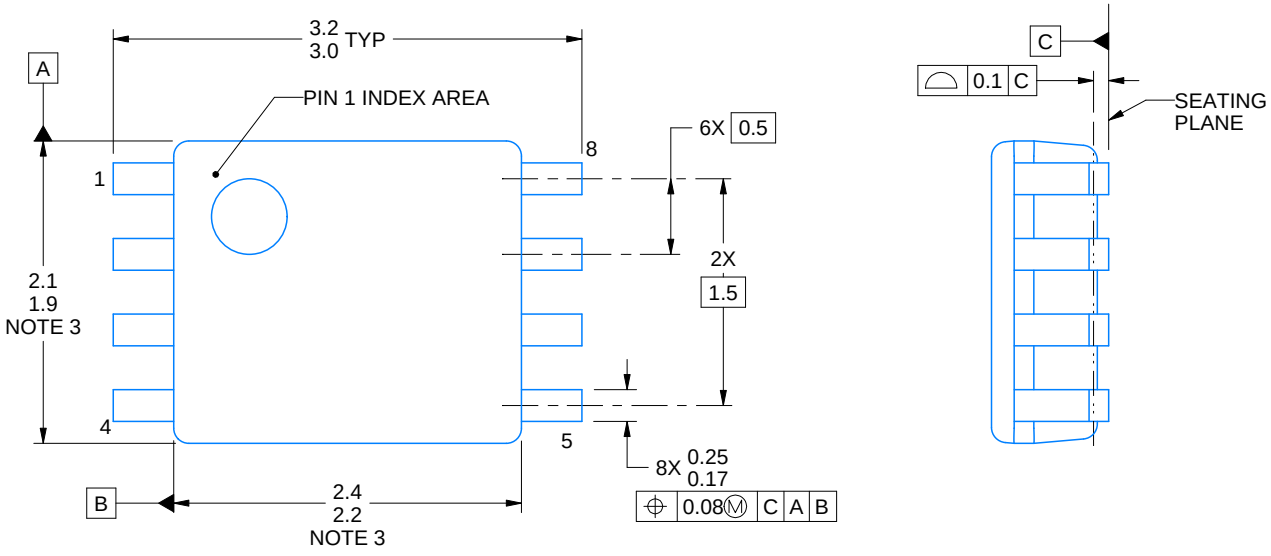
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G241DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AUC2G241DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G241DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G241YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

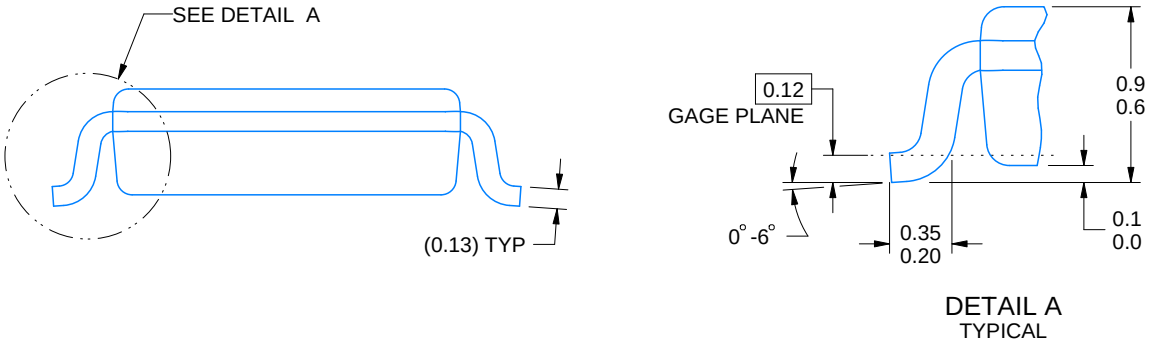
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

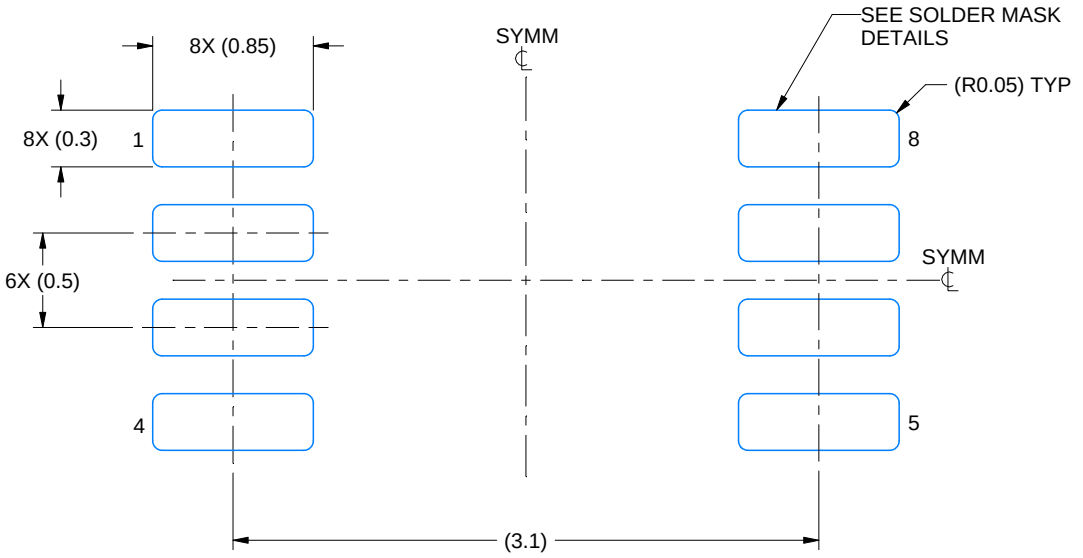




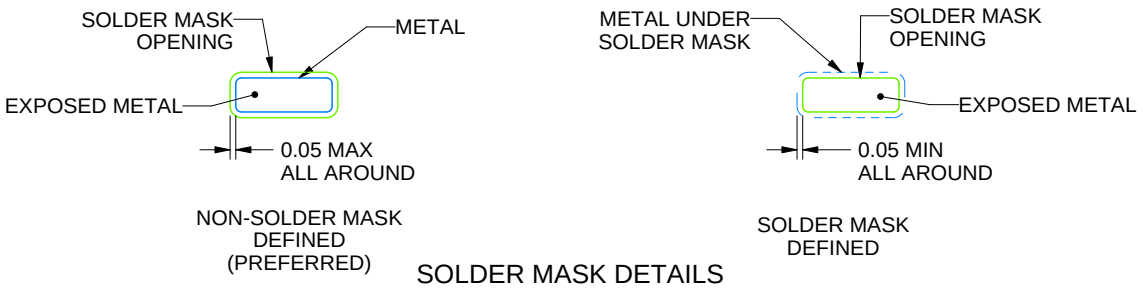
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

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NOTES: (continued)

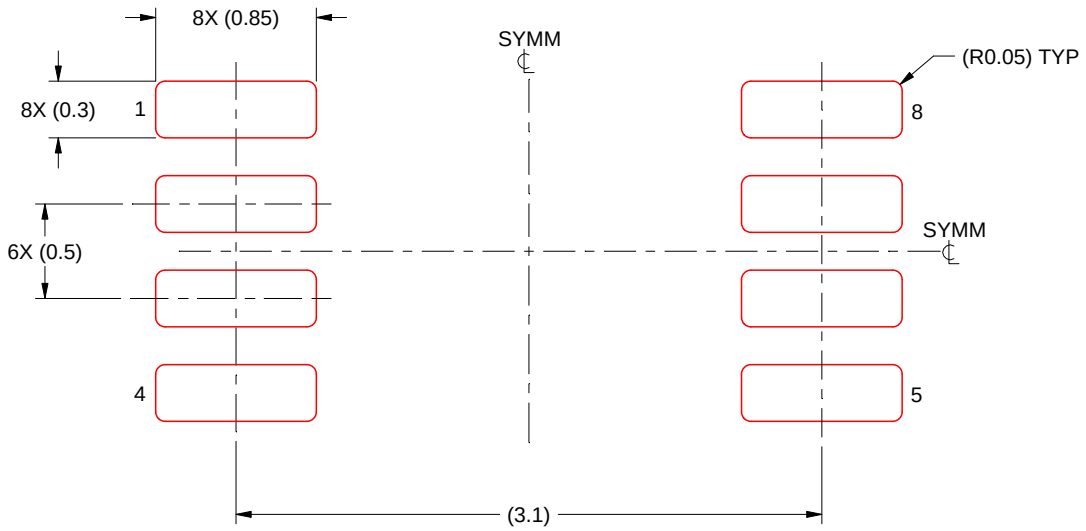
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

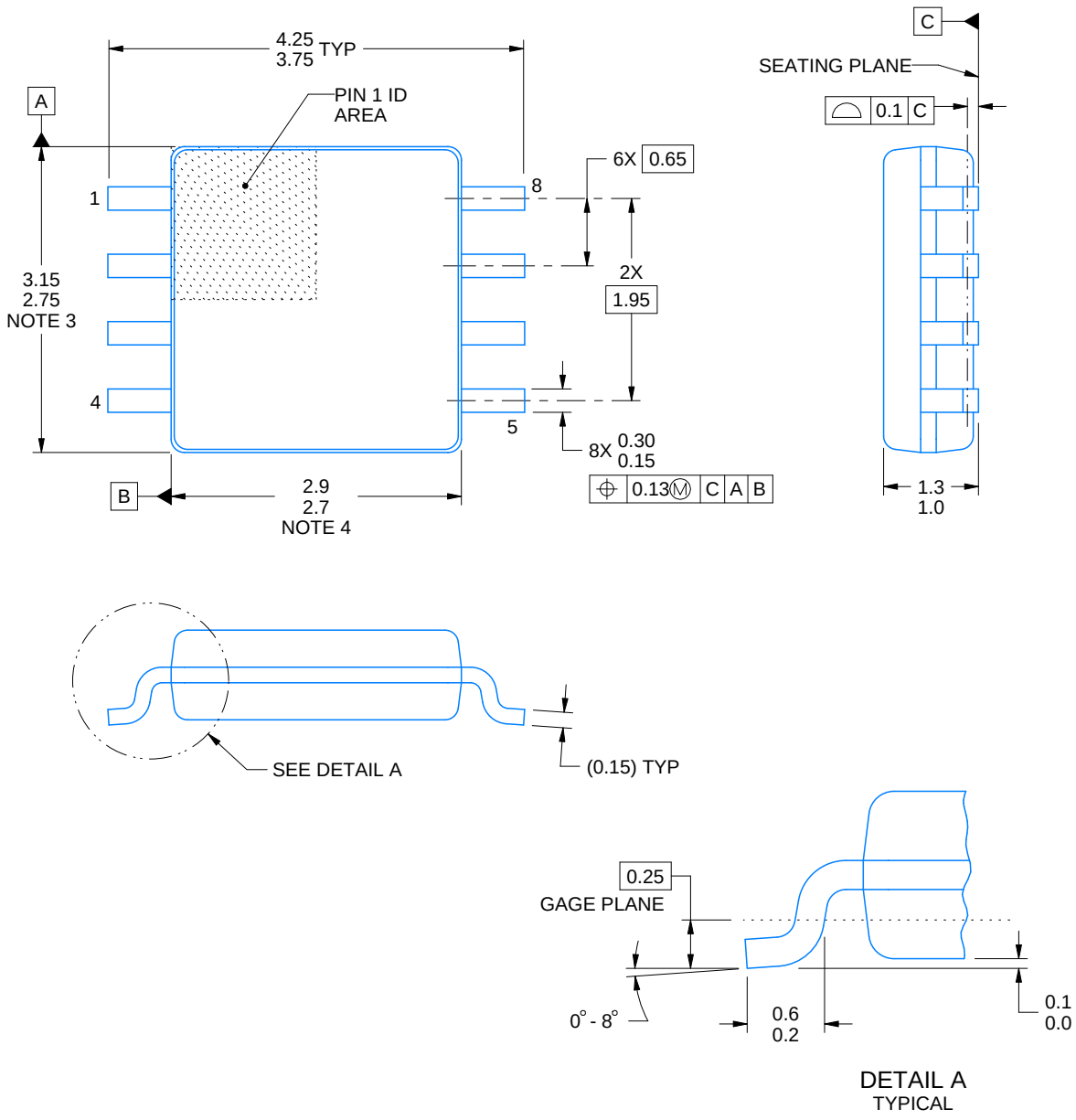
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

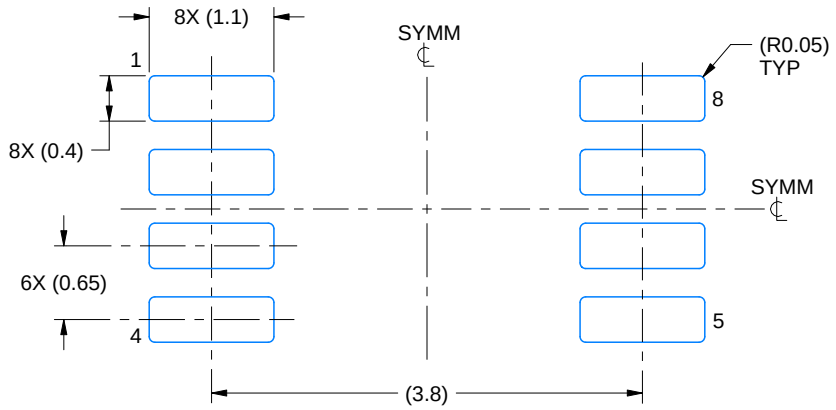
SMALL OUTLINE PACKAGE



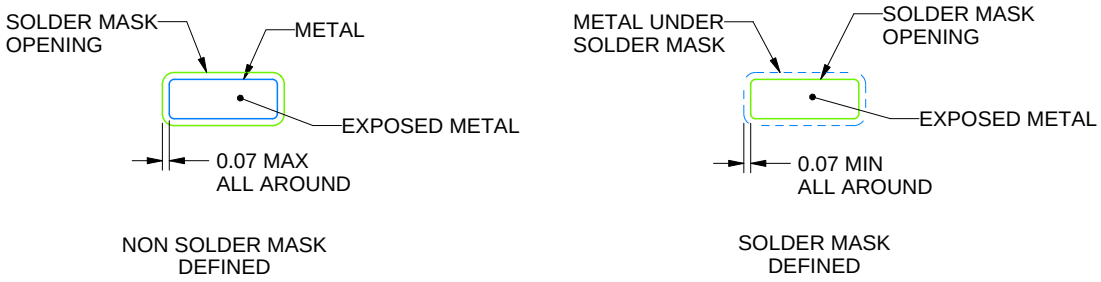
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

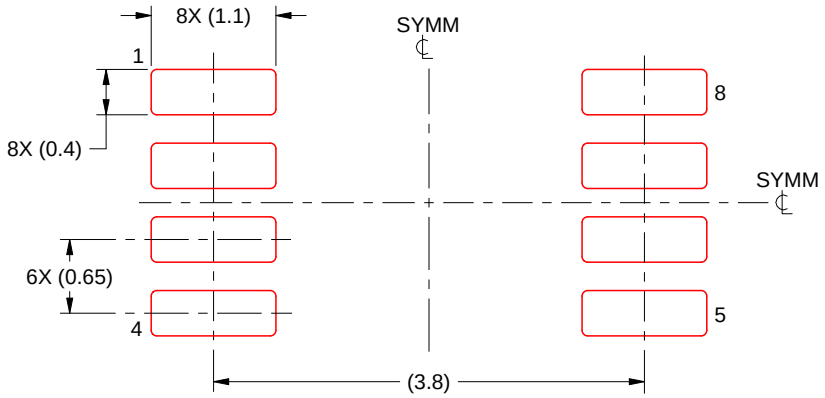


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

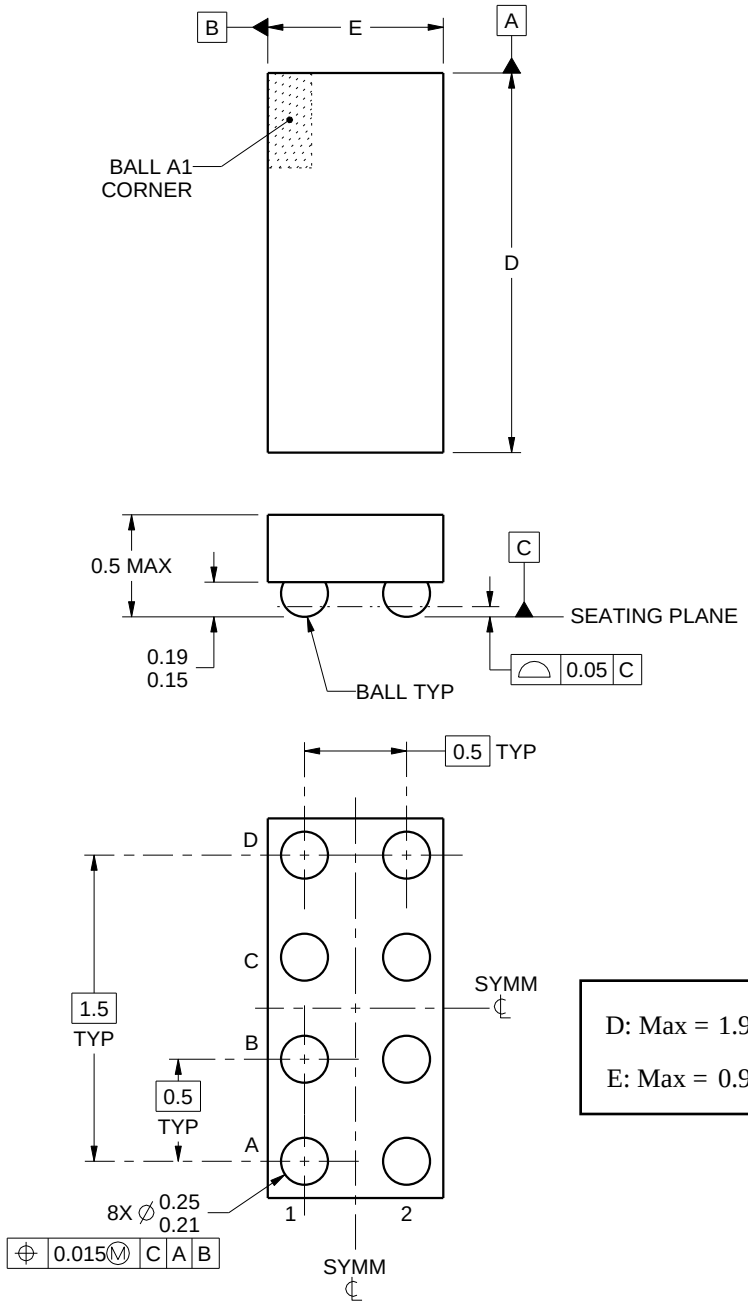


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

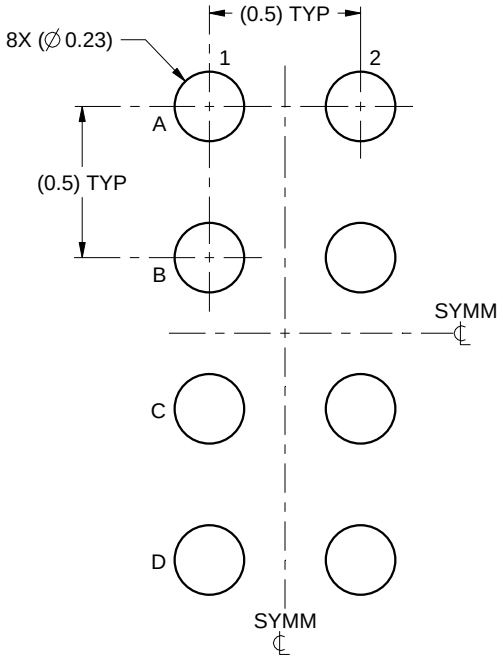
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

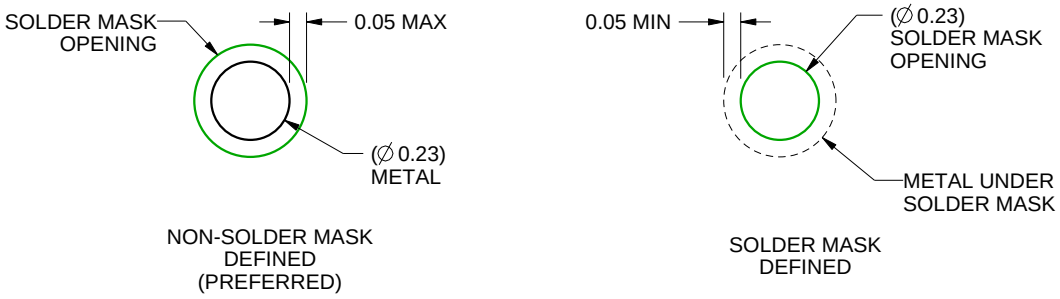


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

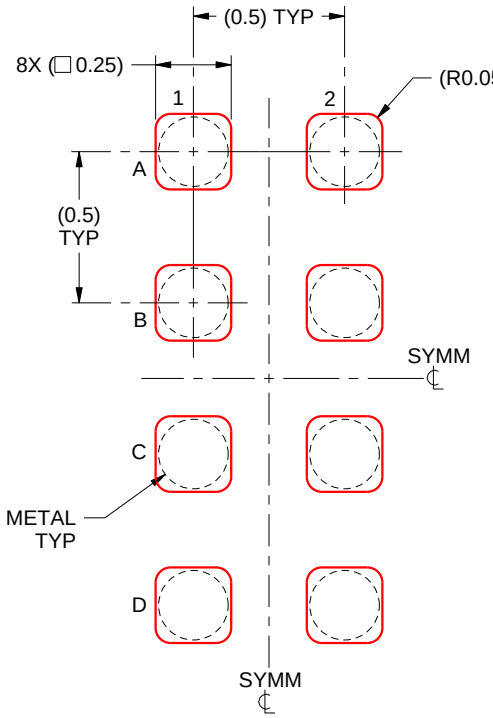


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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