

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## DESCRIPTION/ORDERING INFORMATION

This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH162374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

The output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

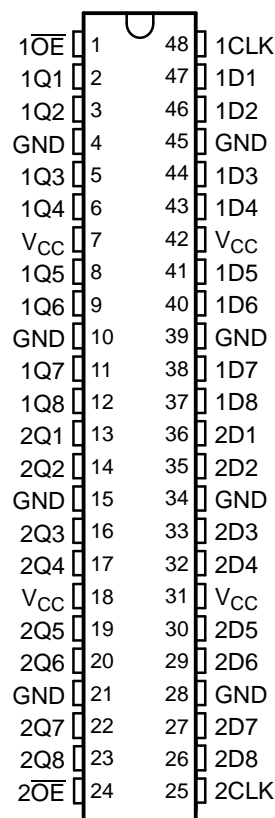
The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

## ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SSOP - DL              | Tube          | SN74ALVCH162374DL     | ALVCH162374      |
|               |                        | Tape and reel | SN74ALVCH162374DLR    |                  |
|               | TSSOP - DGG            | Tape and reel | SN74ALVCH162374GR     | ALVCH162374      |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

DGG OR DL PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN74ALVCH162374**  
**16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCES092F–JANUARY 1997–REVISED OCTOBER 2004

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**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

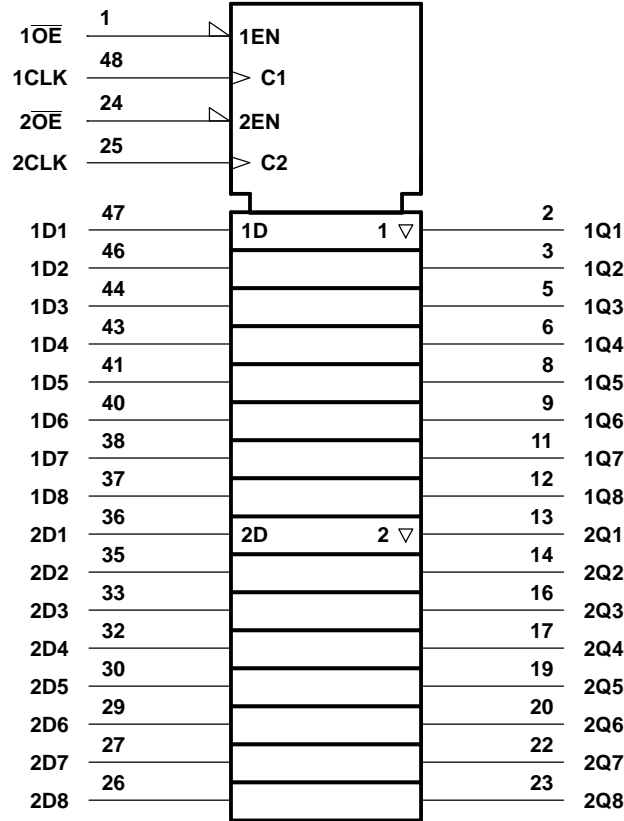
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**FUNCTION TABLE**  
**(each flip-flop)**

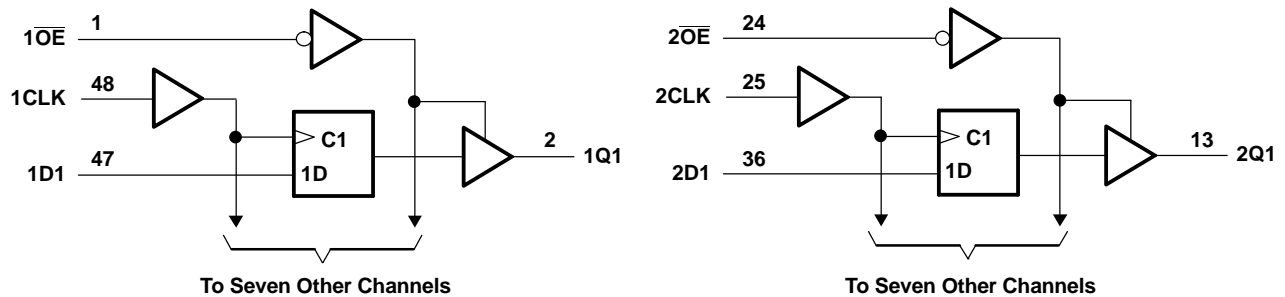
| INPUTS          |        |   | OUTPUT |
|-----------------|--------|---|--------|
| $\overline{OE}$ | CLK    | D | Q      |
| L               | ↑      | H | H      |
| L               | ↑      | L | L      |
| L               | H or L | X | $Q_0$  |
| H               | X      | X | Z      |

**LOGIC SYMBOL<sup>(1)</sup>**



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



# SN74ALVCH162374

## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |  | MIN                | MAX                   | UNIT    |
|------------------|--|--------------------|-----------------------|---------|
| V <sub>CC</sub>  | Supply voltage range                                   | -0.5               | 4.6                   | V       |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                     | -0.5               | 4.6                   | V       |
| V <sub>O</sub>   | Output voltage range <sup>(2)(3)</sup>                 | -0.5               | V <sub>CC</sub> + 0.5 | V       |
| I <sub>IK</sub>  | Input clamp current                                    | V <sub>I</sub> < 0 |                       | -50 mA  |
| I <sub>OK</sub>  | Output clamp current                                   | V <sub>O</sub> < 0 |                       | -50 mA  |
| I <sub>O</sub>   | Continuous output current                              |                    | ±50                   | mA      |
|                  | Continuous current through each V <sub>CC</sub> or GND |                    | ±100                  | mA      |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(4)</sup>               | DGG package        |                       | 89 °C/W |
|                  |  | DL package         |                       | 94 °C/W |
| T <sub>stg</sub> | Storage temperature range                              | -65                | 150                   | °C      |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

|                 |                                    | MIN                                | MAX                    | UNIT |
|-----------------|------------------------------------|------------------------------------|------------------------|------|
| V <sub>CC</sub> | Supply voltage                     | 1.65                               | 3.6                    | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2                      |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.35 × V <sub>CC</sub> | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 0.7                    |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 0.8                    |      |
| V <sub>I</sub>  | Input voltage                      | 0                                  | V <sub>CC</sub>        | V    |
| V <sub>O</sub>  | Output voltage                     | 0                                  | V <sub>CC</sub>        | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V           | -2                     | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | -6                     |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | -8                     |      |
|                 |                                    | V <sub>CC</sub> = 3 V              | -12                    |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V           | 2                      | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | 6                      |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | 8                      |      |
|                 |                                    | V <sub>CC</sub> = 3 V              | 12                     |      |
| Δt/Δv           | Input transition rise or fall rate |                                    | 10                     | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     | -40                                | 85                     | °C   |

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                          | TEST CONDITIONS  | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX  | UNIT |
|----------------------|--------------------------|--|-----------------|-----------------------|--------------------|------|------|
| V <sub>OH</sub>      |                          | I <sub>OH</sub> = -100 μA  | 1.65 V to 3.6 V | V <sub>CC</sub> - 0.2 |                    |      | V    |
|                      |                          | I <sub>OH</sub> = -2 mA  | 1.65 V          | 1.2                   |                    |      |      |
|                      |                          | I <sub>OH</sub> = -4 mA  | 2.3 V           | 1.9                   |                    |      |      |
|                      |                          | I <sub>OH</sub> = -6 mA  | 2.3 V           | 1.7                   |                    |      |      |
|                      |                          |  | 3 V             | 2.4                   |                    |      |      |
|                      |                          | I <sub>OH</sub> = -8 mA  | 2.7 V           | 2                     |                    |      |      |
|                      | I <sub>OH</sub> = -12 mA | 3 V  | 2               |                       |                    |      |      |
| V <sub>OL</sub>      |                          | I <sub>OL</sub> = 100 μA   | 1.65 V to 3.6 V |                       |                    | 0.2  | V    |
|                      |                          | I <sub>OL</sub> = 2 mA   | 1.65 V          |                       |                    | 0.45 |      |
|                      |                          | I <sub>OL</sub> = 4 mA   | 2.3 V           |                       |                    | 0.4  |      |
|                      |                          | I <sub>OL</sub> = 6 mA   | 2.3 V           |                       |                    | 0.55 |      |
|                      |                          |  | 3 V             |                       |                    | 0.55 |      |
|                      |                          | I <sub>OL</sub> = 8 mA   | 2.7 V           |                       |                    | 0.6  |      |
|                      | I <sub>OL</sub> = 12 mA  | 3 V  |                 |                       | 0.8                |      |      |
| I <sub>I</sub>       |                          | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           |                       |                    | ±5   | μA   |
| I <sub>I(hold)</sub> |                          | V <sub>I</sub> = 0.58 V  | 1.65 V          | 25                    |                    |      | μA   |
|                      |                          | V <sub>I</sub> = 1.07 V  | 1.65 V          | -25                   |                    |      |      |
|                      |                          | V <sub>I</sub> = 0.7 V   | 2.3 V           | 45                    |                    |      |      |
|                      |                          | V <sub>I</sub> = 1.7 V   | 2.3 V           | -45                   |                    |      |      |
|                      |                          | V <sub>I</sub> = 0.8 V   | 3 V             | 75                    |                    |      |      |
|                      |                          | V <sub>I</sub> = 2 V   | 3 V             | -75                   |                    |      |      |
|                      |                          | V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>                                   | 3.6 V           |                       |                    | ±500 |      |
| I <sub>OZ</sub>      |                          | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           |                       |                    | ±10  | μA   |
| I <sub>CC</sub>      |                          | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           |                       |                    | 40   | μA   |
| ΔI <sub>CC</sub>     |                          | One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 3.6 V    |                       |                    | 750  | μA   |
| C <sub>i</sub>       | Control inputs           | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           |                       |                    | 3    | pF   |
|                      | Data inputs              |  |                 |                       |                    | 6    |      |
| C <sub>o</sub>       | Outputs                  | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           |                       |                    | 7    | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

|                    |                                 | V <sub>CC</sub> = 1.8 V |     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | UNIT |
|--------------------|---------------------------------|-------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
|                    |                                 | MIN                     | MAX | MIN                                | MAX | MIN                     | MAX | MIN                                | MAX |      |
| f <sub>clock</sub> | Clock frequency                 | (1)                     |     | 150                                |     | 150                     |     | 150                                |     | MHz  |
| t <sub>w</sub>     | Pulse duration, CLK high or low | (1)                     |     | 3.3                                |     | 3.3                     |     | 3.3                                |     | ns   |
| t <sub>su</sub>    | Setup time, data before CLK↑    | (1)                     |     | 2.1                                |     | 2.2                     |     | 1.9                                |     | ns   |
| t <sub>h</sub>     | Hold time, data after CLK↑      | (1)                     |     | 0.6                                |     | 0.5                     |     | 0.5                                |     | ns   |

(1) This information was not available at the time of publication.

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**SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)           | TO (OUTPUT) | V <sub>CC</sub> = 1.8 V |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |     | UNIT |
|------------------|------------------------|-------------|-------------------------|-----|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
|                  |                        |             | MIN                     | TYP | MIN                             | MAX | MIN                     | MAX | MIN                             | MAX |      |
| f <sub>max</sub> |                        |             | (1)                     |     | 150                             |     | 150                     |     | 150                             |     | MHz  |
| t <sub>pd</sub>  | CLK                    | Q           |                         | (1) | 1                               | 5.4 |                         | 5.4 | 1                               | 4.6 | ns   |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | Q           |                         | (1) | 1                               | 6.5 |                         | 6.4 | 1                               | 5.2 | ns   |
| t <sub>dis</sub> | $\overline{\text{OE}}$ | Q           |                         | (1) | 1                               | 5.6 |                         | 5   | 1.2                             | 4.5 | ns   |

(1) This information was not available at the time of publication.

**OPERATING CHARACTERISTICS**

T<sub>A</sub> = 25°C

| PARAMETER                                     |                  | TEST CONDITIONS                | V <sub>CC</sub> = 1.8 V | V <sub>CC</sub> = 2.5 V | V <sub>CC</sub> = 3.3 V | UNIT |
|---|------------------|--------------------------------|-------------------------|-------------------------|-------------------------|------|
|   |                  |                                | TYP                     | TYP                     | TYP                     |      |
| C <sub>pd</sub> Power dissipation capacitance | Outputs enabled  | C <sub>L</sub> = 0, f = 10 MHz | (1)                     | 28                      | 31                      | pF   |
|   | Outputs disabled |                                | (1)                     | 10                      | 11                      |      |

(1) This information was not available at the time of publication.

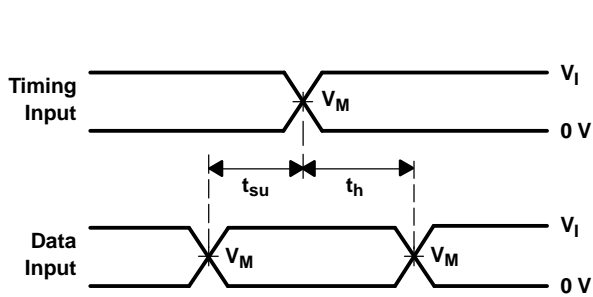
PARAMETER MEASUREMENT INFORMATION



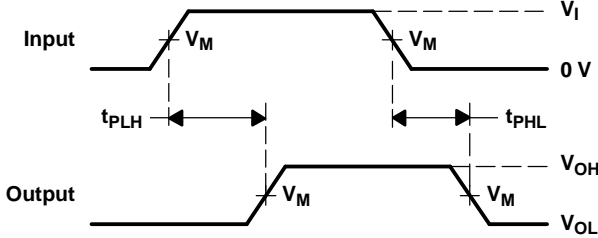
LOAD CIRCUIT

| TEST   | S1                        |
|--|---------------------------|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>$V_{LOAD}$<br>GND |

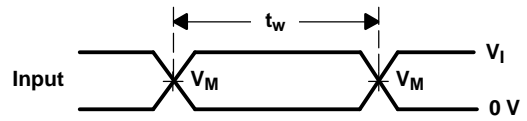
| $V_{CC}$                         | INPUT    |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



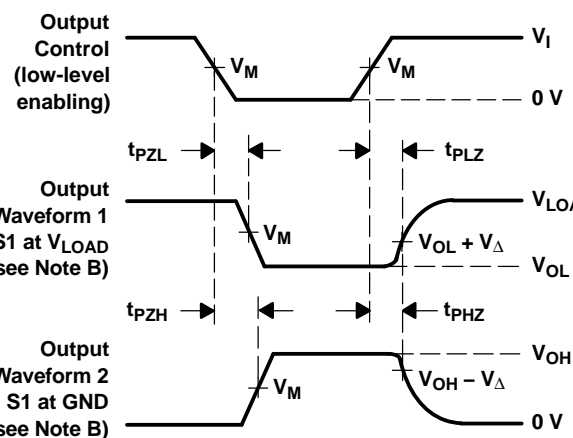
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74ALVCH162374DL</a>  | Active        | Production           | SSOP (DL)   48   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH162374         |
| SN74ALVCH162374DL.B                | Active        | Production           | SSOP (DL)   48   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH162374         |
| <a href="#">SN74ALVCH162374DLR</a> | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH162374         |
| SN74ALVCH162374DLR.B               | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH162374         |
| <a href="#">SN74ALVCH162374GR</a>  | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH162374         |
| SN74ALVCH162374GR.B                | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH162374         |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVCH162374DLR | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |
| SN74ALVCH162374GR  | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVCH162374DLR | SSOP         | DL              | 48   | 1000 | 367.0       | 367.0      | 55.0        |
| SN74ALVCH162374GR  | TSSOP        | DGG             | 48   | 2000 | 367.0       | 367.0      | 45.0        |

**TUBE**


\*All dimensions are nominal

| Device              | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ALVCH162374DL   | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |
| SN74ALVCH162374DL.B | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |



# EXAMPLE BOARD LAYOUT

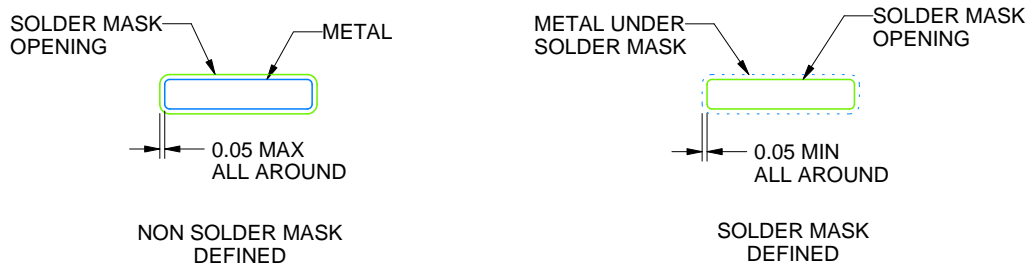
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

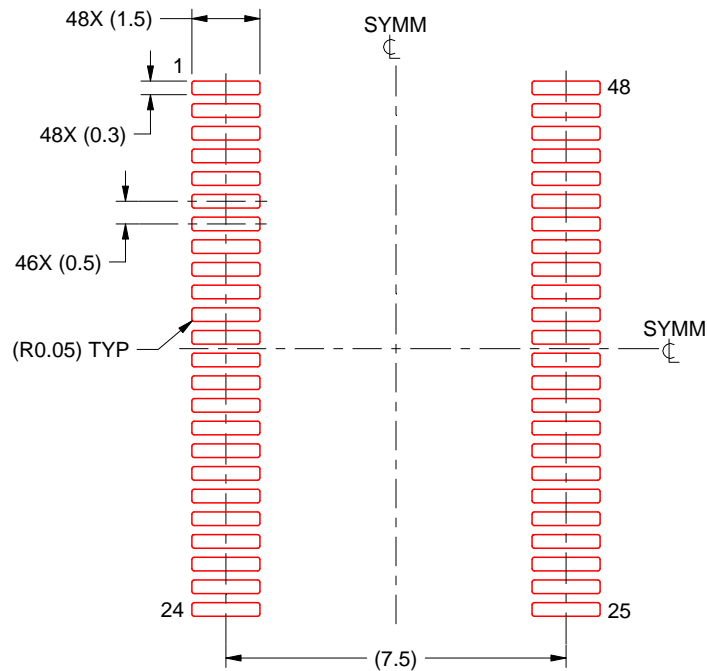
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

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