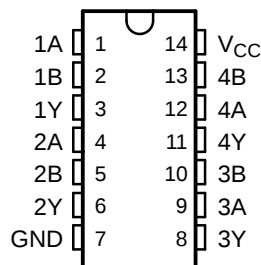


## FEATURES

- Operates From 1.65 V to 3.6 V
- Max  $t_{pd}$  of 2.8 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

D, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

This quadruple 2-input positive-OR gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVC32 performs the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = A + B$  in positive logic.

## ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SOIC - D               | Tube          | SN74ALVC32D           | ALVC32           |
|               |                        | Tape and reel | SN74ALVC32DR          |                  |
|               | SOP - NS               | Tape and reel | SN74ALVC32NSR         | ALVC32           |
|               | TSSOP - PW             | Tube          | SN74ALVC32PW          | VA32             |
|               |                        | Tape and reel | SN74ALVC32PWR         |                  |
|               | TVSOP - DGV            | Tape and reel | SN74ALVC32DGVR        | VA32             |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**  
(each gate)

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| H      | X | H      |
| X      | H | H      |
| L      | L | L      |

**LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74ALVC32

## QUADRUPLE 2-INPUT POSITIVE-OR GATE

SCES108G–JULY 1997–REVISED NOVEMBER 2004

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |                                            | MIN         | MAX            | UNIT   |
|---------------|--------------------------------------------|-------------|----------------|--------|
| $V_{CC}$      | Supply voltage range                       | -0.5        | 4.6            | V      |
| $V_I$         | Input voltage range <sup>(2)</sup>         | -0.5        | 4.6            | V      |
| $V_O$         | Output voltage range <sup>(2)(3)</sup>     | -0.5        | $V_{CC} + 0.5$ | V      |
| $I_{IK}$      | Input clamp current                        | $V_I < 0$   |                | -50 mA |
| $I_{OK}$      | Output clamp current                       | $V_O < 0$   |                | -50 mA |
| $I_O$         | Continuous output current                  |             | ±50            | mA     |
|               | Continuous current through $V_{CC}$ or GND |             | ±100           | mA     |
| $\theta_{JA}$ | Package thermal impedance <sup>(4)</sup>   | D package   |                | 86     |
|               |                                            | DGV package |                | 127    |
|               |                                            | NS package  |                | 76     |
|               |                                            | PW package  |                | 113    |
| $T_{stg}$     | Storage temperature range                  | -65         | 150            | °C     |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

|                     |                                    | MIN                                          | MAX                  | UNIT |
|---------------------|------------------------------------|----------------------------------------------|----------------------|------|
| $V_{CC}$            | Supply voltage                     | 1.65                                         | 3.6                  | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.65 \times V_{CC}$ | V    |
|                     |                                    | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$   | 1.7                  |      |
|                     |                                    | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$   | 2                    |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.35 \times V_{CC}$ | V    |
|                     |                                    | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$   | 0.7                  |      |
|                     |                                    | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$   | 0.8                  |      |
| $V_I$               | Input voltage                      | 0                                            | 3.6                  | V    |
| $V_O$               | Output voltage                     | 0                                            | $V_{CC}$             | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 1.65 \text{ V}$                    | -4                   | mA   |
|                     |                                    | $V_{CC} = 2.3 \text{ V}$                     | -12                  |      |
|                     |                                    | $V_{CC} = 2.7 \text{ V}$                     | -12                  |      |
|                     |                                    | $V_{CC} = 3 \text{ V}$                       | -24                  |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 1.65 \text{ V}$                    | 4                    | mA   |
|                     |                                    | $V_{CC} = 2.3 \text{ V}$                     | 12                   |      |
|                     |                                    | $V_{CC} = 2.7 \text{ V}$                     | 12                   |      |
|                     |                                    | $V_{CC} = 3 \text{ V}$                       | 24                   |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |                                              | 5                    | ns/V |
| $T_A$               | Operating free-air temperature     | -40                                          | 85                   | °C   |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS                                                              | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX | UNIT |
|------------------|------------------------------------------------------------------------------|-----------------|-----------------------|--------------------|-----|------|
| V <sub>OH</sub>  | I <sub>OH</sub> = -100 μA                                                    | 1.65 V to 3.6 V | V <sub>CC</sub> - 0.2 |                    |     | V    |
|                  | I <sub>OH</sub> = -4 mA                                                      | 1.65 V          | 1.2                   |                    |     |      |
|                  | I <sub>OH</sub> = -6 mA                                                      | 2.3 V           | 2                     |                    |     |      |
|                  | I <sub>OH</sub> = -12 mA                                                     | 2.3 V           | 1.7                   |                    |     |      |
|                  |                                                                              | 2.7 V           | 2.2                   |                    |     |      |
|                  |                                                                              | 3 V             | 2.4                   |                    |     |      |
|                  | I <sub>OH</sub> = -24 mA                                                     | 3 V             | 2                     |                    |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA                                                     | 1.65 V to 3.6 V | 0.2                   |                    |     | V    |
|                  | I <sub>OL</sub> = 4 mA                                                       | 1.65 V          | 0.45                  |                    |     |      |
|                  | I <sub>OL</sub> = 6 mA                                                       | 2.3 V           | 0.4                   |                    |     |      |
|                  | I <sub>OL</sub> = 12 mA                                                      | 2.3 V           | 0.7                   |                    |     |      |
|                  |                                                                              | 2.7 V           | 0.4                   |                    |     |      |
|                  | I <sub>OL</sub> = 24 mA                                                      | 3 V             | 0.55                  |                    |     |      |
| I <sub>I</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           | ±5                    |                    |     | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           | 10                    |                    |     | μA   |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 3.6 V    | 750                   |                    |     | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 4                     |                    |     | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

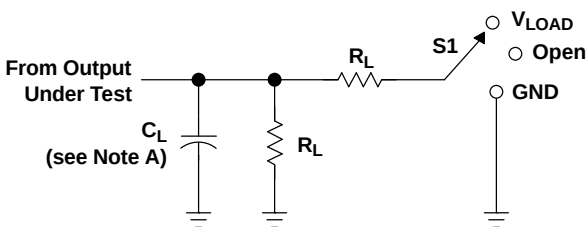
| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | UNIT |
|-----------------|-----------------|----------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
|                 |                 |                | MIN                                 | MAX | MIN                                | MAX | MIN                     | MAX | MIN                                | MAX |      |
| t <sub>pd</sub> | A or B          | Y              | 1                                   | 4.7 | 1                                  | 3.1 | 2.9                     |     | 1                                  | 2.8 | ns   |

## OPERATING CHARACTERISTICS

T<sub>A</sub> = 25°C

| PARAMETER                                              | TEST CONDITIONS                | V <sub>CC</sub> = 1.8 V<br>± 0.15 V | V <sub>CC</sub> = 2.5 V<br>± 0.2 V | V <sub>CC</sub> = 3.3 V<br>± 0.3 V | UNIT |
|--------------------------------------------------------|--------------------------------|-------------------------------------|------------------------------------|------------------------------------|------|
|                                                        |                                | TYP                                 | TYP                                | TYP                                |      |
| C <sub>pd</sub> Power dissipation capacitance per gate | C <sub>L</sub> = 0, f = 10 MHz | 23                                  | 24                                 | 26                                 | pF   |

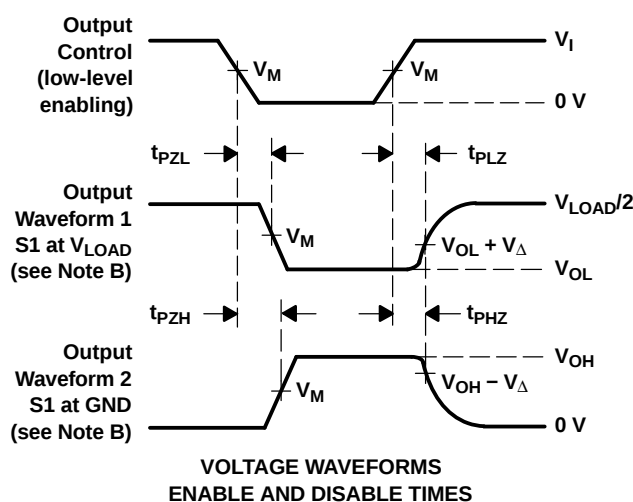
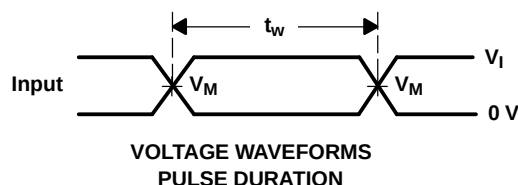
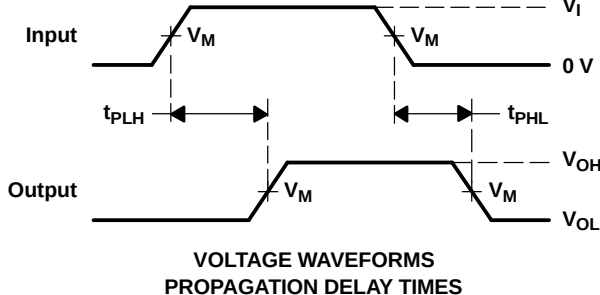
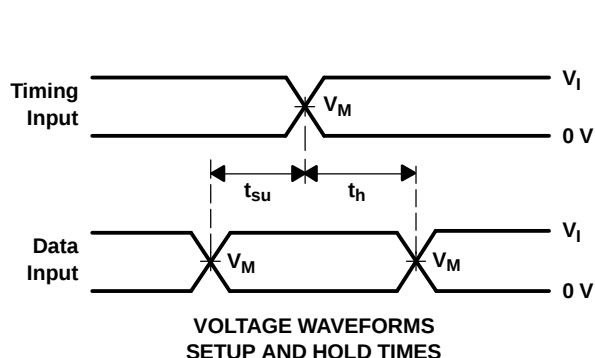
## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{pd}$          | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PHZ}$ | GND        |

| $V_{CC}$                         | INPUT    |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74ALVC32D</a>    | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVC32              |
| SN74ALVC32D.B                  | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVC32              |
| <a href="#">SN74ALVC32DGVR</a> | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| SN74ALVC32DGVR.B               | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| SN74ALVC32DGVRG4               | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| SN74ALVC32DGVRG4.B             | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| <a href="#">SN74ALVC32DR</a>   | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVC32              |
| SN74ALVC32DR.B                 | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVC32              |
| <a href="#">SN74ALVC32NSR</a>  | Active        | Production           | SOP (NS)   14    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVC32              |
| SN74ALVC32NSR.B                | Active        | Production           | SOP (NS)   14    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVC32              |
| <a href="#">SN74ALVC32PW</a>   | Active        | Production           | TSSOP (PW)   14  | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| SN74ALVC32PW.B                 | Active        | Production           | TSSOP (PW)   14  | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| SN74ALVC32PWE4                 | Active        | Production           | TSSOP (PW)   14  | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| <a href="#">SN74ALVC32PWR</a>  | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| SN74ALVC32PWR.B                | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| SN74ALVC32PWR1G4               | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |
| SN74ALVC32PWR1G4.B             | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VA32                |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVC32DGVR   | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74ALVC32DGVRG4 | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74ALVC32DR     | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74ALVC32NSR    | SOP          | NS              | 14   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ALVC32PWR    | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74ALVC32PWR1G4 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVC32DGVR   | TVSOP        | DGV             | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ALVC32DGVRG4 | TVSOP        | DGV             | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ALVC32DR     | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74ALVC32NSR    | SOP          | NS              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ALVC32PWR    | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ALVC32PWR1G4 | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |

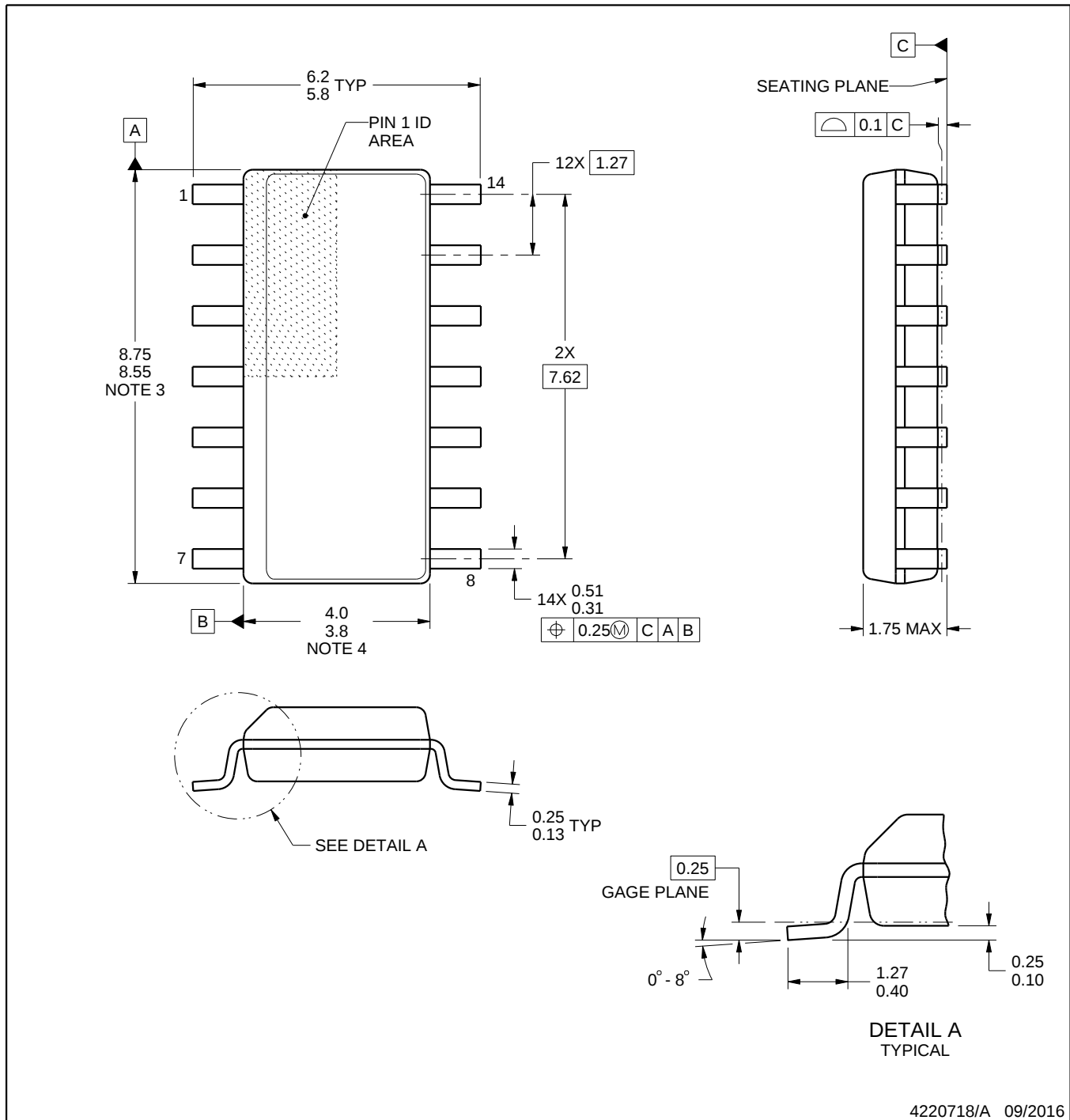
**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ALVC32D    | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74ALVC32D.B  | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74ALVC32PW   | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74ALVC32PW.B | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74ALVC32PWE4 | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

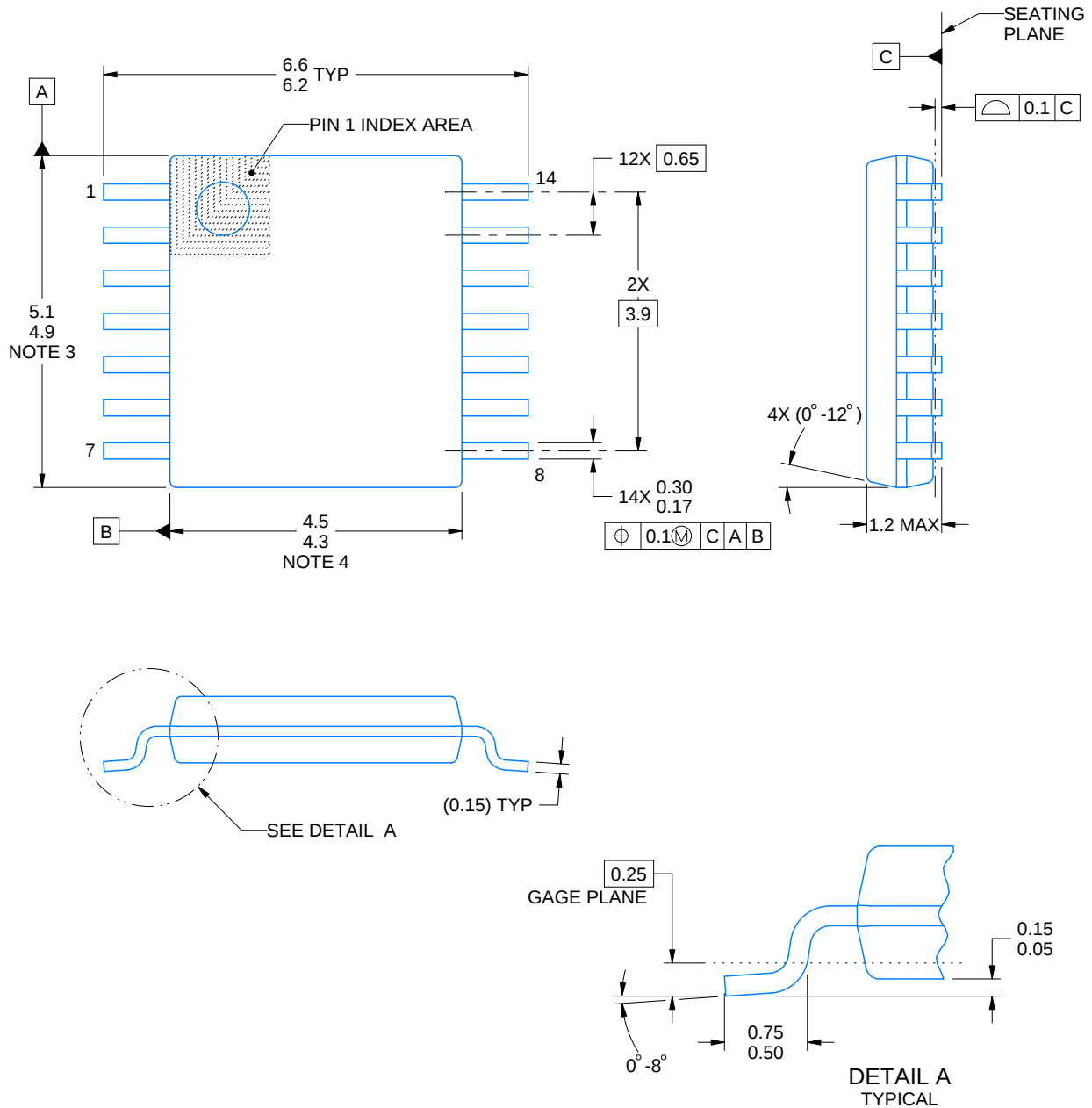
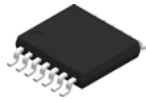
## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



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## NOTES:

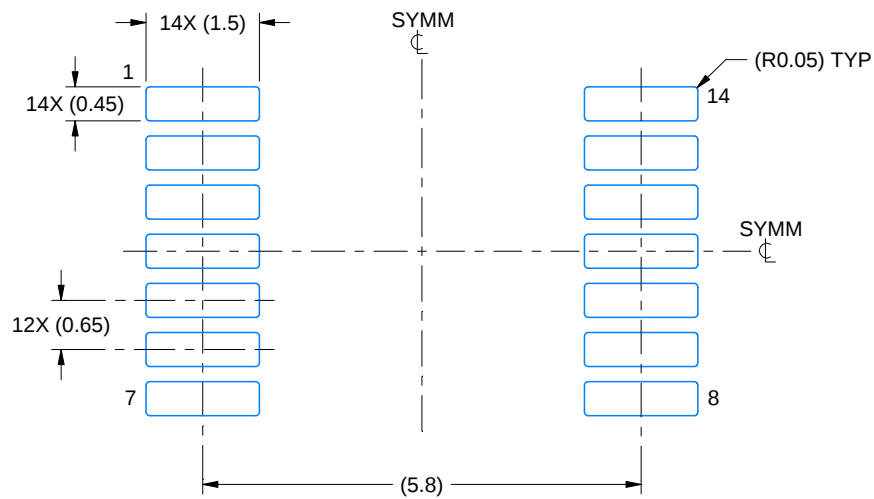
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

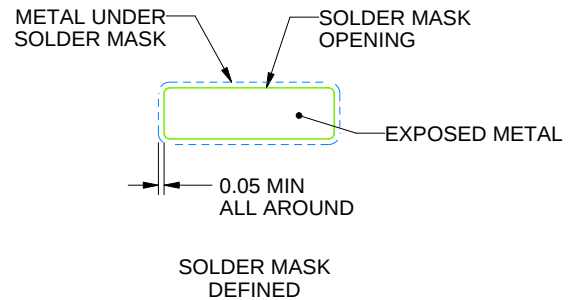
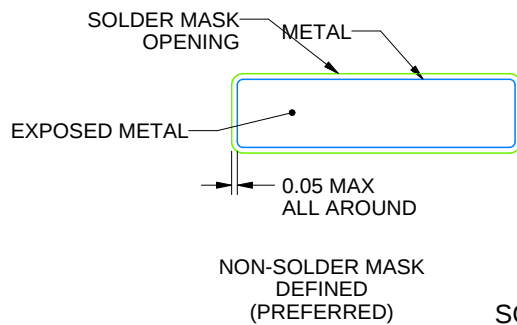
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

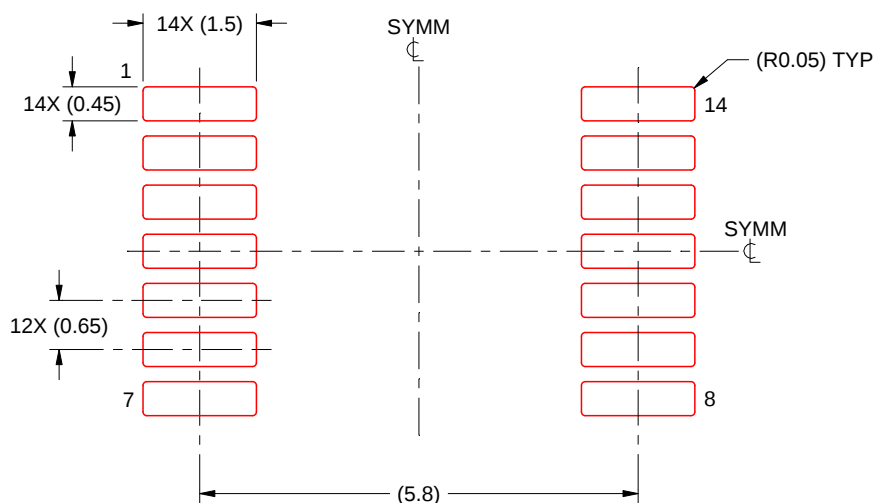
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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