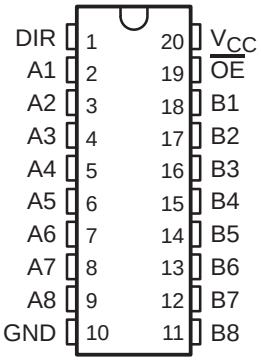
SDAS123A – DECEMBER 1983 – REVISED JANUARY 1995

- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Choice of True or Inverting Logic**
- **A-Bus Outputs Are Open Collector; B-Bus Outputs Are 3 State**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



DEVICE	A OUTPUT	B OUTPUT	LOGIC
SN74ALS638A, SN74AS638A	Open collector	3 state	Inverting
SN74ALS639A, SN74AS639	Open collector	3 state	True

description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3 state) or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are isolated.

The -1 version of SN74ALS638A is identical to the standard version, except that the recommended maximum I_{OL} is increased to 48 mA.

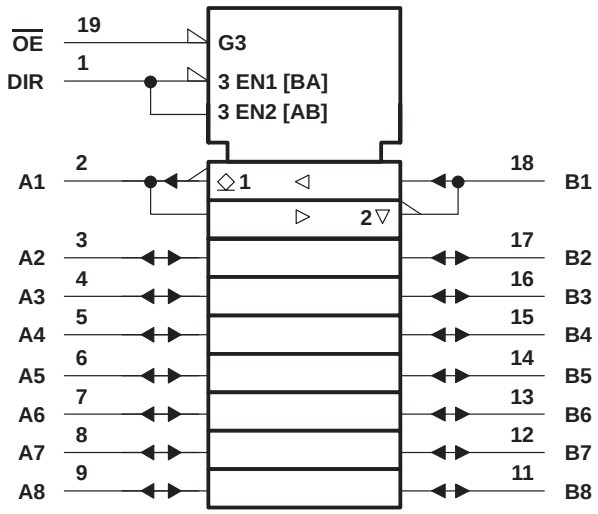
The SN74ALS638A, SN74ALS639A, SN74AS638A, and SN74AS639 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

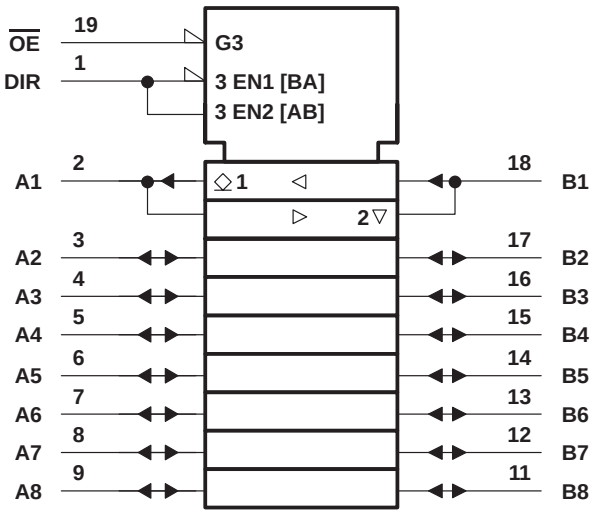
INPUTS		OPERATION	
$\overline{OE}$	DIR	SN74ALS638A SN74AS638A	SN74ALS639A SN74AS639
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

logic symbols†

SN74ALS638A, SN74AS638A



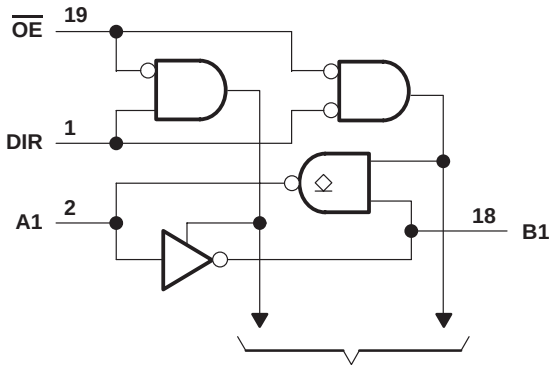
SN74ALS639A, SN74AS639



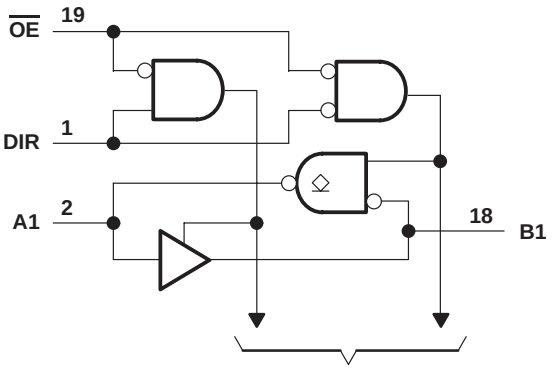
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN74ALS638A, SN74AS638A



SN74ALS639A, SN74AS639



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I: All inputs . . . . . 7 V
A-bus I/O ports . . . . . 7 V
B-bus I/O ports . . . . . 5.5 V
Operating free-air temperature range, T_A: SN74ALS638A, SN74ALS639A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74ALS638A SN74ALS639A			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	A ports			5.5	V
I_{OH}	High-level output current	B ports			–15	mA
I_{OL}	Low-level output current	A or B ports			24	mA
					48†	
T_A	Operating free-air temperature		0		70	°C

† Applies only to the SN74ALS638A-1 version and only if V_{CC} is between 4.75 V and 5.25 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS638A SN74ALS639A			UNIT
				MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} –2			V
		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.2		
			I_{OH} = –15 mA	2			
V_{OL}	A or B ports	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
			I_{OL} = 48 mA†		0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1	mA
	A or B ports		V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports§					20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1	mA
	A or B ports§					–0.1	
I_O¶	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	SN74ALS638A	V_{CC} = 5.5 V	Outputs high		18	30	mA
			Outputs low		26	41	
			Outputs disabled		16	30	
	SN74ALS639A	V_{CC} = 5.5 V	Outputs high		25	40	
			Outputs low		30	50	
			Outputs disabled		33	54	

† Applies only to the SN74ALS638A-1 version and only if V_{CC} is between 4.75 V and 5.25 V
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX†				UNIT
			SN74ALS638A		SN74ALS639A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	12	2	12	ns
t_{PHL}			2	12	2	12	
t_{PLH}	B	A	8	25	10	30	ns
t_{PHL}			8	30	5	22	
t_{PLH}	$\overline{OE}$	A	5	25	10	30	ns
t_{PHL}			10	45	10	35	
t_{PZH}	$\overline{OE}$	B	5	20	6	21	ns
t_{PZL}			5	22	8	25	
t_{PHZ}	$\overline{OE}$	B	2	10	2	10	ns
t_{PLZ}			3	15	3	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I: All inputs . . . . . 7 V
A-bus I/O ports . . . . . 7 V
B-bus I/O ports . . . . . 5.5 V
Operating free-air temperature range, T_A: SN74AS638A, SN74AS639 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74AS638A SN74AS639			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	A ports			5.5	V
I_{OH}	High-level output current	B ports			–15	mA
I_{OL}	Low-level output current	A or B ports			64	mA
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS638A SN74AS639			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} –2			V
		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.2		
			I_{OH} = –15 mA	2.4			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 64 mA		0.35	0.55	V
I_I	Control inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1	mA
	A or B ports		V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports‡					70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5	mA
	A or B ports‡					–0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	–50		–150	mA
I_{CC}	SN74AS638A	V_{CC} = 5.5 V	Outputs high		24	54	mA
			Outputs low		75	122	
			Outputs disabled		37	61	
	SN74AS639	V_{CC} = 5.5 V	Outputs high		56	92	
			Outputs low		95	154	
			Outputs disabled		62	100	

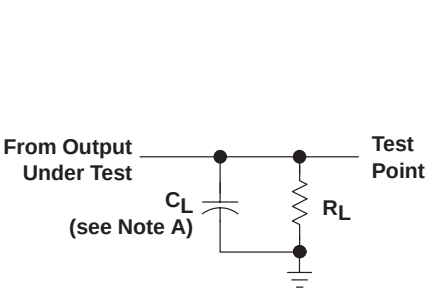
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

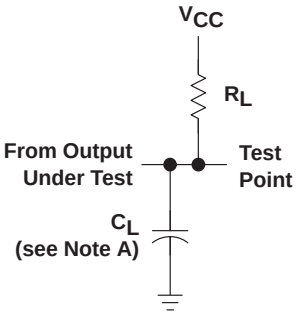
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX¶				UNIT
			SN74AS638A		SN74AS639		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	7	2	9.5	ns
t_{PHL}			2	6.5	2	9	
t_{PLH}	B	A	5	20	5	22	ns
t_{PHL}			2	7	2	9	
t_{PLH}	$\overline{OE}$	A	5	19	5	21.5	ns
t_{PHL}			2	9	2	11.5	
t_{PZH}	$\overline{OE}$	B	2	8	2	10.5	ns
t_{PZL}			2	10	2	10.5	
t_{PHZ}	$\overline{OE}$	B	2	7	2	7	ns
t_{PLZ}			2	10	2	10.5	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

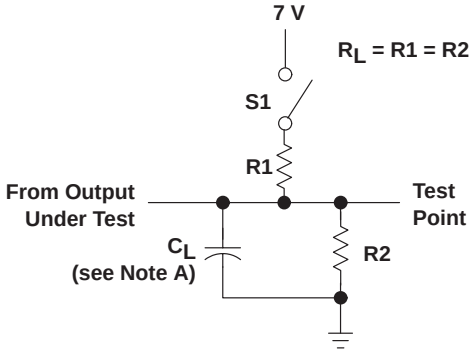
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



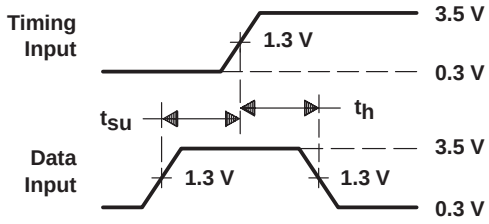
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



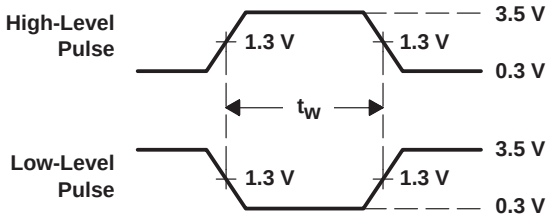
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



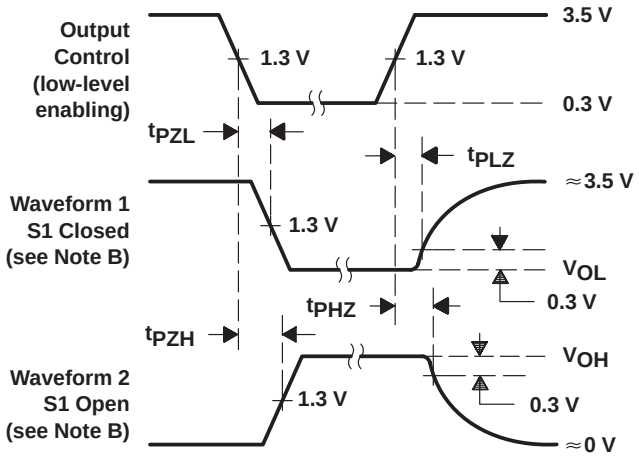
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



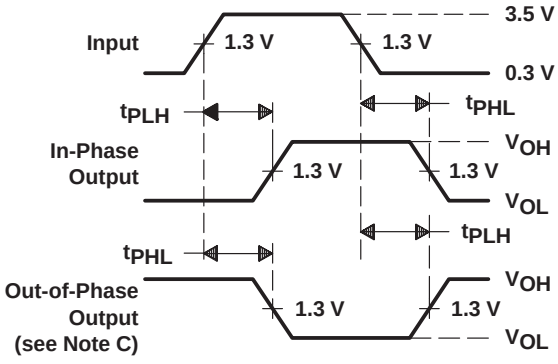
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS638AN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS638AN
SN74ALS638AN.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS638AN
SN74ALS639ADW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS639A
SN74ALS639ADW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS639A
SN74ALS639AN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS639AN
SN74ALS639AN.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS639AN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

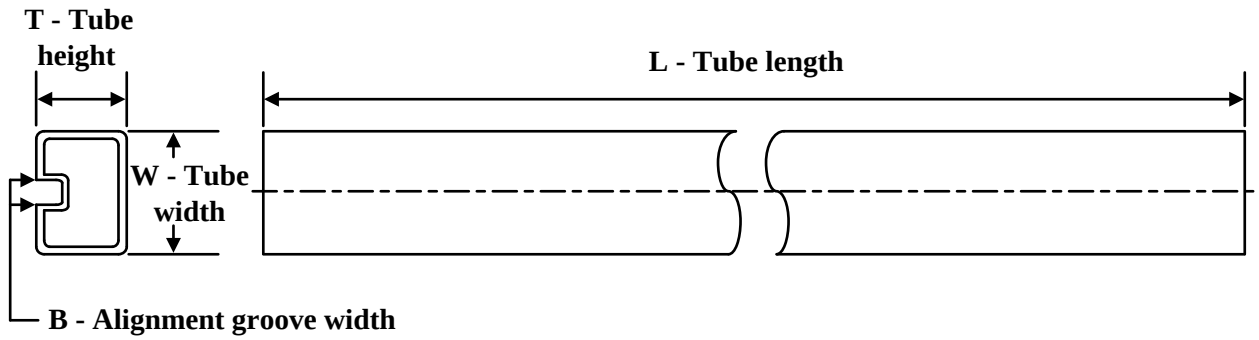
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



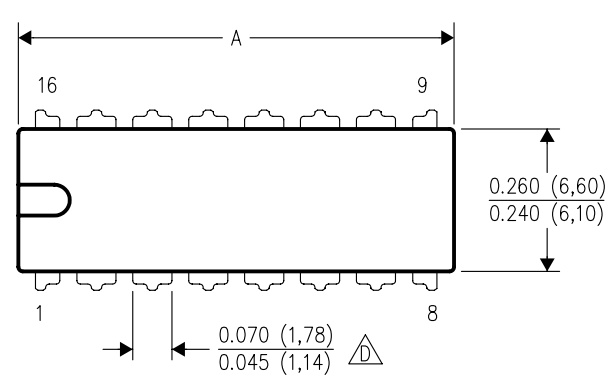
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALS638AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS638AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS639ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS639ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS639AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS639AN.A	N	PDIP	20	20	506	13.97	11230	4.32

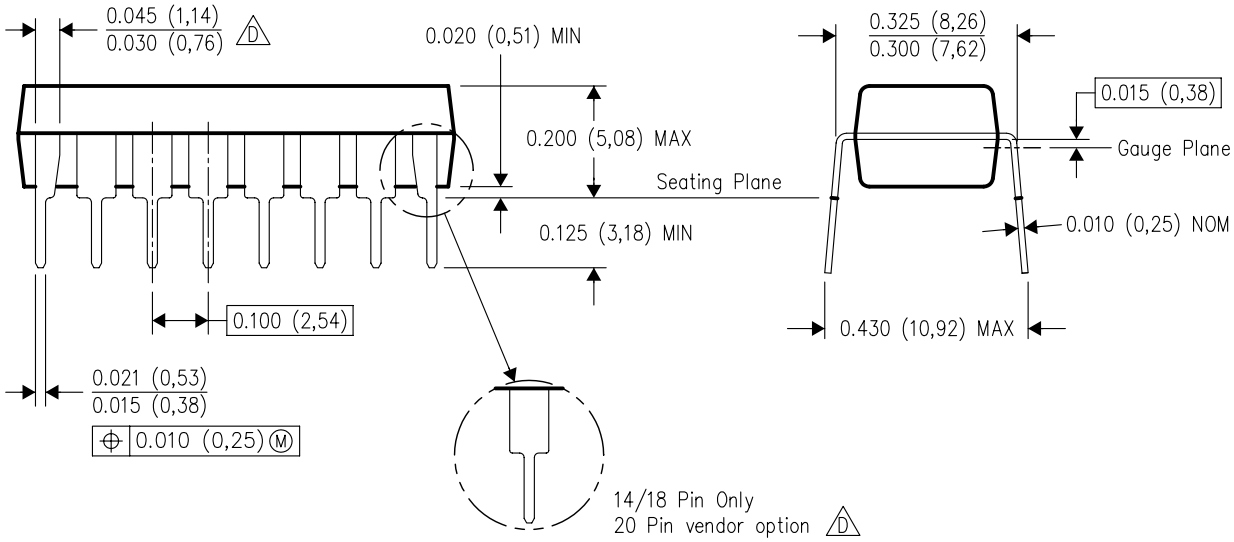
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

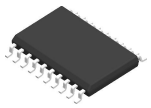


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

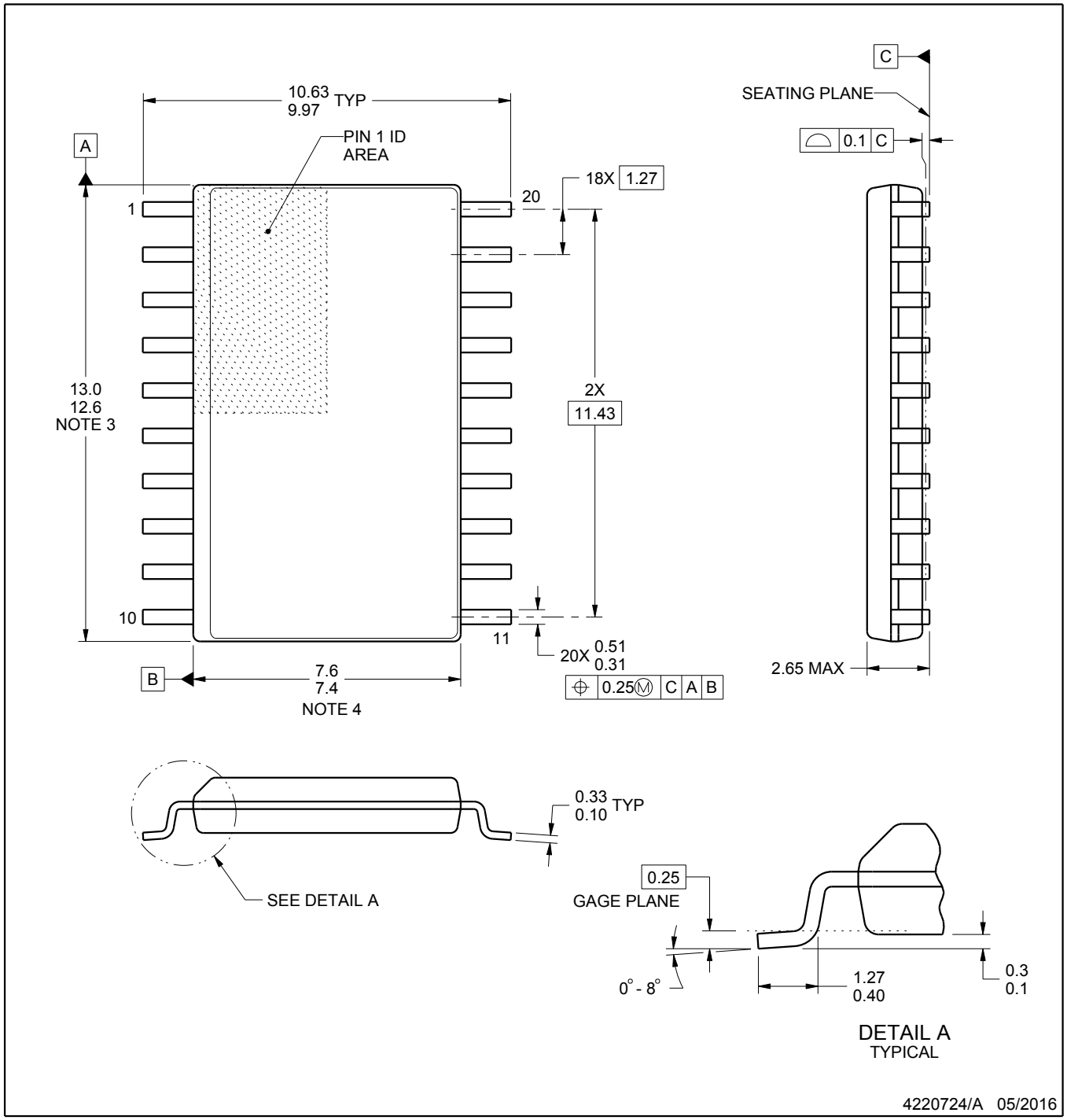


PACKAGE OUTLINE

DW0020A

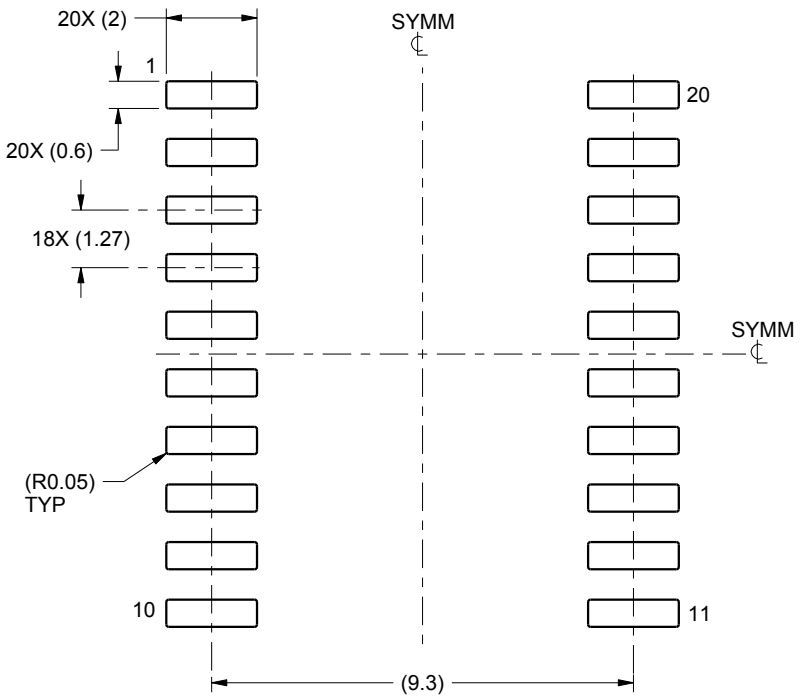
SOIC - 2.65 mm max height

SOIC

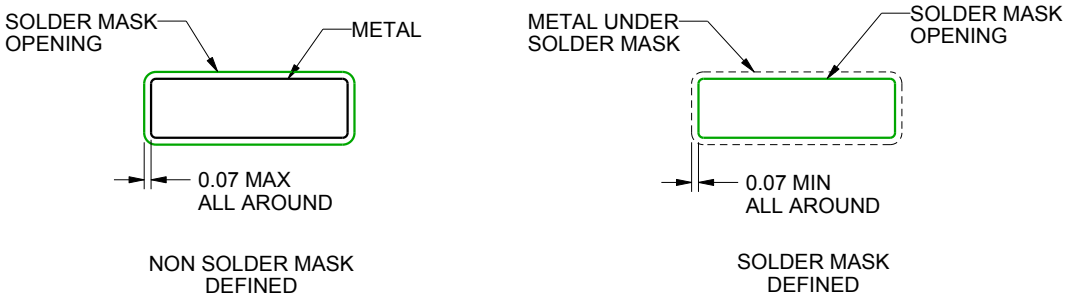


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

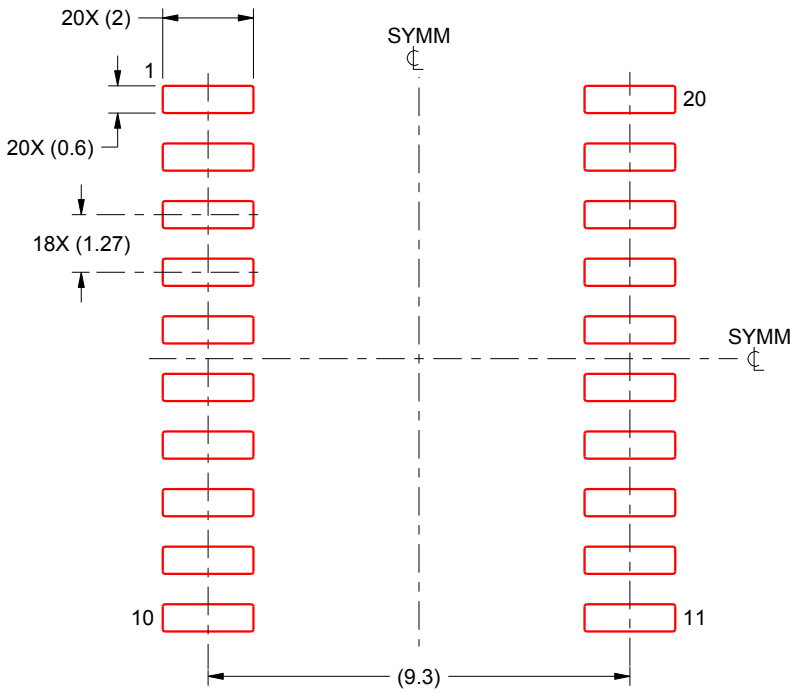


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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