

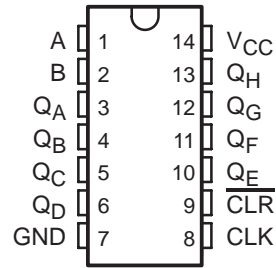
SN74ALS164A

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SDAS159D – APRIL 1982 – REVISED DECEMBER 1994

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs

D OR N PACKAGE
(TOP VIEW)



description

This 8-bit parallel-out serial shift register features AND-gated serial (A and B) inputs and an asynchronous clear ($\overline{\text{CLR}}$) input. The gated serial inputs permit control over incoming data because a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided that the minimum setup-time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input. All inputs are diode clamped to minimize transmission-line effects.

The SN74ALS164A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

| INPUTS | | | | OUTPUTS† | | |
|-------------------------|-----|---|---|----------|-----------|-----|
| $\overline{\text{CLR}}$ | CLK | A | B | QA | QB ... QH | |
| L | X | X | X | L | L | L |
| H | L | X | X | QA0 | QB0 | QH0 |
| H | ↑ | H | H | H | QAn | QGn |
| H | ↑ | L | X | L | QAn | QGn |
| H | ↑ | X | L | L | QAn | QGn |

† QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

QAn, QGn = the level of QA or QG before the most recent

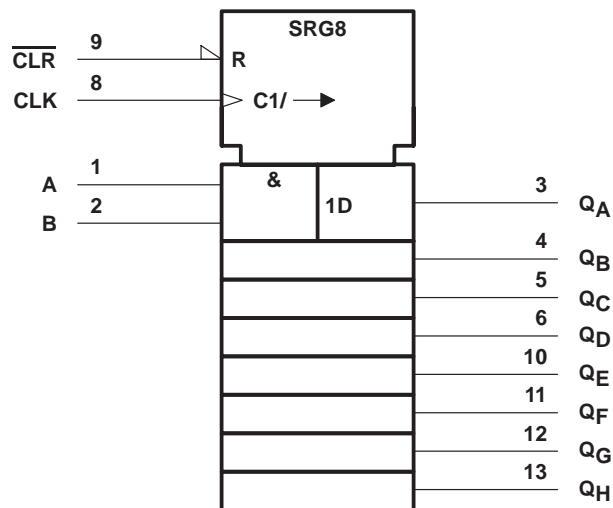
↑ transition of the clock; indicates a 1-bit shift.

SN74ALS164A

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

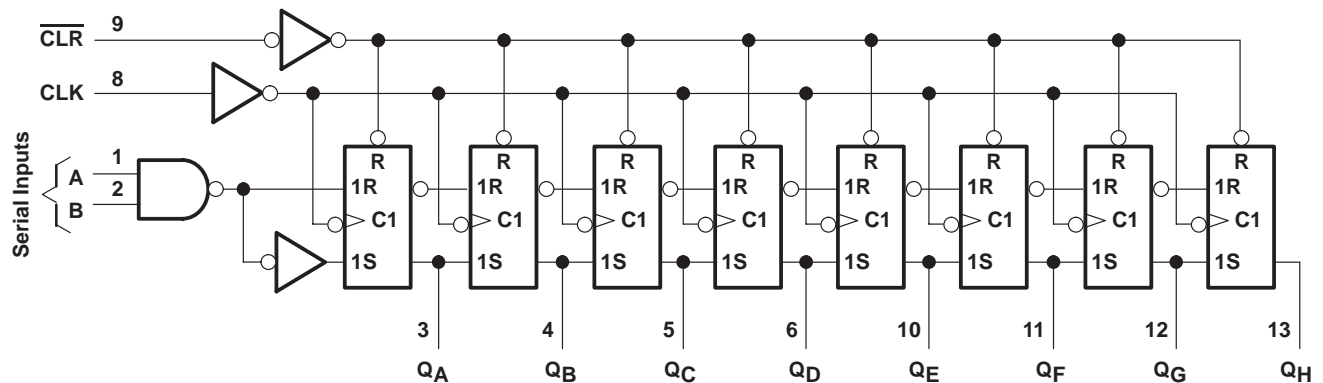
SDAS159D – APRIL 1982 – REVISED DECEMBER 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

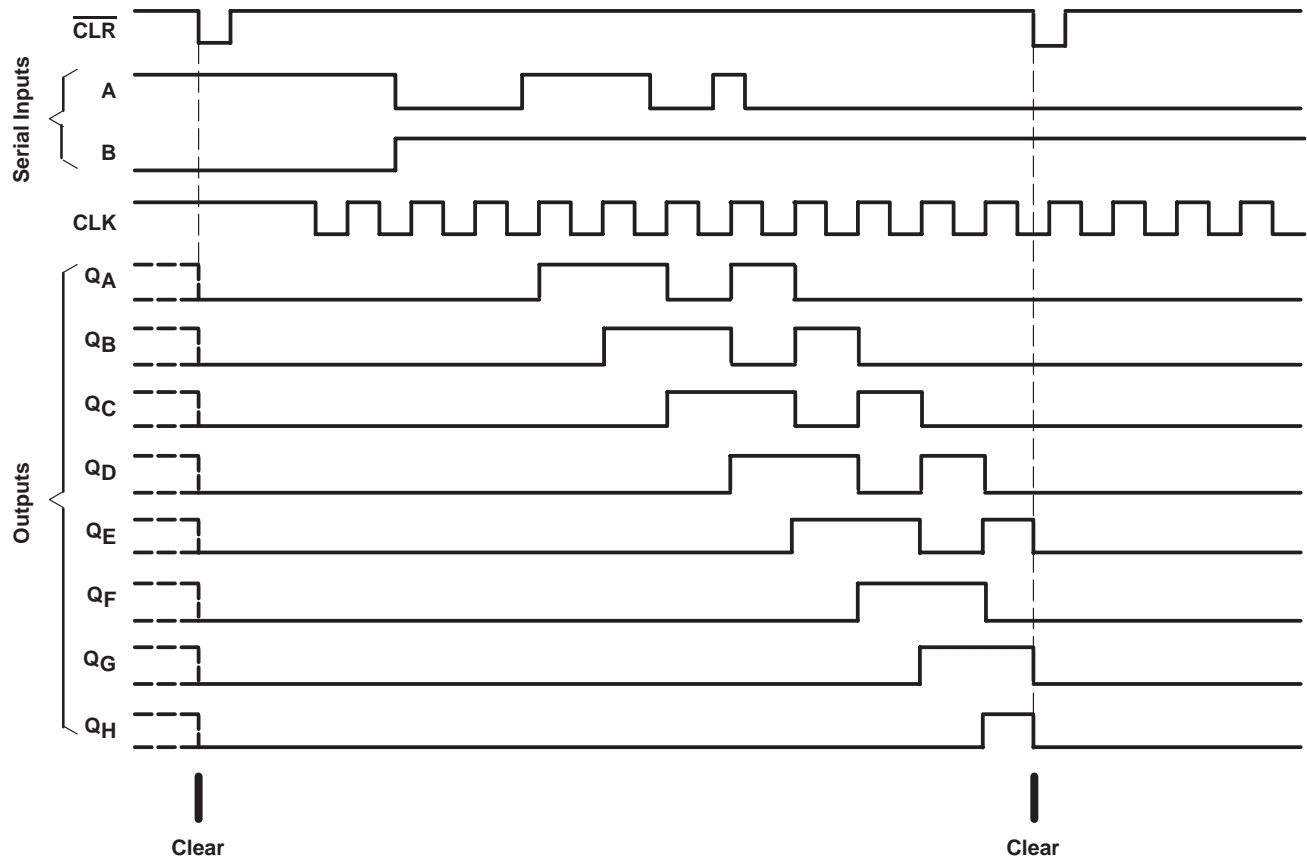


SN74ALS164A

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SDAS159D – APRIL 1982 – REVISED DECEMBER 1994

typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range | –65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

SN74ALS164A

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SDAS159D – APRIL 1982 – REVISED DECEMBER 1994

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|-------------|--------------------------------------|--------------|-----|------|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | -0.4 | mA |
| I_{OL} | Low-level output current | | | 8 | mA |
| f_{clock} | Clock frequency | | | 50 | MHz |
| t_w | Pulse duration | CLK | 10 | | ns |
| | | CLR low | 16 | | |
| t_{su} | Setup time before CLK \uparrow | Data | 6 | | ns |
| | | CLR inactive | 8 | | |
| t_h | Hold time, data after CLK \uparrow | | 2 | | ns |
| T_A | Operating free-air temperature | | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|----------------|---|-----------------|------|------|------|
| V_{IK} | $V_{CC} = 4.5$ V, $I_I = -18$ mA | | | -1.5 | V |
| V_{OH} | $V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA | $V_{CC} - 2$ | | | V |
| V_{OL} | $V_{CC} = 4.5$ V | $I_{OL} = 4$ mA | 0.25 | 0.4 | V |
| | | $I_{OL} = 8$ mA | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5$ V, $V_I = 7$ V | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5$ V, $V_I = 2.7$ V | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5$ V, $V_I = 0.4$ V | | | -0.1 | mA |
| I_O^\ddagger | $V_{CC} = 5.5$ V, $V_O = 2.25$ V | -30 | | -112 | mA |
| I_{CC} | $V_{CC} = 5.5$ V, See Note 1 | | 14 | 24 | mA |

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: With 4.5 V applied to the serial input and all other inputs, except the CLK, grounded, I_{CC} is measured after a clock transition from 0 to 4.5 V.

switching characteristics (see Figure 1)

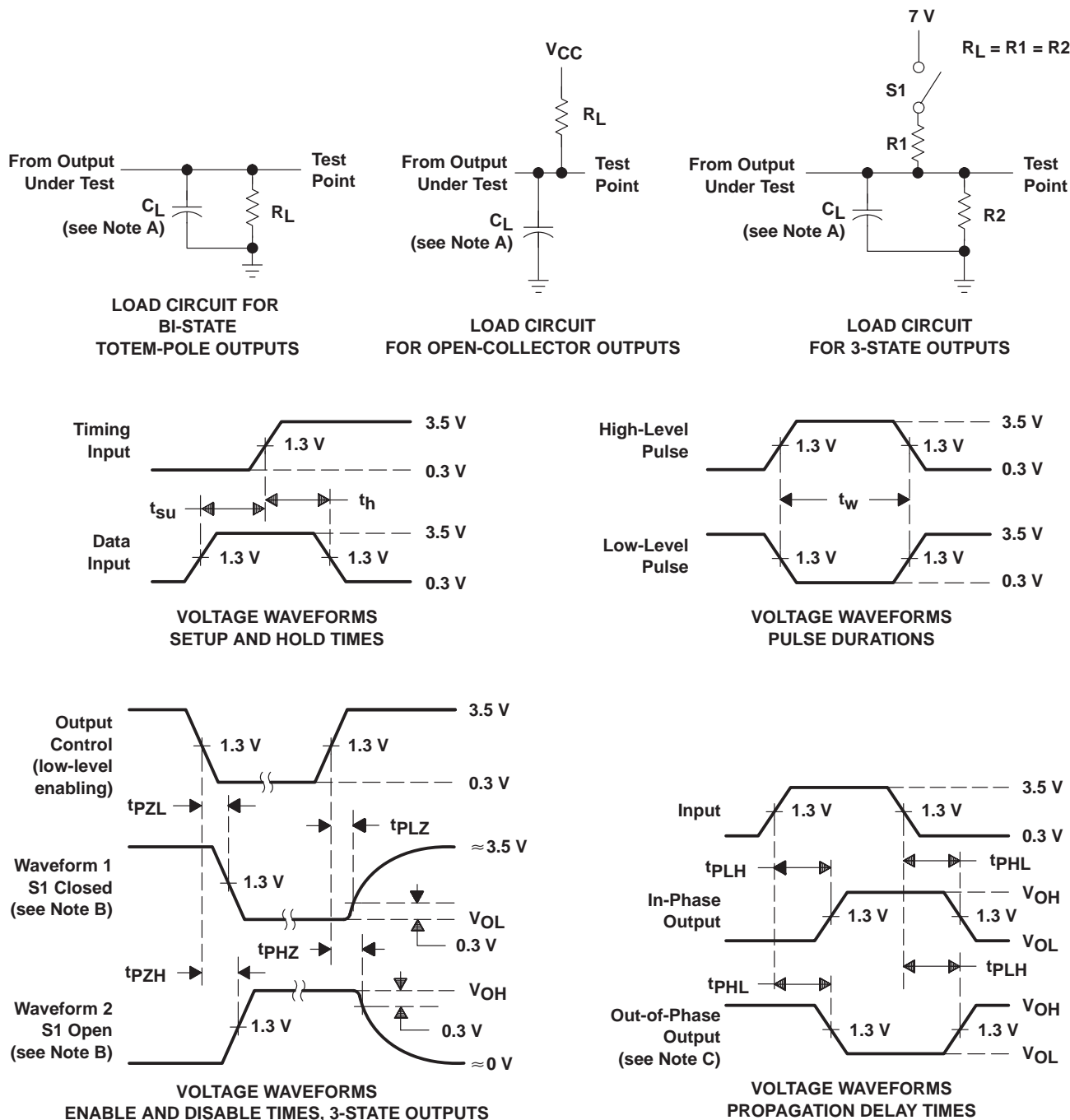
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, $R_L = 500$ Ω, $T_A = \text{MIN to MAX}^\S$ | | | UNIT |
|-----------|--------------|-------------|--|------|-----|------|
| | | | MIN | TYP¶ | MAX | |
| f_{max} | | | 50 | 75 | | MHz |
| t_{PHL} | CLR | Any Q | 6 | 15 | 20 | ns |
| t_{PLH} | CLK | Any Q | 4 | 9 | 16 | ns |
| t_{PHL} | | | 5 | 11 | 17 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

¶ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.



PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74ALS164AD | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | 0 to 70 | ALS164A |
| SN74ALS164ADR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS164A |
| SN74ALS164ADR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS164A |
| SN74ALS164AN | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS164AN |
| SN74ALS164AN.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS164AN |
| SN74ALS164ANSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS164A |
| SN74ALS164ANSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS164A |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

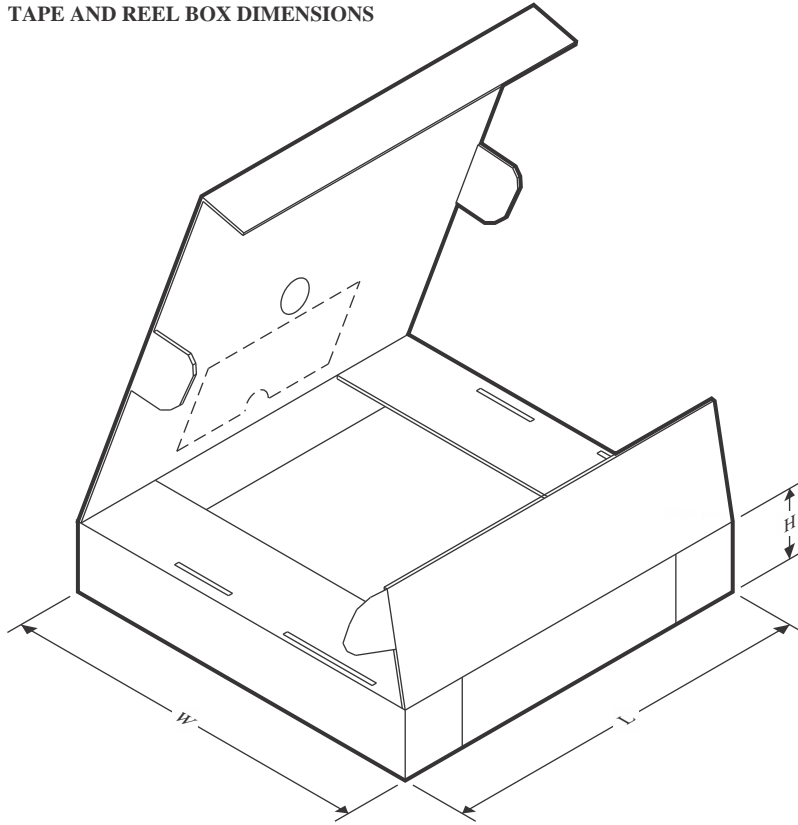
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS164ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS164ANSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

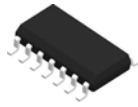
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS164ADR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74ALS164ANSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE

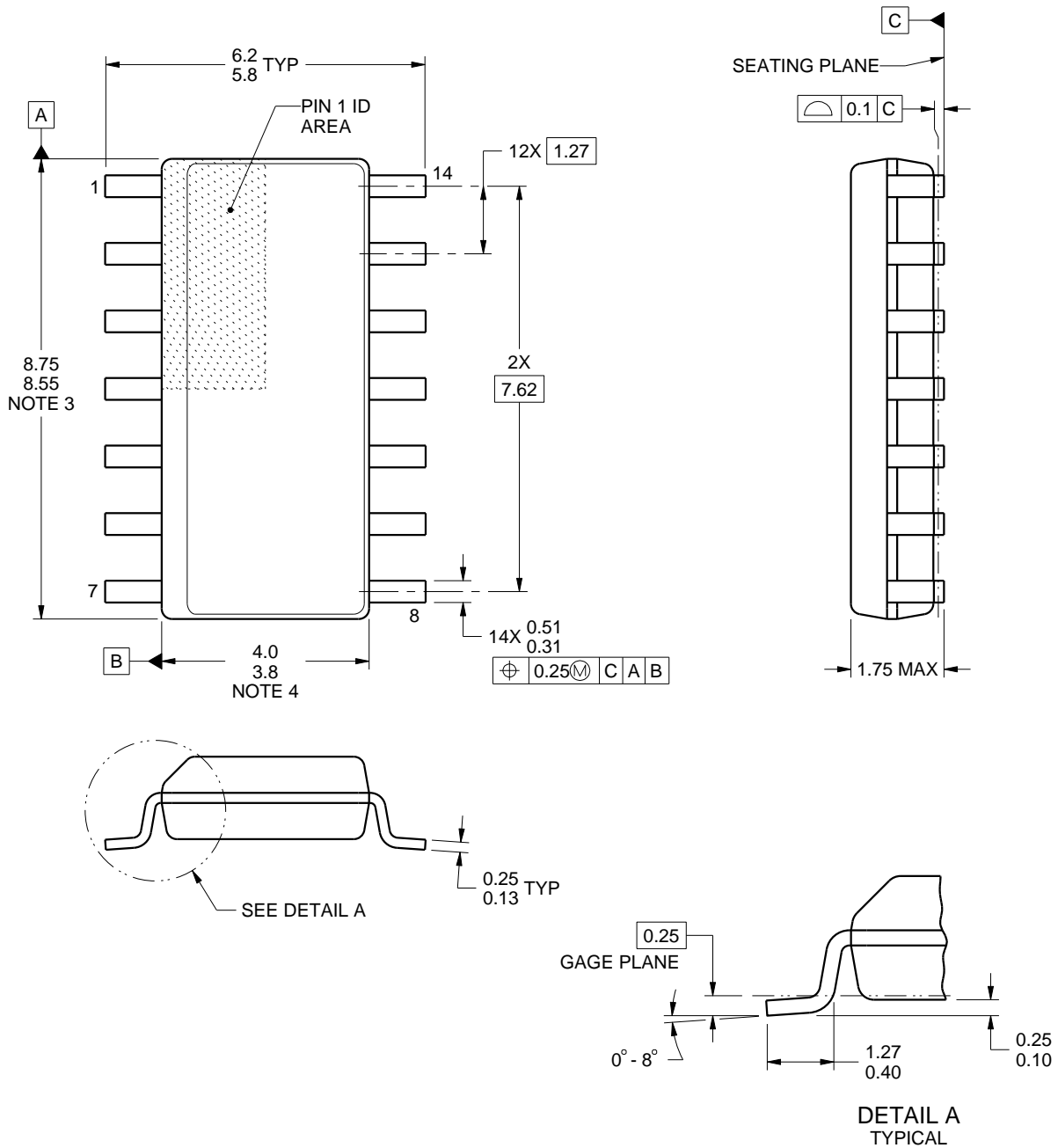


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ALS164AN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS164AN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS164AN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS164AN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

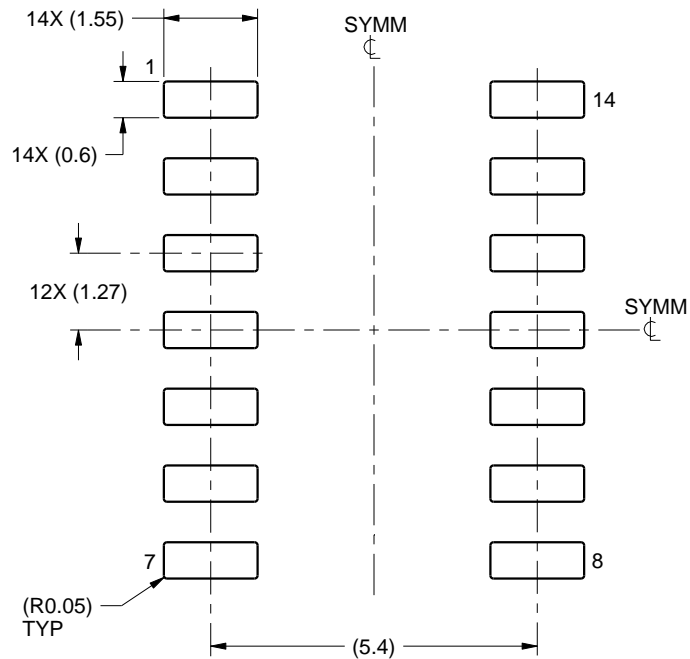
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

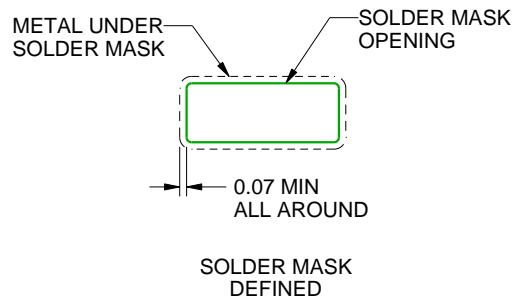
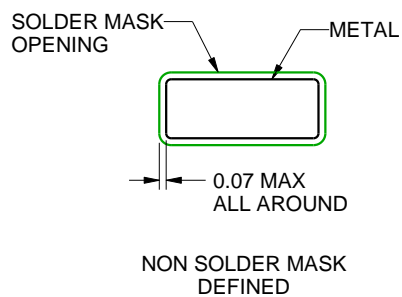
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

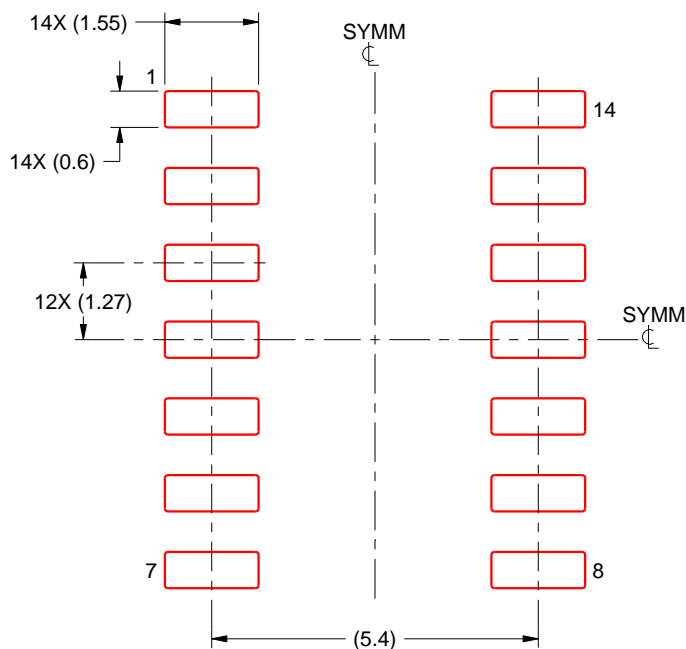
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---------------|-------|-------|-------|-------|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

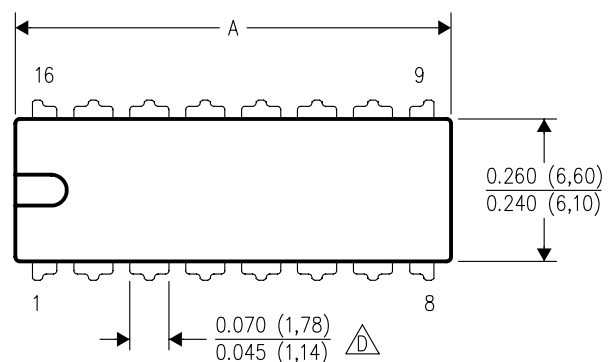
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

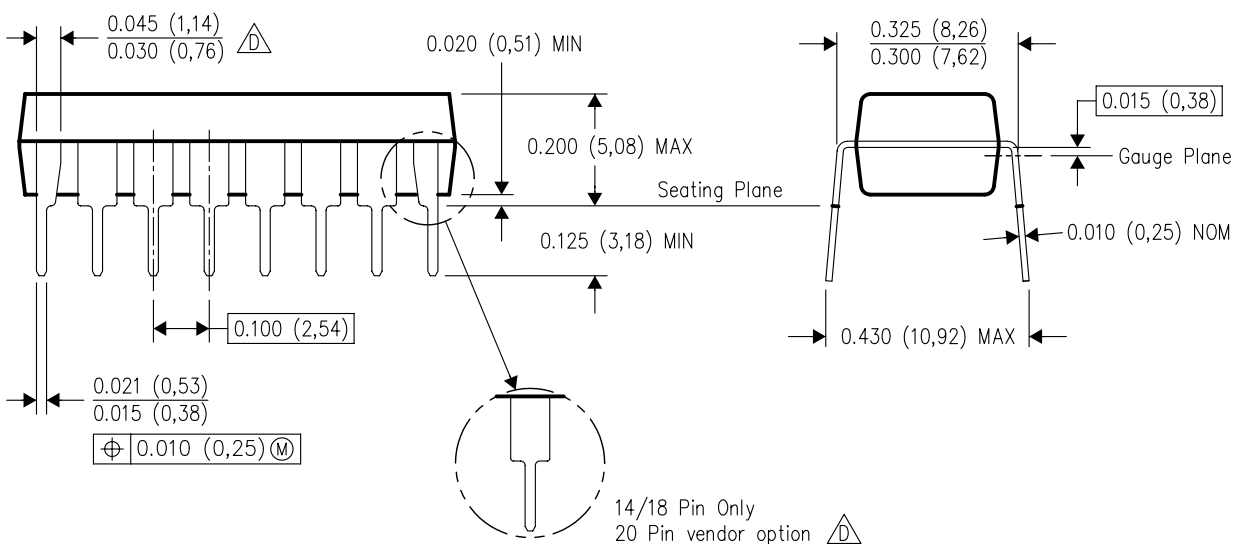
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE





| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated