SN54ALS1035, SN74ALS1035 HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS SDAS243B – APRIL 1982 – REVISED AUGUST 2001

Noninverting Buffers With Open-Collector Outputs

description

These devices contain six independent noninverting buffers. They perform the Boolean function Y = A. The open-collector outputs require pullup resistors to perform correctly. They can be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

SN54ALS1035	. J OR	w	PACK	AGE
SN74ALS1035	. D OR	Ν	PACK	AGE
(TO		•		

1A [1	υ	14] V _{CC}							
1Y [2		13] 6A							
2A [3		12] 6Y							
2Y [4		11] 5A							
3A [5		10] 5Y							
3Y [6		9] 4A							
GND [7		8] 4Y							

SN54ALS1035 ... FK PACKAGE (TOP VIEW)

	AL NC VC 11× 6A CC	
2A NC 2Y NC 3A	$\begin{bmatrix} 3 & 2 & 1 & 20 & 19 \\ 4 & & & 18 \\ 5 & & & 17 \\ 6 & & & 16 \\ 7 & & & 15 \\ 8 & & & 14 \\ 9 & 10 & 11 & 12 & 13 \\ \hline 9 & 10 & 11 & 12 & 13 \\ \hline 9 & 10 & 11 & 12 & 13 \\ \hline 6 & & & 14 \\ \hline 9 & 0 & 11 & 12 & 13 \\ \hline 6 & & & 14 \\ \hline 7 & & & & 14 \\ \hline 9 & 0 & 11 & 12 & 13 \\ \hline 7 & & & & & 14 \\ \hline 9 & 0 & 11 & 12 & 13 \\ \hline 7 & & & & & 14 \\ \hline 9 & 0 & 11 & 12 & 13 \\ \hline 7 & & & & & & 14 \\ \hline 7 & & & & & & & 14 \\ \hline 7 & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & \\ \hline 7 & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ \hline 7 & & & & & & & & & \\ 7 & & & & & & & &$	6Y NC 5A NC 5Y
	~ ~	

NC - No internal connection

ORDERING INFORMATION

TA	РАСКА	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
		Tube	SN7ALS1035D	AL 04005	
0°C to 70°C	30IC - D	Tape and reel	SN7ALS1035DR	AL31035	
	PDIP – N Tube		SN74ALS1035N	SN74ALS1035N	
	CDIP – J	Tube	SNJ54ALS1035J	SNJ54ALS1035J	
–55°C to 125°C	CFP – W	Tube	SNJ54ALS1035W	SNJ54ALS1035W	
	LCCC - FK	Tube	SNJ54ALS1035FK	SNJ54ALS1035FK	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each buffer)								
INPUT A	OUTPUT Y							
н	Н							
L	L							



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logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	
Input voltage, V ₁	
Off-state output voltage	
Package thermal impedance, θ_{JA} (see Note 1): D package	
N package	80°C/W
Storage temperature range, T _{sto}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

1. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54ALS1035		SN	LINIT			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
VOH	High-level output voltage			5.5			5.5	V
IOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C



SN54ALS1035, SN74ALS1035 HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED			SN54ALS10)35	SN74ALS		
PARAMETER		TEST CONDITIONS		MAX	MIN TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	lj = -18 mA		-1.5		-1.5	V
Ve		I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V
VOL VCC = 4.5 V	I _{OL} = 24 mA			0.35	0.5	v	
ЮН	V _{CC} = 4.5 V,	V _{OH} = 5.5 V		0.1		0.1	mA
lı	V _{CC} = 5.5 V,	V _I = 7 V		0.1		0.1	mA
ЧΗ	V _{CC} = 5.5 V,	V _I = 2.7 V		20		20	μA
١ _{١L}	V _{CC} = 5.5 V,	V _I = 0.4 V		-0.1		-0.1	mA
ІССН	V _{CC} = 5.5 V,	VI = 4.5 V	3	6	3	6	mA
ICCL	V _{CC} = 5.5 V,	$V_{I} = 0$	8	14	8	14	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C C _L R _L T _A	UNIT			
			SN54AL	S1035	SN74AL	S1035	
			MIN	MAX	MIN	MAX	
^t PLH	٨	v	5	35	5	30	200
^t PHL	ň		2	14	2	12	115

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_f = t_f = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.







PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	(3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-88742012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88742012A SNJ54ALS 1035FK
5962-8874201CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8874201CA SNJ54ALS1035J
SN54ALS1035J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS1035J
SN54ALS1035J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS1035J
SN74ALS1035D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	ALS1035
SN74ALS1035DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS1035
SN74ALS1035DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS1035
SN74ALS1035DR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS1035
SN74ALS1035N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS1035N
SN74ALS1035N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS1035N
SNJ54ALS1035FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88742012A SNJ54ALS 1035FK
SNJ54ALS1035FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88742012A SNJ54ALS 1035FK
SNJ54ALS1035J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8874201CA SNJ54ALS1035J
SNJ54ALS1035J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8874201CA SNJ54ALS1035J

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ALS1035, SN74ALS1035 :

• Catalog : SN74ALS1035

• Military : SN54ALS1035

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications



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TAPE AND REEL INFORMATION



SN74ALS1035DR



6.5

B0

(mm)

9.0

K0

(mm)

2.1

P1

(mm)

8.0

w

(mm)

16.0

Pin1

Quadrant

Q1

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



330.0

16.4

*All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter	Reel Width	A0 (mm)
					(mm)	W1 (mm)	

D

14

2500

SOIC



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PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS1035DR	SOIC	D	14	2500	353.0	353.0	32.0

TEXAS INSTRUMENTS

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TUBE



- B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
5962-88742012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS1035N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS1035N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS1035N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS1035N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ALS1035FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS1035FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



D0014A

EXAMPLE BOARD LAYOUT

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



D0014A

EXAMPLE STENCIL DESIGN

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



FK 20

8.89 x 8.89, 1.27 mm pitch

GENERIC PACKAGE VIEW

LCCC - 2.03 mm max height

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



J0014A

EXAMPLE BOARD LAYOUT

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE





N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



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