

## SN74AHCT1G32 シングル 2 入力、正論理 OR ゲート

### 1 特長

- 動作範囲: 4.5V~5.5V
- 最大  $t_{pd}$  8ns (5V 時)
- 低消費電力、最大  $I_{CC}$ : 10 $\mu$ A
- 5V で  $\pm 8$ mA の出力駆動能力
- 入力は TTL 電圧互換
- JESD 17 準拠  
250mA 超のラッチアップ性能

### 2 アプリケーション

- I/O モジュール: アナログ PLC/DCS 入力
- サーバー マザーボード
- オートモーティブ クラスタ
- モータ駆動および制御
- DLP フロント プロジェクション システム
- テレビ
- セットトップ ボックス
- オーディオ

### 3 概要

SN74AHCT1G32 はシングル 2 入力正論理 OR ゲートです。このデバイスはブール関数  $Y = A + B$  or  $Y = \overline{A \cdot B}$  を正論理で実行します。

表 3-1. パッケージ情報

| 部品番号         | パッケージ (1)        | パッケージ サイズ (2)  | 本体サイズ (3)       |
|--------------|------------------|----------------|-----------------|
| SN74AHCT1G32 | DBV (SOT-23, 5)  | 2.90mm × 2.8mm | 2.90mm × 1.60mm |
|              | DCK (SC-70, 5)   | 2.00mm × 2.1mm | 2.00mm × 1.30mm |
|              | DRL (SOT-553, 5) | 1.65mm × 1.6mm | 1.65mm × 1.20mm |

- 詳細については、[セクション 11](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



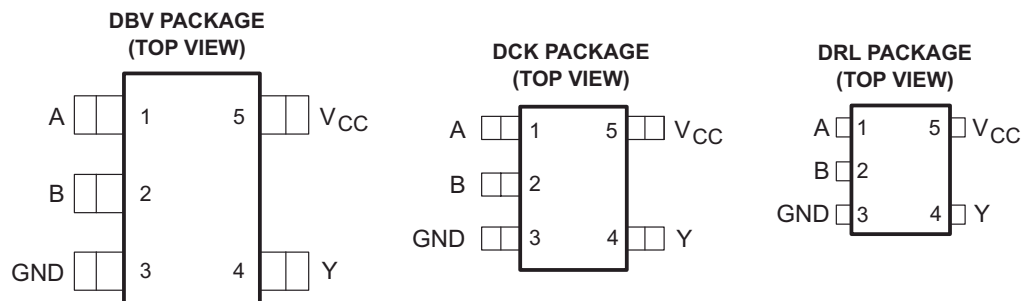
概略回路図



## Table of Contents

|                                                  |          |                                                                  |           |
|--------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 特長</b> .....                                | <b>1</b> | 7.3 Feature Description.....                                     | <b>8</b>  |
| <b>2 アプリケーション</b> .....                          | <b>1</b> | 7.4 Device Functional Modes.....                                 | <b>8</b>  |
| <b>3 概要</b> .....                                | <b>1</b> | <b>8 Application and Implementation</b> .....                    | <b>9</b>  |
| <b>4 Pin Configuration and Functions</b> .....   | <b>3</b> | 8.1 Application Information.....                                 | <b>9</b>  |
| <b>5 Specifications</b> .....                    | <b>4</b> | 8.2 Typical Application.....                                     | <b>9</b>  |
| 5.1 Absolute Maximum Ratings.....                | <b>4</b> | 8.3 Power Supply Recommendations.....                            | <b>10</b> |
| 5.2 ESD Ratings.....                             | <b>4</b> | 8.4 Layout.....                                                  | <b>10</b> |
| 5.3 Recommended Operating Conditions.....        | <b>4</b> | <b>9 Device and Documentation Support</b> .....                  | <b>11</b> |
| 5.4 Thermal Information.....                     | <b>5</b> | 9.1 ドキュメントの更新通知を受け取る方法.....                                      | <b>11</b> |
| 5.5 Electrical Characteristics.....              | <b>5</b> | 9.2 サポート・リソース.....                                               | <b>11</b> |
| 5.6 Switching Characteristics.....               | <b>5</b> | 9.3 Trademarks.....                                              | <b>11</b> |
| 5.7 Operating Characteristics.....               | <b>5</b> | 9.4 静電気放電に関する注意事項.....                                           | <b>11</b> |
| 5.8 Typical Characteristics.....                 | <b>6</b> | 9.5 用語集.....                                                     | <b>11</b> |
| <b>6 Parameter Measurement Information</b> ..... | <b>7</b> | <b>10 Revision History</b> .....                                 | <b>11</b> |
| <b>7 Detailed Description</b> .....              | <b>8</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>11</b> |
| 7.1 Overview.....                                | <b>8</b> |                                                                  |           |
| 7.2 Functional Block Diagram.....                | <b>8</b> |                                                                  |           |

## 4 Pin Configuration and Functions



See mechanical drawings for dimensions.

**表 4-1. Pin Functions**

| PIN |                 | TYPE <sup>(1)</sup> | DESCRIPTION |
|-----|-----------------|---------------------|-------------|
| NO. | NAME            |                     |             |
| 1   | A               | I                   | Input A     |
| 2   | B               | I                   | Input B     |
| 3   | GND             | —                   | Ground Pin  |
| 4   | Y               | O                   | Output Y    |
| 5   | V <sub>CC</sub> | —                   | Power Pin   |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |                                                     | MIN  | MAX            | UNIT |
|-----------|-----------------------------------------------------|------|----------------|------|
| $V_{CC}$  | Supply voltage range                                | –0.5 | 7              | V    |
| $V_I$     | Input voltage range <sup>(2)</sup>                  | –0.5 | 7              | V    |
| $V_O$     | Output voltage range <sup>(2)</sup>                 | –0.5 | $V_{CC} + 0.5$ | V    |
| $I_{IK}$  | Input clamp current<br>$V_I < 0$                    |      | –20            | mA   |
| $I_{OK}$  | Output clamp current<br>$V_O < 0$ or $V_O > V_{CC}$ |      | ±20            | mA   |
| $I_O$     | Continuous output current<br>$V_O = 0$ to $V_{CC}$  |      | ±25            | mA   |
|           | Continuous current through $V_{CC}$ or GND          |      | ±50            | mA   |
| $T_{stg}$ | Storage temperature range                           | –65  | 150            | °C   |
| $T_J$     | Junction Temperature                                |      | 150            | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [セクション 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

|             |                                                                                          | VALUE | UNIT |
|-------------|------------------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge                                                                  |       |      |
|             | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 | V    |
|             | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1000 |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                     |                                    | MIN | MAX      | UNIT |
|---------------------|------------------------------------|-----|----------|------|
| $V_{CC}$            | Supply voltage                     | 4.5 | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | 2   |          | V    |
| $V_{IL}$            | Low-level input voltage            |     | 0.8      | V    |
| $V_I$               | Input voltage                      | 0   | 5.5      | V    |
| $V_O$               | Output voltage                     | 0   | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          |     | –8       | mA   |
| $I_{OL}$            | Low-level output current           |     | 8        | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |     | 20       | ns/V |
| $T_A$               | Operating free-air temperature     | –40 | 125      | °C   |

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* ([SCBA004](#)).

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74AHCT1G32 |       |       | UNIT |
|-------------------------------|----------------------------------------------|--------------|-------|-------|------|
|                               |                                              | DBV          | DCK   | DRL   |      |
|                               |                                              | 5 PINS       |       |       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 278          | 287.6 | 328.7 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 180.5        | 97.7  | 105.1 |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 184.4        | 65.   | 150.3 |      |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 115.4        | 2.0   | 6.9   |      |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 183.4        | 64.2  | 148.4 |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A          | N/A   | N/A   |      |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       |                           | TEST CONDITIONS                                                | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |             | –40°C to 85°C |             | –40°C to 125°C |             | UNIT |
|---------------------------------|---------------------------|----------------------------------------------------------------|-----------------|-----------------------|-----|-------------|---------------|-------------|----------------|-------------|------|
|                                 |                           |                                                                |                 | MIN                   | TYP | MAX         | MIN           | MAX         | MIN            | MAX         |      |
| V <sub>OH</sub>                 | High level output voltage | I <sub>OH</sub> = –50 μA<br>I <sub>OH</sub> = –8 mA            | 4.5 V           | 4.4                   | 4.5 |             | 4.4           |             | 4.4            |             | V    |
| V <sub>OL</sub>                 | Low level output voltage  | I <sub>OL</sub> = 50 μA<br>I <sub>OL</sub> = 8 mA              | 4.5 V           |                       |     | 0.1<br>0.36 |               | 0.1<br>0.44 |                | 0.1<br>0.44 | V    |
| I <sub>I</sub>                  | Input leakage current     | V <sub>I</sub> = 5.5 V or GND                                  | 0 V to 5.5 V    |                       |     | ±0.1        |               | ±1          |                | ±1          | μA   |
| I <sub>CC</sub>                 | Supply current            | V <sub>I</sub> = V <sub>CC</sub> or GND,<br>I <sub>O</sub> = 0 | 5.5 V           |                       |     | 1           |               | 10          |                | 10          | μA   |
| ΔI <sub>CC</sub> <sup>(1)</sup> | Supply-current change     | One input at 3.4 V,<br>Other inputs at V <sub>CC</sub> or GND  | 5.5 V           |                       |     | 1.35        |               | 1.5         |                | 1.5         | mA   |
| C <sub>i</sub>                  | Input Capacitance         | V <sub>I</sub> = V <sub>CC</sub> or GND                        | 5 V             |                       | 2   | 10          |               | 10          |                | 10          | pF   |

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 6-1](#))

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |     |     | –40°C to 85°C |     | –40°C to 125°C |     | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|-----|-----|---------------|-----|----------------|-----|------|
|                  |              |             |                        | MIN                   | TYP | MAX | MIN           | MAX | MIN            | MAX |      |
| t <sub>PLH</sub> | A or B       | Y           | C <sub>L</sub> = 15 pF |                       | 5   | 6.9 | 1             | 8   | 1              | 9   | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 5   | 6.9 | 1             | 8   | 1              | 9   |      |
| t <sub>PLH</sub> | A or B       | Y           | C <sub>L</sub> = 50 pF |                       | 5.5 | 7.9 | 1             | 9   | 1              | 10  | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 5.5 | 7.9 | 1             | 9   | 1              | 10  |      |

## 5.7 Operating Characteristics

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER       | TEST CONDITIONS                                     | TYP  | UNIT |
|-----------------|-----------------------------------------------------|------|------|
| C <sub>pd</sub> | Power dissipation capacitance<br>No load, f = 1 MHz | 11.5 | pF   |

## 5.8 Typical Characteristics

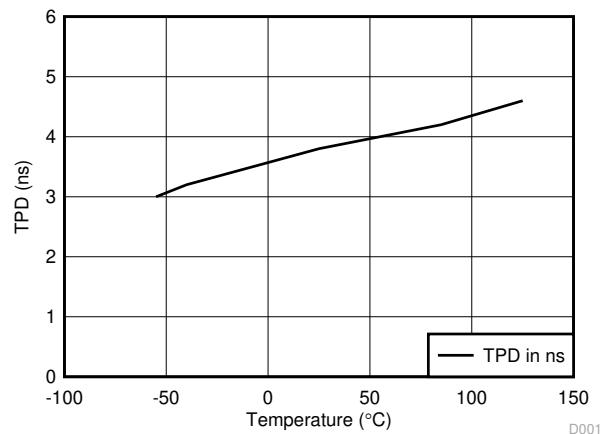
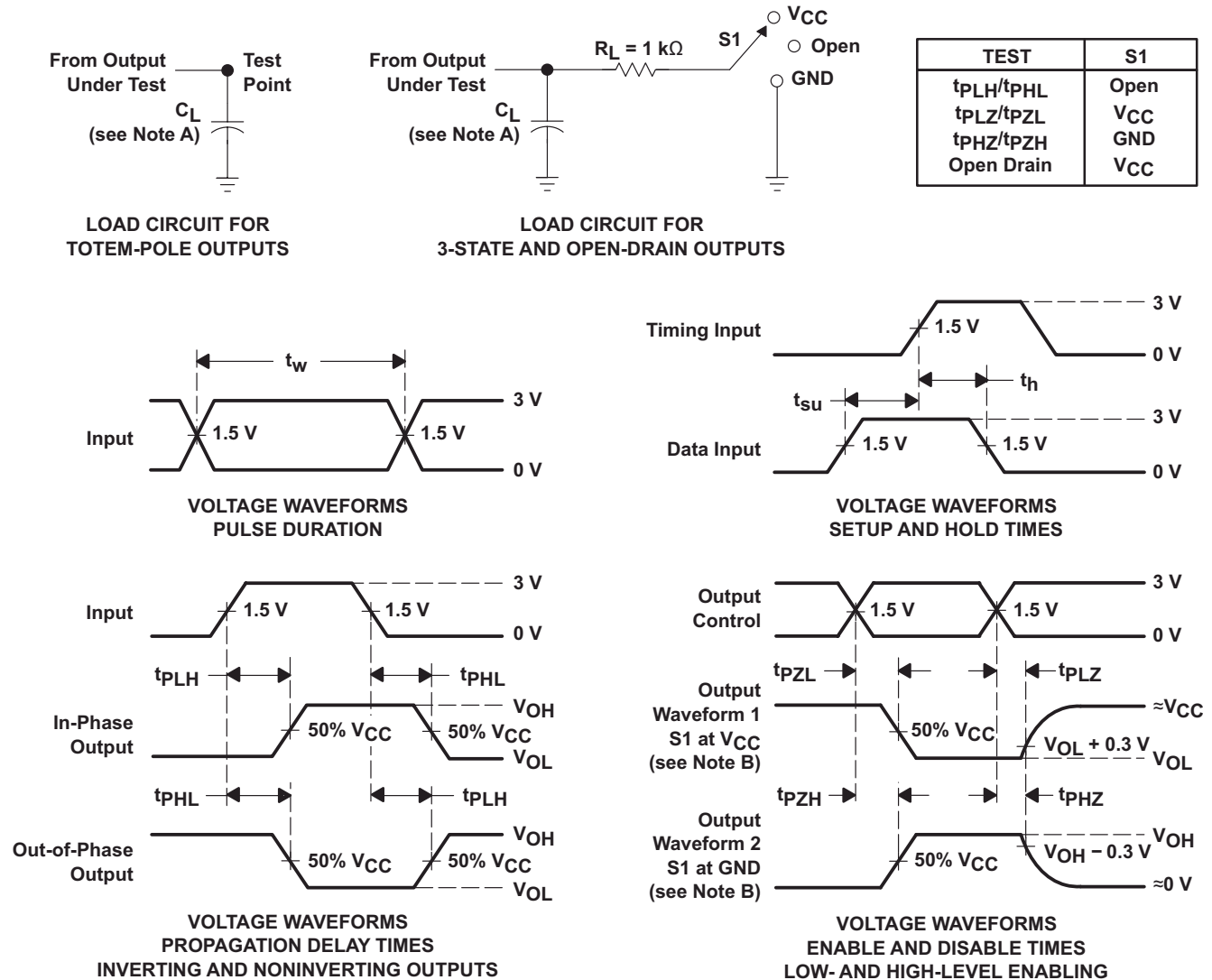


図 5-1. TPD vs Temperature

## 6 Parameter Measurement Information

### 6.1



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - The outputs are measured one at a time, with one input transition per measurement.
  - All parameters and waveforms are not applicable to all devices.

✎ 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SN74AHCT1G32 device is a single 2-input positive-OR gate. The device performs the Boolean function  $Y = A + B$  or  $Y = \overline{A \cdot B}$  in positive logic.

The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when  $V_{CC} = 0$  V.

### 7.2 Functional Block Diagram



图 7-1. Logic Diagram (Positive Logic)

### 7.3 Feature Description

- Slow rise and fall time on outputs allow for low noise outputs.
- TTL inputs
  - Allows up translation from 3.3 V to 5 V

### 7.4 Device Functional Modes

表 7-1. Function Table

| INPUTS <sup>(1)</sup> |   | OUTPUT <sup>(2)</sup> |
|-----------------------|---|-----------------------|
| A                     | B | Y                     |
| H                     | X | H                     |
| X                     | H | H                     |
| L                     | L | L                     |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State



## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

SN74AHCT1G32 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can accept voltages down to 3.3 V and translate up to 5 V.

### 8.2 Typical Application

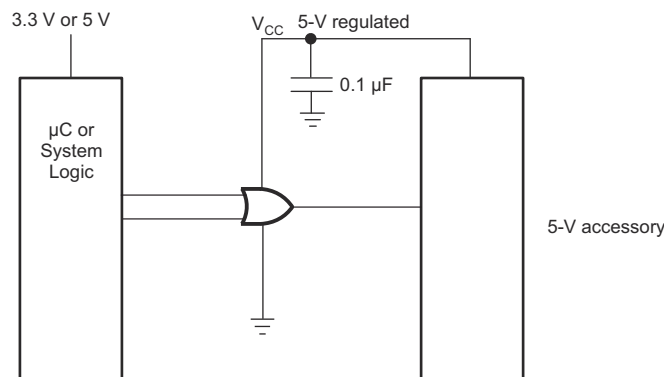


図 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [セクション 5.3](#) table.
  - For specified High and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [セクション 5.3](#) table.
2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## 8.2.3 Application Curves

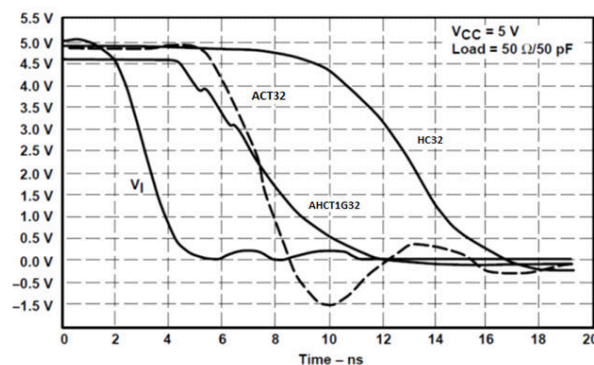


図 8-2. Switching Characteristics Comparison

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [セクション 5.3](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [図 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 8.4.2 Layout Example

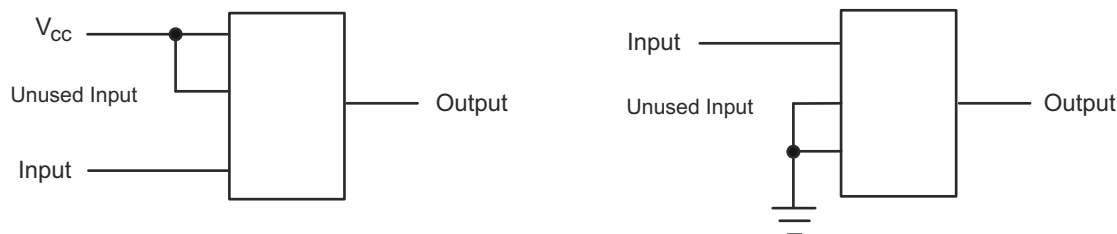


図 8-3. Layout Diagram

## 9 Device and Documentation Support

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.2 サポート・リソース

**TI E2E™ サポート・フォーラム**は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.5 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

| Changes from Revision O (December 2014) to Revision P (March 2024)                                                                                                                                    | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....                                                                                                                                                                    | 1    |
| Updated thermal values for DBV package from RθJA = 231.3 to 278, RθJC(top) = 119.9 to 180.5, RθJB = 60.6 to 184.4, ΨJT = 17.8 to 115.4, ΨJB = 60.1 to 183.4, RθJC(bot) = N/A, all values in °C/W..... | 5    |

| Changes from Revision N (June 2005) to Revision O (December 2014)                                                                                                                                    | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 「アプリケーション」、「製品情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「代表的特性」、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加。..... | 1    |
| 「注文情報」表を削除。.....                                                                                                                                                                                     | 1    |
| Changed MAX operating temperature to 125°C in <i>Recommended Operating Conditions</i> table. ....                                                                                                    | 4    |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                        |
|----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--------------------------------------------|
| <a href="#">74AHCT1G32DBVRG4</a> | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | (3CCF, B32G)                               |
| 74AHCT1G32DBVRG4.A               | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | (3CCF, B32G)                               |
| <a href="#">74AHCT1G32DCKRG4</a> | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | BG3                                        |
| 74AHCT1G32DCKRG4.A               | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | BG3                                        |
| <a href="#">SN74AHCT1G32DBVR</a> | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (36FH, 3CBF, B323, B32G, B32J, B32L, B32S) |
| SN74AHCT1G32DBVR.A               | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (36FH, 3CBF, B323, B32G, B32J, B32L, B32S) |
| <a href="#">SN74AHCT1G32DCK3</a> | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -40 to 85    | BGY                                        |
| SN74AHCT1G32DCK3.A               | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -40 to 85    | BGY                                        |
| <a href="#">SN74AHCT1G32DCKR</a> | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (1QU, BG3, BGG, BGJ, BGL, BGS)             |
| SN74AHCT1G32DCKR.A               | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (1QU, BG3, BGG, BGJ, BGL, BGS)             |
| <a href="#">SN74AHCT1G32DCKT</a> | Obsolete      | Production           | SC70 (DCK)   5    | -                     | -           | Call TI                              | Call TI                           | -40 to 125   | (BG3, BGG, BGJ, BGS)                       |
| <a href="#">SN74AHCT1G32DRLR</a> | Active        | Production           | SOT-5X3 (DRL)   5 | 4000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | BGS                                        |
| SN74AHCT1G32DRLR.A               | Active        | Production           | SOT-5X3 (DRL)   5 | 4000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | BGS                                        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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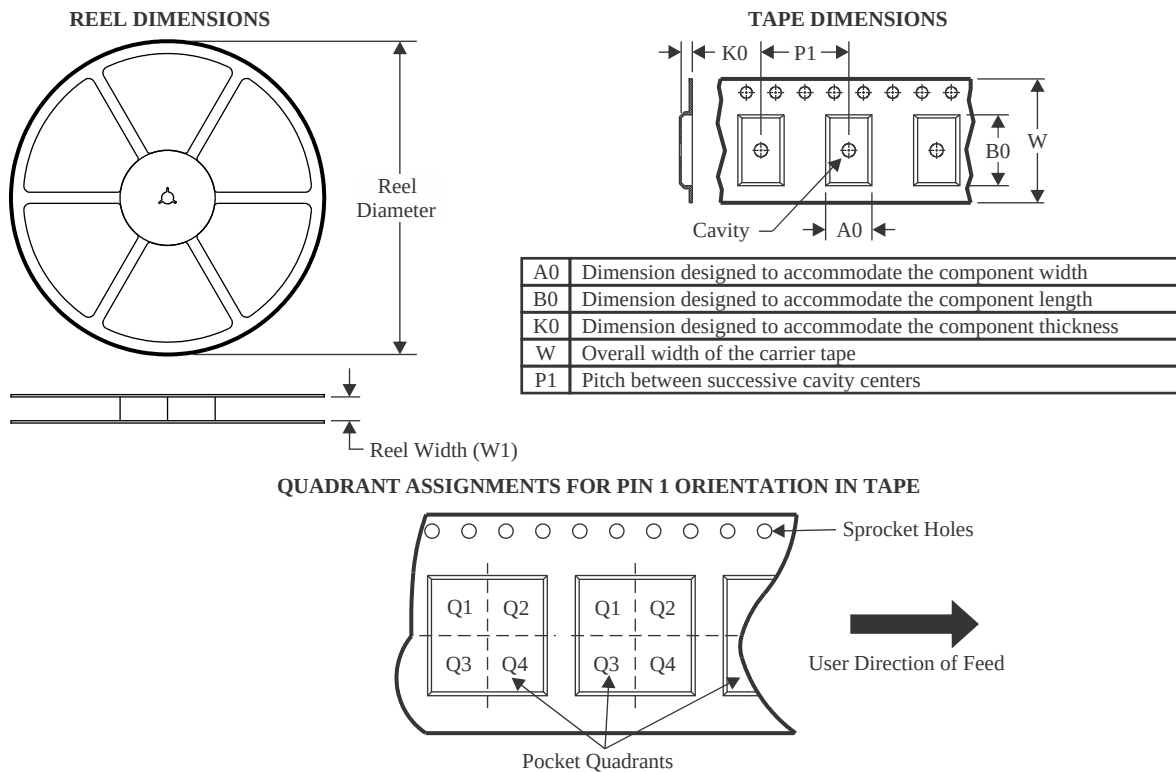
**OTHER QUALIFIED VERSIONS OF SN74AHCT1G32 :**

- Automotive : [SN74AHCT1G32-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

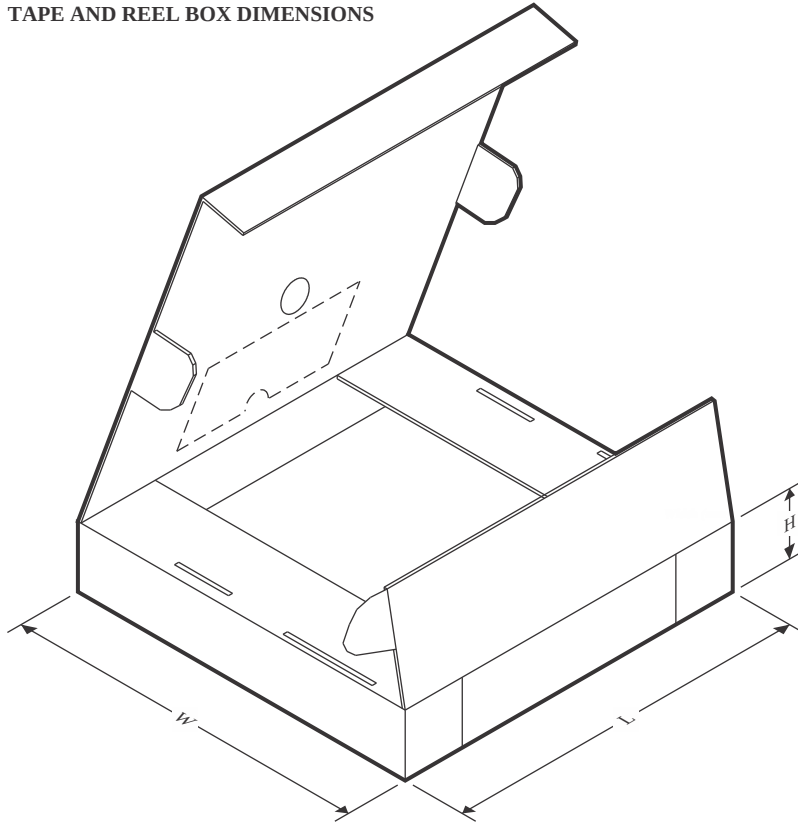
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

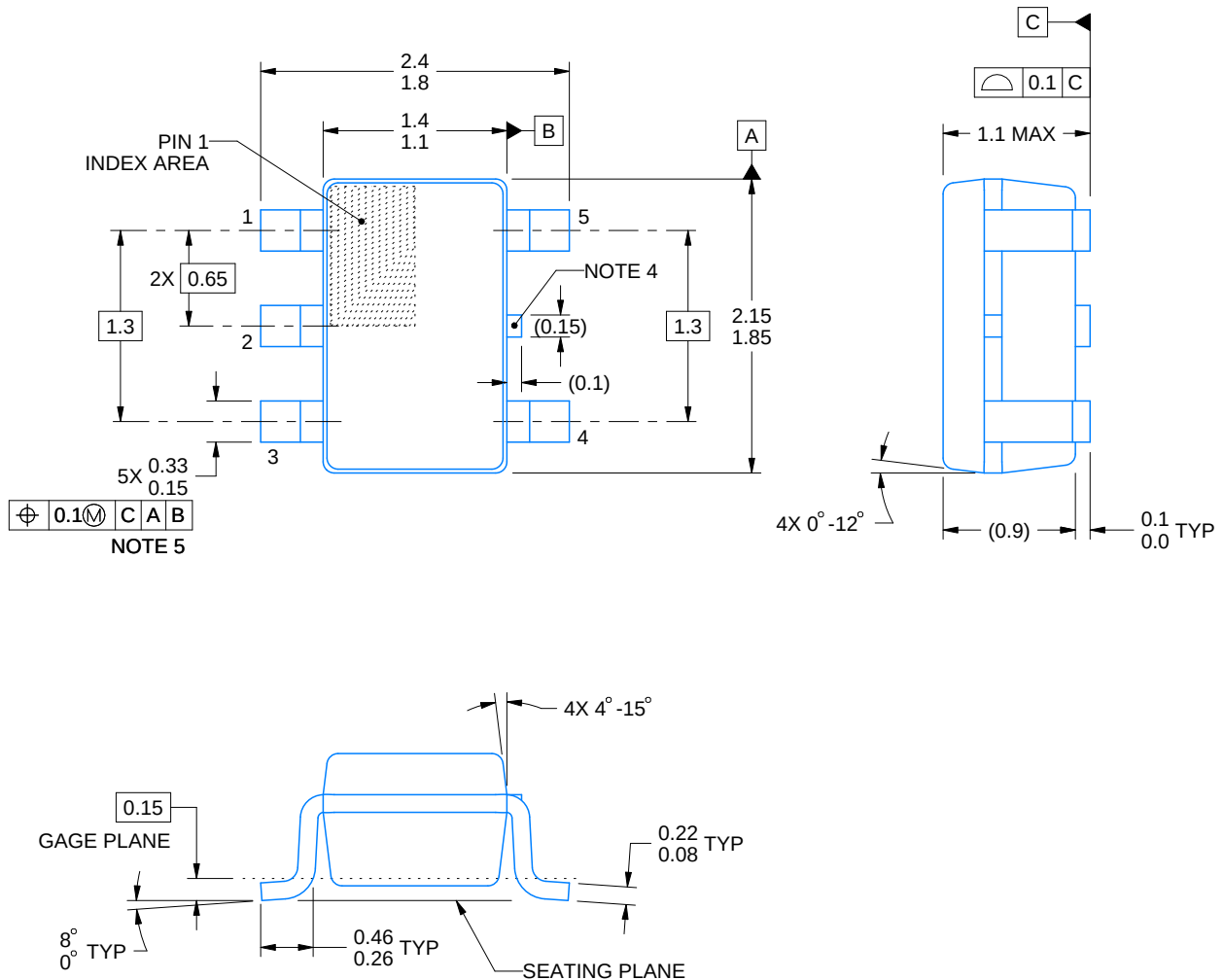
| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74AHCT1G32DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| 74AHCT1G32DCKRG4 | SC70         | DCK             | 5    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74AHCT1G32DBVR | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74AHCT1G32DCKR | SC70         | DCK             | 5    | 3000 | 180.0              | 8.4                | 2.3     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74AHCT1G32DRLR | SOT-5X3      | DRL             | 5    | 4000 | 180.0              | 8.4                | 1.98    | 1.78    | 0.69    | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74AHCT1G32DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| 74AHCT1G32DCKRG4 | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74AHCT1G32DBVR | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| SN74AHCT1G32DCKR | SC70         | DCK             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| SN74AHCT1G32DRLR | SOT-5X3      | DRL             | 5    | 4000 | 202.0       | 201.0      | 28.0        |



4214834/G 11/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

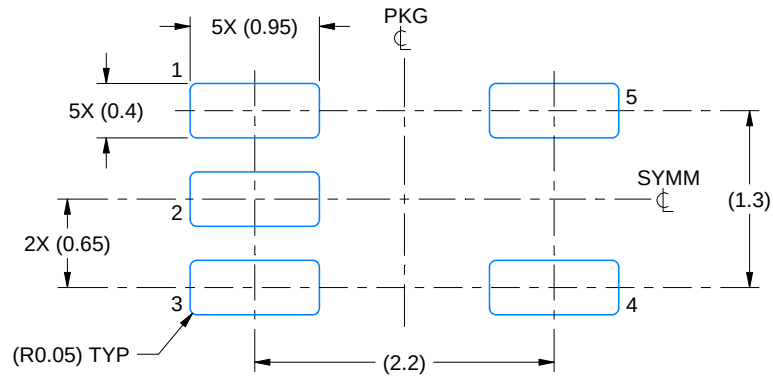


# EXAMPLE BOARD LAYOUT

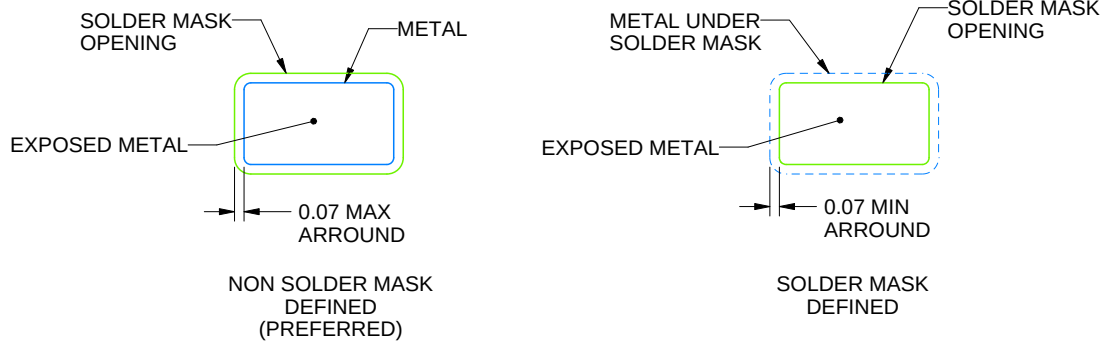
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

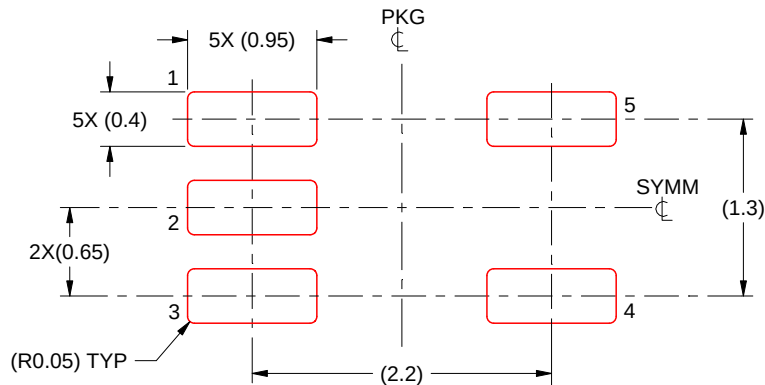


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



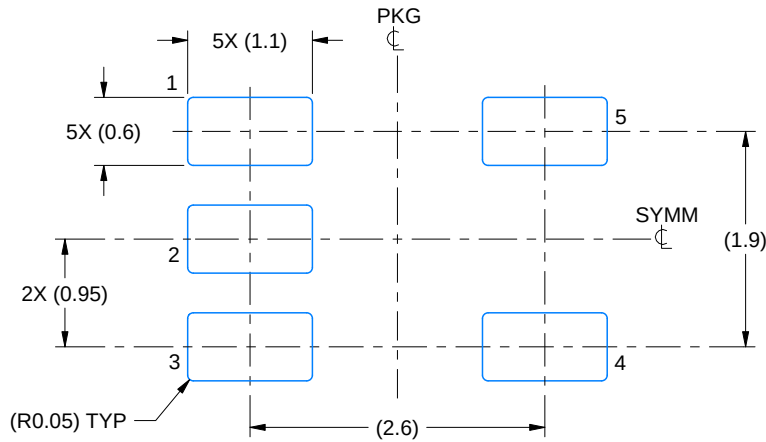
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

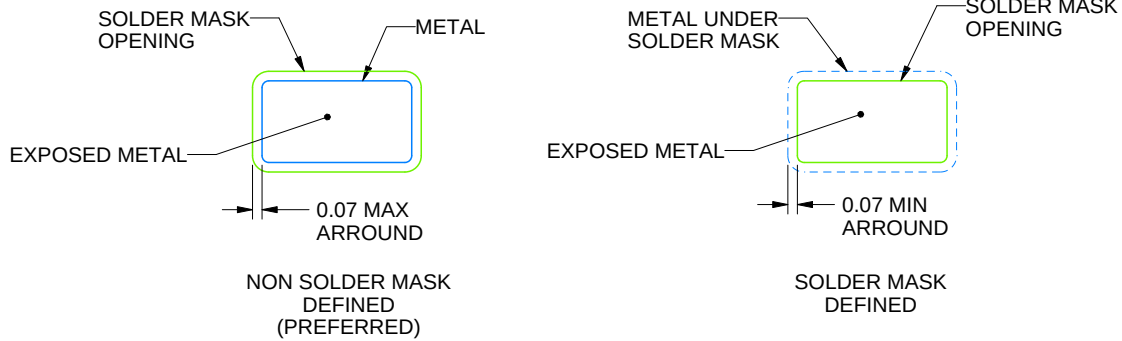
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

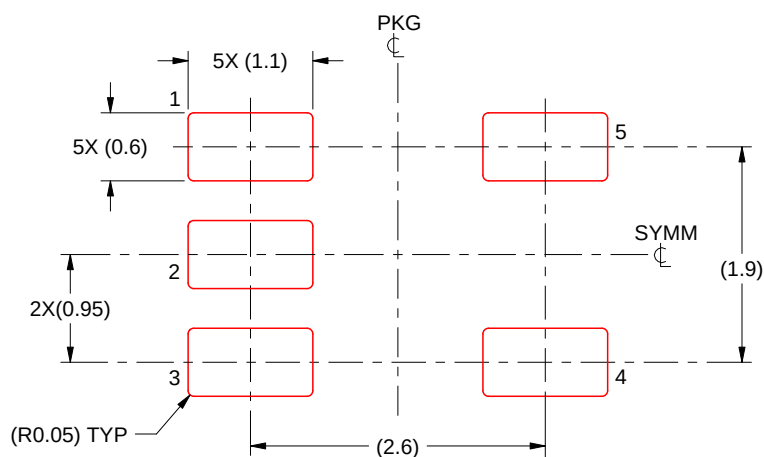
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



**SOT - 0.6 mm max height**

[illegible]

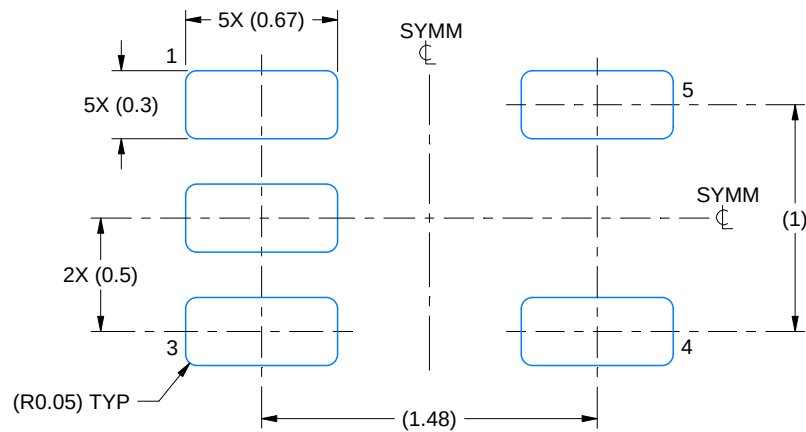
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

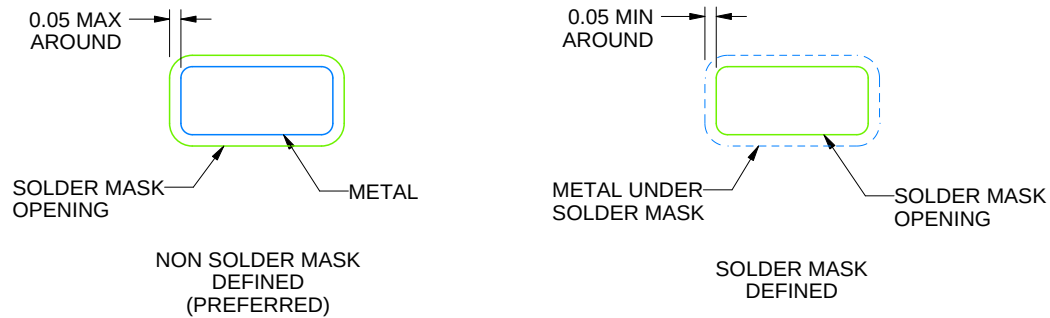
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

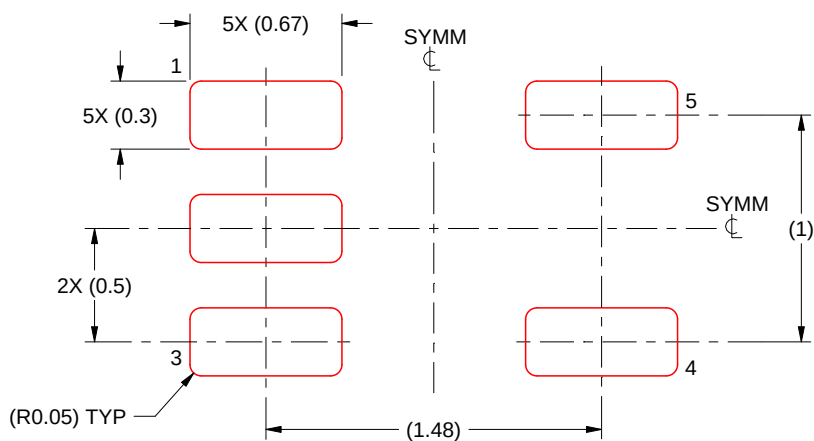
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



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