

# SN74AHCT1G14 シングル・シュミット・トリガ・インバータ・ゲート

## 1 特長

- 動作範囲: 4.5V~5.5V
- 最大  $t_{pd}$ : 8ns (5V 時)
- 低消費電力、最大  $I_{CC}$ : 1μA
- 5V で ±8mA の出力駆動能力
- 入力は TTL 電圧互換
- JESD 17 準拠で 250mA 超のラッチアップ性能

## 2 アプリケーション

- デジタル信号のイネーブルまたはディセーブル
- インジケータ LED の制御
- 通信モジュールとシステム・コントローラの間の変換

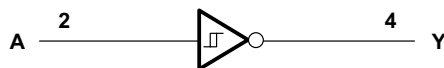
## 3 概要

SN74AHCT1G14 には 1 つのインバータ ゲートが搭載されています。このデバイスは、ブール関数  $Y = \overline{A}$  を実行します。

### パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)	本体サイズ (3)
SN74AHCT1G14	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC-70, 5)	2.00mm × 1.25mm	2.00mm × 1.25mm

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージ サイズ (長さ×幅) は公称値で、該当する場合はピンも含まれます。
- 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。

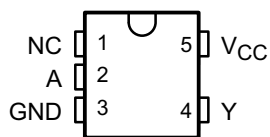


論理図 (正論理)

## Table of Contents

<b>1 特長</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>10</b>
<b>2 アプリケーション</b> .....	<b>1</b>	8.1 Application Information.....	10
<b>3 概要</b> .....	<b>1</b>	8.2 Typical Application.....	10
<b>4 Pin Configuration and Functions</b> .....	<b>3</b>	8.3 Power Supply Recommendations.....	12
<b>5 Specifications</b> .....	<b>4</b>	8.4 Layout.....	12
5.1 Absolute Maximum Ratings.....	4	<b>9 Device and Documentation Support</b> .....	<b>14</b>
5.2 Recommended Operating Conditions.....	4	9.1 Documentation Support (Analog).....	14
5.3 Thermal Information.....	4	9.2 ドキュメントの更新通知を受け取る方法.....	14
5.4 Electrical Characteristics.....	5	9.3 サポート・リソース.....	14
5.5 Switching Characteristics.....	6	9.4 Trademarks.....	14
5.6 Operating Characteristics.....	7	9.5 静電気放電に関する注意事項.....	14
<b>6 Parameter Measurement Information</b> .....	<b>8</b>	9.6 用語集.....	14
<b>7 Detailed Description</b> .....	<b>9</b>	<b>10 Revision History</b> .....	<b>14</b>
7.1 Overview.....	9	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>15</b>
7.2 Functional Block Diagram.....	9		
7.3 Device Functional Modes.....	9		

## 4 Pin Configuration and Functions



NC – No internal connection

See [セクション 11](#) for dimensions.

**図 4-1. DBV or DCK Package 5-Pin SOT-23 or SC70 (Top View)**

**表 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	NC	—	No connect
2	A	I	Data Input
3	GND	—	Ground
4	Y	O	Data Output
5	V <sub>CC</sub>	—	Power

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	–0.5	7	V
V <sub>I</sub> <sup>(2)</sup>	Input voltage range	–0.5	7	V
V <sub>O</sub> <sup>(2)</sup>	Output voltage range	–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0)	–20	mA
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20	mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±50	mA
T <sub>stg</sub>	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		–8	mA
I <sub>OL</sub>	Low-level output current		8	mA
T <sub>A</sub>	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHCT1G14		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	278	289.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>T+</sub> Positive-going input threshold voltage	T <sub>A</sub> = 25°C	4.5 V	0.9		2	V
	T <sub>A</sub> = –40°C to 85°C		0.9			
	T <sub>A</sub> = –40°C to 125°C		0.9		2	
	T <sub>A</sub> = 25°C	5.5 V	1.1		2	
	T <sub>A</sub> = –40°C to 85°C		1.1			
	T <sub>A</sub> = –40°C to 125°C		1.1		2	
V <sub>T–</sub> Negative-going input threshold voltage	T <sub>A</sub> = 25°C	4.5 V	0.5		1.6	V
	T <sub>A</sub> = –40°C to 85°C		0.5			
	T <sub>A</sub> = –40°C to 125°C		0.5		1.6	
	T <sub>A</sub> = 25°C	5.5 V	0.6		1.5	
	T <sub>A</sub> = –40°C to 85°C		0.6			
	T <sub>A</sub> = –40°C to 125°C		0.6		1.5	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> – V <sub>T–</sub> )	T <sub>A</sub> = 25°C	4.5 V	0.4		1.4	V
	T <sub>A</sub> = –40°C to 85°C		0.4			
	T <sub>A</sub> = –40°C to 125°C		0.4		1.4	
	T <sub>A</sub> = 25°C	5.5 V	0.5		1.6	
	T <sub>A</sub> = –40°C to 85°C		0.4			
	T <sub>A</sub> = –40°C to 125°C		0.5		1.6	
V <sub>OH</sub> High level output voltage	T <sub>A</sub> = 25°C	4.5 V	4.4	4.5		V
	T <sub>A</sub> = –40°C to 85°C		4.4			
	T <sub>A</sub> = –40°C to 125°C		4.4			
	T <sub>A</sub> = 25°C		3.94			
	T <sub>A</sub> = –40°C to 85°C		3.88			
	T <sub>A</sub> = –40°C to 125°C		3.7			

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 50 mA	T <sub>A</sub> = 25°C	4.5 V			0.1	V
			T <sub>A</sub> = −40°C to 85°C				0.1	
			T <sub>A</sub> = −40°C to 125°C				0.1	
	I <sub>OL</sub> = 8 mA	T <sub>A</sub> = 25°C				0.36		
		T <sub>A</sub> = −40°C to 85°C				0.44		
		T <sub>A</sub> = −40°C to 125°C				0.55		
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = 5.5 V or GND	T <sub>A</sub> = 25°C	0 V to 5.5 V			±0.1	μA
			T <sub>A</sub> = −40°C to 85°C				±1	
			T <sub>A</sub> = −40°C to 125°C				±1	
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	T <sub>A</sub> = 25°C	5.5 V			1	μA
			T <sub>A</sub> = −40°C to 85°C				10	
			T <sub>A</sub> = −40°C to 125°C				10	
C <sub>i</sub>	Input Capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	T <sub>A</sub> = 25°C	5 V		2	10	pF
			T <sub>A</sub> = −40°C to 85°C				10	
			T <sub>A</sub> = −40°C to 125°C				10	

(1) Recommended T<sub>A</sub> = –40°C to 125°C

## 5.5 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

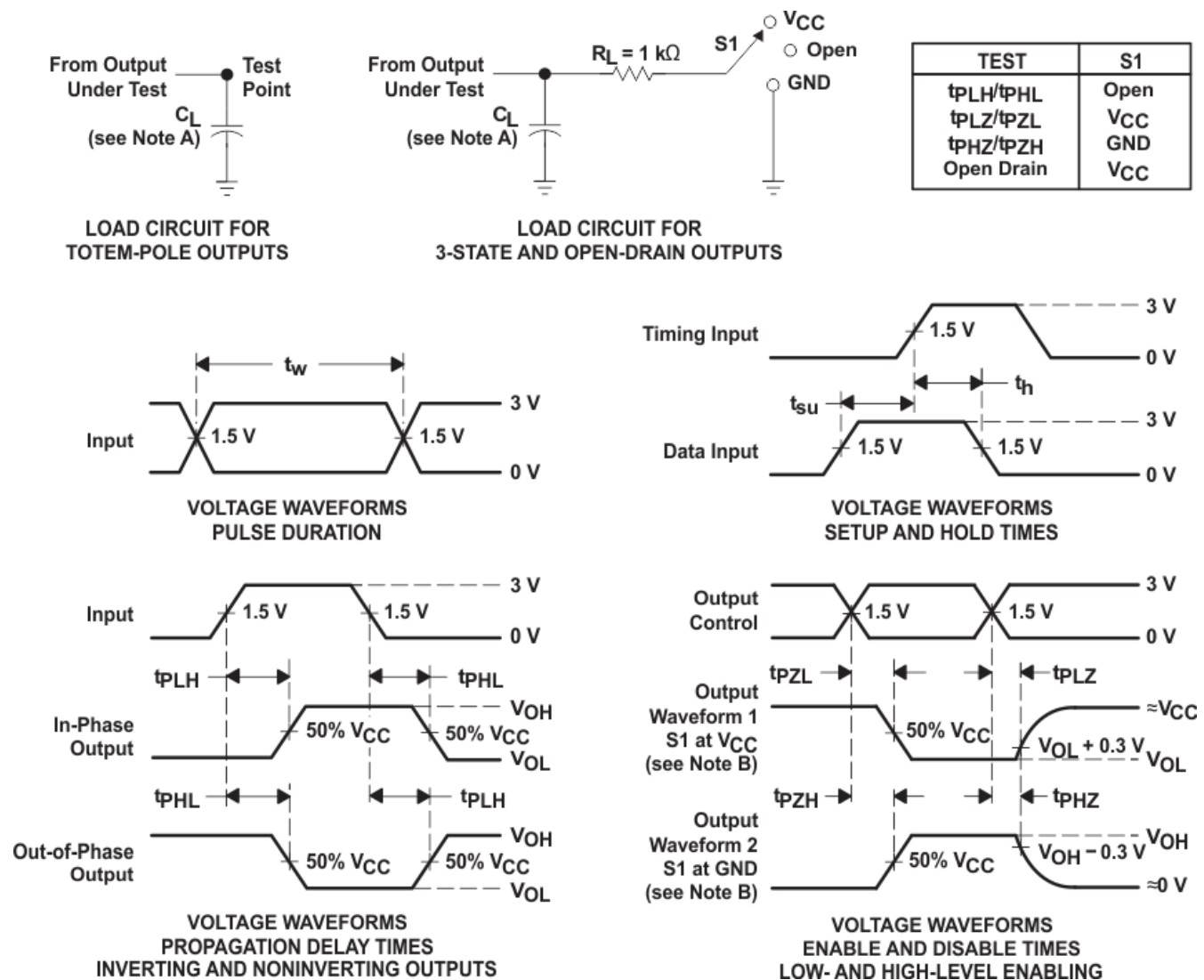
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	T <sub>A</sub> = 25°C		4	7	ns
				T <sub>A</sub> = −40°C to 85°C	1		8	
				T <sub>A</sub> = −40°C to 125°C	1		9	
t <sub>PHL</sub>				T <sub>A</sub> = 25°C		4	7	
				T <sub>A</sub> = −40°C to 85°C	1		8	
				T <sub>A</sub> = −40°C to 125°C	1		9	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	T <sub>A</sub> = 25°C		5.5	8	ns
				T <sub>A</sub> = −40°C to 85°C	1		9	
				T <sub>A</sub> = −40°C to 125°C	1		10	
t <sub>PHL</sub>				T <sub>A</sub> = 25°C		5.5	8	
				T <sub>A</sub> = −40°C to 85°C	1		9	
				T <sub>A</sub> = −40°C to 125°C	1		10	

## 5.6 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	12	pF

## 6 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**图 6-1. Load Circuit and Voltage Waveforms**

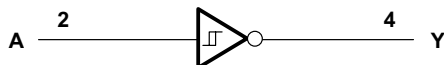
## 7 Detailed Description

### 7.1 Overview

The SN74AHCT1G14 contains a single inverter gate. The device performs the Boolean function  $Y = \bar{A}$ .

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

INPUTS <sup>(1)</sup>	OUTPUT <sup>(2)</sup>
A	Y
H	L
L	H

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in [Typical Application Block Diagram](#). The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74AHCT1G14 is used to directly control the **RESET** pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

### 8.2 Typical Application

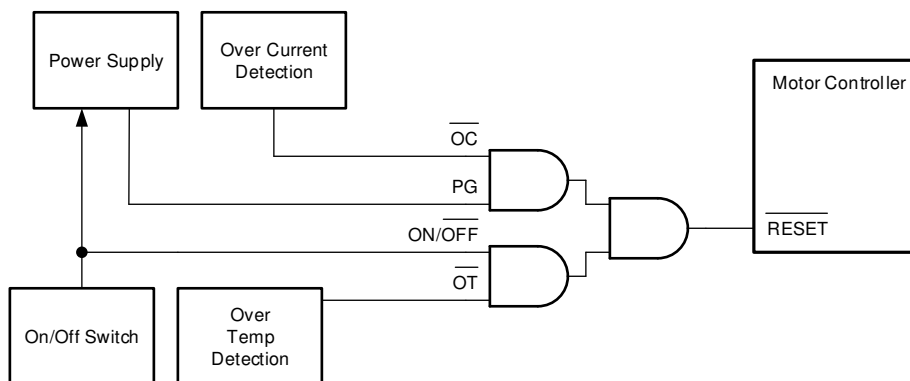


図 8-1. Typical Application Block Diagram

#### 8.2.1 Design Requirements

##### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHCT1G14 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74AHCT1G14 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74AHCT1G14 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OL}$ . When outputting in the HIGH state, the output

voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation](#) application note.

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#) application note.

#### 注意

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHCT1G14 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

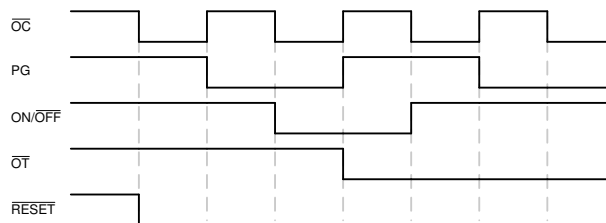
Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

## 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHCT1G14 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ , so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

## 8.2.3 Application Curves



8-2. Application Timing Diagram

## 8.3 Power Supply Recommendations

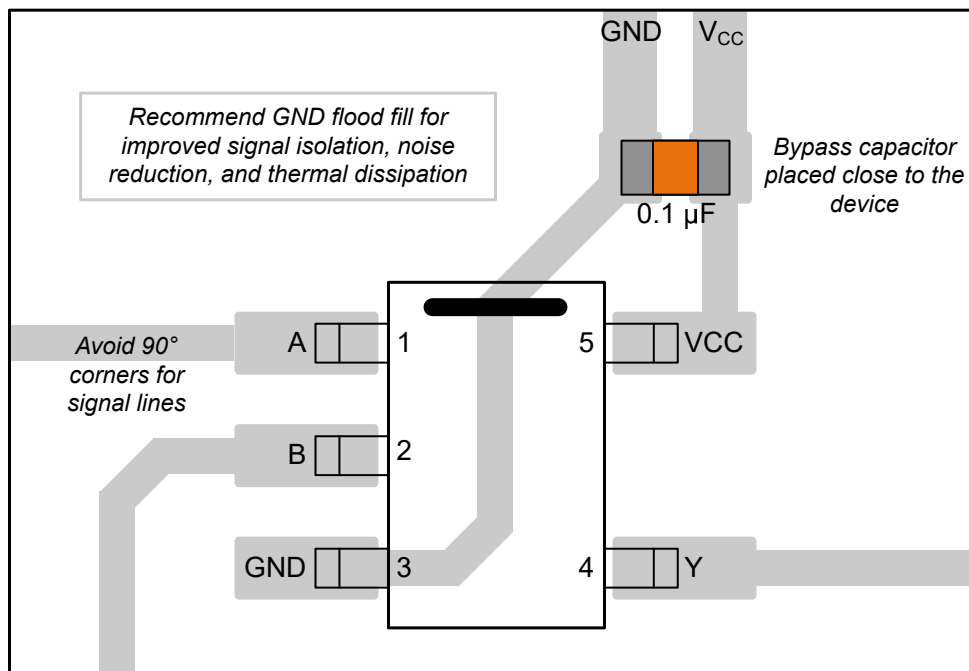
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 8.4.2 Layout Example



✎ 8-3. Example Layout for the SN74AHCT1G14

## 9 Device and Documentation Support

### 9.1 Documentation Support (Analog)

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision Q (October 2023) to Revision R (February 2024) Page

- |   |   |
|---|---|
| • 「パッケージ情報」表に本体サイズを追加 .....                                       | 1 |
| • Updated RθJA values: DBV = 206 to 278, all values in °C/W ..... | 4 |

### Changes from Revision P (June 2013) to Revision Q (October 2023) Page

- |   |   |
|---|---|
| • 「アプリケーション」セクション、「パッケージ情報」の表、「ピン機能」の表、「熱に関する情報」の表、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「アプリケーションと実装」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ..... | 1 |
| • Updated thermal values for DCK package from RθJA = 252 to 289.2, all values in °C/W .....   | 4 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">74AHCT1G14DBVRE4</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(B143, B14G, B14L, B14S)
74AHCT1G14DBVRE4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(B143, B14G, B14L, B14S)
<a href="#">74AHCT1G14DBVRG4</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B14G
74AHCT1G14DBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B14G
74AHCT1G14DBVTE4	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B14G
74AHCT1G14DBVTG4.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B14G
74AHCT1G14DCKTE4	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BF3
<a href="#">74AHCT1G14DCKTG4</a>	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BF3
74AHCT1G14DCKTG4.A	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BF3
<a href="#">SN74AHCT1G14DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(36DH, 3CAF, B143, B14G, B14J, B14L, B14S)
SN74AHCT1G14DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(36DH, 3CAF, B143, B14G, B14J, B14L, B14S)
<a href="#">SN74AHCT1G14DBVT</a>	Obsolete	Production	SOT-23 (DBV)   5	-	-	Call TI	Call TI	-40 to 125	(B143, B14G, B14J, B14S)
<a href="#">SN74AHCT1G14DCKR</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QN, BF3, BFG, BFJ, BFL, BFS)
SN74AHCT1G14DCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QN, BF3, BFG, BFJ, BFL, BFS)
SN74AHCT1G14DCKRG4.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BF3
<a href="#">SN74AHCT1G14DCKT</a>	Obsolete	Production	SC70 (DCK)   5	-	-	Call TI	Call TI	-40 to 125	(BF3, BFG, BFJ, BFS)

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74AHCT1G14 :

- Automotive : [SN74AHCT1G14-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G14DBVRE4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G14DBVRE4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G14DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G14DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G14DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G14DBVRE4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G14DBVRE4	SOT-23	DBV	5	3000	202.0	201.0	28.0
74AHCT1G14DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G14DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHCT1G14DCKR	SC70	DCK	5	3000	210.0	185.0	35.0

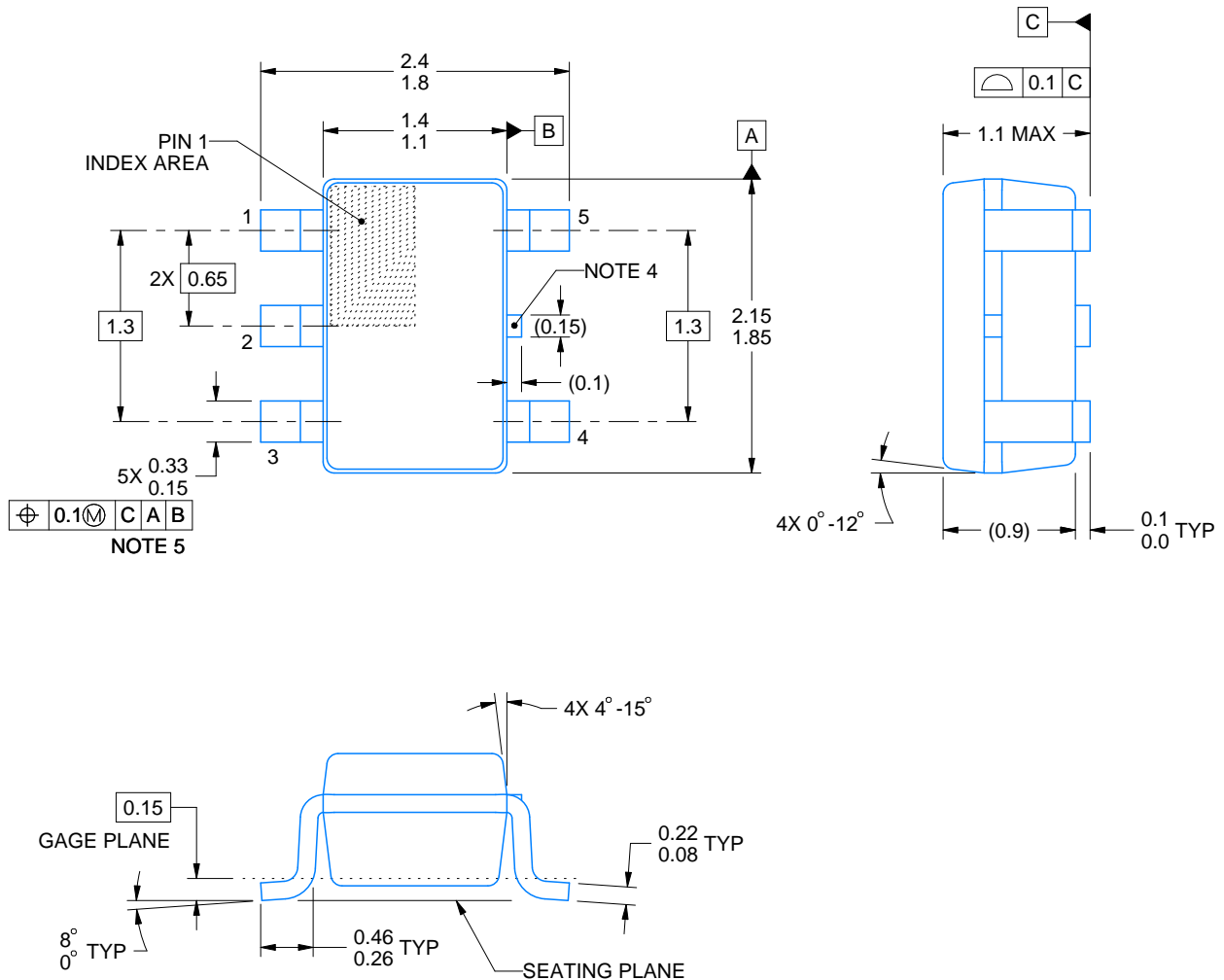
DCK0005A



## PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

### NOTES:

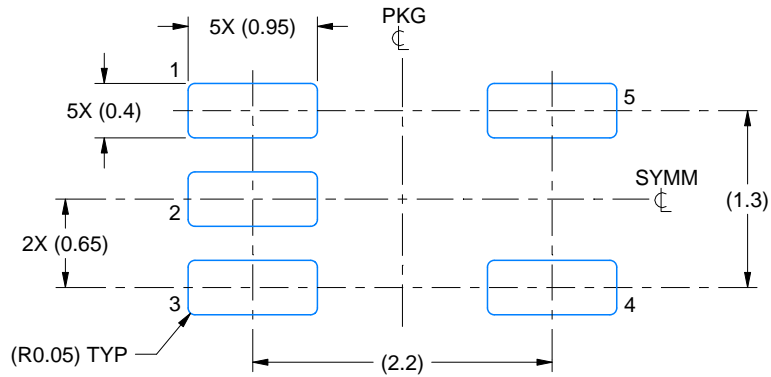
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

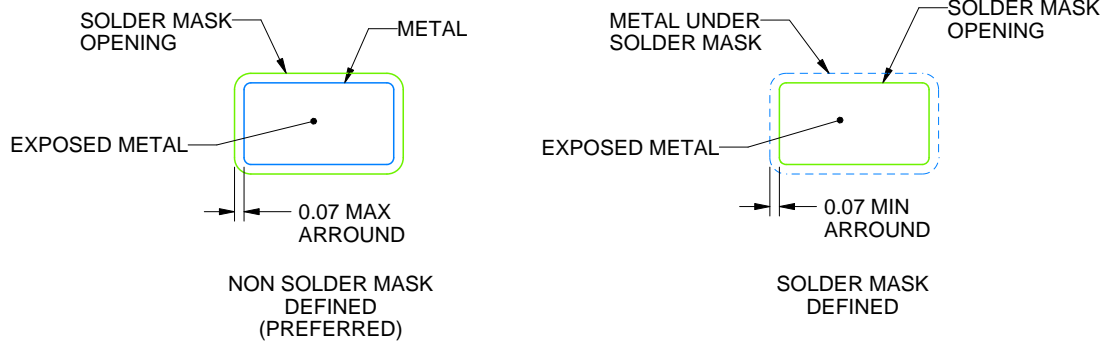
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

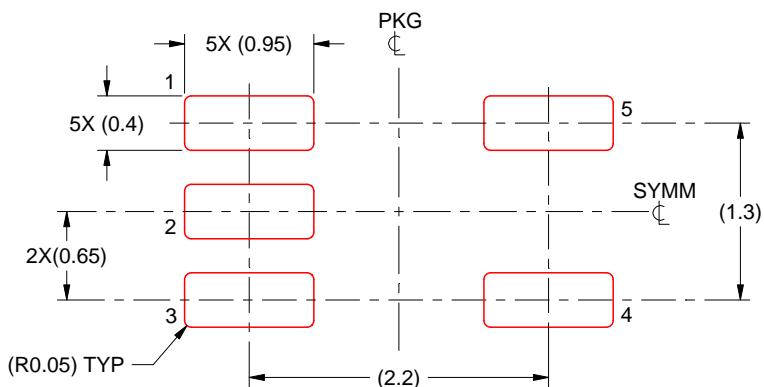


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



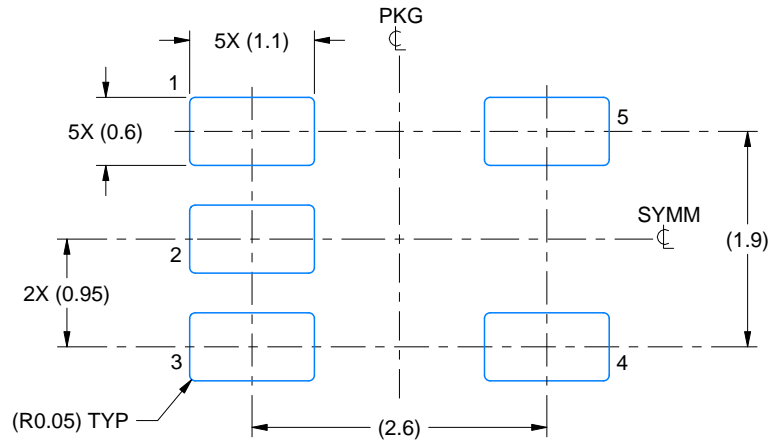
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

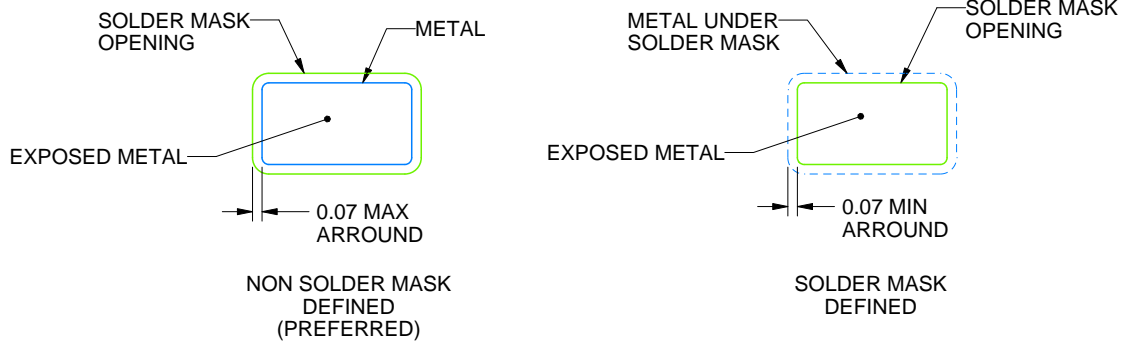
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

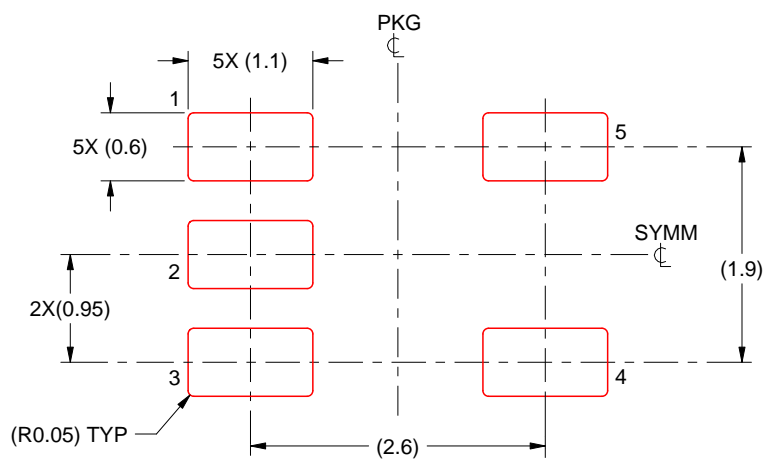
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](https://www.ti.com) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月