

SNx4AHC540 3 ステート出力、オクタール バッファ / ドライバ

1 特長

- 2V~5.5V の V_{CC} で動作
- JESD 17 準拠で 250mA 超のラッチアップ性能
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

2 アプリケーション

- サーバー
- PC およびノートパソコン
- ネットワーク スイッチ
- ウェアラブルなヘルスケア / フィットネス機器
- テレコム インフラストラクチャ
- 電子 POS

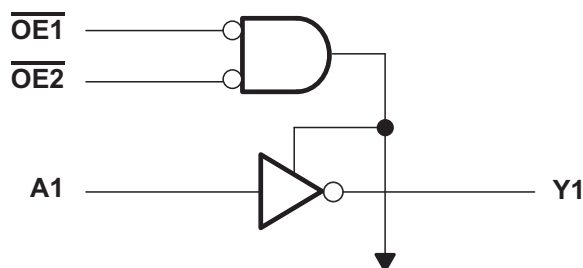
3 概要

SNx4AHC540 オクタール バッファ / ドライバは、バスラインまたはバッファ メモリ アドレス レジスタの駆動に最適です。入力と出力をパッケージの反対側に配置しているため、プリント基板のレイアウトが容易です。

製品情報

部品番号	パッケージ (ピン数) ⁽¹⁾	本体サイズ (公称)
SN74AHC540N	PDIP (20)	25.40mm × 6.35mm
SN74AHC540DB	SSOP (20)	7.50mm × 5.30mm
SN74AHC540PW	TSSOP (20)	6.50mm × 4.40mm
SN74AHC540DGV	TVSOP (20)	5.00mm × 4.40mm
SN74AHC540DW	SOIC (20)	12.80mm × 7.50mm
SNJ54AHC540FK	LCCC (20)	9.0mm × 9.0mm
SNJ54AHC540W	CFP (20)	13.72mm × 8.13mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



To Seven Other Channels
概略回路図



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4 Pin Configuration and Functions

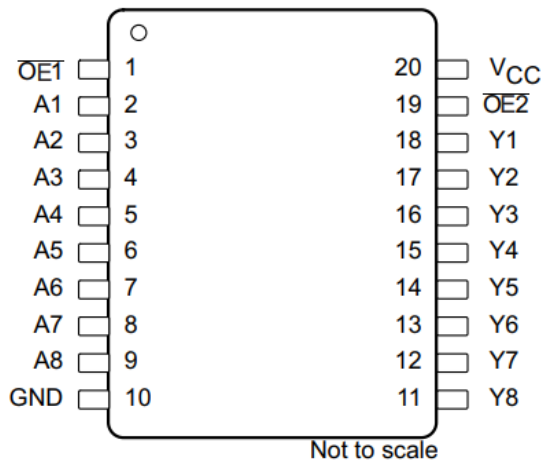


図 4-1. SN54AHC540: J or W Package;
SN74AHC540: DB, DGV, DW, N, NS, or PW Package
SN54AHC540: 20-Pin CDIP or CFP; SN74AHC540:
20-Pin SSOP, TVSOP, SOIC, PDIP, PDIP, or TSSOP
Top View

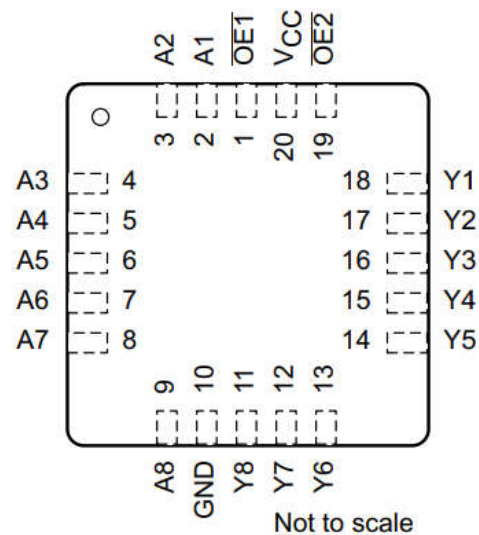


図 4-2. SN54AHC540: FK Package 20-Pin LCCC Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OE1	I	Output Enable 1
2	A1	I	A1 Input
3	A2	I	A2 Input
4	A3	I	A3 Input
5	A4	I	A4 Input
6	A5	I	A5 Input
7	A6	I	A6 Input
8	A7	I	A7 Input
9	A8	I	A8 Input
10	GND	—	Ground
11	Y8	O	Y8 Output
12	Y7	O	Y7 Output
13	Y6	O	Y6 Output
14	Y5	O	Y5 Output
15	Y4	O	Y4 Output
16	Y3	O	Y3 Output
17	Y2	O	Y2 Output
18	Y1	O	Y1 Output
19	OE2	I	Output Enable 2
20	V _{CC}	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	7	V
V _I	Input voltage range ⁽²⁾		−0.5	7	V
V _O	Output voltage range ⁽²⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−20		mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}	±20		mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25		mA
	Continuous current through V _{CC} or GND		±75		mA
T _J	Junction temperature		150		°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54AHC540		SN74AHC540		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 3 V	2.1		2.1		
		V _{CC} = 5.5 V	3.85		3.85		
V _{IL}	Low-level Input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 3 V		0.9		0.9	
		V _{CC} = 5.5 V		1.65		1.65	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		−50		−50	μA
		V _{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V _{CC} = 5 V ± 0.5 V		−8		−8	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 3.3 V ± 0.3 V		4		4	mA
		V _{CC} = 5 V ± 0.5 V		8		8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V _{CC} = 5 V ± 0.5 V		20		20	
T _A	Operating free-air temperature		−55	125	−40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC540						UNIT
		DB (SSOP)	DGV (TVSOP)	DW (SOIC)	N (PDIP)	NS (PDIP)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	99.9	119.2	81.1	54.9	80.4	116.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	61.7	34.5	48.9	41.7	46.9	58.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	55.2	60.7	53.8	35.8	47.9	78.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	22.6	1.2	19.5	27.9	19.9	12.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	54.8	60.0	53.1	35.7	47.5	77.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC540		SN74AHC540		–40°C to 125°C SN74AHC540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	2 V	1.9	2		1.9		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	I _{OH} = –4 mA	3 V	2.58			2.48		2.48		2.48		
	I _{OH} = –8 mA	4.5 V	3.94			3.8		3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1		0.1	
	I _{OH} = 4 mA	3 V			0.36		0.5		0.44		0.44	
	I _{OH} = 8 mA	4.5 V			0.36		0.5		0.44		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 ⁽¹⁾		±1		±1	μA
I _{OZ} ⁽²⁾	V _O = V _{CC} or GND V _I (OE) = V _{IL} or V _{IH}	5.5 V			±0.25		±2.5		±2.5		±2.5	μA
I _{CC}	V _I = V _{CC} or GND I _O = 0	5.5 V			4		40		40		40	μA
C _i	V _I = V _{CC} or GND	5 V		2	10				10			pF
C _O	V _O = V _{CC} or GND	5 V		4								pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) For input and output pins, I_{OZ} includes the input leakage current.

5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		SN54AHC540		SN74AHC540		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$ SN74AHC540		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	4.8 ⁽¹⁾	7 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	9.5	ns
t_{PHL}				4.8 ⁽¹⁾	7 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	9.5	
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$	6.8 ⁽¹⁾	10.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	1	13.5	ns
t_{PZL}				6.8 ⁽¹⁾	10.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	1	13.5	
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$	6.8 ⁽¹⁾	10.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	1	13.5	ns
t_{PLZ}				6.8 ⁽¹⁾	10.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	1	13.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	7.3	10.5	1	12	1	12	1	13.5	ns
t_{PHL}				7.3	10.5	1	12	1	12	1	13.5	
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$	8	14	1	16	1	16	1	17	ns
t_{PZL}				8	14	1	16	1	16	1	17	
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$	8	15.4	1	17.5	1	17.5	1	18.5	ns
t_{PLZ}				8	15.4	1	17.5	1	17.5	1	18.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1.5 ⁽²⁾				1.5			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		SN54AHC540		SN74AHC540		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$ SN74AHC540		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.7 ⁽¹⁾	5 ⁽¹⁾	1 ⁽¹⁾	6 ⁽¹⁾	1	6	1	7	ns
t_{PHL}				3.7 ⁽¹⁾	5 ⁽¹⁾	1 ⁽¹⁾	6 ⁽¹⁾	1	6	1	7	
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$	4.7 ⁽¹⁾	7.2 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	9.5	ns
t_{PZL}				4.7 ⁽¹⁾	7.2 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	9.5	
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$	4.5 ⁽¹⁾	6.8 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	8.5	ns
t_{PLZ}				4.5 ⁽¹⁾	6.8 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	8.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.2	7	1	8	1	8	1	9	ns
t_{PHL}				5.2	7	1	8	1	8	1	9	
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$	6.2	9.2	1	10.5	1	10.5	1	11.5	ns
t_{PZL}				6.2	9.2	1	10.5	1	10.5	1	11.5	
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$	6	8.8	1	10	1	10	1	10.5	ns
t_{PLZ}				6	8.8	1	10	1	10	1	10.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1 ⁽²⁾				1			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		SN74AHC540		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	12	pF

5.10 Typical Characteristics

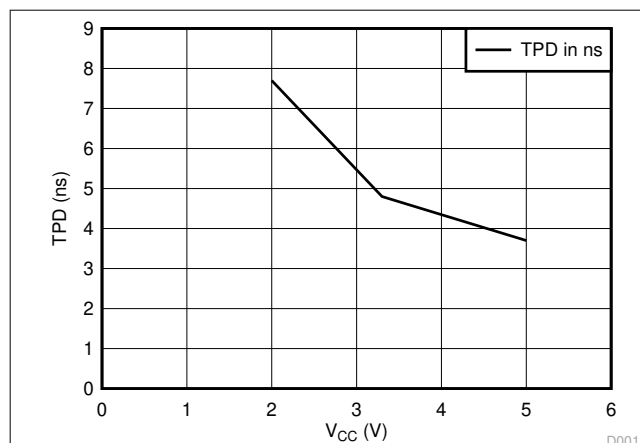


図 5-1. TPD vs V_{CC}

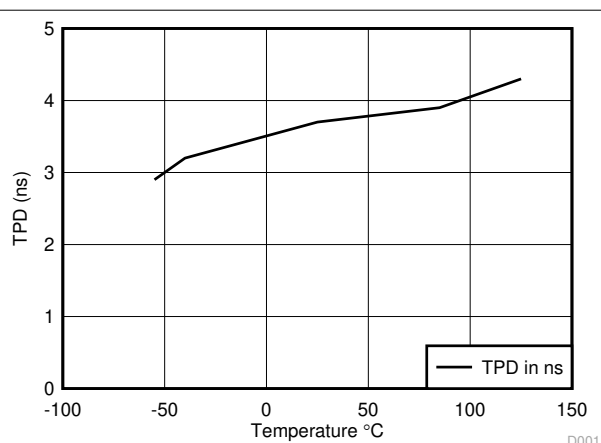
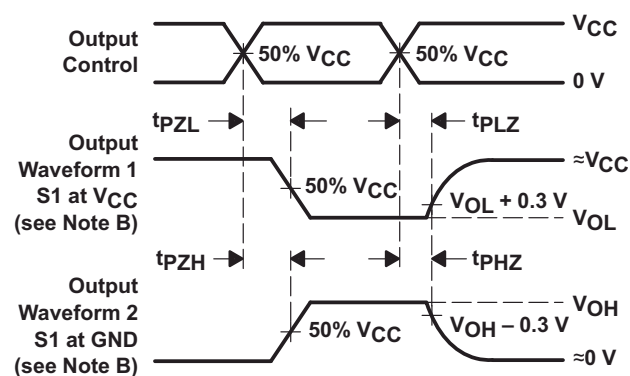
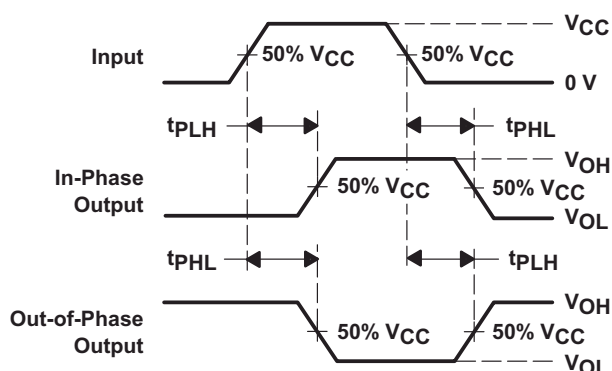
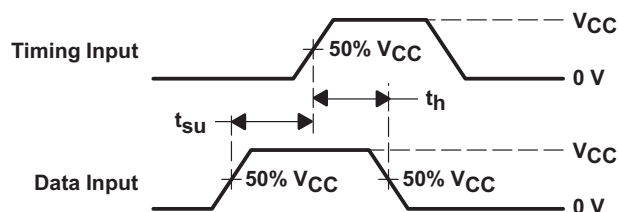
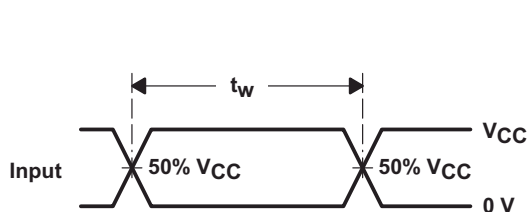
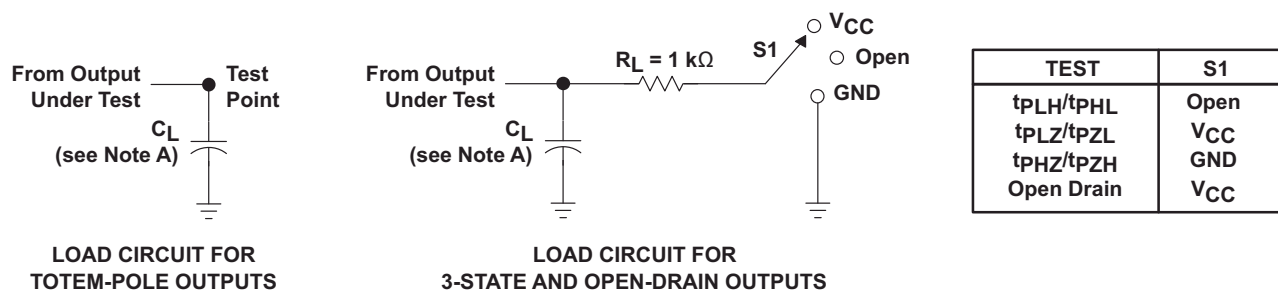


図 5-2. TPD vs Temperature

6 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

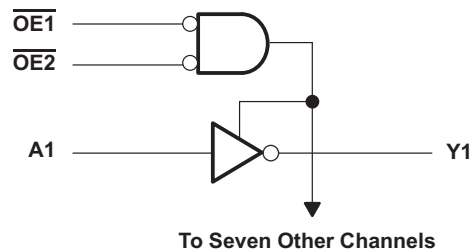
7.1 Overview

The SNx4AHC540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

$\overline{OE}$ should be tied to V_{CC} through a pullup resistor to ensure the high-impedance state during power up or power down. The minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

SNx4AHC540 device has a wide operating voltage range and operates from 2 V to 5.5 V. The inputs accept voltages up to 5.5 V, which allows for down translation. Slow input edges and low drive will minimize output overshoots and undershoots.

7.4 Device Functional Modes

表 7-1 shows the device functions for each buffer and driver.

表 7-1. Function Table (Each Buffer/Driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Hi-Z
X	H	X	Hi-Z

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The SN74AHC540 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V, which allows down translation to the V_{CC} level. 図 8-2 shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

8.2 Typical Application

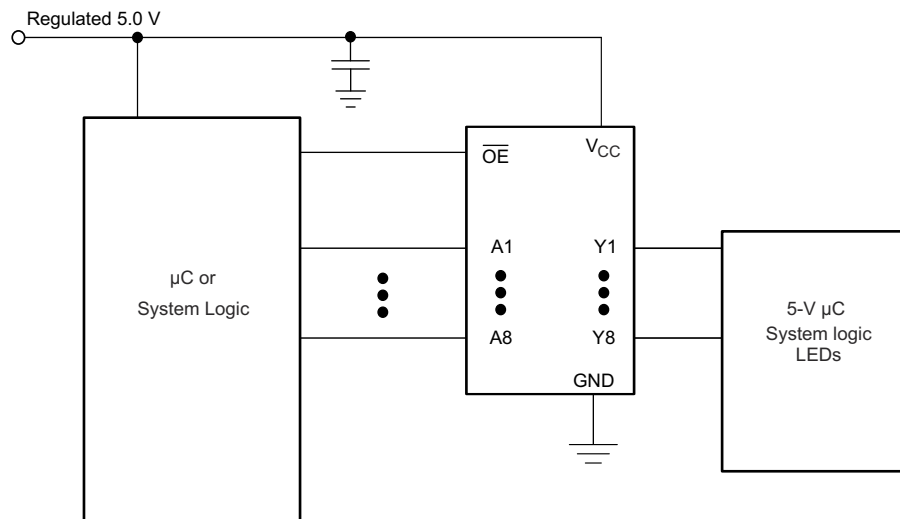


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommended Output Conditions:
 - Load currents should not exceed 25 mA per output and 75 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

8.2.3 Application Curve

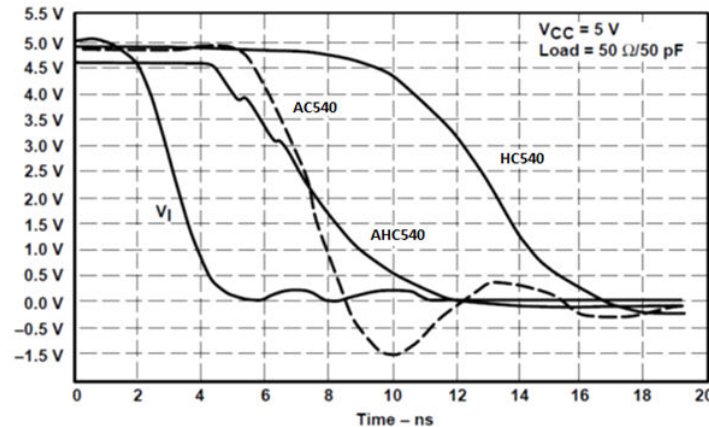


図 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.3.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the [Figure 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4 Layout

8.4.1 Layout Example

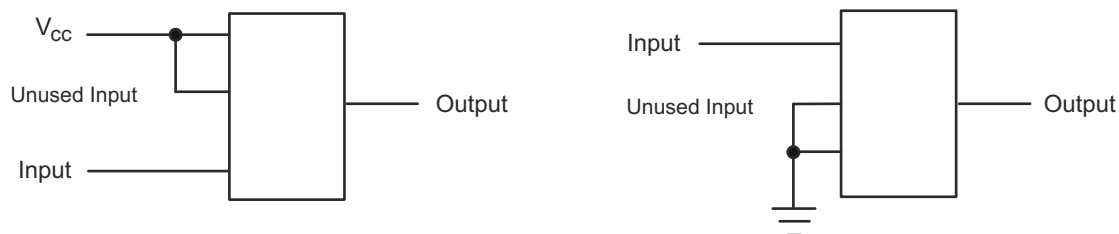


図 8-3. Layout Diagram

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。
[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

[テキサス・インスツルメンツ E2E™ サポート・フォーラム](#) は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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9.3 Trademarks

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9.4 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision N (July 2024) to Revision O (January 2025)	Page
• Updated HBM and CDM values in <i>ESD Ratings</i> table.....	4

Changes from Revision M (May 2016) to Revision N (July 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• Updated RθJA values: PW = 105.4 to 116.8, DW = 83.0 to 81.1; Updated PW and DW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9685001Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9685001Q2A SNJ54AHC 540FK
5962-9685001QSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685001QS A SNJ54AHC540W
SN74AHC540DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540
SN74AHC540DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540
SN74AHC540DGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540
SN74AHC540DGVR.A	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540
SN74AHC540DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	AHC540
SN74AHC540DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC540
SN74AHC540DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC540
SN74AHC540N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC540N
SN74AHC540N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC540N
SN74AHC540PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 125	HA540
SN74AHC540PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540
SN74AHC540PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA540
SNJ54AHC540FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9685001Q2A SNJ54AHC 540FK
SNJ54AHC540FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9685001Q2A SNJ54AHC 540FK
SNJ54AHC540W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685001QS A SNJ54AHC540W
SNJ54AHC540W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685001QS A SNJ54AHC540W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54AHC540, SN74AHC540 :

- Catalog : [SN74AHC540](#)
- Military : [SN54AHC540](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC540DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC540DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC540DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHC540DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC540PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC540PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC540DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AHC540DGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74AHC540DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC540DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC540PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC540PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9685001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9685001QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC540N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC540N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC540FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC540FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC540W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHC540W.A	W	CFP	20	25	506.98	26.16	6220	NA

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

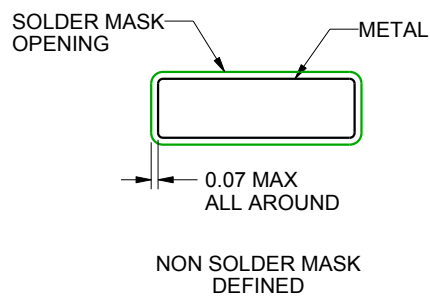
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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