

SN74AHC1G09-Q1 車載用オープン・ドレイン出力のシングル 2 入力正論理 AND ゲート

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - デバイス温度グレード 1:
-40°C~+125°C、T_A
 - デバイス HBM ESD 分類レベル 2
 - デバイス CDM ESD 分類レベル C6
- 2V~5.5V の動作範囲
- 低消費電力、I_{CC} の最大値 10μA
- 最大 t_{pd} 6ns (5V 時)
- 5V で ±8mA の出力駆動能力
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

- パワー・グッド信号の結合
- デジタル信号のイネーブル

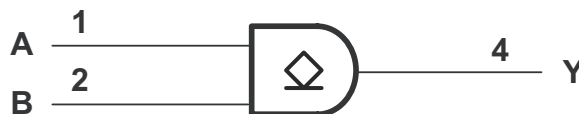
3 概要

SN74AHC1G09-Q1 は、オープン・ドレイン出力構成のシングル 2 入力正論理 AND ゲートです。このデバイスは、ブール関数 $Y = A \times B$ を正論理で実行します。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ・サイズ ⁽²⁾	本体サイズ (公称) ⁽³⁾
SN74AHC1G09-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC70, 5)	2mm × 2.1mm	2mm × 1.25mm

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ×幅) は公称値で、該当する場合はピンも含まれます。
- 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



論理図



Table of Contents

1 特長	1	8.2 Functional Block Diagram.....	8
2 アプリケーション	1	8.3 Feature Description.....	8
3 概要	1	8.4 Device Functional Modes.....	8
4 Revision History	2	9 Application and Implementation	9
5 Pin Configuration and Functions	3	9.1 Application Information.....	9
6 Specifications	4	9.2 Typical Application.....	9
6.1 Absolute Maximum Ratings.....	4	9.3 Power Supply Recommendations.....	10
6.2 ESD Ratings.....	4	9.4 Layout.....	10
6.3 Recommended Operating Conditions.....	4	10 Device and Documentation Support	11
6.4 Thermal Information.....	5	10.1 Documentation Support.....	11
6.5 Electrical Characteristics.....	5	10.2 ドキュメントの更新通知を受け取る方法.....	11
6.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	5	10.3 サポート・リソース.....	11
6.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	5	10.4 Trademarks.....	11
6.8 Operating Characteristics.....	5	10.5 静電気放電に関する注意事項.....	11
6.9 Typical Characteristics.....	6	10.6 用語集.....	11
7 Parameter Measurement Information	7	11 Mechanical, Packaging, and Orderable Information	11
8 Detailed Description	8		
8.1 Overview.....	8		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2023) to Revision A (October 2023)	Page
• データシート全体にわたって DBV パッケージ情報を追加.....	1

5 Pin Configuration and Functions

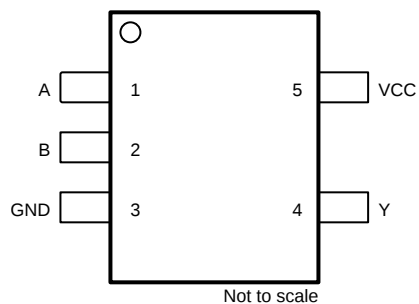


図 5-1. DBV or DCK Package, 5-Pin SOT-23 or SC70 (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
A	1	I	Input
B	2	I	Input
GND	3	—	Ground
V _{CC}	5	—	Power pin
Y	4	O	Output

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	−0.5	7	V
V _I	Input voltage ⁽²⁾	−0.5	7	V
V _O	Output voltage ⁽²⁾	−0.5	V _{CC} + 0.7	V
I _{IK}	Input clamp current (V _I < 0)	−20		mA
I _{OK}	Output clamp current (V _O < 0 or V _O > V _{CC})	−20		mA
I _O	Continuous output current (V _O = 0 to V _{CC})	−25	+25	mA
	Continuous current through V _{CC} or GND	−50	+50	mA
T _J	Maximum junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 3 V	2.1	
		V _{CC} = 5.5 V	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 3 V	0.9	
		V _{CC} = 5.5 V	1.65	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	5.5	V
I _{OL}	Low-level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 3.3 V ± 0.3 V	4	mA
		V _{CC} = 5 V ± 0.5 V	8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	ns/V
		V _{CC} = 5 V ± 0.5 V	20	
T _A	Operating free-air temperature	−40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC1G09-Q1		UNIT
		DCK (SC70)	DBV (SOT-23)	
		5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	293.4	278.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	208.8	180.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	180.6	184.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	120.6	115.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	179.5	183.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OL}	I _{OL} = 50 μA	2 V to 5 V			0.1			0.1	V
	I _{OL} = 4 mA	3 V			0.36			0.55	
	I _{OL} = 8 mA	4.5 V			0.36			0.55	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1			±2	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			1			20	μA
C _i	V _I = V _{CC} or GND	5 V		4	10			10	pF

6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T _A = 25°C			T _A = –40°C to +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PD}	A or B	Y	C _L = 15 pF		3.6	7	1		8	ns
			C _L = 50 pF		6.5	11	1.5		12.5	ns

6.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

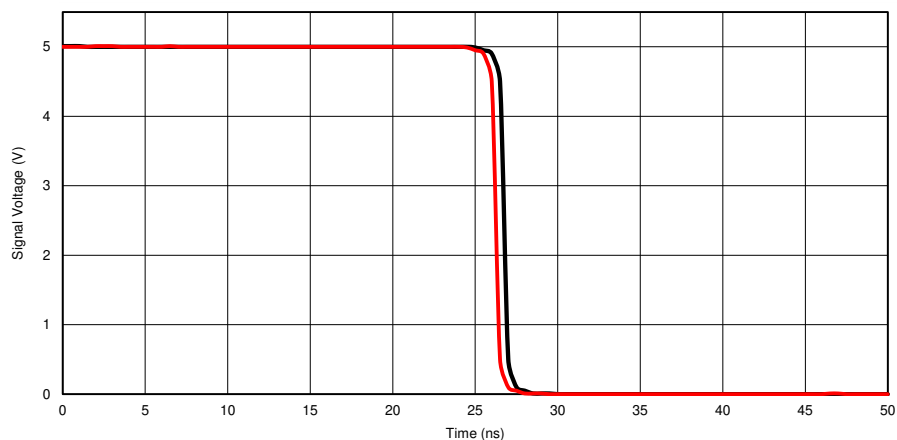
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T _A = 25°C			T _A = –40°C to +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PD}	A or B	Y	C _L = 15 pF		2.5	5	1		6.5	ns
			C _L = 50 pF		4.6	7.5	1.5		8.5	ns

6.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

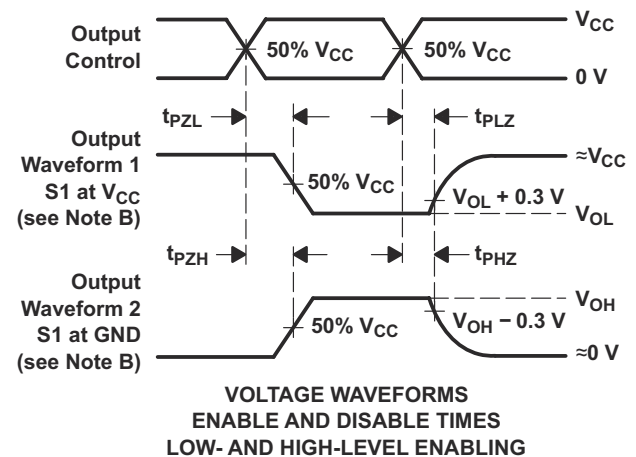
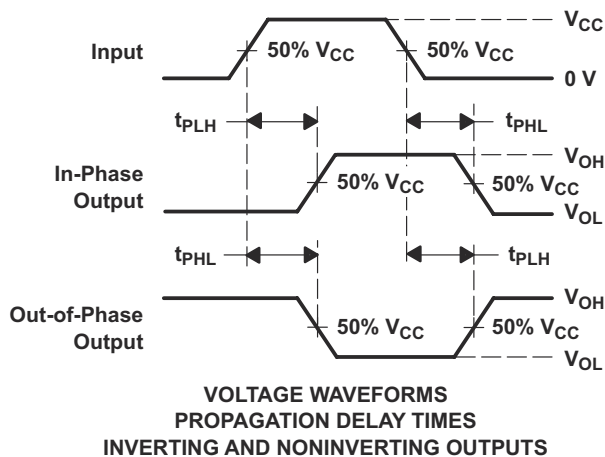
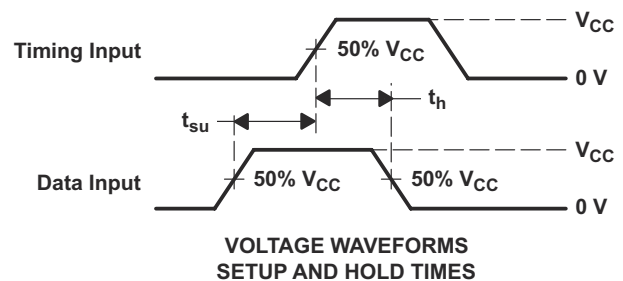
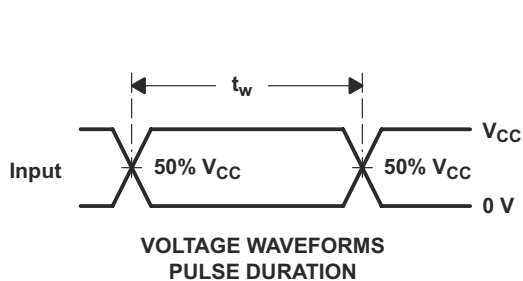
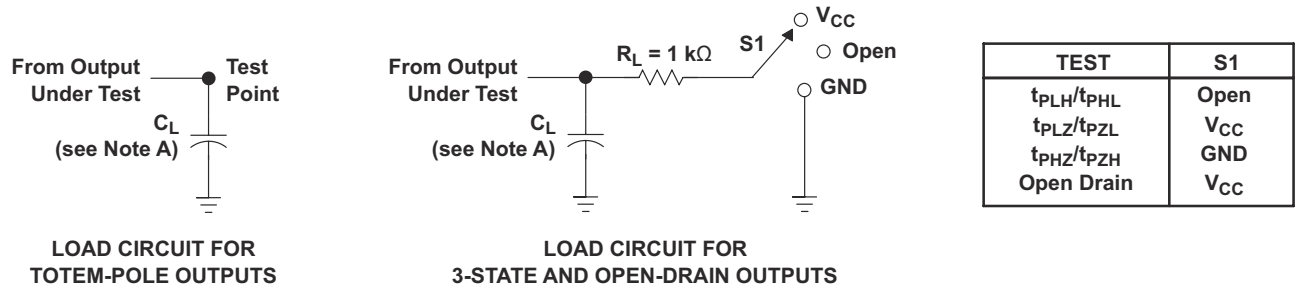
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance No load, f = 1 MHz	5	pF

6.9 Typical Characteristics



6-1. TPD Across V_{CC} at 25°C

7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.
- F. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{PD} .
- G. t_{PZL} is measured at $V_{CC}/2$.
- H. t_{PLZ} is measured at $V_{OL} + 0.3\text{ V}$.

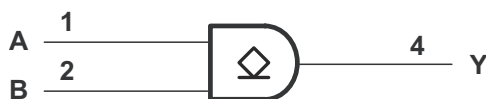
図 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AHC1G09-Q1 device contains one open-drain positive-AND gate with a maximum sink current of 8 mA. A wide operating range of 2 V to 5.5 V enables this device to be used in many different systems, and a low t_{pd} qualifies this device to be used in high-speed applications.

8.2 Functional Block Diagram



8.3 Feature Description

The wide operating voltage range of 2 V to 5 V allows the SN74AHC1G09-Q1 to be used in systems with many different voltage rails. In addition, the voltage tolerance on the output allows the device to be used for inverting up-translation or down-translation. The device is also equipped with Schmitt-trigger inputs, which increase the ability of the device to reject noise.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74AHC1G09-Q1.

表 8-1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	H(Z)
L	X	L
X	L	L

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証テストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74AHC1G09-Q1 is used in the following example in a basic power sequencing configuration. Power sequencing is often used in applications that require a processor or other delicate device with specific voltage timing requirements to protect the device from malfunctioning.

9.2 Typical Application

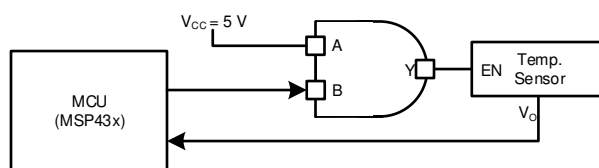


図 9-1. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended Input Conditions:
 - Rise time and fall time specifications. See $(\Delta t/\Delta V)$ in [Recommended Operating Conditions](#).
 - Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in [Recommended Operating Conditions](#).
 - Inputs are overvoltage-tolerant, allowing them to go as high as (V_I) maximum) in [Recommended Operating Conditions](#) at any valid V_{CC} .
- Absolute Maximum Conditions:
 - Load currents should not exceed (I_O) maximum) per output and should not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in [Absolute Maximum Ratings](#).
 - Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves

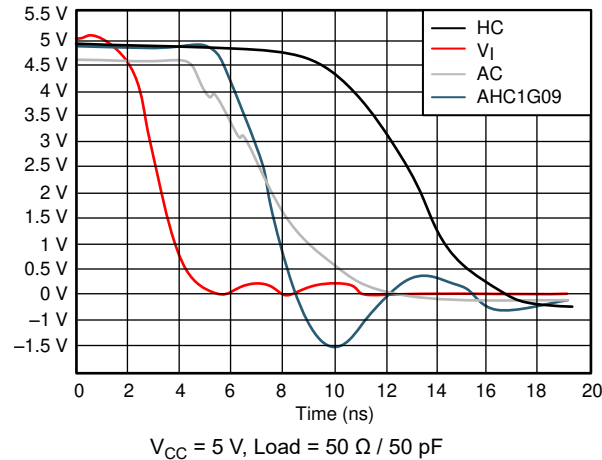


図 9-2. I_{CC} vs Input Voltage

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#).

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a $0.1\text{-}\mu\text{F}$ capacitor is recommended; if there are multiple V_{CC} pins, then a $0.01\text{-}\mu\text{F}$ or $0.022\text{-}\mu\text{F}$ capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. $0.1\text{-}\mu\text{F}$ and $1\text{-}\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used, or only 3 of the 4 buffer gates are used). Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

The following are the rules that must be observed under all circumstances:

- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that should be applied to any particular unused input depends on the function of the device. Generally the unused inputs will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

9.4.2 Layout Example

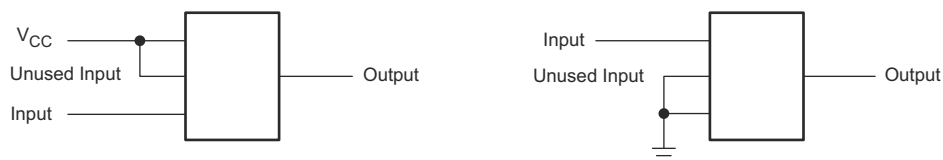


図 9-3. Layout Diagram

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Introduction to Logic application report](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC1G09QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	38RH
SN74AHC1G09QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	38RH
SN74AHC1G09QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P5
SN74AHC1G09QDCKRQ1.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P5

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC1G09-Q1 :

- Catalog : [SN74AHC1G09](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

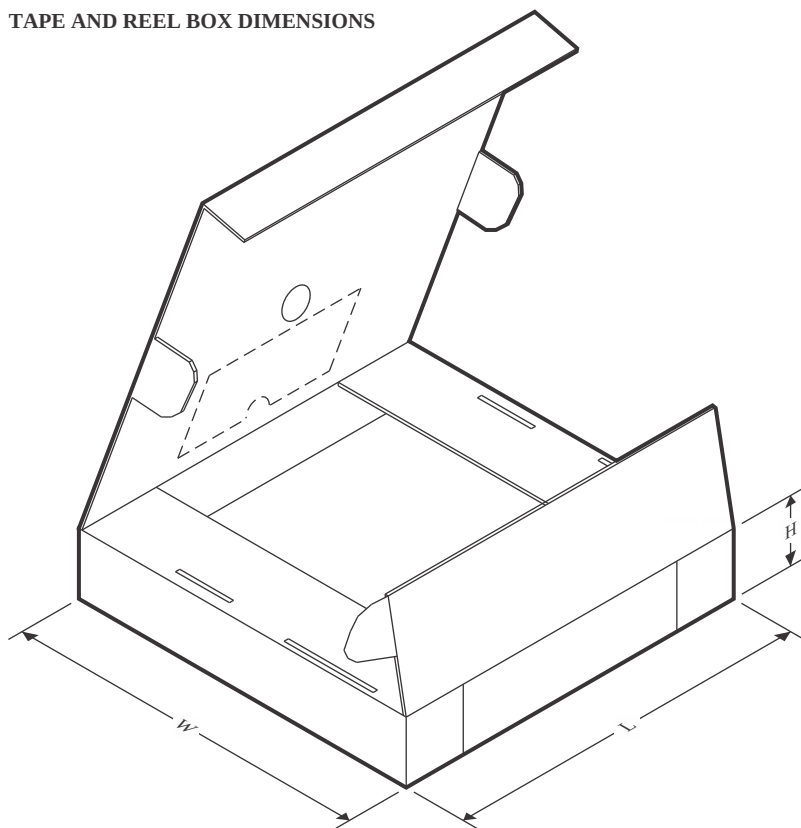
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G09QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G09QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G09QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

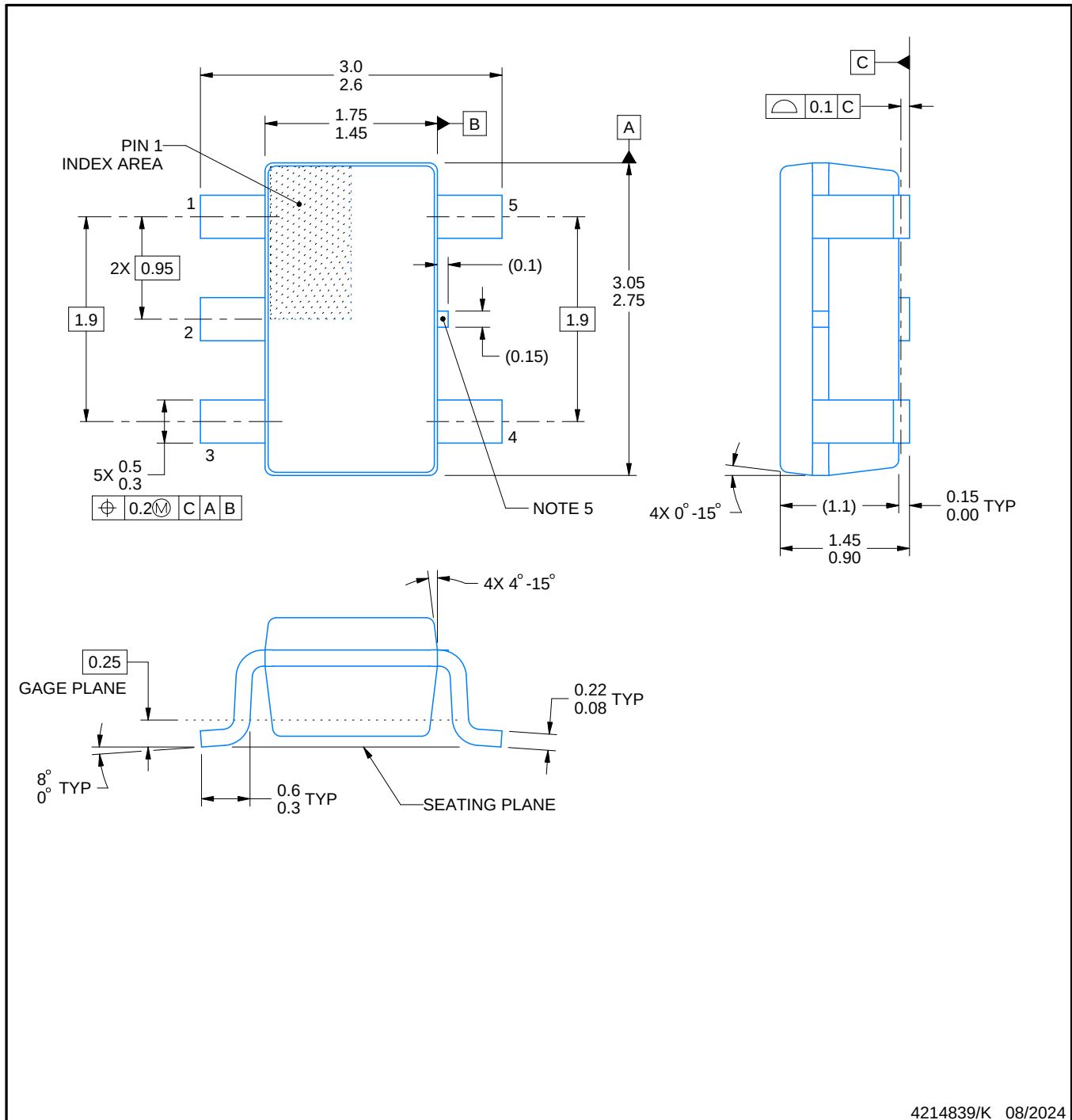


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G09QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G09QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G09QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR

**NOTES:**

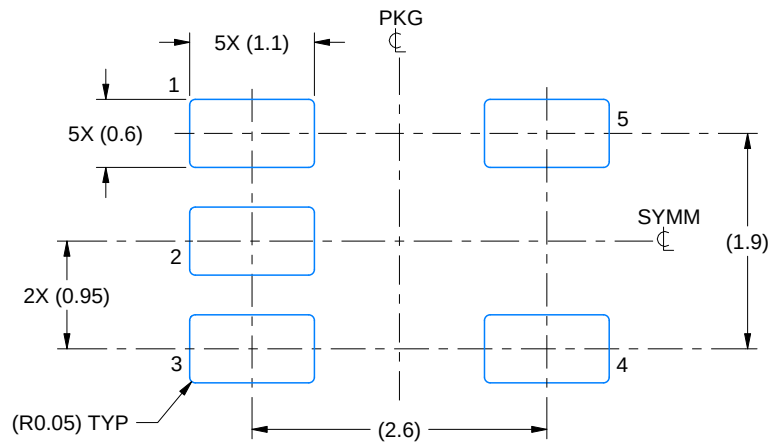
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

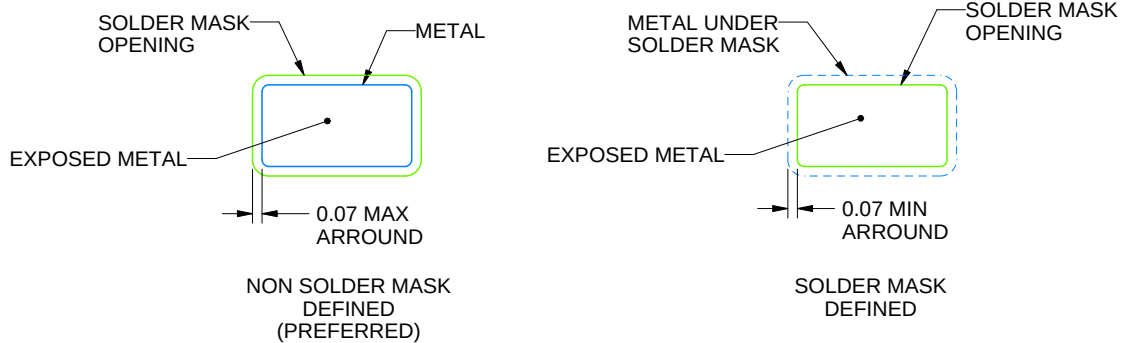
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

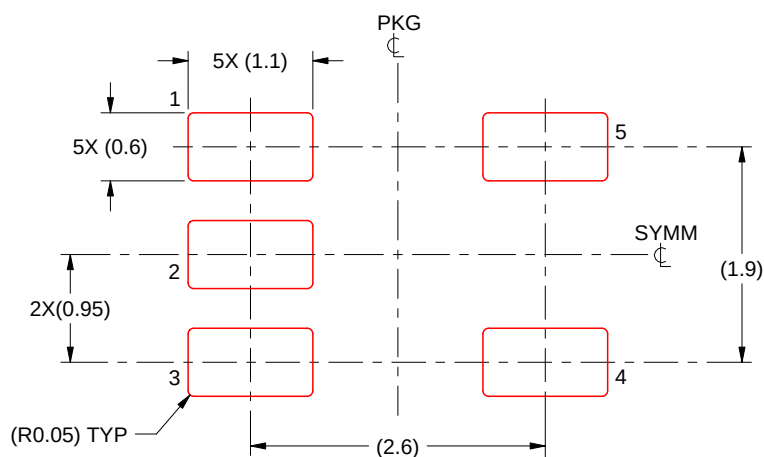
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

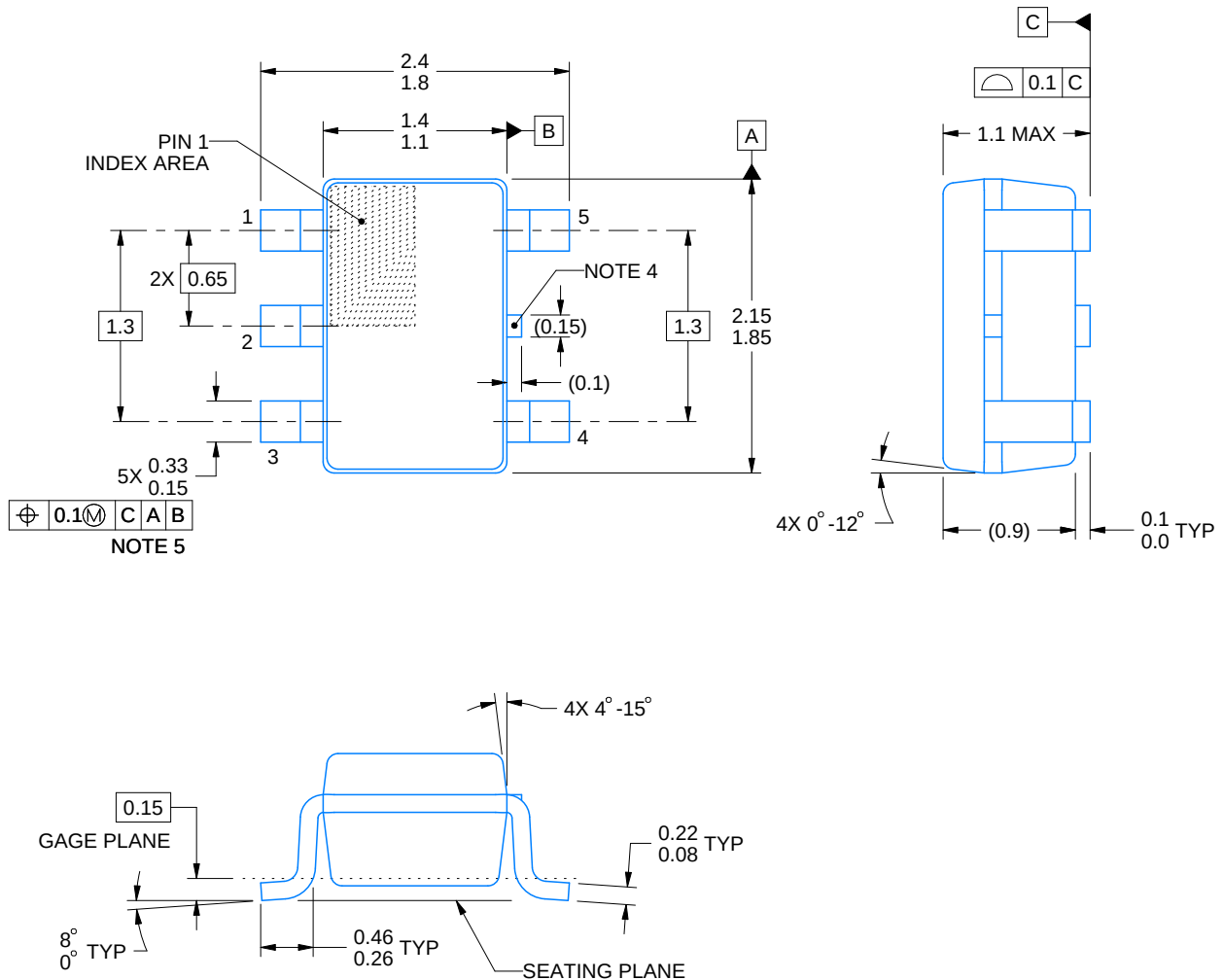


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

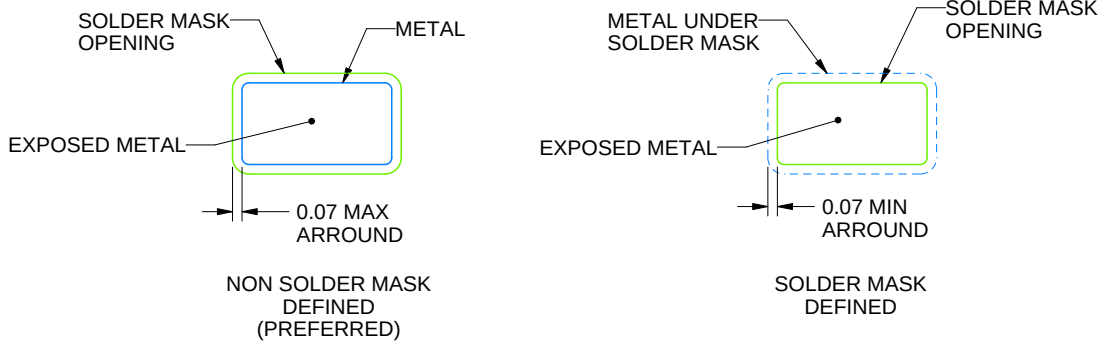
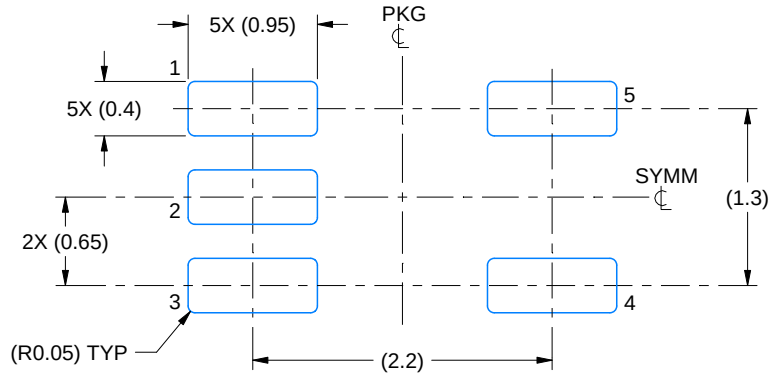
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214834/G 11/2024

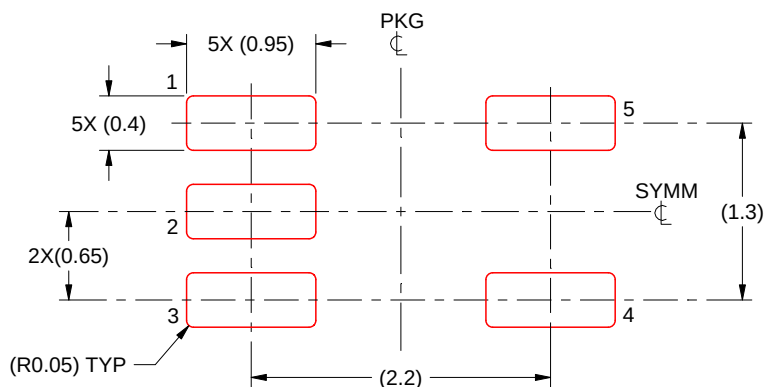
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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