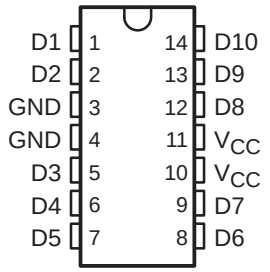
- **Designed to Ensure Defined Voltage Levels on Floating Bus Lines in CMOS Systems**
- **Reduces Undershoot and Overshoot Caused By Line Reflections**
- **Repetitive Peak Forward Current . . . I_{FRM} = 100 mA**
- **Inputs Are TTL-Voltage Compatible**
- **Low Power Consumption (Like CMOS)**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**

D PACKAGE
(TOP VIEW)



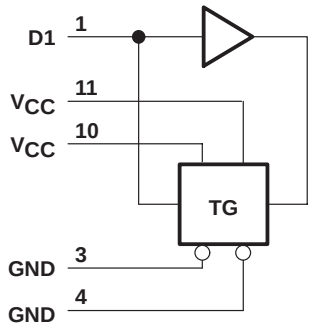
description

This device is designed to terminate bus lines in CMOS systems. The integrated low-impedance diodes clamp the voltage of undershoots and overshoots caused by line reflections and ensure signal integrity. The device also contains a bus-hold function that consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. The SN74ACT1071 prevents bus lines from floating without using pullup or pulldown resistors.

The high-impedance inputs of these internal buffers are connected to the input terminals of the device. The feedback path on each internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver before the bus switches to the high-impedance state.

The SN74ACT1071 is characterized for operation from –40°C to 85°C.

logic diagram, one of ten channels (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Continuous input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Positive-peak input clamp current, I_{IK} (V_I > V_{CC}) (t_w < 1 µs, duty cycle < 20%) . . . . . 100 mA
Negative-peak input clamp current, I_{IK} (V_I < 0) (t_w < 1 µs, duty cycle < 20%) . . . . . –100 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.5		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
T_A	Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TA = 25°C			MIN	MAX	UNIT
			MIN	TYP†	MAX			
I_{IL}	V_{CC} = 4.5 to 5.5 V,	V_I = 0.8 V	0.15	0.3	0.9	0.1	1	mA
I_{IH}	V_{CC} = 4.5 to 5.5 V,	V_I = 2.5 V	–0.2	–0.5	–1.4	–0.15	–1.5	mA
V_{IKL}	I_{IN} = –18 mA				–1.5		–1.5	V
V_{IKH}	I_{IN} = 18 mA				V_{CC}+2		V_{CC}+2	V
I_{CC}‡	V_{CC} = 5.5 V,	Inputs open			4		40	µA
ΔI_{CC}§	One input at 3.4 V,	Other inputs at V_{CC} or GND			0.9		1	mA
C_i	V_I = V_{CC} or GND			3				pF

† All typical values are at V_{CC} = 5 V.
‡ Inputs may be set high or low prior to the I_{CC} measurement.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

TYPICAL CHARACTERISTICS

FORWARD CURRENT vs INPUT VOLTAGE (UPPER CLAMPING DIODE)

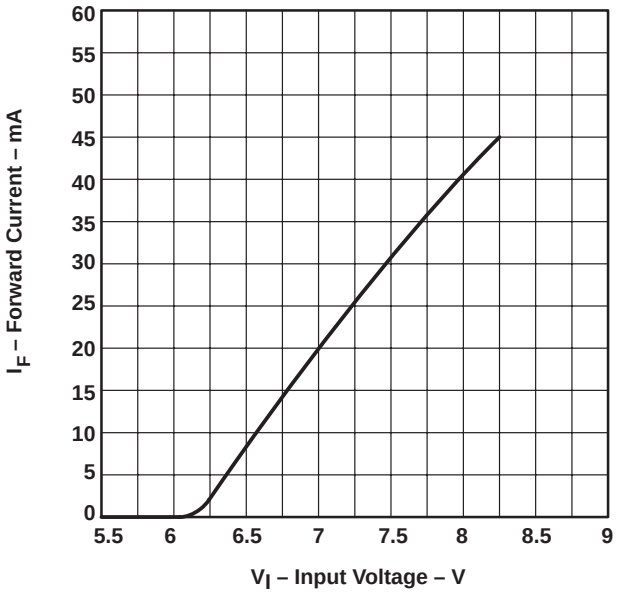


Figure 1

FORWARD CURRENT vs INPUT VOLTAGE (LOWER CLAMPING DIODE)

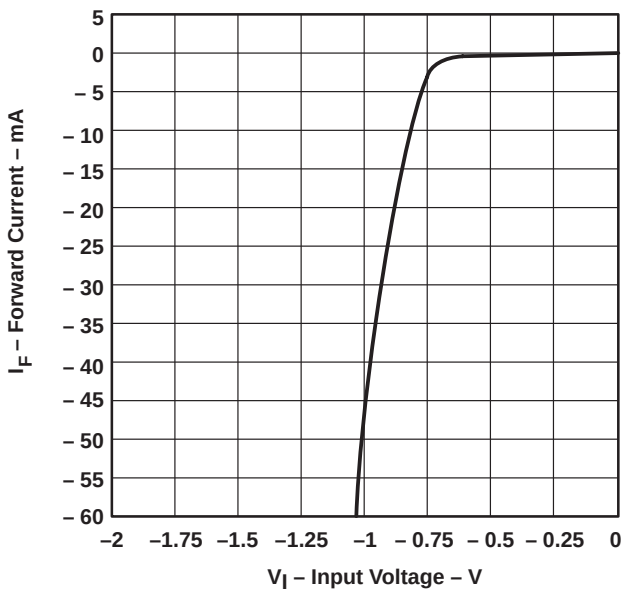


Figure 2

INPUT CURRENT vs INPUT VOLTAGE

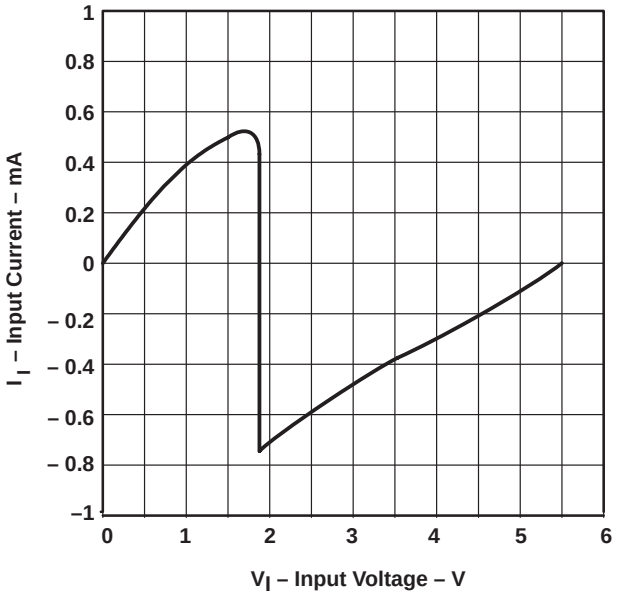


Figure 3

SUPPLY CURRENT vs INPUT VOLTAGE

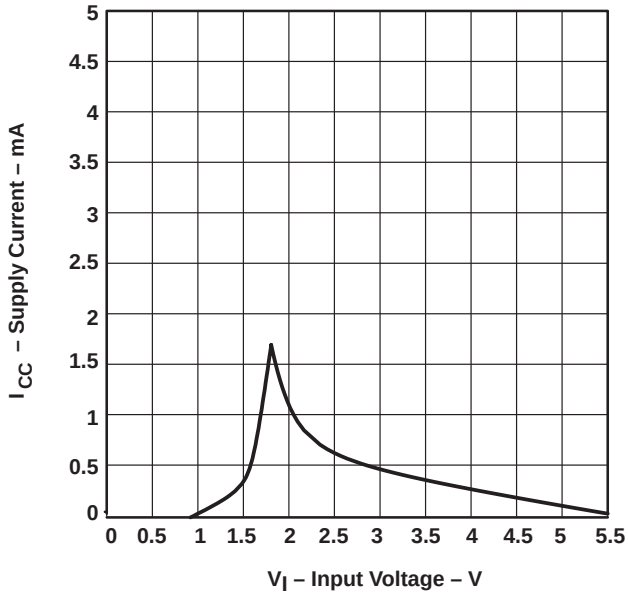


Figure 4

APPLICATION INFORMATION

The SN74ACT1071 terminates the output of a driving device and holds the input of the driven device at the logic level of the driver output prior to establishment of the high-impedance state on that output (see Figure 5).

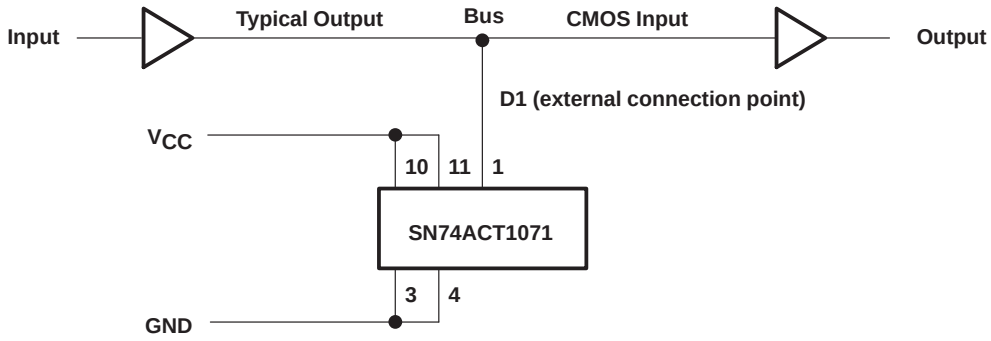


Figure 5. Bus-Hold Application

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ACT1071D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	ACT1071
SN74ACT1071DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT1071
SN74ACT1071DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT1071

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

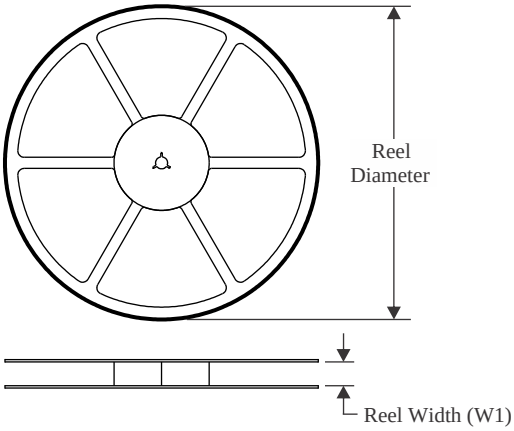
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

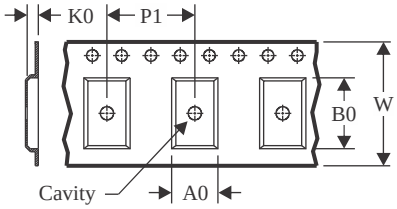
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

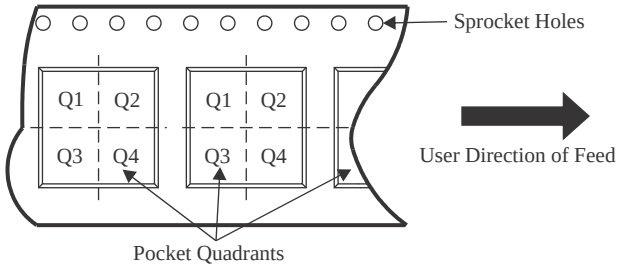


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

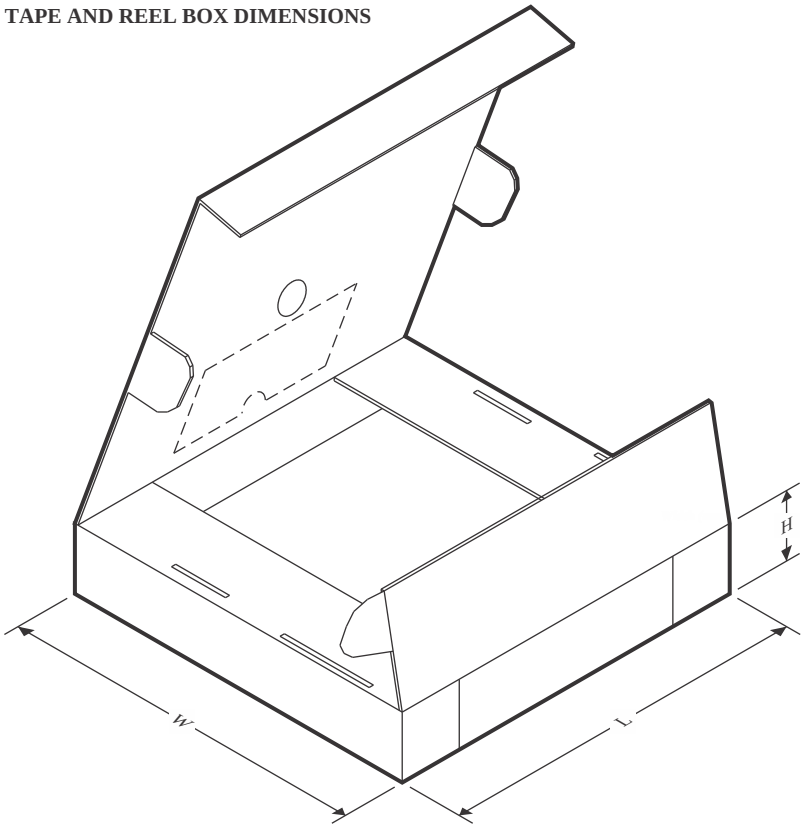
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

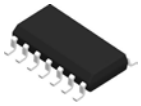
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT1071DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT1071DR	SOIC	D	14	2500	353.0	353.0	32.0

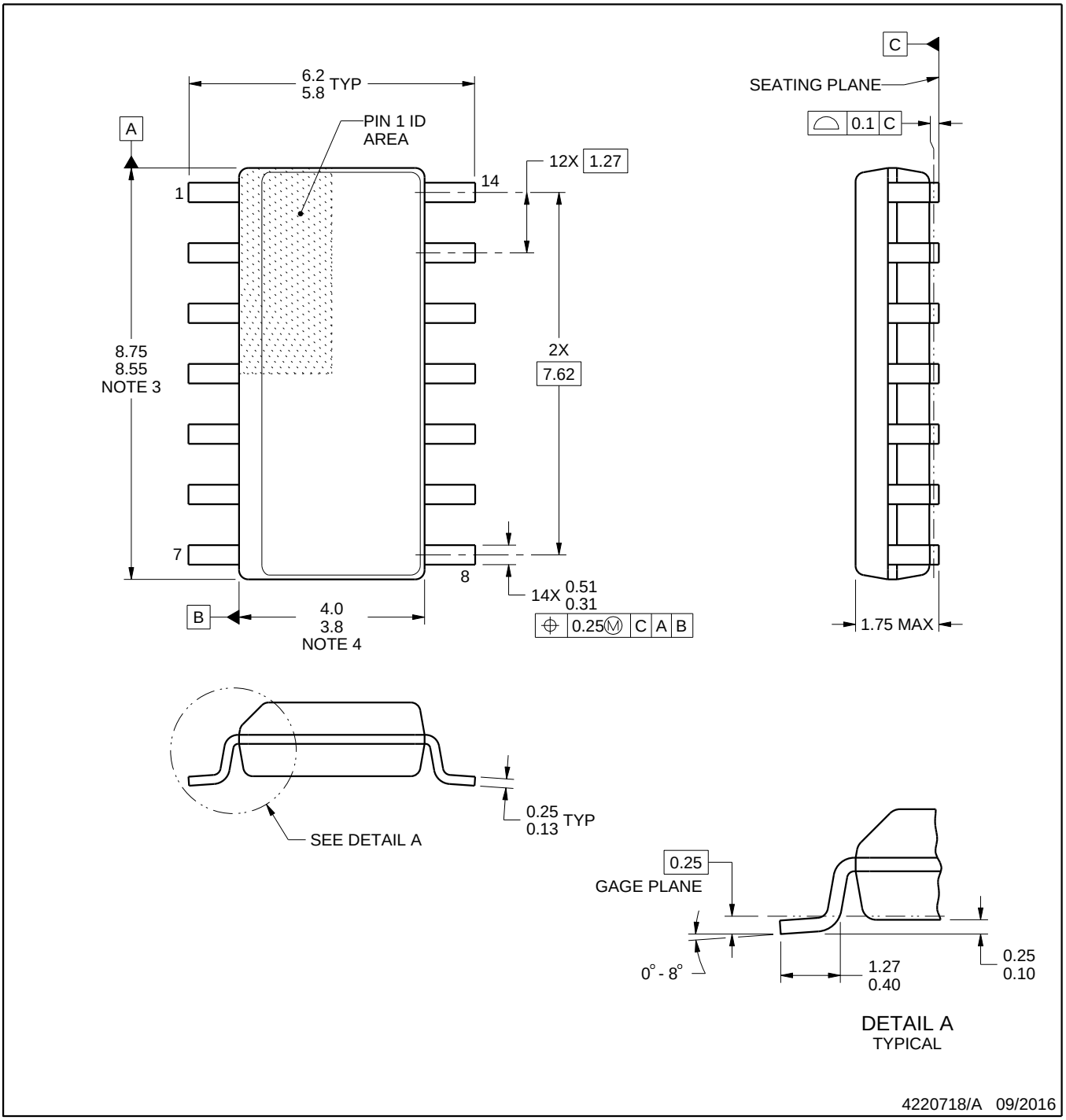


PACKAGE OUTLINE

D0014A

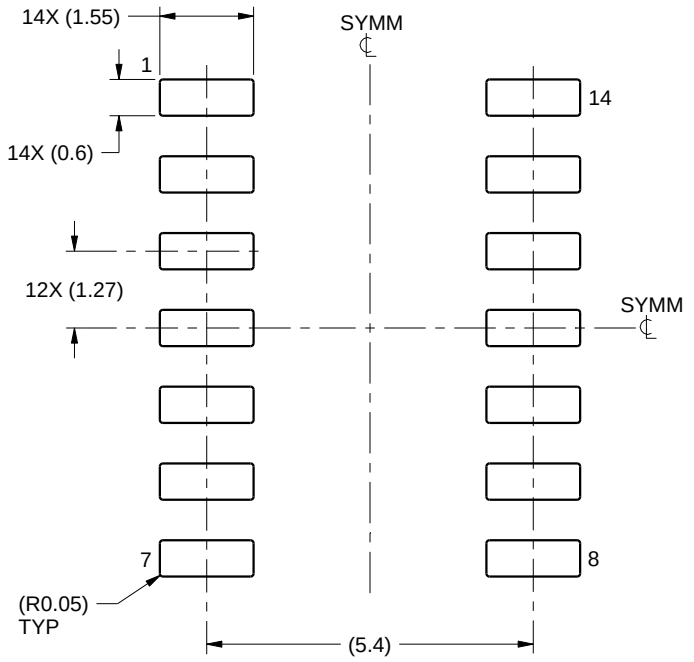
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

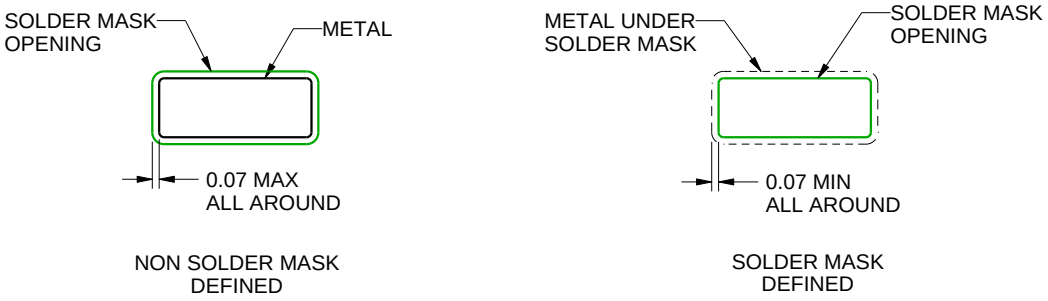


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

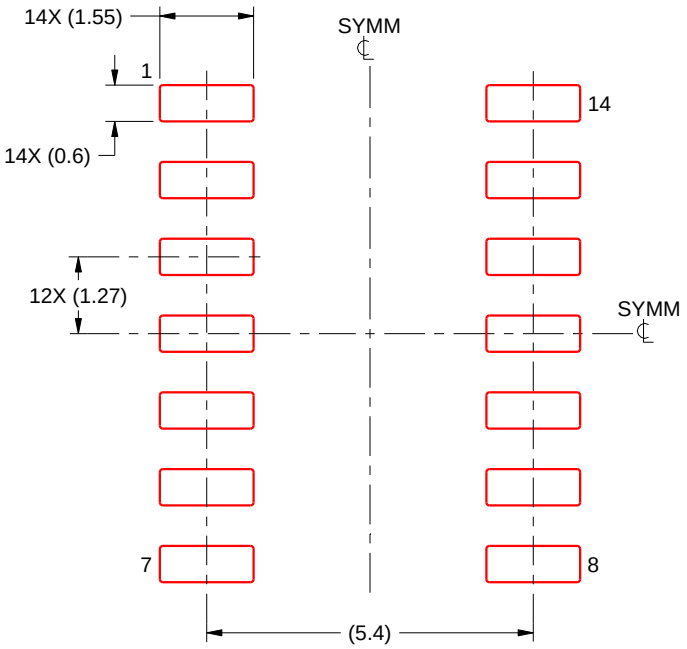
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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