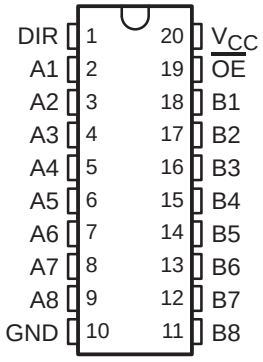
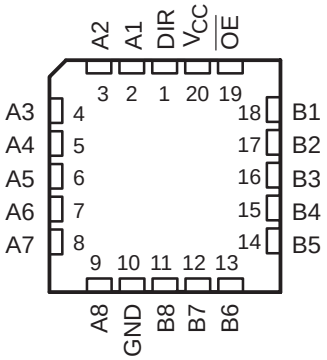
- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package**

SN54ABT2245 . . . J OR W PACKAGE
SN74ABT2245 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT2245 . . . FK PACKAGE
(TOP VIEW)



description

These octal transceivers and line drivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The B-port outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

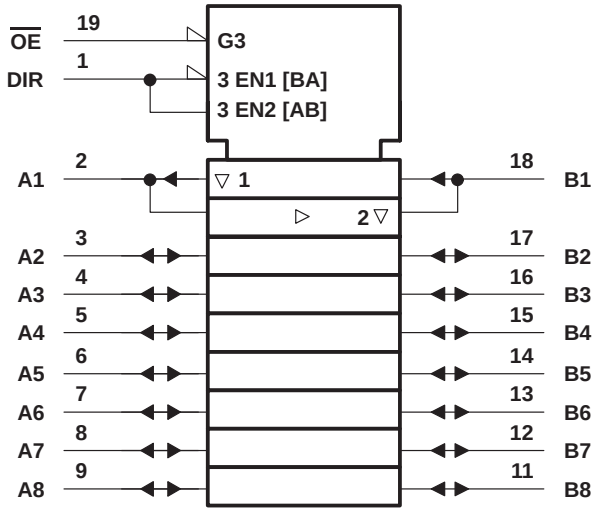
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT2245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

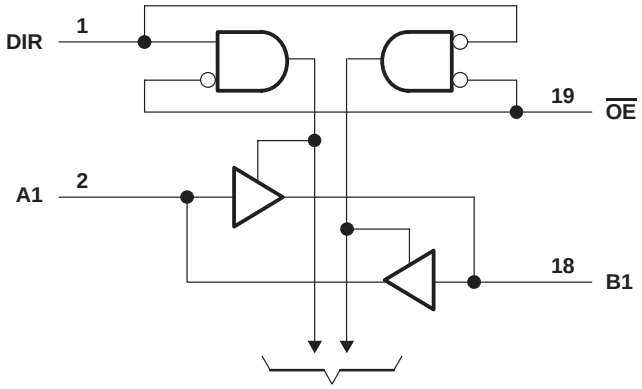
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†

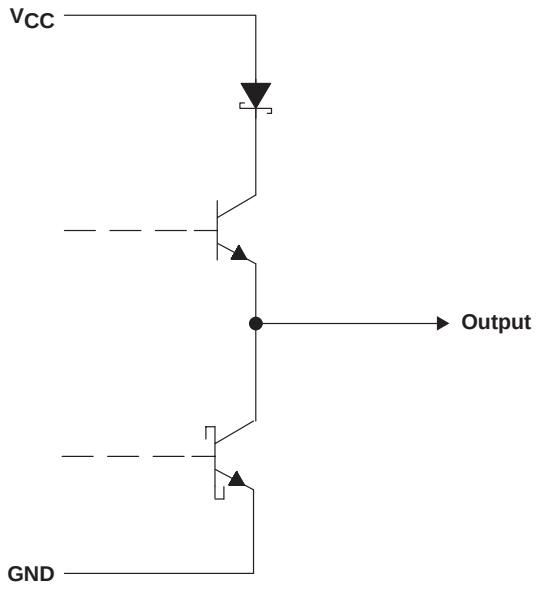


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

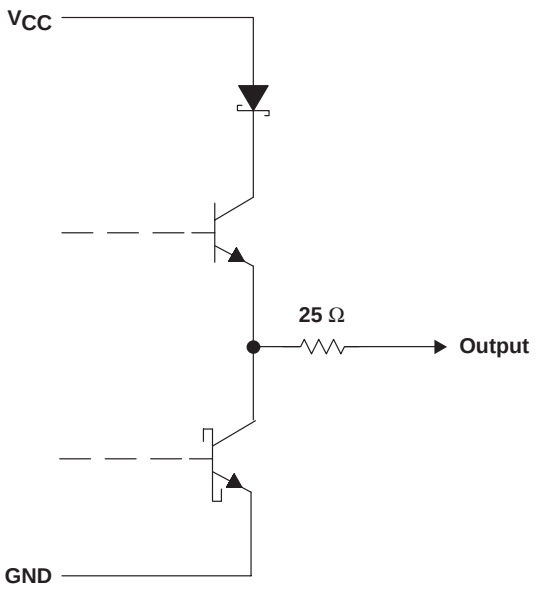
logic diagram (positive logic)



schematic of A-port outputs



schematic of B-port outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT2245 (except B port) . . . . . 96 mA
SN74ABT2245 (except B port) . . . . . 128 mA
B port . . . . . 30 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54ABT2245		SN74ABT2245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		–24		–32	mA
		B port		–12		–12	
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

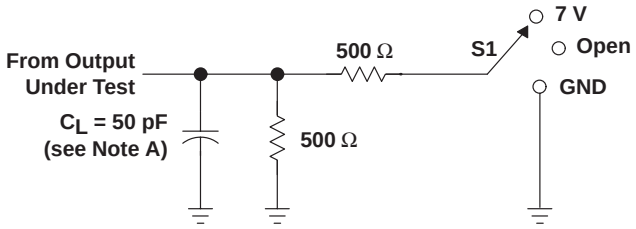
PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT2245		SN74ABT2245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}	B port	V_{CC} = 4.5 V,	I_{OH} = –1 mA	3.35			3.3		3.35		V
		V_{CC} = 5 V,	I_{OH} = –1 mA	3.85			3.8		3.85		
		V_{CC} = 4.5 V	I_{OH} = –3 mA				3		3.1		
			I_{OH} = –12 mA	2.6					2.6		
	A port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5		2.5		
		V_{CC} = 5 V,	I_{OH} = –3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = –24 mA	2			2				
			I_{OH} = –32 mA	2*					2		
V_{OL}	B port	V_{CC} = 4.5 V	I_{OL} = 8 mA			0.65		0.8		0.65	V
			I_{OL} = 12 mA			0.8				0.8	
	A port		I_{OL} = 48 mA			0.55		0.55			
			I_{OL} = 64 mA			0.55*				0.55	
V_{hys}					100						mV
I_I	Control inputs	V_{CC} = 0 to 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
	A or B ports	V_{CC} = 2.1 V to 5.5 V, V_I = V_{CC} or GND				±20		±20		±20	
I_{OZH}‡		V_{CC} = 2.1 V to 5.5 V, V_O = 2.7 V, $\overline{OE}$ ≥ 2 V				10		10		10	µA
I_{OZL}‡		V_{CC} = 2.1 V to 5.5 V, V_O = 0.5 V, $\overline{OE}$ ≥ 2 V				–10		–10		–10	µA
I_{OZPU}§		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50		±50	µA
I_{OZPD}§		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50		±50	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}	Outputs high	V_{CC} = 5.5 V,	V_O = 5.5 V			50		50		50	µA
I_O¶	B port	V_{CC} = 5.5 V,	V_O = 2.5 V	–25		–100	–25	–100	–25	–100	mA
	A port			–50	–100	–180	–50	–180	–50	–180	
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
			Outputs low		24	32		32		32	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	Data inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	
C_i		V_I = 2.5 V or 0.5 V			3						pF
C_{io}		V_O = 2.5 V or 0.5 V			6						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ This parameter is characterized but not production tested.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

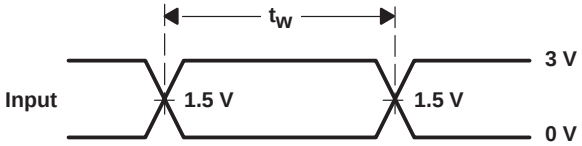
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2245		SN74ABT2245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	2.5	3.4	1	4	1	3.8	ns
t_{PHL}			1	3.2	4.2	1	4.6	1	4.5	
t_{PLH}	B	A	1	2.2	3.2	1	3.8	1	3.6	ns
t_{PHL}			1	2.7	3.6	1	4.2	1	4	
t_{PZH}	$\overline{OE}$	A	1	3.3	4.6	1	5.6	1	5.5	ns
t_{PZL}			1	3.2	4.7	1	6	1	5.7	
t_{PHZ}	$\overline{OE}$	A	2	4	5.1	2	5.7	2	5.6	ns
t_{PLZ}			1	2.9	4	1	4.6	1	4.5	
t_{PZH}	$\overline{OE}$	B	1.5	3.6	4.9	1.5	6.3	1.5	6.1	ns
t_{PZL}			1.5	3.9	5.3	1.5	6.6	1.5	6.3	
t_{PHZ}	$\overline{OE}$	B	1.5	3.6	4.7	1.5	5.5	1.5	5.3	ns
t_{PLZ}			1.5	3.3	4.4	1.5	4.9	1.5	4.8	

PARAMETER MEASUREMENT INFORMATION

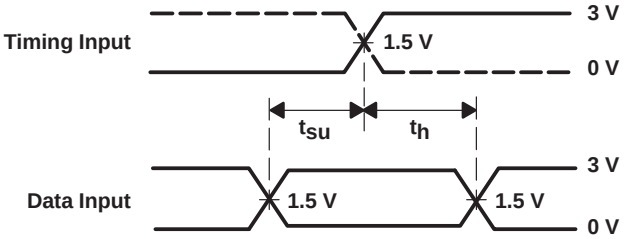


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

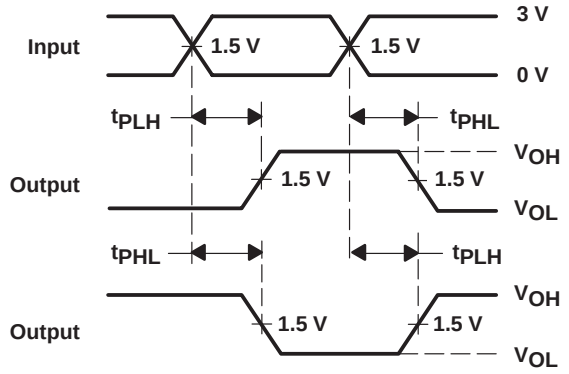
LOAD CIRCUIT



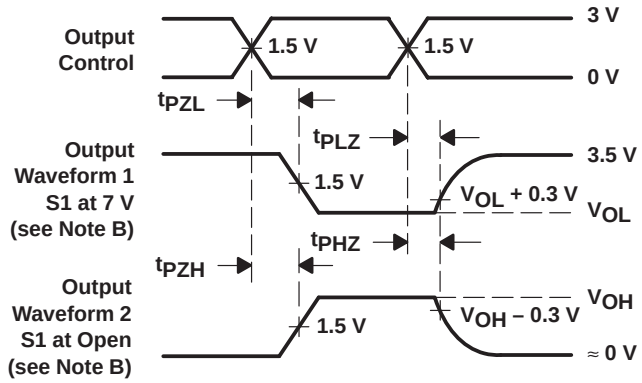
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9560601Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9560601Q2A SNJ54ABT2245FK
5962-9560601QRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9560601QRA SNJ54ABT2245J
5962-9560601QSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9560601QSA SNJ54ABT2245W
SN74ABT2245DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA245
SN74ABT2245DBR.B	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA245
SN74ABT2245DBRG4	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA245
SN74ABT2245DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2245
SN74ABT2245DW.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2245
SN74ABT2245DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2245
SN74ABT2245DWR.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2245
SN74ABT2245N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT2245N
SN74ABT2245N.B	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT2245N
SN74ABT2245PW	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA245
SN74ABT2245PW.B	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA245
SN74ABT2245PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA245
SN74ABT2245PWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA245
SN74ABT2245PWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA245
SN74ABT2245PWRG4.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA245
SNJ54ABT2245FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9560601Q2A SNJ54ABT2245FK
SNJ54ABT2245J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9560601QRA SNJ54ABT2245J

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ABT2245W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9560601QS A SNJ54ABT2245W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54ABT2245, SN74ABT2245 :

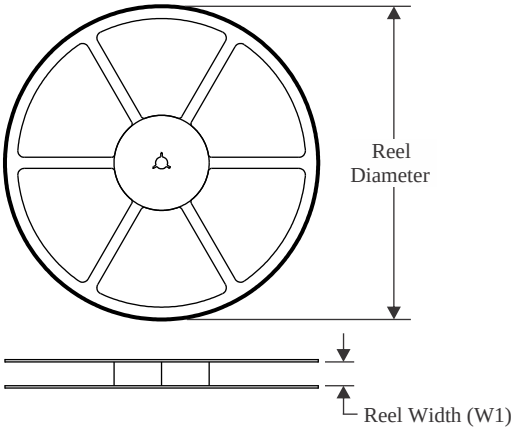
- Catalog : SN74ABT2245
- Military : SN54ABT2245

NOTE: Qualified Version Definitions:

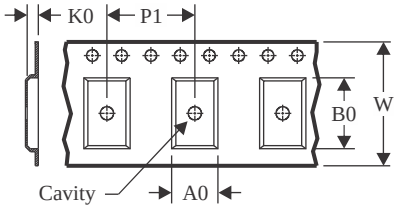
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

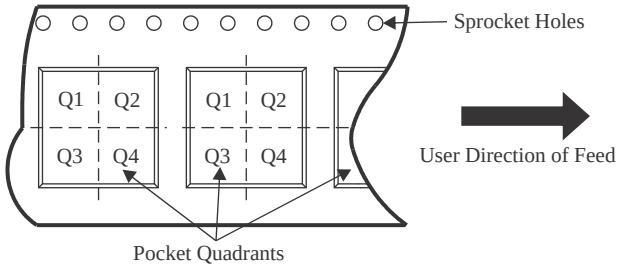


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

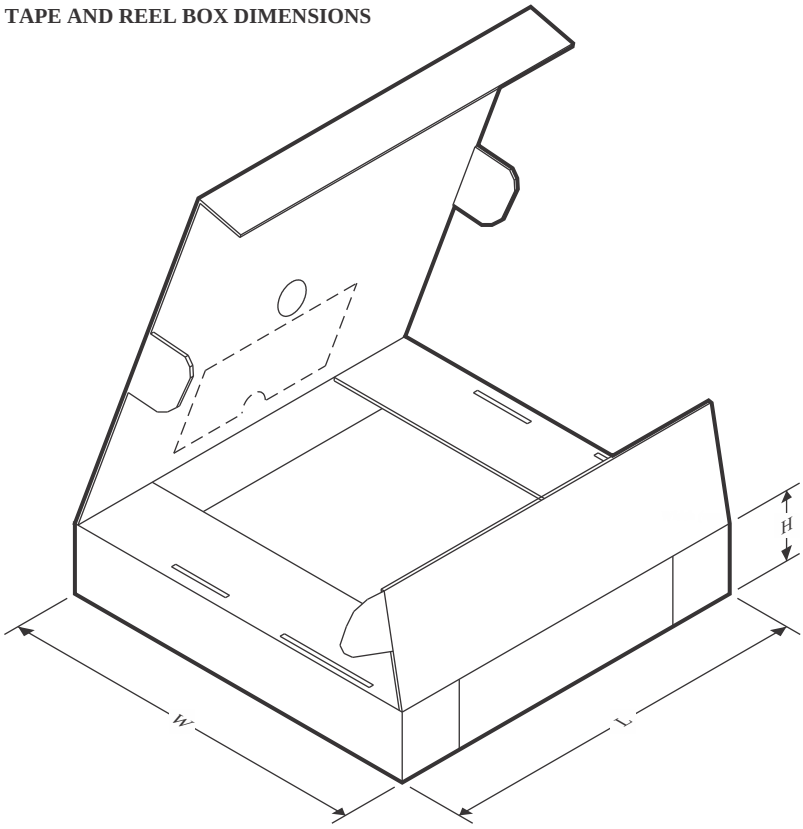
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT2245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT2245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT2245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ABT2245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

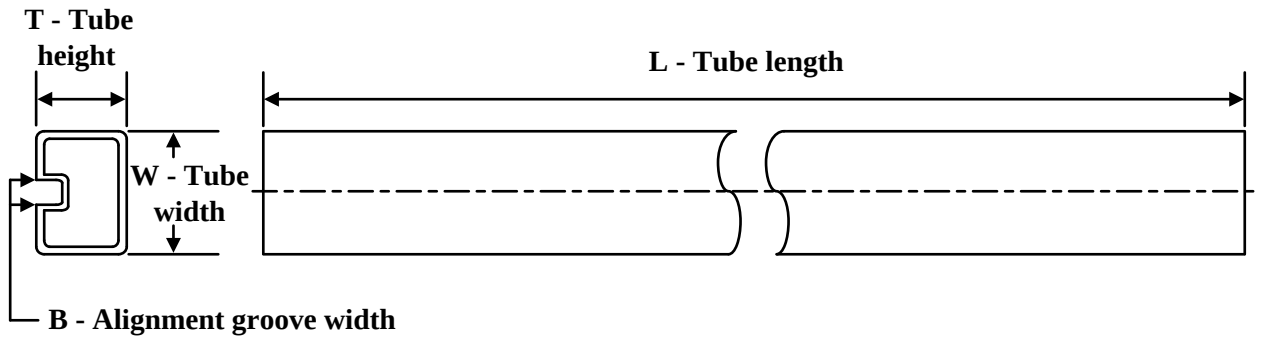
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT2245DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT2245DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ABT2245PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74ABT2245PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



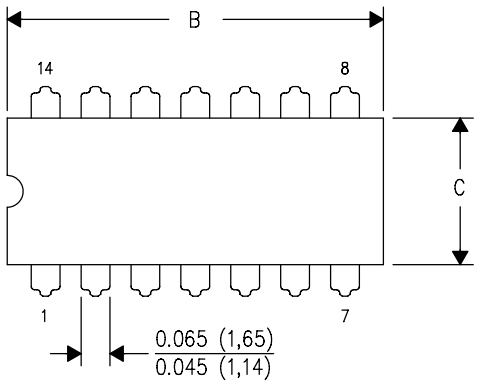
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9560601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9560601QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ABT2245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT2245DW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT2245N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT2245N.B	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT2245PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74ABT2245PW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54ABT2245FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ABT2245W	W	CFP	20	25	506.98	26.16	6220	NA

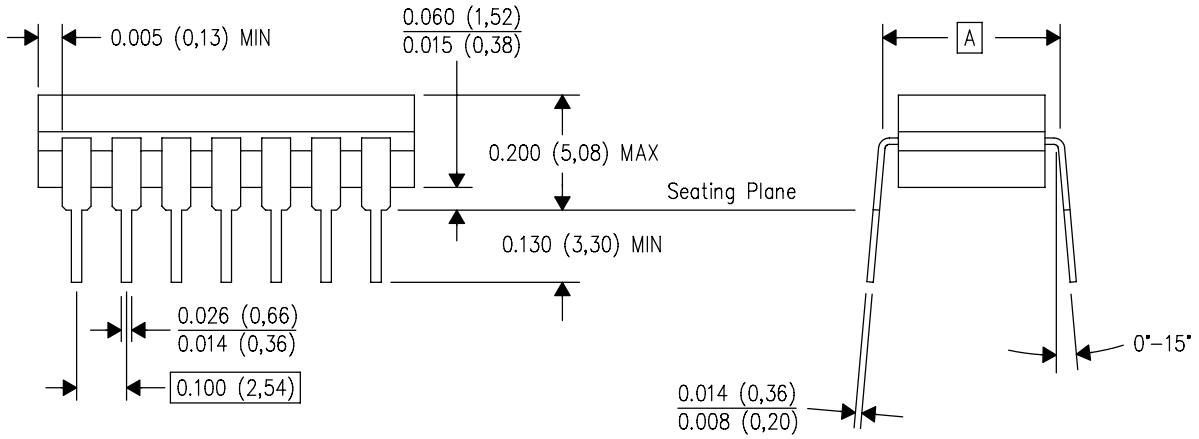
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

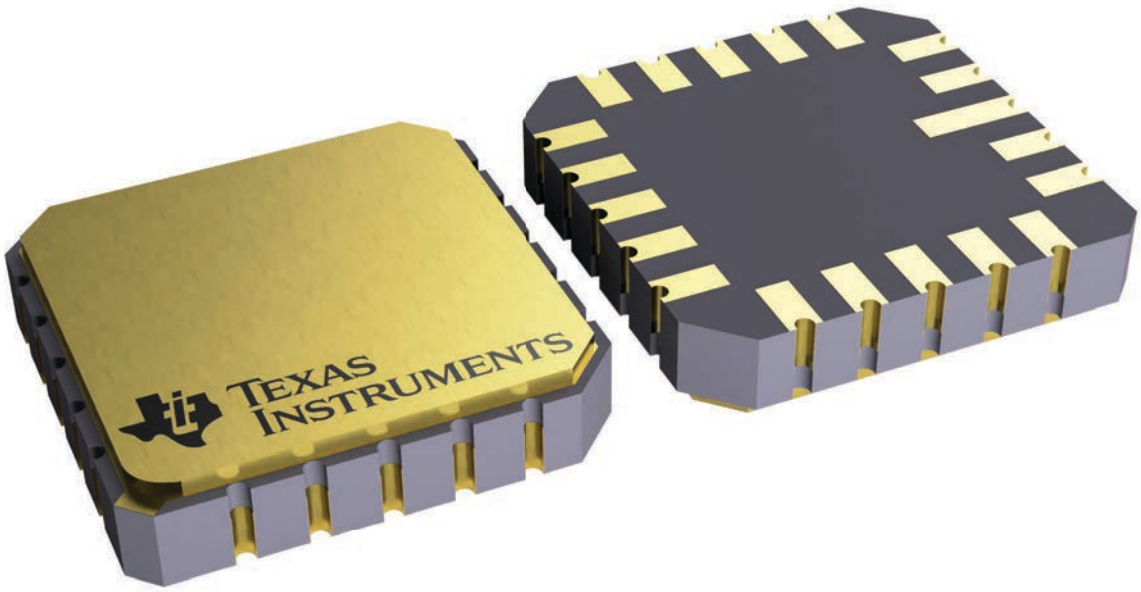
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

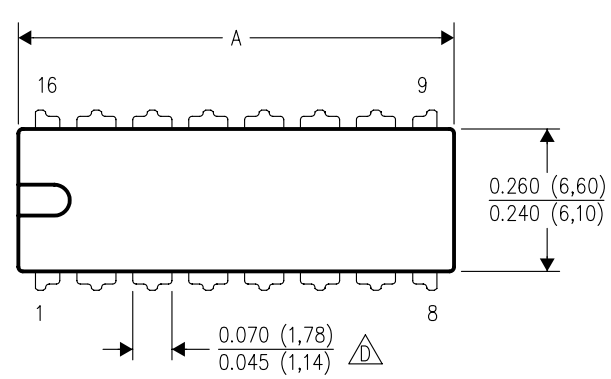


4229370VA\

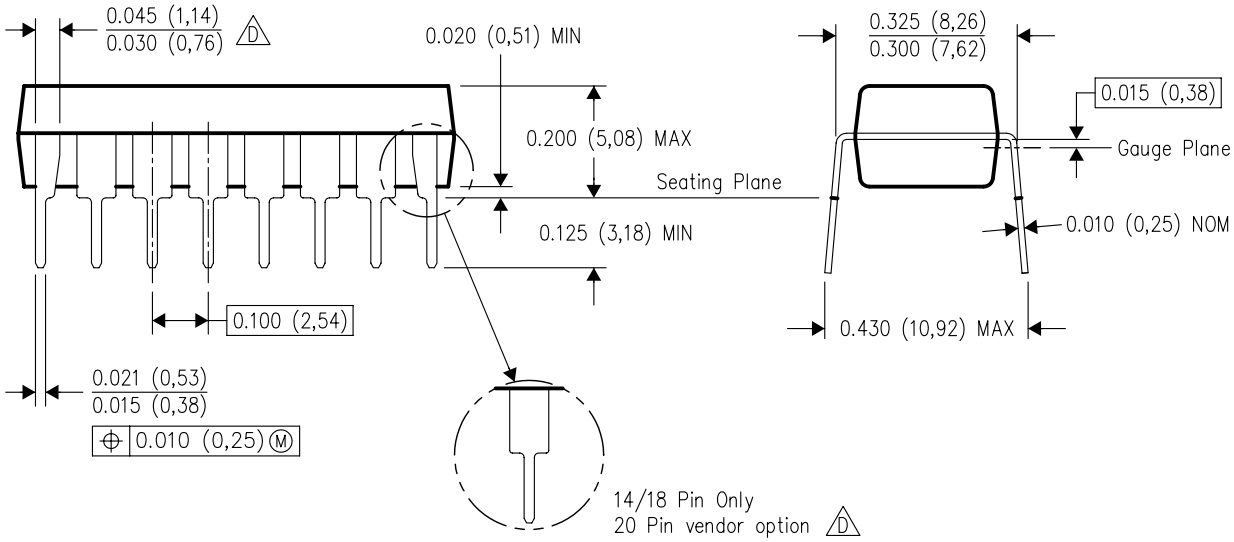
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

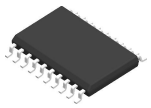


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

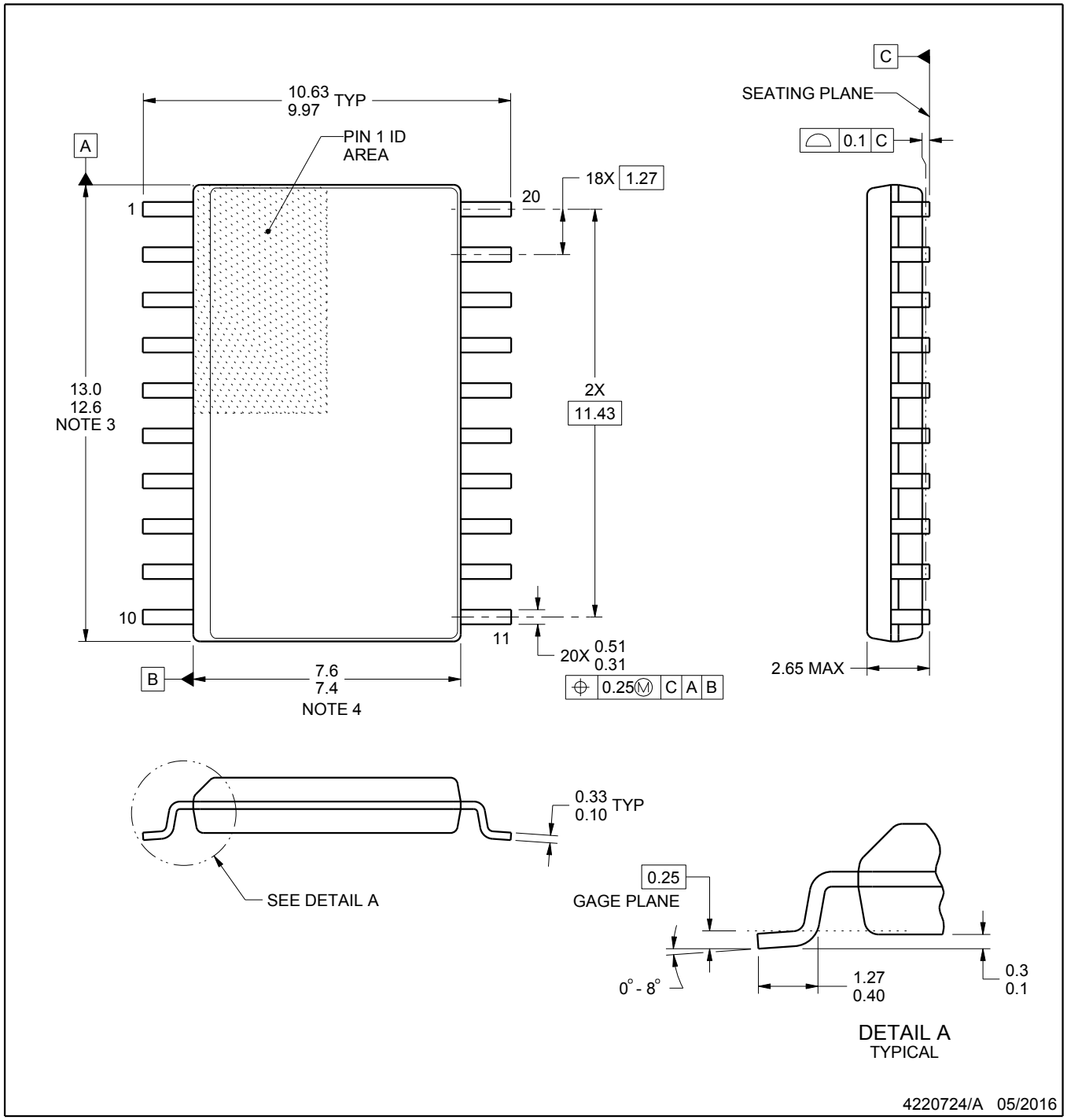


PACKAGE OUTLINE

DW0020A

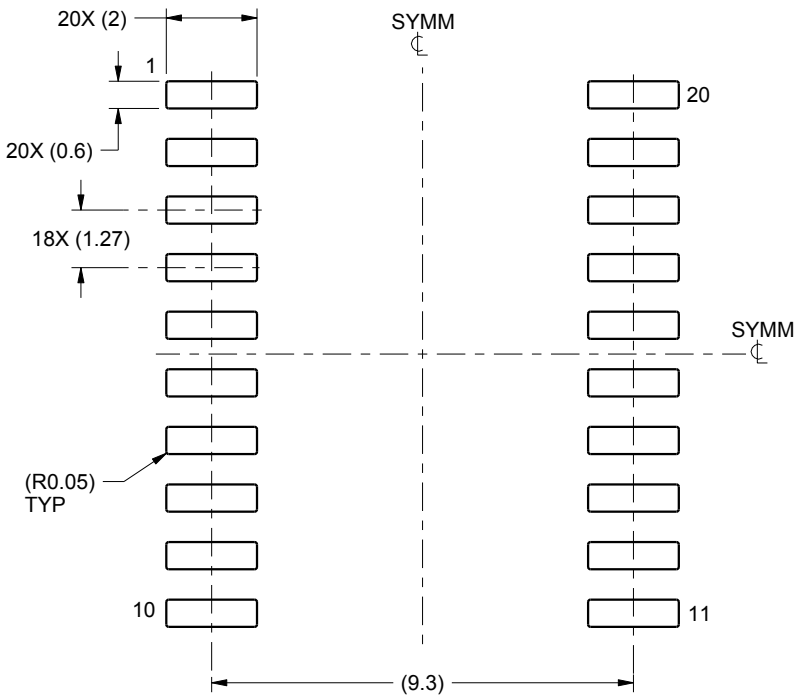
SOIC - 2.65 mm max height

SOIC

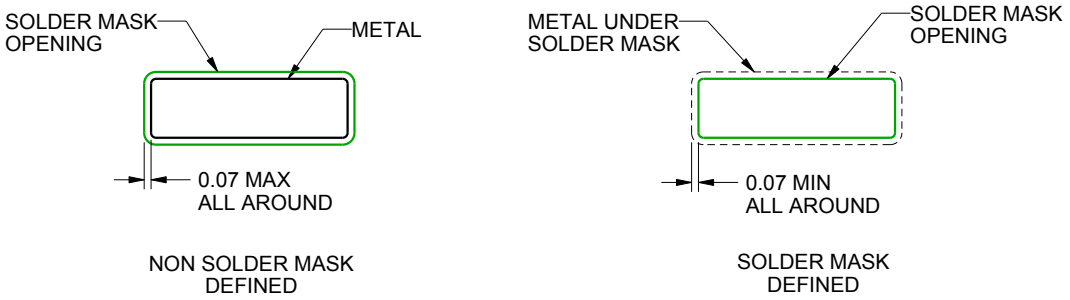


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

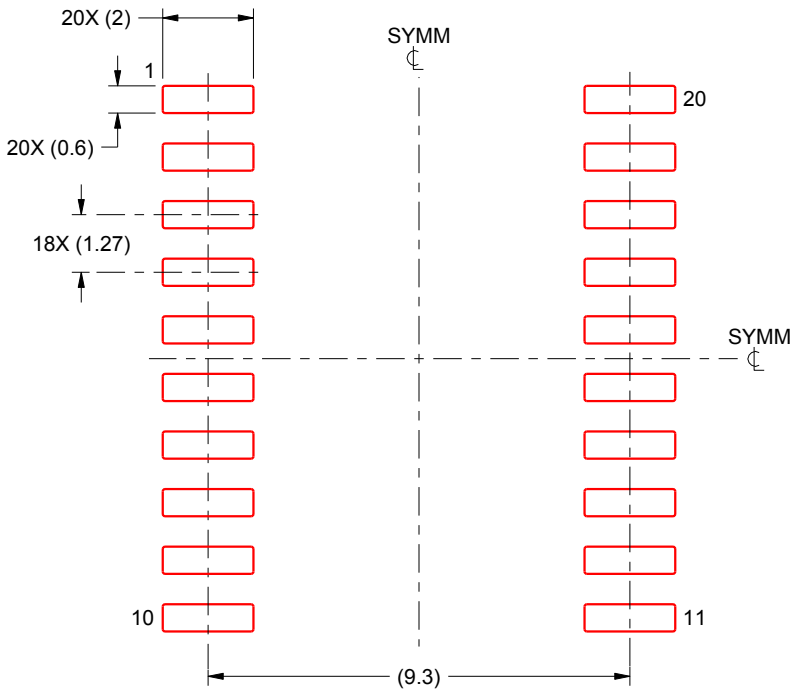


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



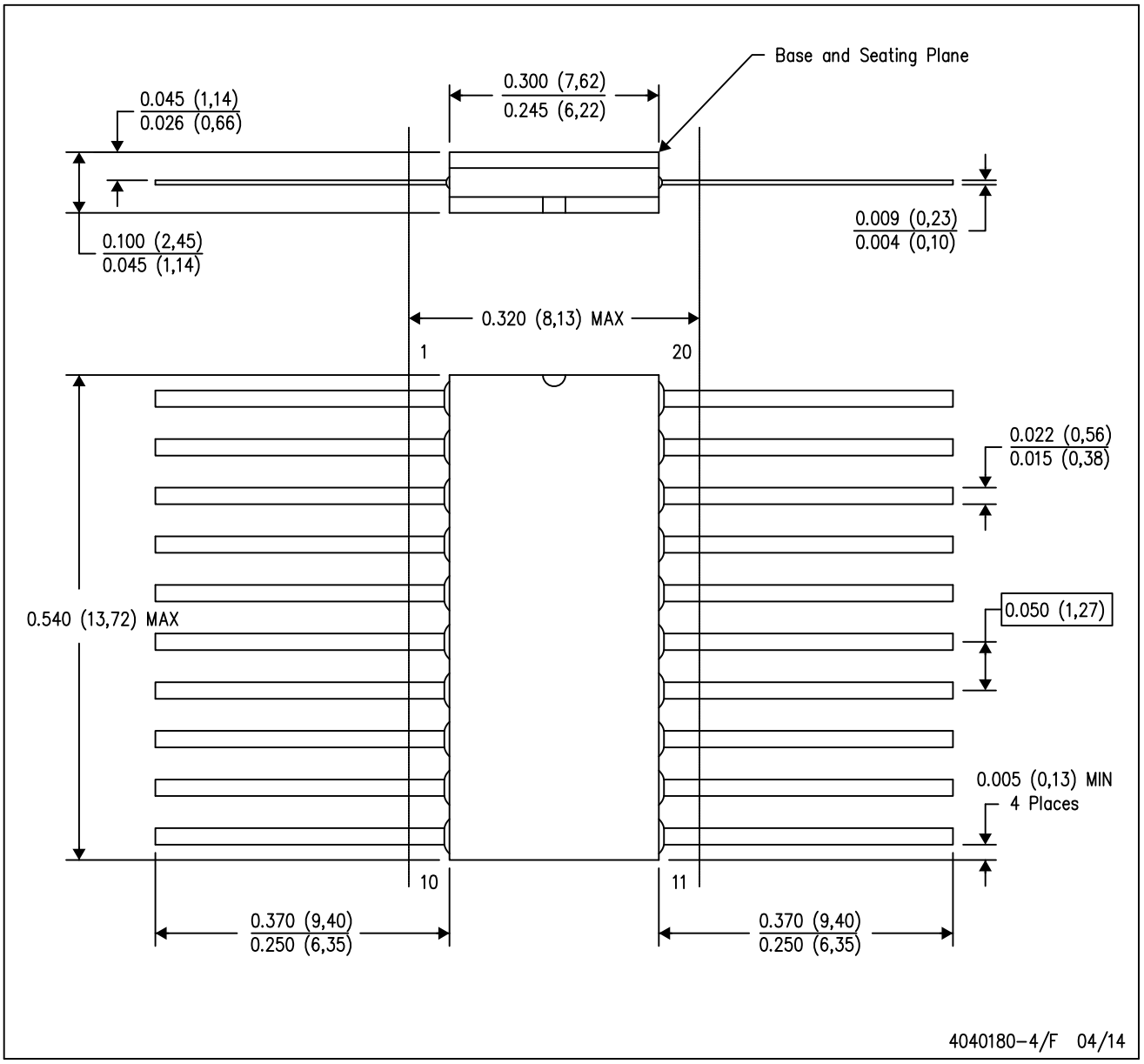
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



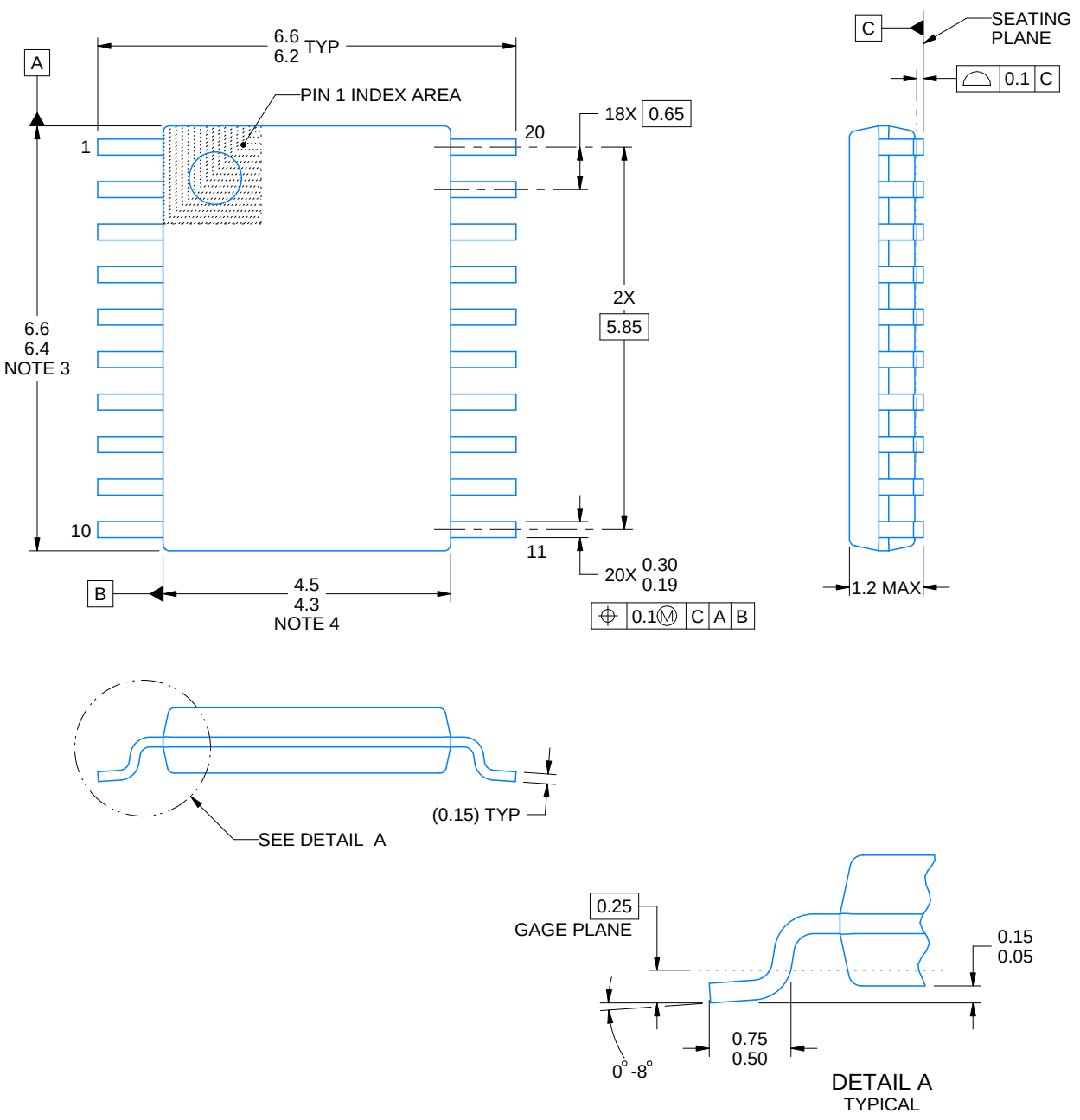
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

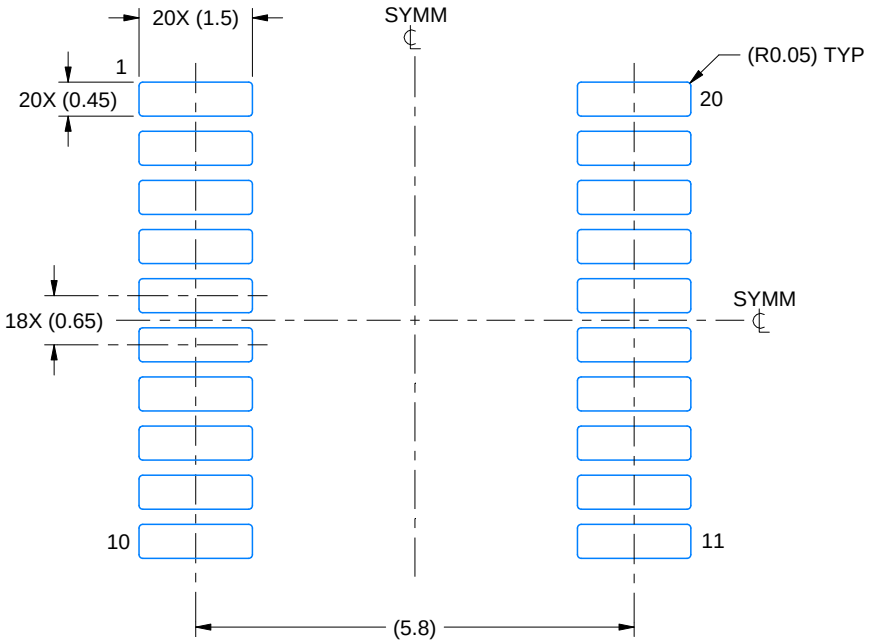
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



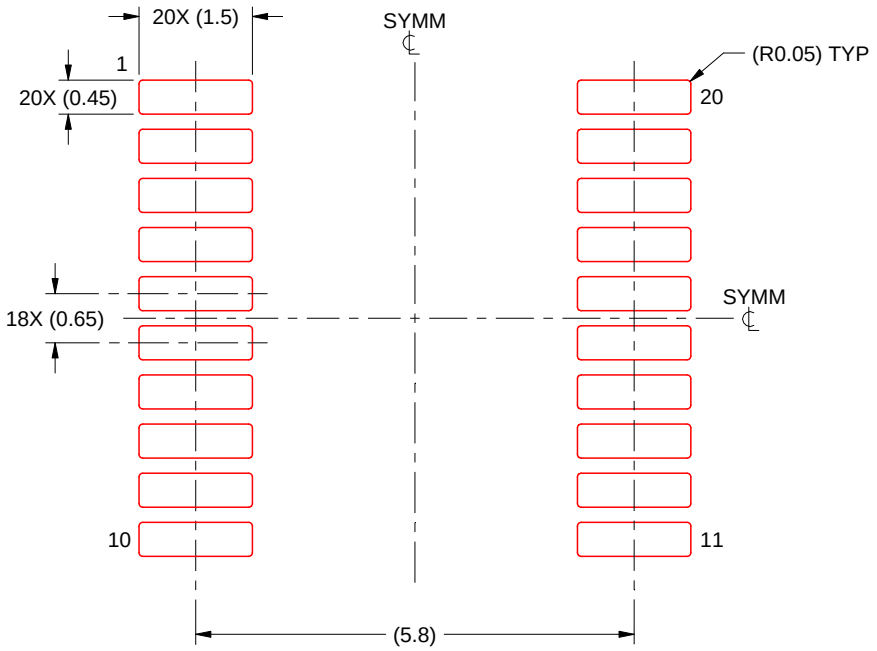
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

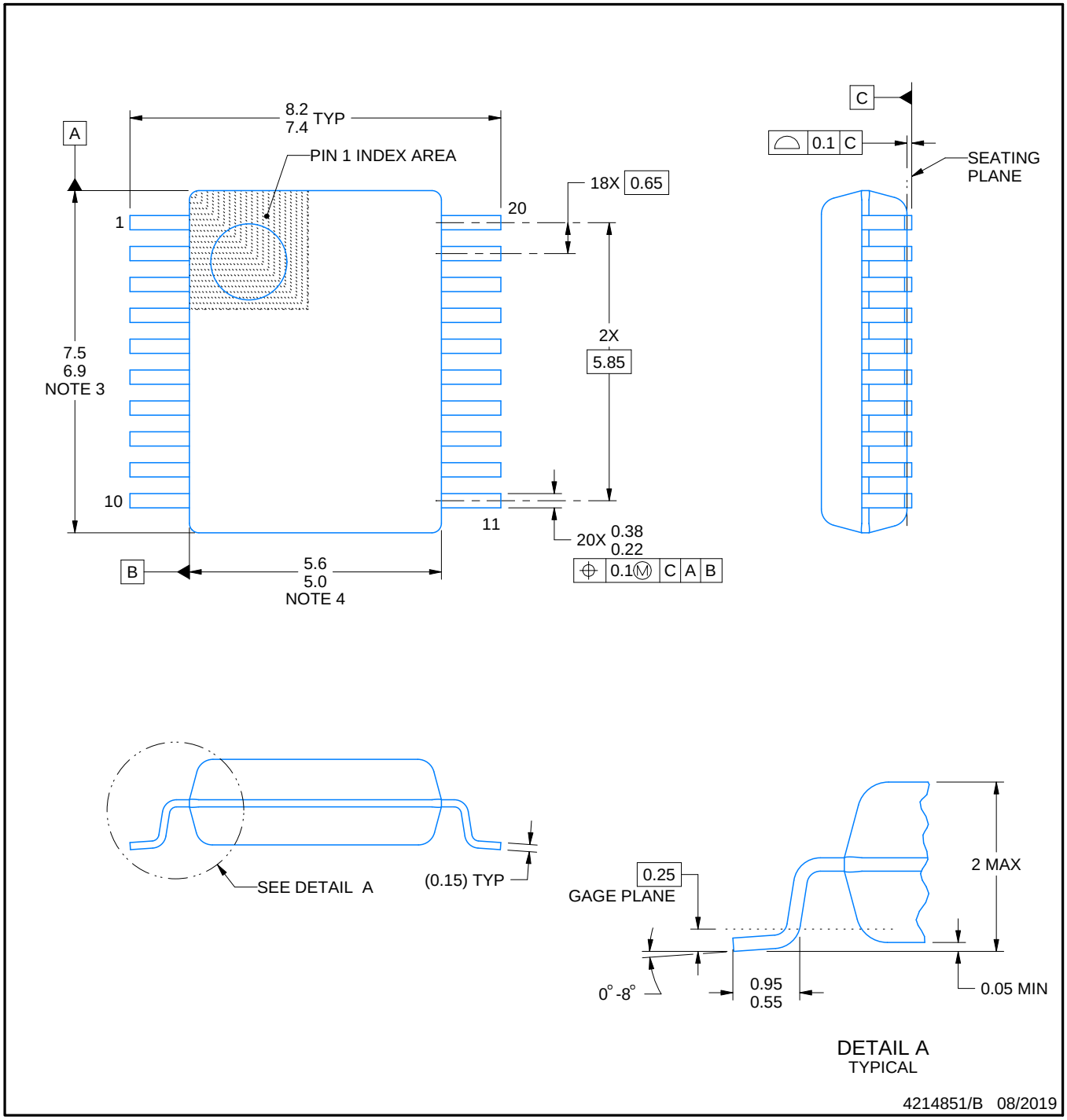
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0020A

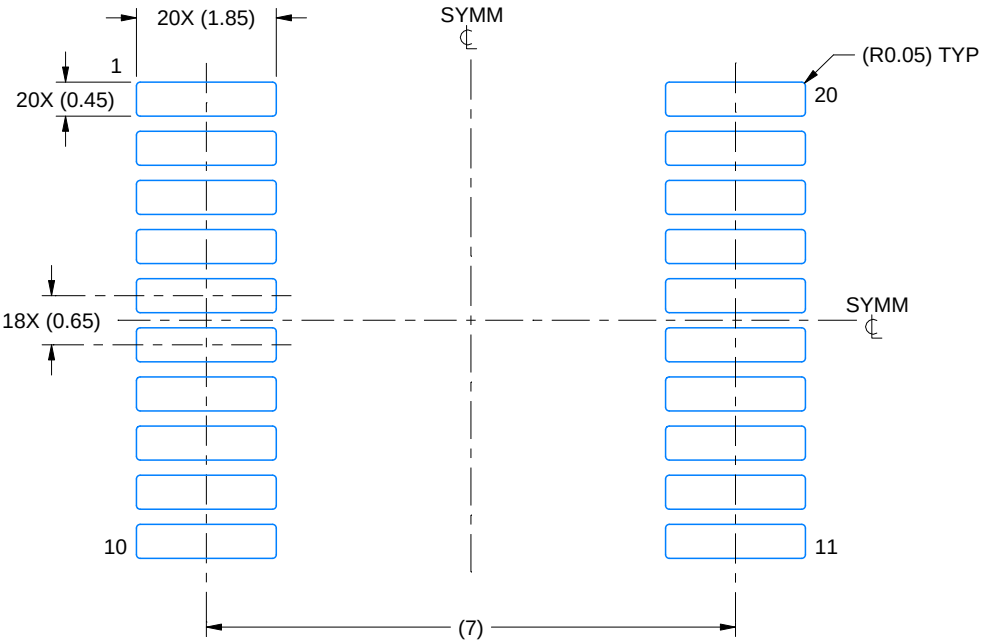
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

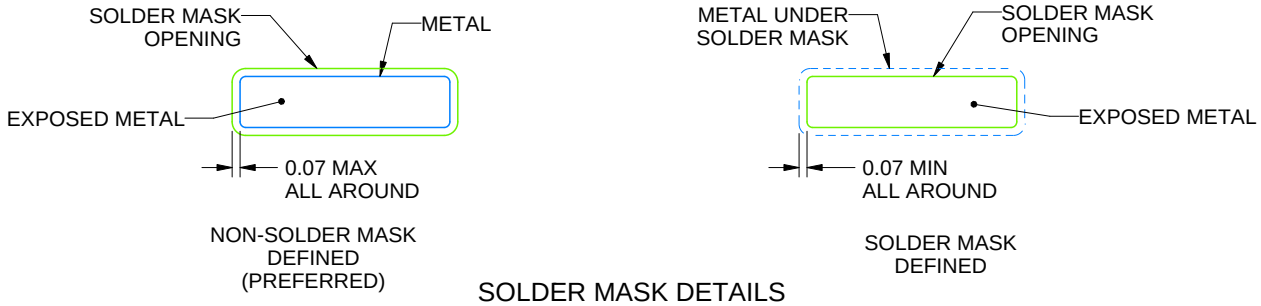


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

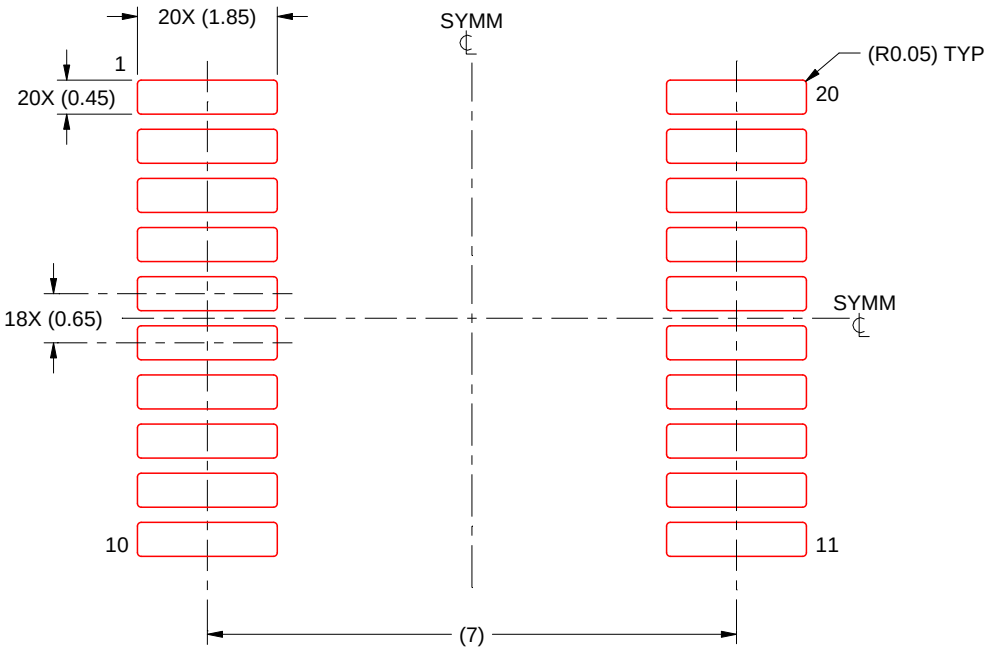
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265