SNx5LVDSxx 高速差動ライン・ドライバ

1 特長

- ANSI TIA/EIA-644 標準の要件を満たす、または超える性能
- 低電圧差動信号処理で、標準出力電圧は 350mV、負荷は 100Ω です
- 出力電圧の立ち上がり / 立ち下がり時間の標準値は 500ps (400Mbps) です
- 伝搬遅延時間の標準値は 1.7ns です
- 単一の 3.3V 電源で動作
- ドライバごとに 200MHz で標準 25mW の消費電力
- ディセーブル時、または V_{CC} = 0 の場合、ドライバは高インピーダンス
- 8kV を超えるバス端子 ESD 保護
- 低電圧 TTL (LVTTL) ロジック入力レベル
- AM26LS31、MC3487、および µA9638 とピン互換
- 冗長性を必要とする宇宙および高信頼性アプリケーション用のコールド・スペアリング

2 アプリケーション

- ワイヤレス・インフラ
- 通信インフラ
- プリンタ

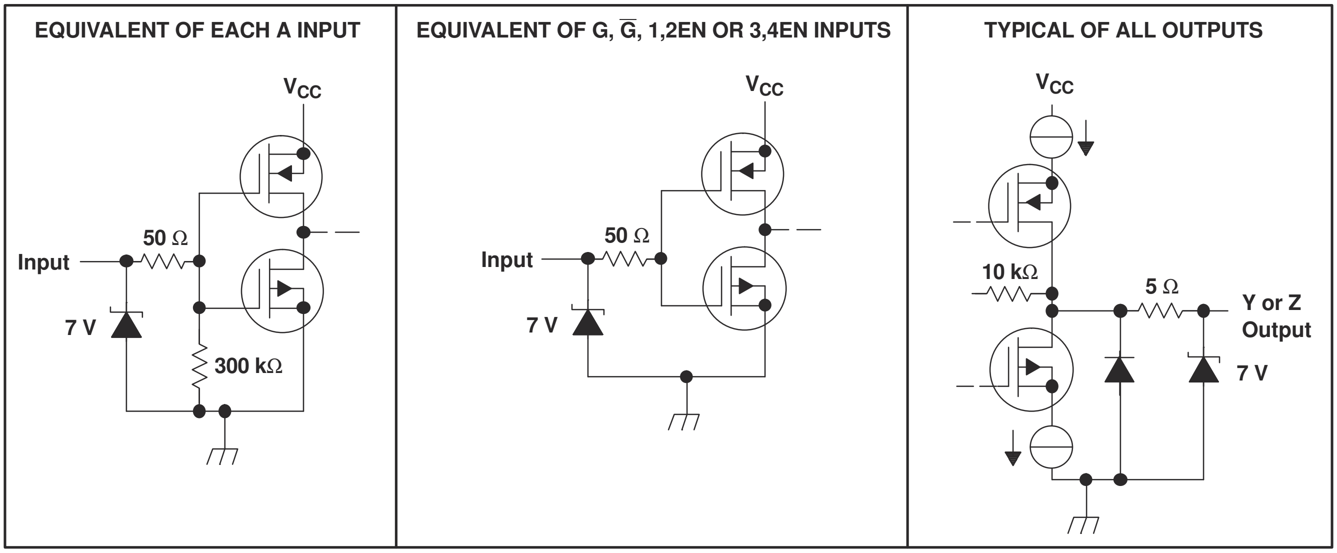
3 概要

SN55LVDS31 、 SN65LVDS31 、 SN65LVDS3487 、SN65LVDS9638 デバイスは差動ライン・ドライバで、低電圧差動信号 (LVDS) の電気的特性を実装しています。この信号方式により、出力電圧レベルが 5V の差動標準レベル (TIA/EIA-422B など) まで低下することで、消費電力が低減し、スイッチング速度が向上し、3.3V 電源レールでの動作が可能になります。4 つの電流モード・ドライバのいずれも、イネーブル時に 100Ω の負荷に対して 247mV の最小差動出力電圧振幅を供給します。

デバイス情報 (1)

部品番号	パッケージ	本体サイズ (公称)
SN55LVDS31	LCCC (20)	8.89mm × 8.89mm
	CDIP (16)	19.56mm × 6.92mm
	CFP (16)	10.30mm × 6.73mm
SN65LVDS31	SOIC (16)	9.90mm × 3.91mm
	SOP (16)	10.30mm × 5.30mm
	TSSOP (16)	5.00mm × 4.40mm
SN65LVDS3487	SOIC (16)	9.90mm × 3.91mm
	TSSOP (16)	5.00mm × 4.40mm
SN65LVDS9638	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
	HVSSOP (8)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



等価な入力および出力回路図

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4 Revision History

Changes from Revision M (August 2014) to Revision N (April 2021) — Page

- Added thermal data for SN65LVDS9638 in DGK package........ 7

Changes from Revision L (July 2007) to Revision M (August 2014) — Page

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加........ 1

Changes from Revision K (March 2004) to Revision L (July 2007) — Page

- コールド・スペアリング機能を追加........ 1
- Added Cold Sparing information........ 15

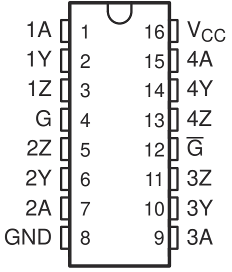
5 概要 (続き)

これらのデバイスと信号処理手法の意図するアプリケーションは、約 100Ω の制御インピーダンス・メディアを介した、ポイント・ツー・ポイントおよびマルチドロップ (1 つのドライバと複数のレシーバ) データ転送の両方です。伝送媒体にはプリント基板のトレース、バックプレーン、ケーブルを使用できます。データ転送の最高速度および最大距離は、メディアの減衰特性と周囲からのノイズに依存します。

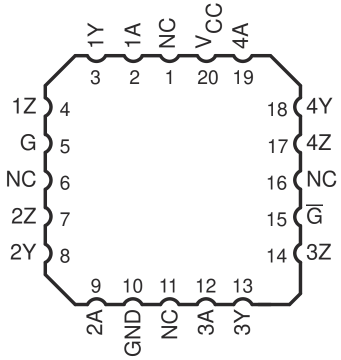
SN65LVDS31、SN65LVDS3487、SN65LVDS9638 デバイスは -40℃～85℃、SN55LVDS31 デバイスは -55℃～125℃での動作が規定されています。

6 Pin Configuration and Functions

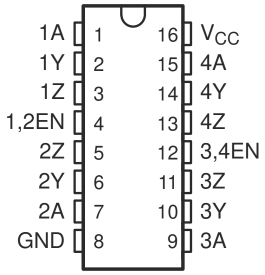
SN55LVDS31 . . . J OR W
SN65LVDS31 . . . D OR PW
(Marked as **LVDS31** or **65LVDS31**)
(TOP VIEW)



SN55LVDS31FK
(TOP VIEW)



SN65LVDS3487D
(Marked as **LVDS3487** or **65LVDS3487**)
(TOP VIEW)



SN65LVDS9638D (Marked as **DK638** or **LVDS38**)
SN65LVDS9638DGN (Marked as **L38**)
SN65LVDS9638DGK (Marked as **AXG**)
(TOP VIEW)

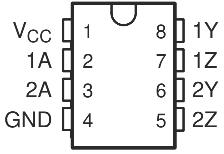


表 6-1. Pin Functions: SN55LVDS31 J or W, SN65LVDS31 D or PW

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	16	–	Supply voltage
GND	8	–	Ground
1A	1	I	LVTTL input signal

表 6-1. Pin Functions: SN55LVDS31 J or W, SN65LVDS31 D or PW (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
1Y	2	O	Differential (LVDS) non-inverting output
1Z	3	O	Differential (LVDS) inverting output
2A	7	I	LVTTL input signal
2Y	6	O	Differential (LVDS) non-inverting output
2Z	5	O	Differential (LVDS) inverting output
3A	9	I	LVTTL input signal
3Y	10	O	Differential (LVDS) non-inverting output
3Z	11	O	Differential (LVDS) inverting output
4A	15	I	LVTTL input signal
4Y	14	O	Differential (LVDS) non-inverting output
4Z	13	O	Differential (LVDS) inverting output
G	4	I	Enable (HI = ENABLE)
G/	12	I	Enable (LO = ENABLE)

表 6-2. Pin Functions: SN65LVDS31FK

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	20	–	Supply voltage
GND	10	–	Ground
1A	2	I	LVTTL input signal
1Y	3	O	Differential (LVDS) non-inverting output
1Z	4	O	Differential (LVDS) inverting output
2A	9	I	LVTTL input signal
2Y	8	O	Differential (LVDS) non-inverting output
2Z	7	O	Differential (LVDS) inverting output
3A	12	I	LVTTL input signal
3Y	13	O	Differential (LVDS) non-inverting output
3Z	14	O	Differential (LVDS) inverting output
4A	19	I	LVTTL input signal
4Y	18	O	Differential (LVDS) non-inverting output
4Z	17	O	Differential (LVDS) inverting output
G	5	I	Enable (HI = ENABLE)
G/	15	I	Enable (LO = ENABLE)
NC	1, 6, 11, 16	–	No connection

表 6-3. Pin Functions: SN65LVDS3487D

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	16	–	Supply voltage
GND	8	–	Ground
1A	1	I	LVTTL input signal
1Y	2	O	Differential (LVDS) non-inverting output
1Z	3	O	Differential (LVDS) inverting output
2A	7	I	LVTTL input signal

表 6-3. Pin Functions: SN65LVDS3487D (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
2Y	6	O	Differential (LVDS) non-inverting output
2Z	5	O	Differential (LVDS) inverting output
3A	9	I	LVTTL input signal
3Y	10	O	Differential (LVDS) non-inverting output
3Z	11	O	Differential (LVDS) inverting output
4A	15	I	LVTTL input signal
4Y	14	O	Differential (LVDS) non-inverting output
4Z	13	O	Differential (LVDS) inverting output
1,2EN	4	I	Enable for channels 1 and 2
3,4EN	12	I	Enable for channels 3 and 4

表 6-4. Pin Functions: SN65LVDS9638D, SN65LVDS9638DGN, SN65LVDS9638DGK

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	1	–	Supply voltage
GND	4	–	Ground
1A	2	I	LVTTL input signal
1Y	8	O	Differential (LVDS) non-inverting output
1Z	7	O	Differential (LVDS) inverting output
2A	3	I	LVTTL input signal
2Y	6	O	Differential (LVDS) non-inverting output
2Z	5	O	Differential (LVDS) inverting output

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]	–0.5	4	V
V_I	Input voltage range	–0.5	V_{CC} + 0.5	V
	Continuous total power dissipation	See *セクション 7.4*		
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 7.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±8000	V
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
T_A	Operating free-air temperature	SN65 prefix	–40		85	°C
		SN55 prefix	–55		125	

7.4 Thermal Information

THERMAL METRIC[1]		SN55LVDS31			SN65LVDS31			SN65LVDS3487		SN65LVDS9638			UNIT
		FK	J	W	D	NS	PW	D	PW	D	DGK	DGN[2]	
		20 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance				84.8	86.0					179.5		°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance				46.0	44.2					72.3		
$R_{\theta JB}$	Junction-to-board thermal resistance				41.8	26.4					101.5		
Ψ_{JT}	Junction-to-top characterization parameter				11.1	10.9					11		
Ψ_{JB}	Junction-to-board characterization parameter				41.5	46.1					99.7		

THERMAL METRIC[1]		SN55LVDS31			SN65LVDS31			SN65LVDS3487		SN65LVDS9638			UNIT
		FK	**J**	**W**	**D**	**NS**	**PW**	**D**	**PW**	**D**	**DGK**	**DGN**[2]	
		20 PINS	**16 PINS**	**16 PINS**	**16 PINS**	**16 PINS**	**16 PINS**	**16 PINS**	**16 PINS**	**8 PINS**	**8 PINS**	**8 PINS**	
Power Rating	$T_A \le 25°C$	1375	1375	1000	950	—	774	950	774	725	425	2140	mW
	$T_A \le 70°C$	880	880	640	608	—	496	608	496	464	272	1370	
	$T_A \le 85°C$	715	715	520	494	—	402	494	402	377	221	1110	
	$T_A \le 125°C$	275	275	200	—	—-	—	—	—	—	—	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

(2) The PowerPAD™ must be soldered to a thermal land on the printed-circuit board. See the application note *PowerPAD Thermally Enhanced Package* (SLMA002).

7.5 Electrical Characteristics: SN55LVDS31

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{OD}	Differential output voltage magnitude	R_L = 100 Ω, See 図 8-2	247	340	454	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states	R_L = 100 Ω, See 図 8-2	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 図 8-3	1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See 図 8-3	–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See 図 8-3		50	150	mV
I_{CC}	Supply current	V_I = 0.8 or 2 V, Enabled, No load		9	20	mA
		V_I = 0.8 or 2 V, R_L = 100 Ω, Enabled		25	35	
		V_I = 0 or V_{CC}, Disabled		0.25	1	
I_{IH}	High-level input current	V_{IH} = 2		4	20	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V		0.1	10	μA
I_{OS}	Short-circuit output current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0		–4	–24	mA
		V_{OD} = 0			±12	
I_{OZ}	High-impedance output current	V_O = 0 or 2.4 V			±1	μA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 0, V_O = 2.4 V			±4	μA
C_i	Input capacitance			3		pF

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

7.6 Electrical Characteristics: SN65LVDSxxxx

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN65LVDS31 SN65LVDS3487 SN65LVDS9638			UNIT
					MIN	TYP[1]	MAX	
V_{OD}	Differential output voltage magnitude		R_L = 100 Ω, See 図 8-2		247	340	454	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states		R_L = 100 Ω, See 図 8-2		–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		See 図 8-3		1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		See 図 8-3		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		See 図 8-3			50	150	mV
I_{CC}	Supply current	SN65LVDS31 SN65LVDS3487	V_I = 0.8 V or 2 V, Enabled, No load			9	20	mA
			V_I = 0.8 or 2 V, R_L = 100 Ω, Enabled			25	35	
			V_I = 0 or V_{CC}, Disabled			0.25	1	
		SN65LVDS9638	V_I = 0.8 V or 2 V	No load		4.7	8	mA
				R_L = 100 Ω		9	13	
I_{IH}	High-level input current		V_{IH} = 2			4	20	μA
I_{IL}	Low-level input current		V_{IL} = 0.8 V			0.1	10	μA
I_{OS}	Short-circuit output current		$V_{O(Y)}$ or $V_{O(Z)}$ = 0			–4	–24	mA
			V_{OD} = 0				±12	
I_{OZ}	High-impedance output current		V_O = 0 or 2.4 V				±1	μA
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0, V_O = 2.4 V				±1	μA
C_i	Input capacitance					3		pF

[1] All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

7.7 Switching Characteristics: SN55LVDS31

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF See 図 8-2	0.5	1.4	4	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	1.7	4.5	ns
t_r	Differential output signal rise time (20% to 80%)		0.4	0.5	1	ns
t_f	Differential output signal fall time (80% to 20%)		0.4	0.5	1	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			0.3	0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew[2]			0.3	0.6	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See 図 8-4		5.4	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			2.5	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			8.1	17	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			7.3	15	ns

[1] All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
[2] $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

7.8 Switching Characteristics: SN65LVDSxxxx

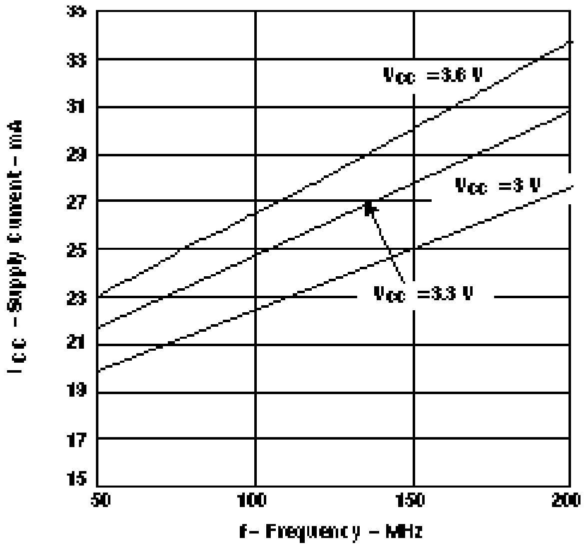
over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LVDS31 SN65LVDS3487 SN65LVDS9638			UNIT
			MIN	TYP[1]	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See 図 8-2	0.5	1.4	2	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	1.7	2.5	ns
t_r	Differential output signal rise time (20% to 80%)		0.4	0.5	0.6	ns
t_f	Differential output signal fall time (80% to 20%)		0.4	0.5	0.6	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)			0.3	0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew[2]			0	0.3	ns
$t_{sk(pp)}$	Part-to-part skew[3]				800	ps
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See 図 8-4		5.4	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			2.5	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			8.1	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			7.3	15	ns

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

7.9 Typical Characteristics

7.9.1



Four Drivers Loaded Per 図 8-3 and Switching Simultaneously

図 7-1. SN55LVDS31, SN65LVDS31 Supply Current vs Frequency

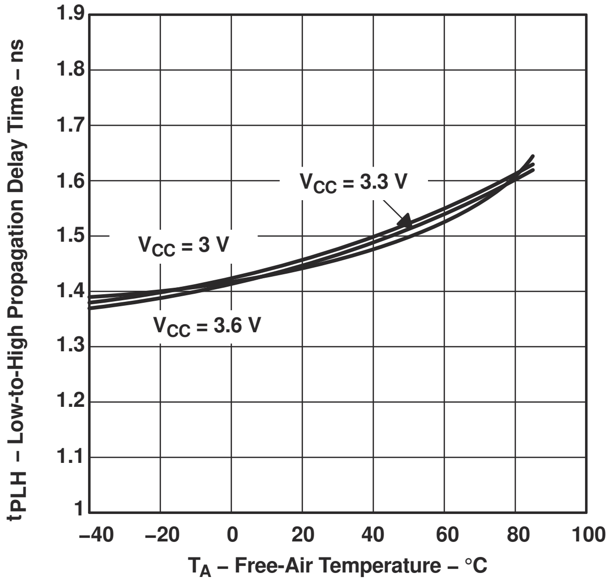


図 7-2. Low-to-High Propagation Delay Time vs Free-Air Temperature

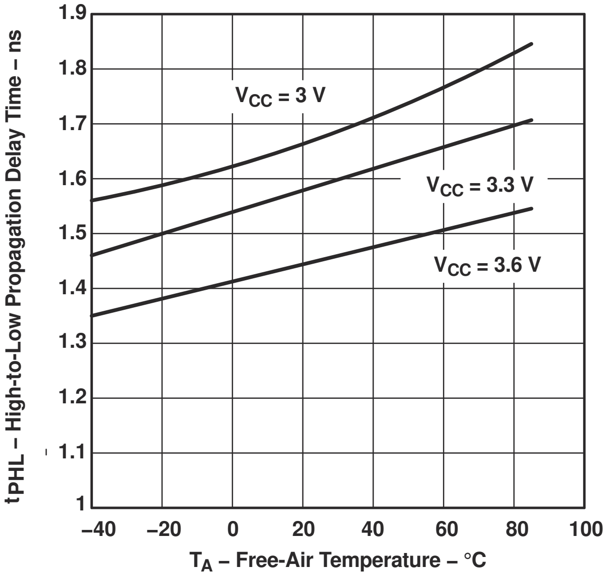


図 7-3. High-to-Low Propagation Delay Time vs Free-Air Temperature

8 Parameter Measurement Information

8.1

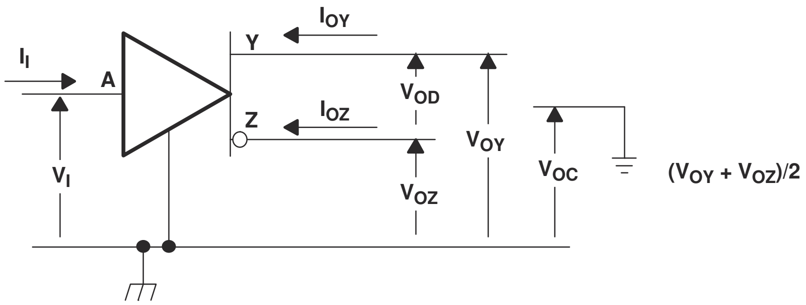
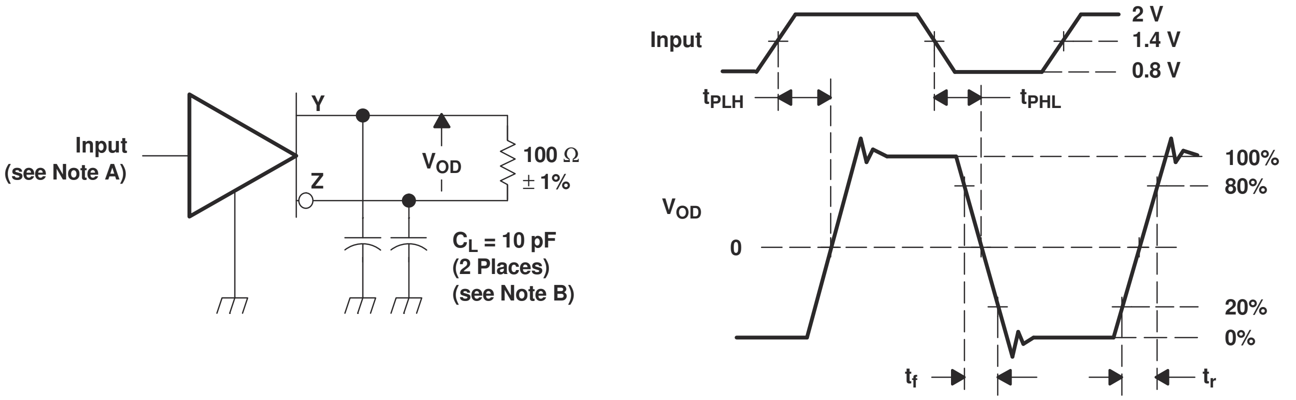


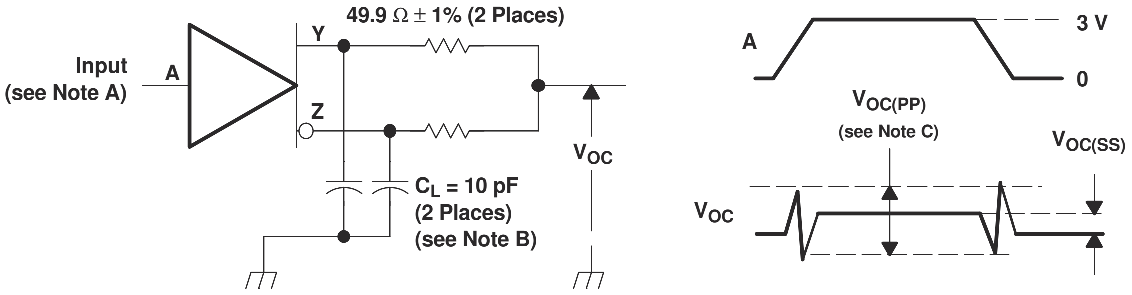
図 8-1. Voltage and Current Definitions



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

図 8-2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

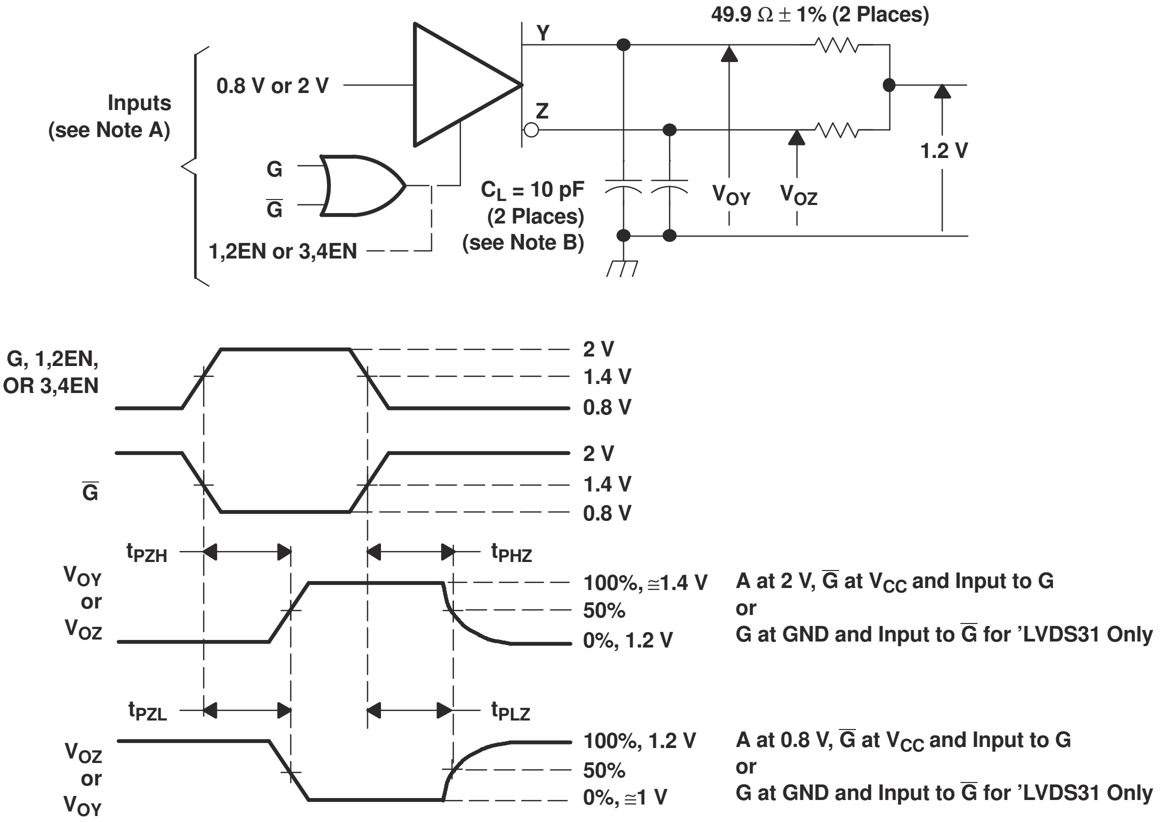


NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

C. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 300 MHz.

図 8-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f < 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

図 8-4. Enable or Disable Time Circuit and Definitions

9 Detailed Description

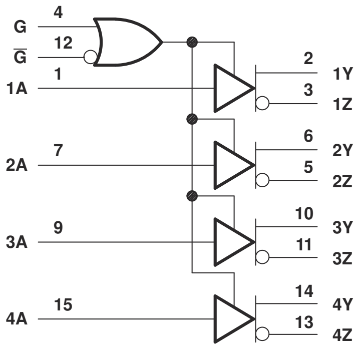
9.1 Overview

The SNx5LVDSxx devices are dual- and quad-channel LVDS line drivers. They operate from a single supply that is nominally 3.3 V, but can be as low as 3 V and as high as 3.6 V. The input signal to the SN65LVDS1 device is an LVTTL signal. The output of the device is a differential signal complying with the LVDS standard (TIA/EIA-644A). The differential output signal operates with a signal level of 340 mV, nominally, at a common-mode voltage of 1.2 V. This low differential output voltage results in a low emitted radiated energy, which is dependent on the signal slew rate. The differential nature of the output provides immunity to common-mode coupled signals.

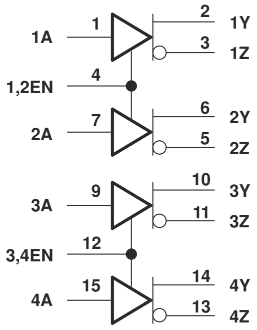
The SNx5LVDSxx devices are intended to drive a 100-Ω transmission line. This transmission line may be a printed-circuit board (PCB) or cabled interconnect. With transmission lines, the optimum signal quality and power delivery is reached when the transmission line is terminated with a load equal to the characteristic impedance of the interconnect. Likewise, the driven 100-Ω transmission line should be terminated with a matched resistance.

9.2 Functional Block Diagram

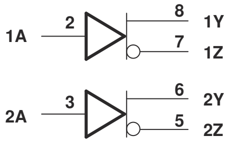
’LVDS31 logic diagram (positive logic)



SN65LVDS3487 logic diagram (positive logic)



SN65LVDS9638 logic diagram (positive logic)



9.3 Feature Description

9.3.1 Driver Disabled Output

When the SNx5LVDSxx driver is disabled, or when power is removed from the device, the driver outputs are high-impedance.

9.3.2 NC Pins

NC (not connected) pins are pins where the die is not physically connected to the lead frame or package. For optimum thermal performance, a good rule of thumb is to ground the NC pins at the board level.

9.3.3 Unused Enable Pins

Unused enable pins should be tied to V_{CC} or GND as appropriate.

9.3.4 Driver Equivalent Schematics

The driver input is represented by a CMOS inverter stage with a 7-V Zener diode. The input stage is high-impedance, and includes an internal pulldown to ground. If the driver input is left open, the driver input provides a low-level signal to the rest of the driver circuitry, resulting in a low-level signal at the driver output pins. The Zener diode provides ESD protection. The driver output stage is a differential pair, one half of which is shown in 図 9-1. Like the input stage, the driver output includes Zener diodes for ESD protection. The schematic shows an output stage that includes a set of current sources (nominally 3.5 mA) that are connected to the output load circuit based upon the input stage signal. To the first order, the SNx5LVDSxx output stage acts a constant-current source.

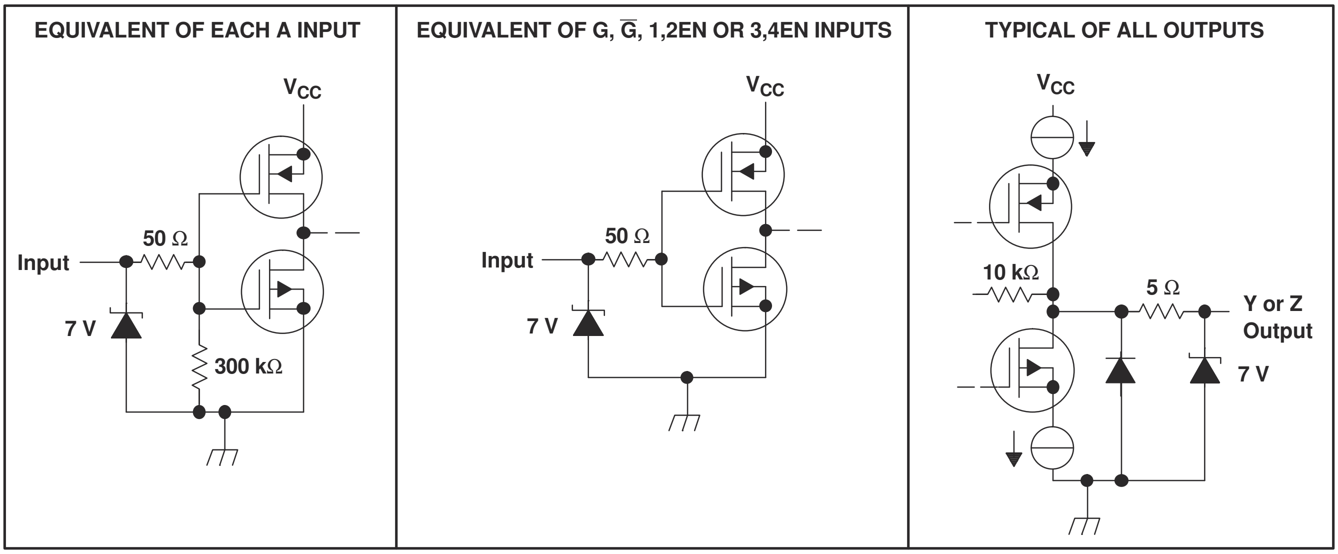


図 9-1. Equivalent Input and Output Schematic Diagrams

9.4 Device Functional Modes

表 9-1. SN55LVDS31, SN65LVDS31(1)

INPUT A	ENABLES		OUTPUTS	
	G	G	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high-impedance (off)

表 9-2. SN65LVDS3487(1)

INPUT A	ENABLE EN	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high-impedance (off)

表 9-3. SN65LVDS9638(1)

INPUT A	OUTPUTS	
	Y	Z
H	H	L
L	L	H
Open	L	H

(1) H = high level, L = low level

10 Application and Implementation

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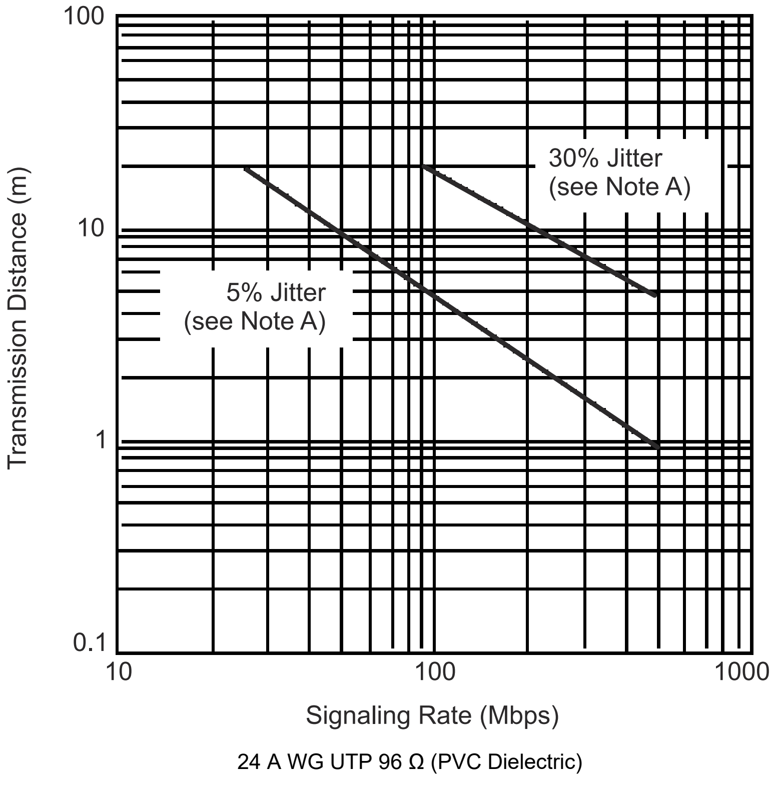
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SNx5LVDSxx devices are dual- and quad-channel LVDS drivers. These devices are generally used as building blocks for high-speed, point-to-point, data transmission where ground differences are less than 1 V. LVDS drivers and receivers provide high-speed signaling rates that are often implemented with ECL class devices without the ECL power and dual-supply requirements. A common question with any class of driver is how far and how fast can the devices operate. While individual drivers and receivers have specifications that define their inherent switching rate, a communication link will quite often be limited by the impairments introduced by the interconnecting media. 図 10-1 shows the typical relationship between signaling rate and distance achievable depends on the quality of the eye pattern at the receiver that is either desired or needed. 図 10-1 shows the curves representing 5% and 30% eye closure due to inter-symbol interference (ISI).



A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

図 10-1. Typical Transmission Distance vs Signaling Rate

10.2 Typical Application

10.2.1 Point-to-Point Communications

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in 図 10-2.

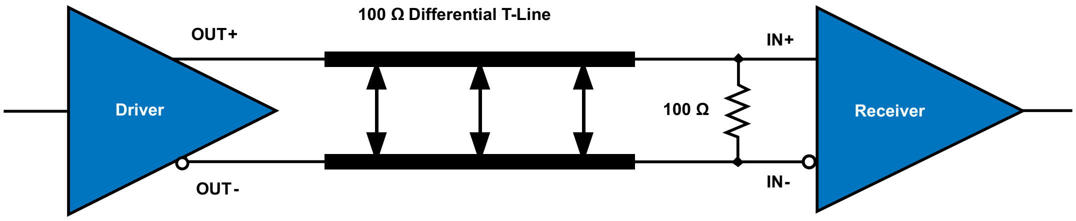


図 10-2. Point-to-Point Topology

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In 図 10-2 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

10.2.1.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6 V
Driver Input Voltage	0.8 to 3.3 V
Driver Signaling Rate	DC to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6 V
Receiver Input Voltage	0 to 2.4 V
Receiver Signaling Rate	DC to 400 Mbps
Ground shift between driver and receiver	±1 V

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Driver Supply Voltage

The SNx5LVDSxx driver is operated from a single supply. The device can support operation with a supply as low as 3 V and as high as 3.6 V. The differential output voltage is nominally 340 mV over the complete output range. The minimum output voltage stays within the specified LVDS limits (247 mV to 454 mV) for a 3.3-V supply.

10.2.1.2.2 Driver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very-low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 to 1000 µF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one should resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson[1], equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV; however, this figure varies depending on the noise budget available in your design. [1]

$$C_{\text{chip}} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{\text{LVDS}} = \left(\frac{1\text{A}}{0.2\text{V}} \right) \times 200\ \text{ps} = 0.001\ \mu\text{F} \quad (2)$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.001 µF). You should place the smallest value of capacitance as close as possible to the chip.

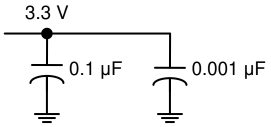


図 10-3. Recommended LVDS Bypass Capacitor Layout

10.2.1.2.3 Driver Output Voltage

The SNx5LVDSxx driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 340 mV. This 340 mV is the absolute value of the differential swing ($V_{OD} = |V^+ - V^-|$). The peak-to-peak differential voltage is twice this value, or 680 mV.

10.2.1.2.4 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces. The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with a variation of no more than 10% (90 Ω to 132 Ω).

10.2.1.2.5 PCB Transmission Lines

As per SNLA187, 図 10-4 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. 図 10-4 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

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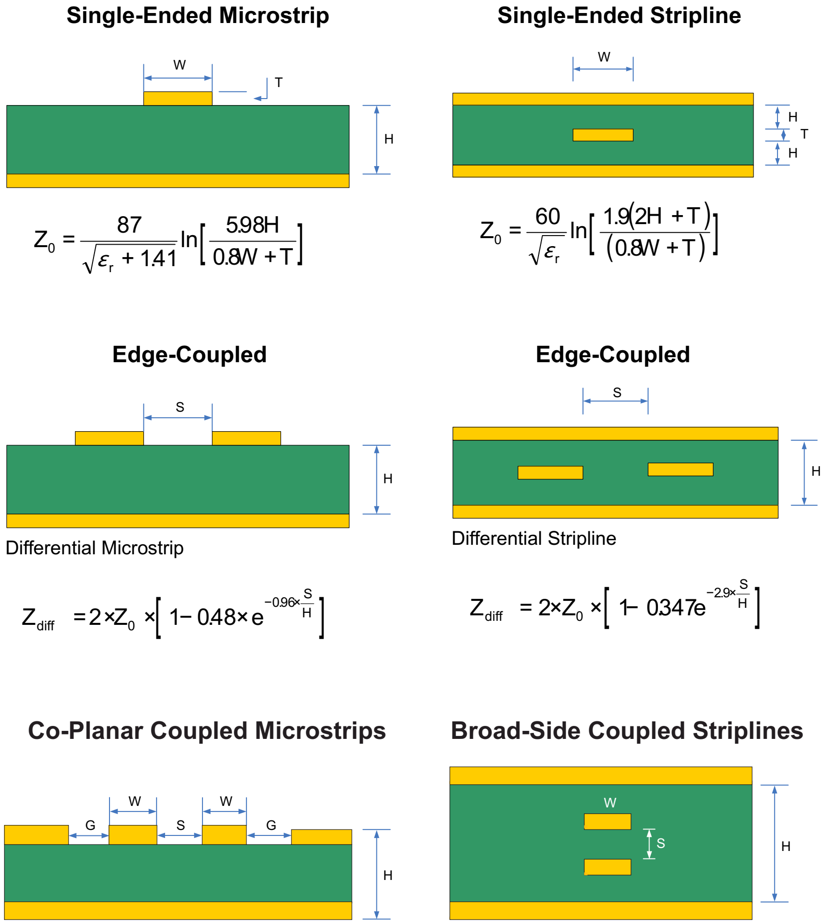
[1] Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.



Single-Ended Microstrip

Single-Ended Stripline

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{0.8W + T}\right]$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(2H + T)}{(0.8W + T)}\right]$$

Edge-Coupled

Edge-Coupled

Differential Microstrip

Differential Stripline

$$Z_{diff} = 2 \times Z_0 \times \left[1 - 0.48 \times e^{-0.96 \times \frac{S}{H}}\right]$$

$$Z_{diff} = 2 \times Z_0 \times \left[1 - 0.347e^{-2.9 \times \frac{S}{H}}\right]$$

Co-Planar Coupled Microstrips

Broad-Side Coupled Striplines

図 10-4. Controlled-Impedance Transmission Lines

10.2.1.2.6 Termination Resistor

As shown earlier, an LVDS communication channel employs a current source driving a transmission line which is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure incident wave switching (which is necessary to operate the channel at the highest signaling rate), the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be between 90 and 110 Ω.

The line termination resistance should be located as close as possible to the receiver, thereby minimizing the stub length from the resistor to the receiver. The limiting case would be to incorporate the termination resistor into the receiver, which is exactly what is offered with a device like the SN65LVDT386. The SN65LVDT386 provides all the functionality and performance of the SN65LVDT386 receiver, with the added feature of an integrated termination load.

While we talk in this section about point-to-point communications, a word of caution is useful when a multidrop topology is used. In such topologies, line termination resistors are to be located only at the end(s) of the transmission line. In such an environment, SN65LVDT386 receivers could be used for loads branching off the main bus with an SN65LVDT386 used only at the bus end.

10.2.1.2.7 Driver NC Pins

NC (not connected) pins are pins where the die is not physically connected to the lead frame and package. For optimum thermal performance, a good rule of thumb is to ground the NC pins at the board level.

10.2.1.3 Application Curve

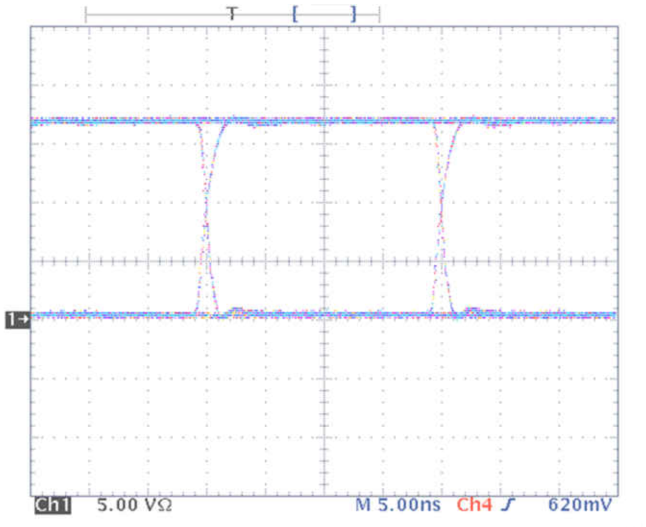


図 10-5. Typical Driver Output Eye Pattern in Point-to-Point System

10.2.2 Multidrop Communications

A second common application of LVDS buffers is a multidrop topology. In a multidrop configuration, a single driver and a shared bus are present along with two or more receivers (with a maximum permissible number of 32 receivers). 図 10-6 shows an example of a multidrop system.

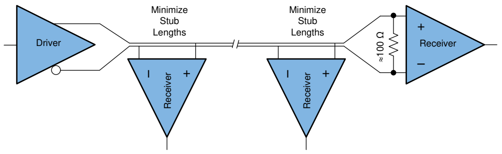


図 10-6. Multidrop Topology

10.2.2.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6 V
Driver Input Voltage	0.8 to 3.3 V
Driver Signaling Rate	DC to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	2 to 32
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6 V
Receiver Input Voltage	0 to 2.4 V
Receiver Signaling Rate	DC to 400 Mbps
Ground shift between driver and receiver	±1 V

10.2.2.2 Detailed Design Procedure

10.2.2.2.1 Interconnecting Media

The interconnect in a multidrop system differs considerably from a point-to-point system. While point-to-point interconnects are straightforward and well understood, the bus type architecture encountered with multidrop systems requires more careful attention. We will use 図 10-6 above to explore these details.

The most basic multidrop system would include a single driver, located at a bus origin, with multiple receiver nodes branching off the main line, and a final receiver at the end of the transmission line, co-located with a bus termination resistor. While this would be the most basic multidrop system, it has several considerations not yet explored.

The location of the transmitter at one bus end allows the design concerns to be simplified, but this comes at the cost of flexibility. With a transmitter located at the origin, a single bus termination at the far-end is required. The far-end termination absorbs the incident traveling wave. The flexibility lost with this arrangement is thus: if the single transmitter needed to be relocated on the bus, at any location other than the origin, we would be faced with a bus with one open-circuited end, and one properly terminated end. Locating the transmitter say in the middle of the bus may be desired to reduce (by ½) the maximum flight time from the transmitter to receiver.

Another new feature in 図 10-6 is clear in that every node branching off the main line results in stubs. The stubs should be minimized in any case, but have the unintended effect of locally changing the loaded impedance of the bus.

To a good approximation, the characteristic transmission line impedance seen into any cut point in the unloaded multipoint or multidrop bus is defined by $\sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. As capacitance is added to the bus in the form of devices and interconnections, the bus characteristic impedance is lowered. This may result in signal reflections from the impedance mismatch between the unloaded and loaded segments of the bus.

If the number of loads is constant and can be distributed evenly along the line, reflections can be reduced by changing the bus termination resistors to match the loaded characteristic impedance. Normally, the number of loads are not constant or distributed evenly and the reflections resulting from any mismatching should be accounted for in the noise budget.

10.2.2.3 Application Curve

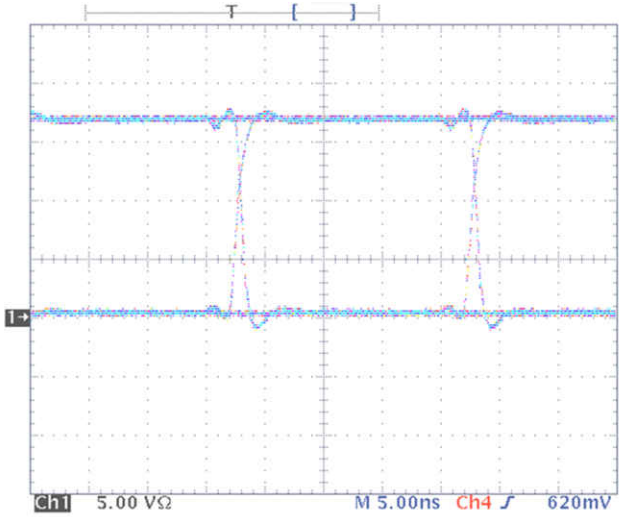


図 10-7. Typical Driver Output Eye Pattern in Multi-Drop System

11 Power Supply Recommendations

11.1

The LVDS drivers in this data sheet are designed to operate from a single power supply, with supply voltages in the range of 3.0 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than |±1 V|. Board-level and local device-level bypass capacitance should be used and are covered in *セクション 10.2.1.2.2*.

12 Layout

12.1 Layout Guidelines

12.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in 図 12-1.

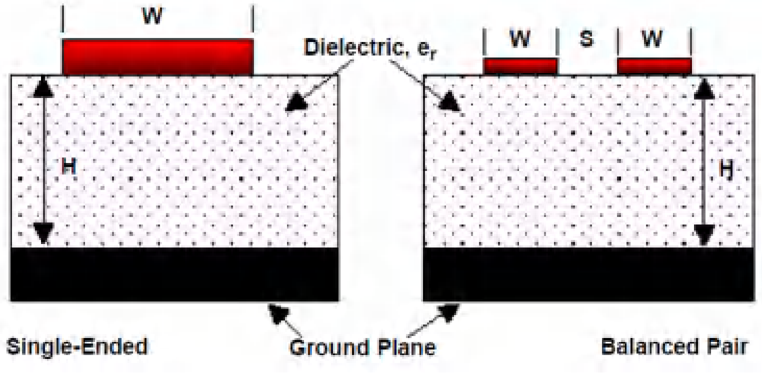


図 12-1. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1[2], 2[3], and 3[4] provide formulas for Z_O and t_{PD} for differential and single-ended traces. [2] [3] [4]

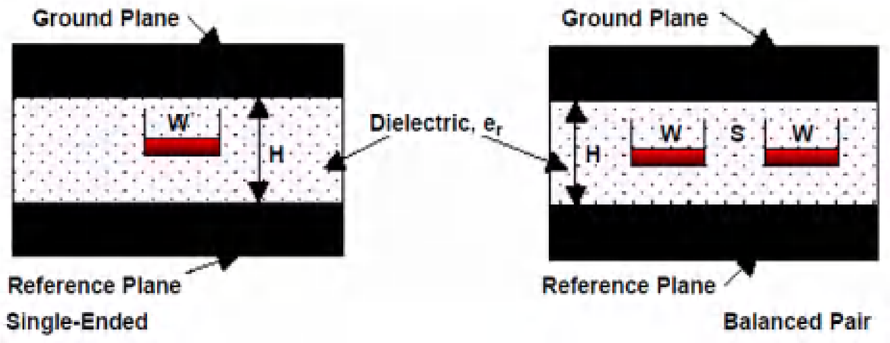


図 12-2. Stripline Topology

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[2] Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
[3] Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
[4] Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

12.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

12.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you should decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in 図 12-3.

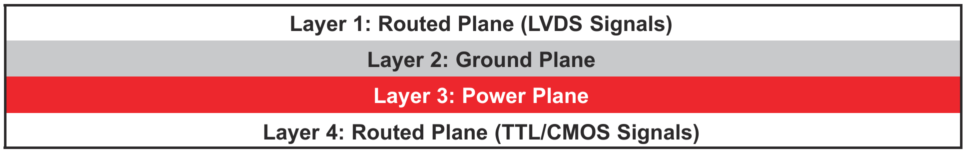

図 12-3. Four-Layer PCB Board

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The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in 図 12-4.

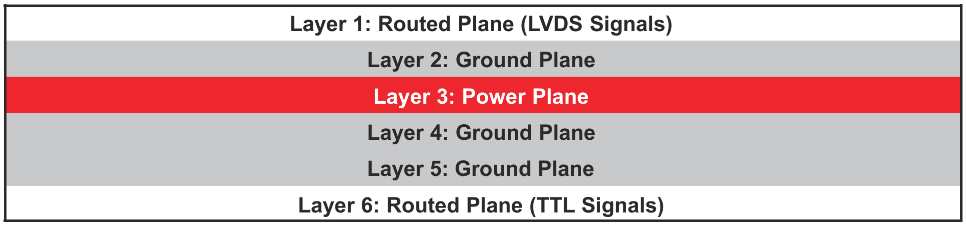


図 12-4. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

12.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces should be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

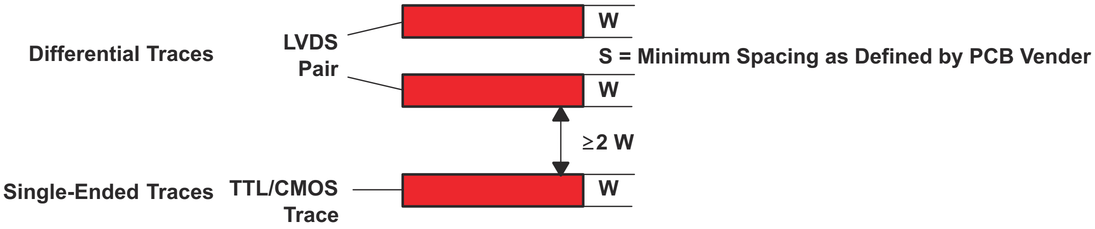


図 12-5. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

12.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

12.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in 図 12-6.

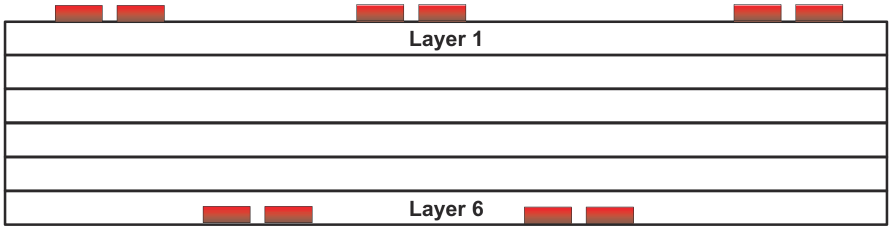


図 12-6. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in 図 12-7. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 0.5 pF to 1 pF in FR4.

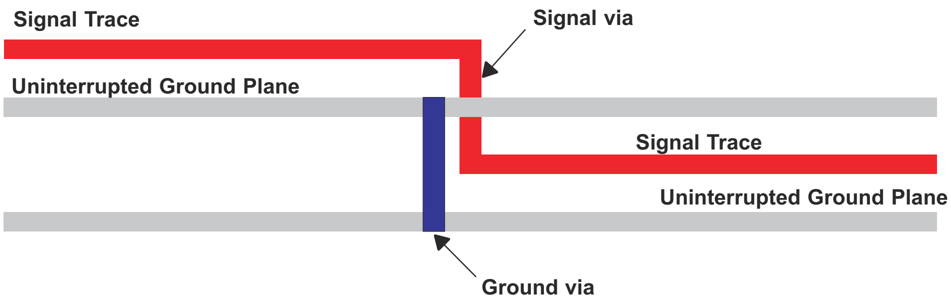


図 12-7. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Other LVDS Products

For other products and application notes in the LVDS and LVDM product families visit our Web site at http://www.ti.com/sc/datatran.

13.2 Documentation Support

13.2.1 Related Information

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

13.2.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.2.3 Related Links

表 13-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 13-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN55LVDS31	Click here	Click here	Click here	Click here	Click here
SN65LVDS31	Click here	Click here	Click here	Click here	Click here
SN65LVDS3487	Click here	Click here	Click here	Click here	Click here
SN65LVDS9638	Click here	Click here	Click here	Click here	Click here

13.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

13.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
Rogers™ is a trademark of Rogers Corporation.
すべての商標は、それぞれの所有者に帰属します。

13.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

13.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9762101Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762101Q2A SNJ55 LVDS31FK
5962-9762101QEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762101QEA SNJ55LVDS31J
5962-9762101QFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762101QFA SNJ55LVDS31W
SN55LVDS31W	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55LVDS31W
SN65LVDS31D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31DG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31DRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31NS.B	Active	Production	SOP (NS) | 16	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31NSR.B	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31PWG4	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS31PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31
SN65LVDS3487D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3487
SN65LVDS3487D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3487
SN65LVDS3487DG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3487
SN65LVDS3487DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3487
SN65LVDS3487DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3487

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS9638D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638
SN65LVDS9638D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638
SN65LVDS9638DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638
SN65LVDS9638DG4.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638
SN65LVDS9638DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXG
SN65LVDS9638DGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXG
SN65LVDS9638DGKG4	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXG
SN65LVDS9638DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXG
SN65LVDS9638DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXG
SN65LVDS9638DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L38
SN65LVDS9638DGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L38
SN65LVDS9638DGNG4	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L38
SN65LVDS9638DGNG4.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L38
SN65LVDS9638DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L38
SN65LVDS9638DGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L38
SN65LVDS9638DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638
SN65LVDS9638DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638
SNJ55LVDS31FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762101Q2A SNJ55LVDS31FK
SNJ55LVDS31J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762101QEA SNJ55LVDS31J
SNJ55LVDS31W	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762101QFA SNJ55LVDS31W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55LVDS31, SN65LVDS31 :

- Catalog : SN75LVDS31

- Enhanced Product : SN65LVDS31-EP

- Space : SN55LVDS31-SP

NOTE: Qualified Version Definitions:

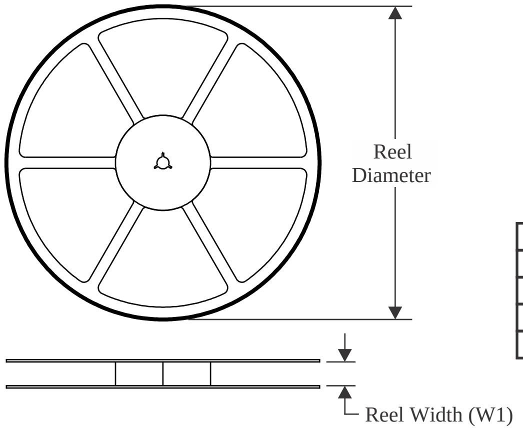
- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

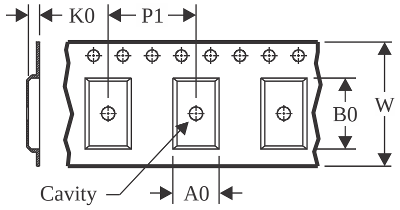
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

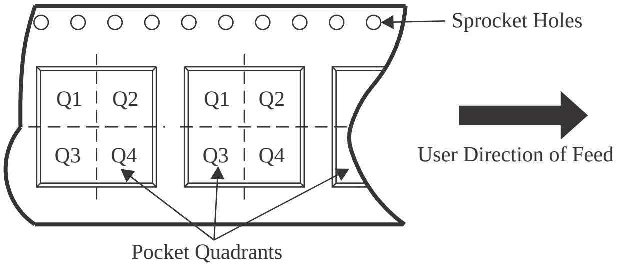


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

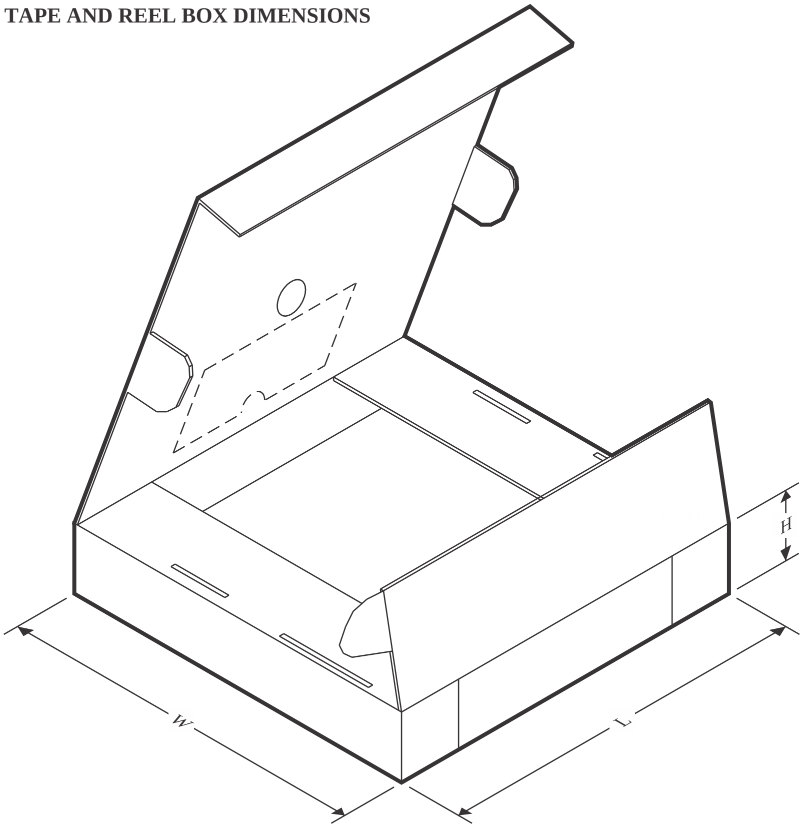
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS31DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS31NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN65LVDS31PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS3487DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS9638DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS9638DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS9638DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

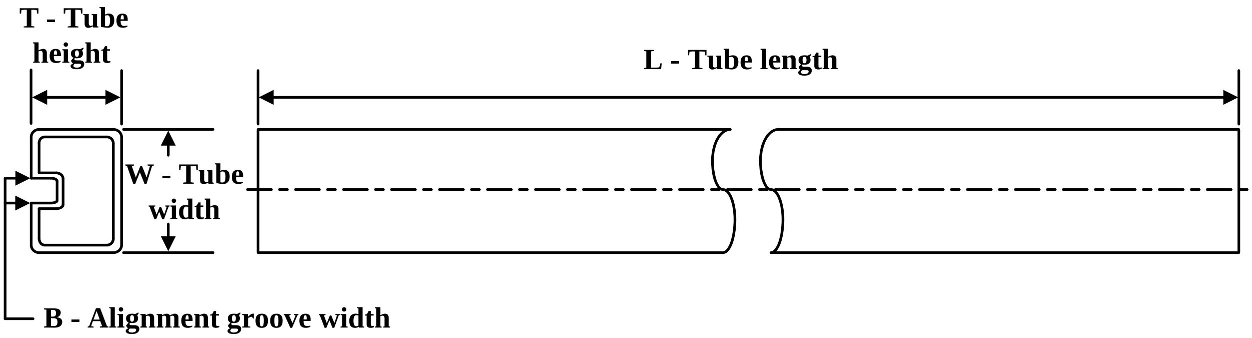
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

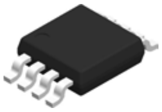
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS31DR	SOIC	D	16	2500	353.0	353.0	32.0
SN65LVDS31NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN65LVDS31PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDS3487DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS9638DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDS9638DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
SN65LVDS9638DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

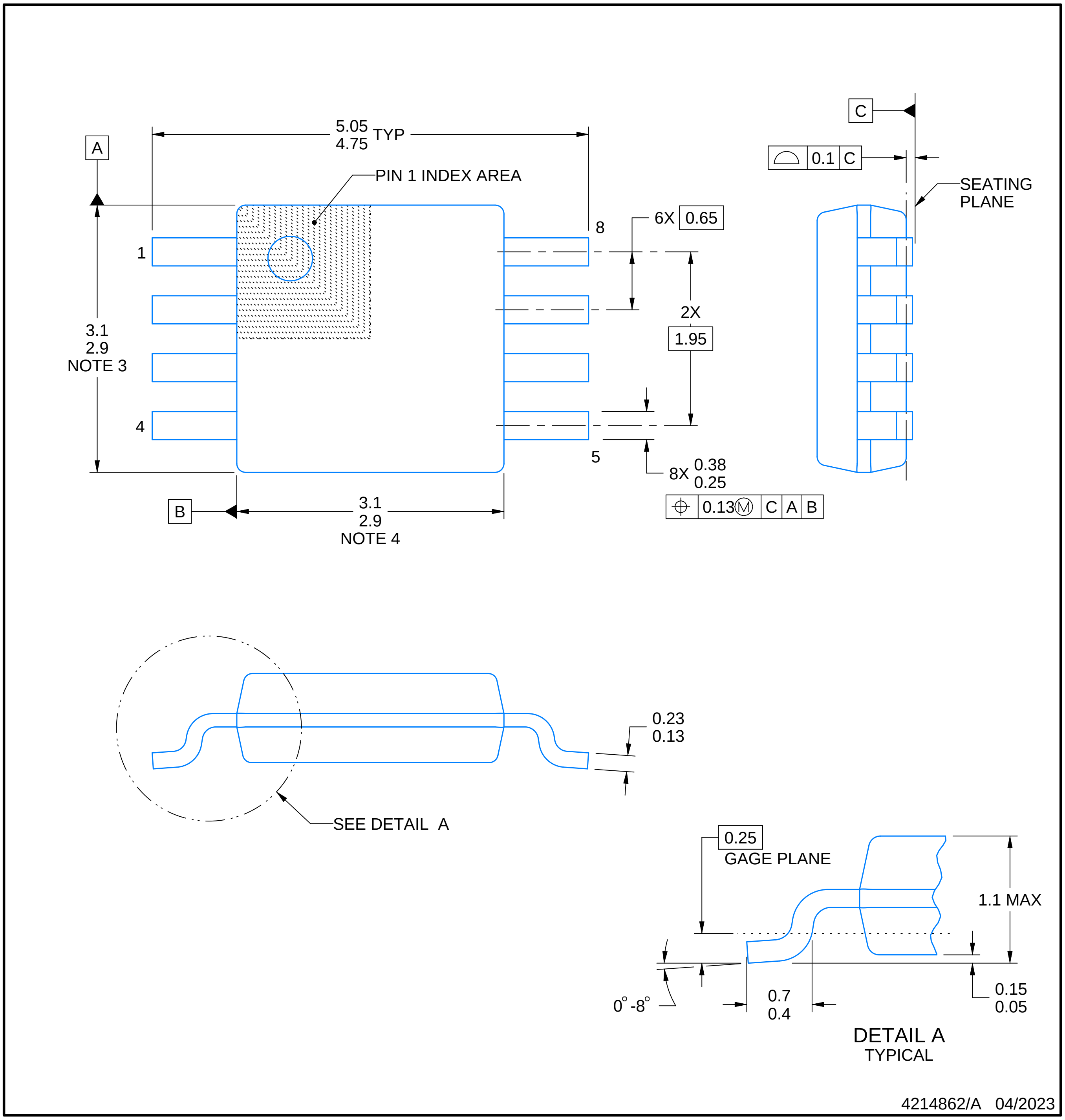
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9762101Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9762101QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN55LVDS31W	W	CFP	16	25	506.98	26.16	6220	NA
SN65LVDS31D	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS31D.B	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS31DG4	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS31NS.B	NS	SOP	16	50	530	10.5	4000	4.1
SN65LVDS31PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS31PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS31PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS3487D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS3487D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS3487DG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS9638D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDS9638D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDS9638D.B	D	SOIC	8	75	507	8	3940	4.32
SN65LVDS9638D.B	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDS9638DG4	D	SOIC	8	75	507	8	3940	4.32
SN65LVDS9638DG4.B	D	SOIC	8	75	507	8	3940	4.32
SNJ55LVDS31FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55LVDS31W	W	CFP	16	25	506.98	26.16	6220	NA



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

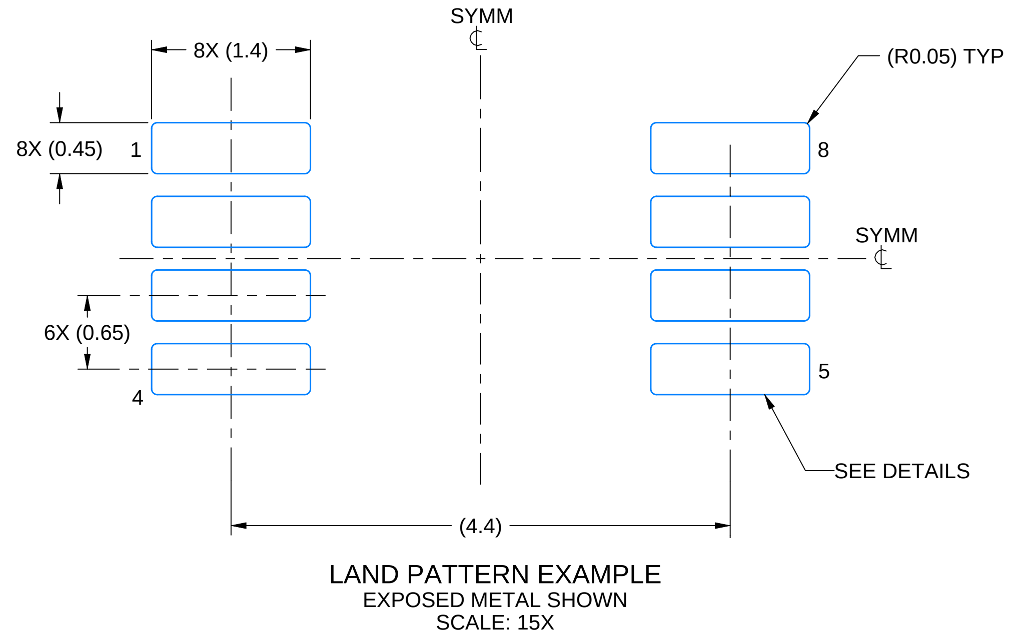


4214862/A 04/2023

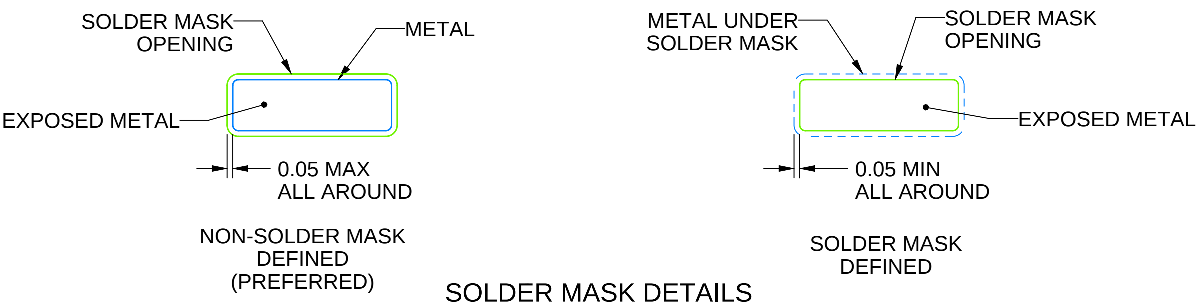
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

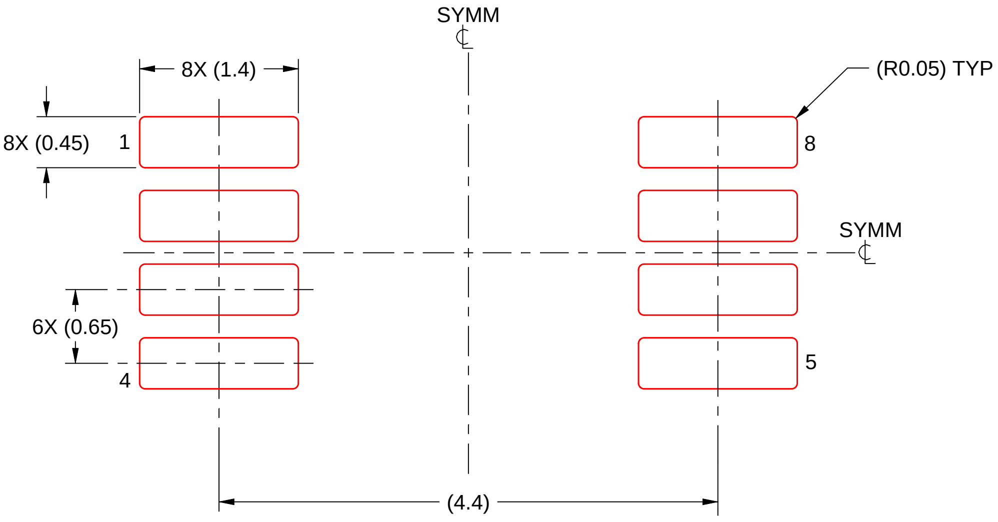


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

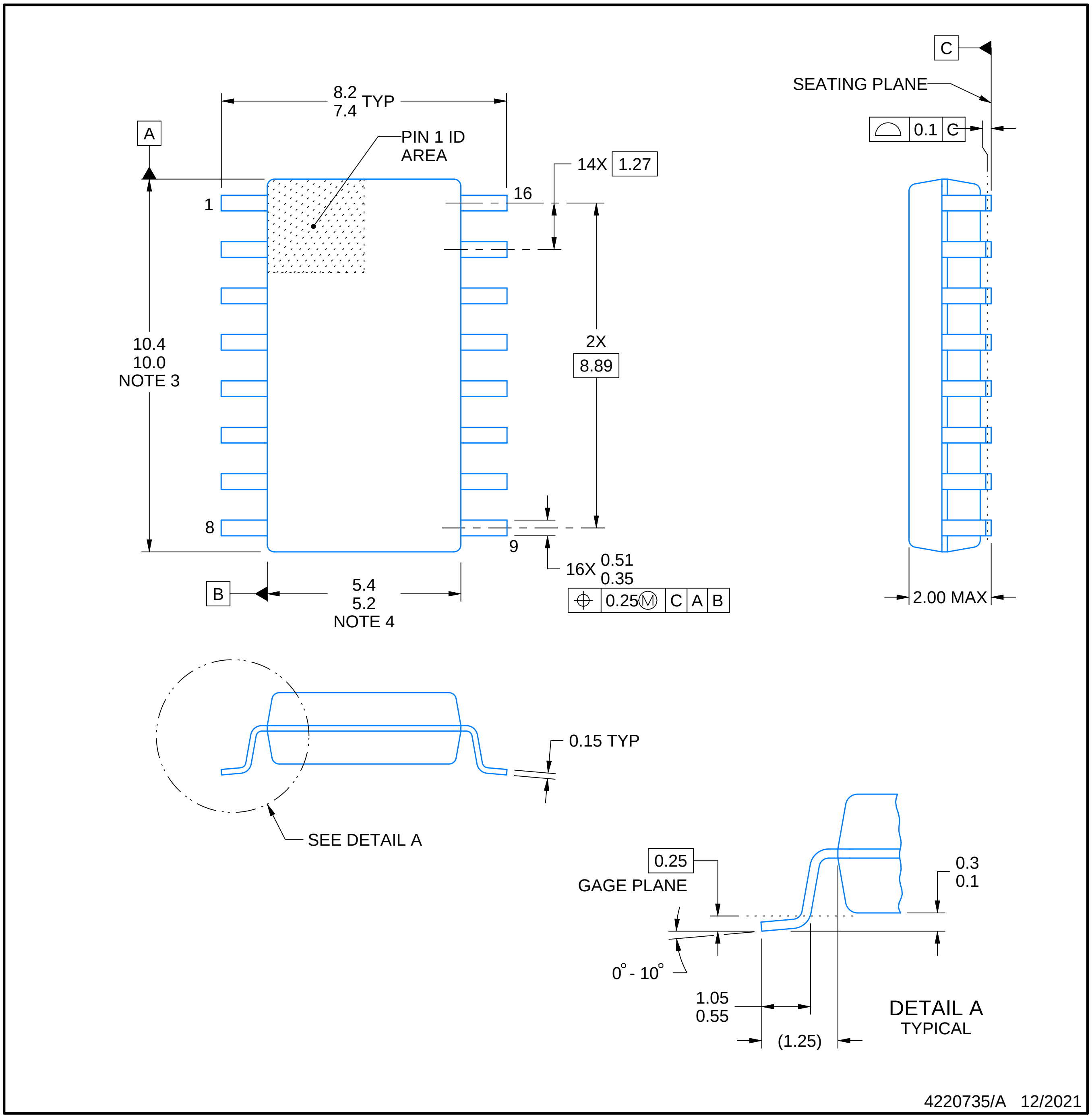


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

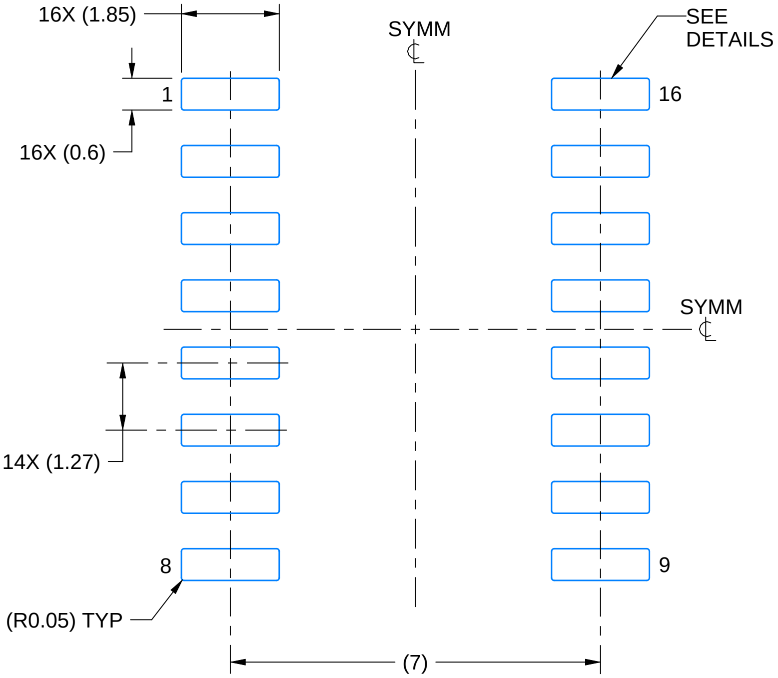
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

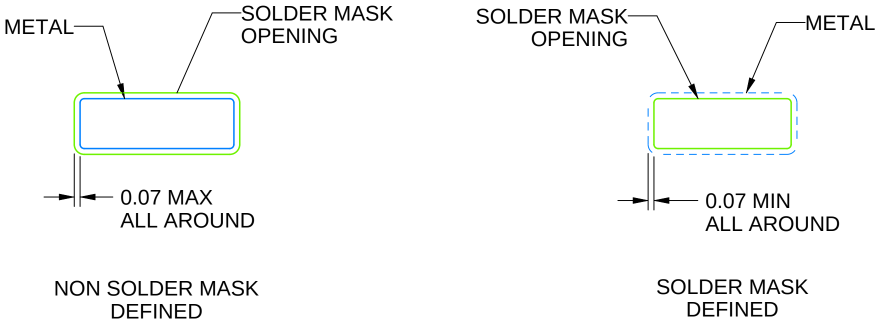


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

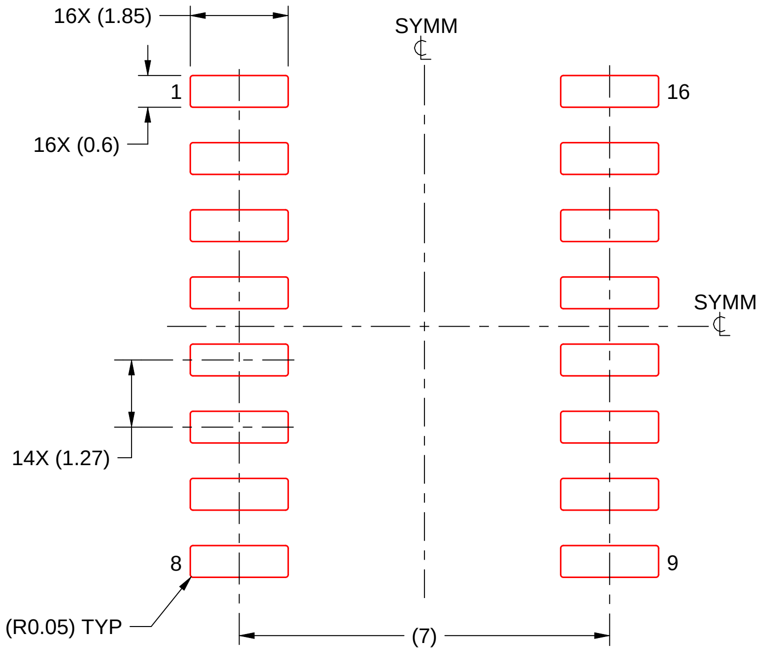


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

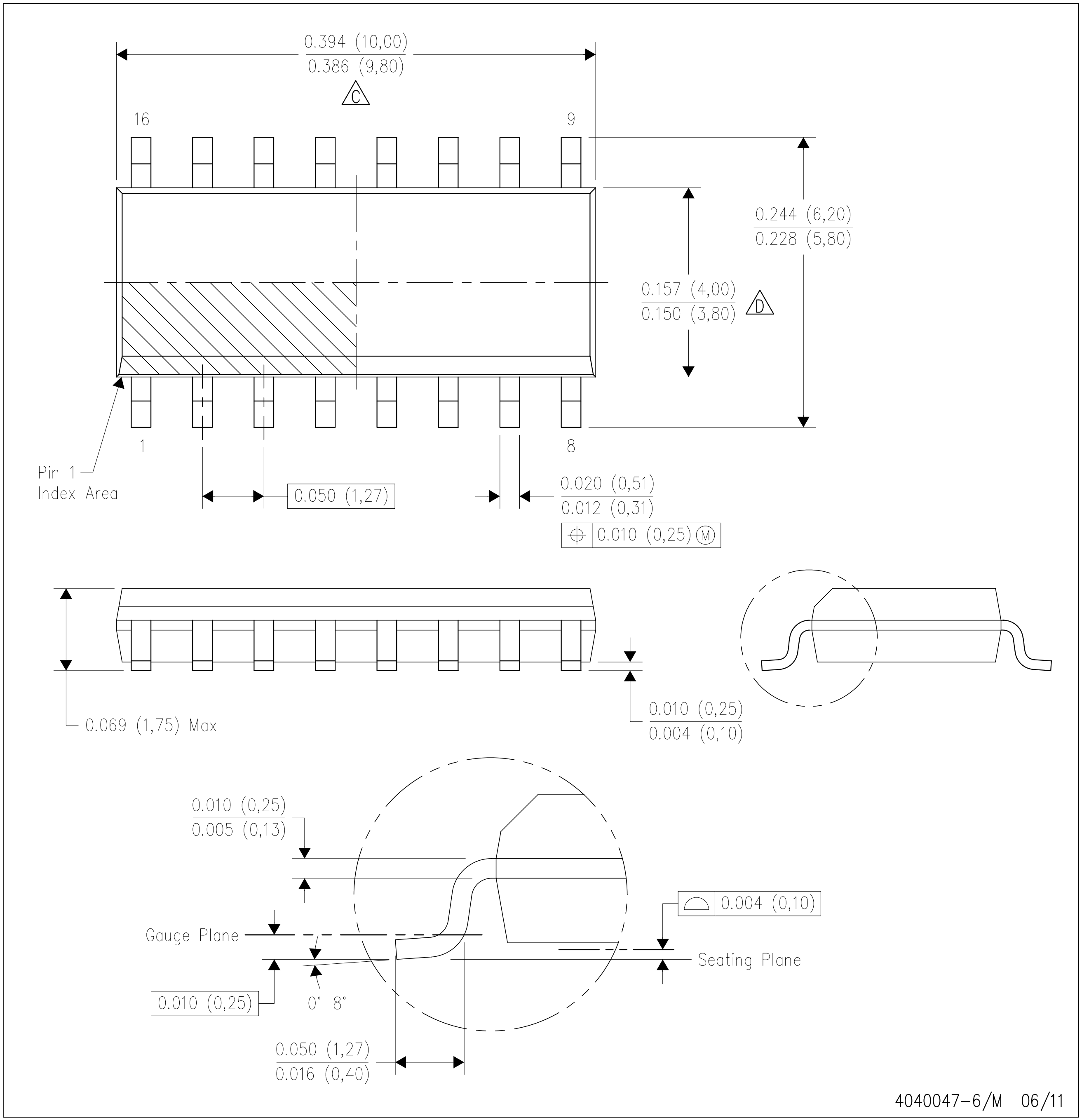


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

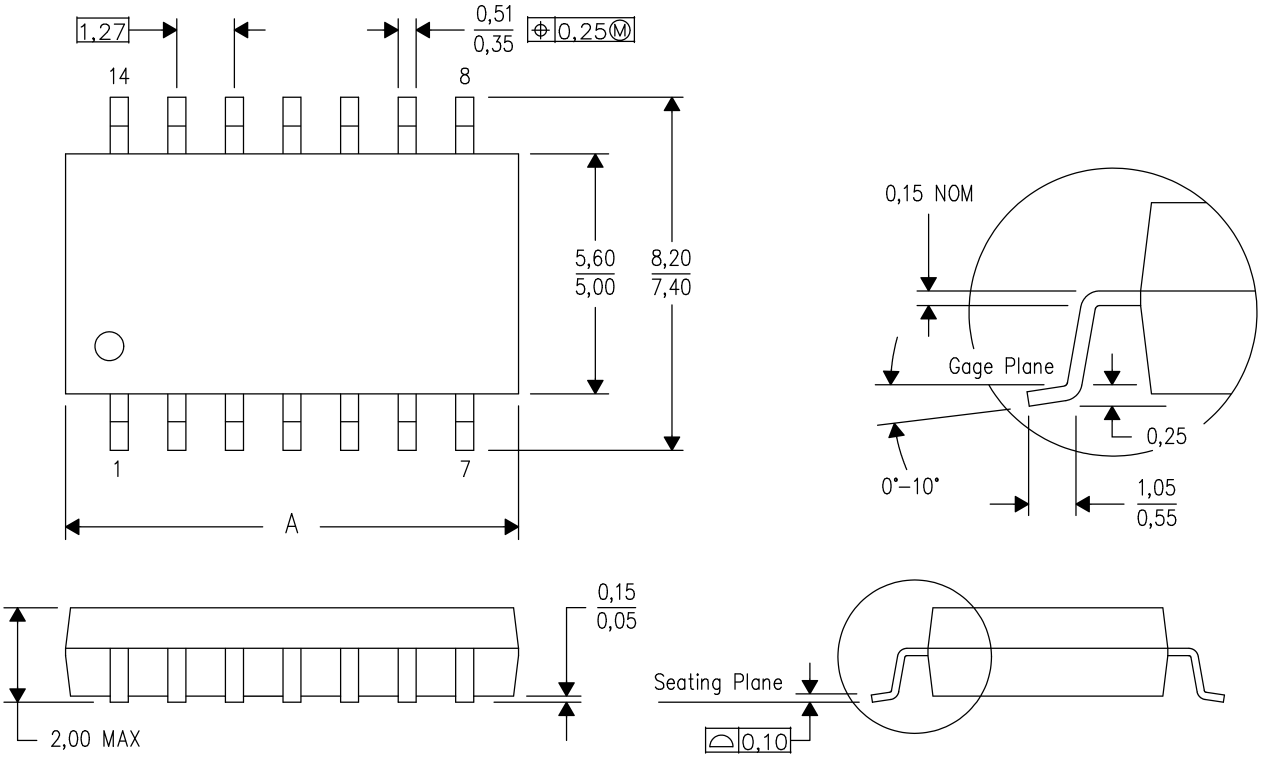


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

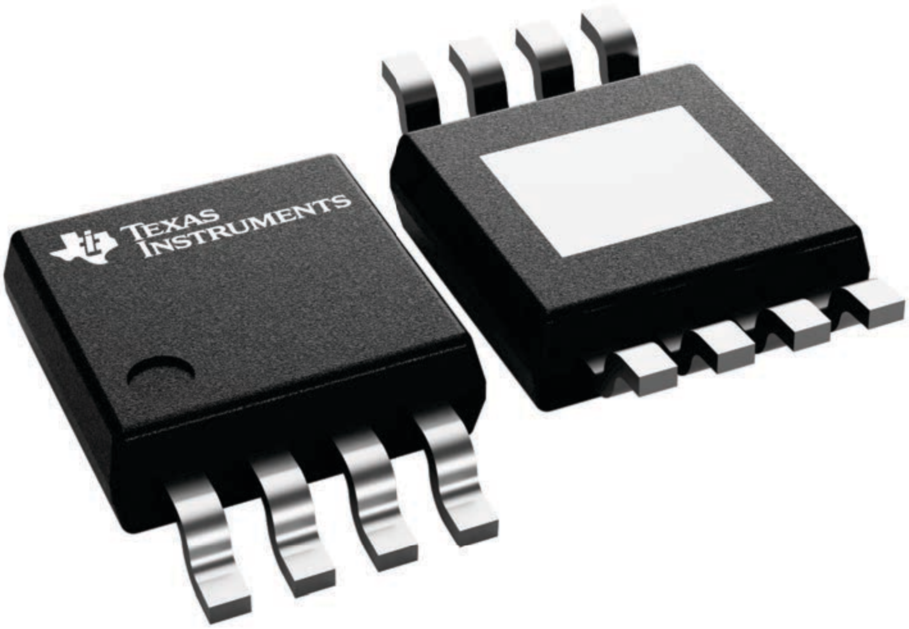
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

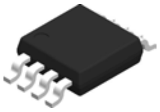
DGN 8 **PowerPAD™ HVSSOP - 1.1 mm max height**

3 x 3, 0.65 mm pitch SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



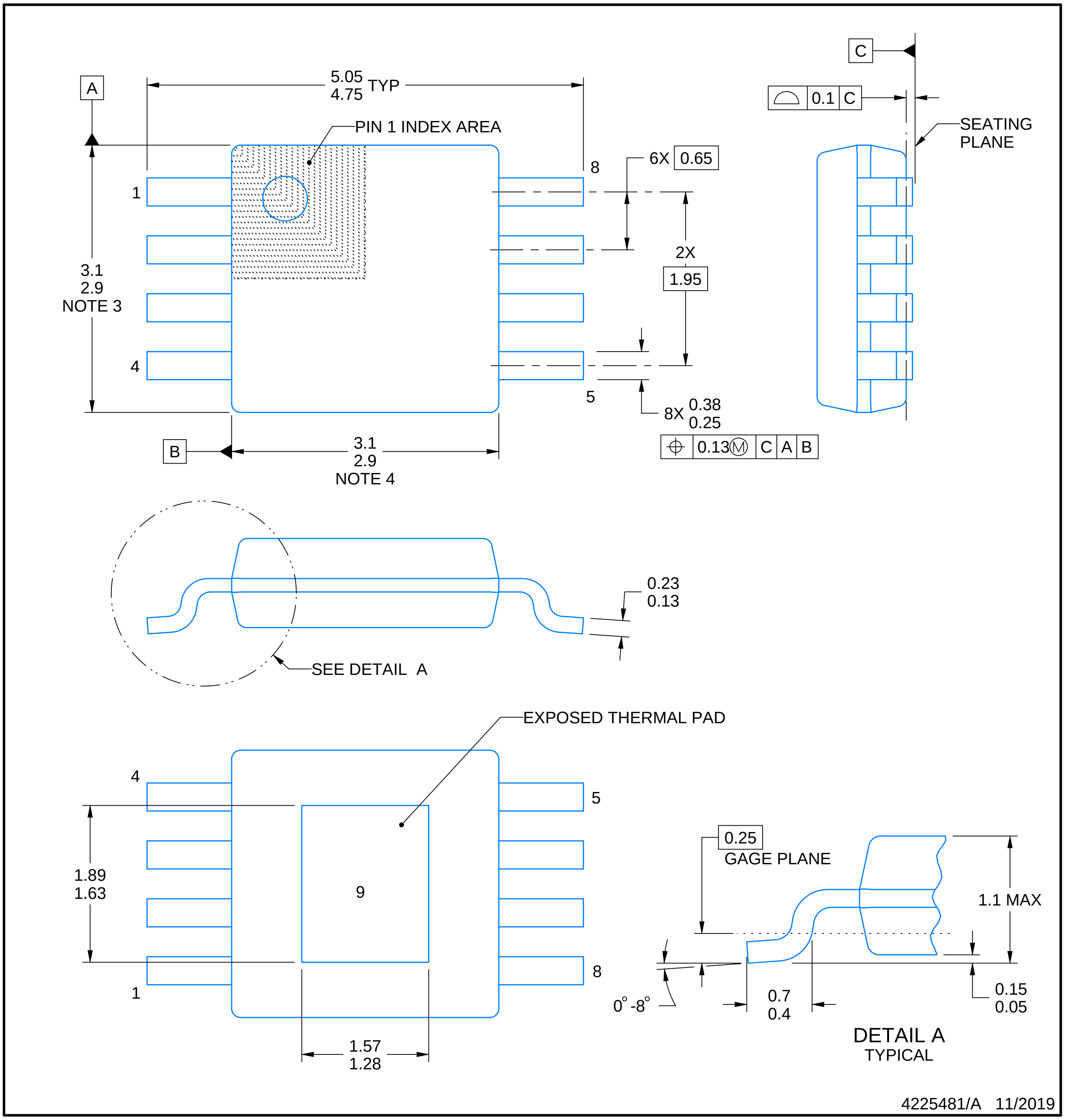
PACKAGE OUTLINE



DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

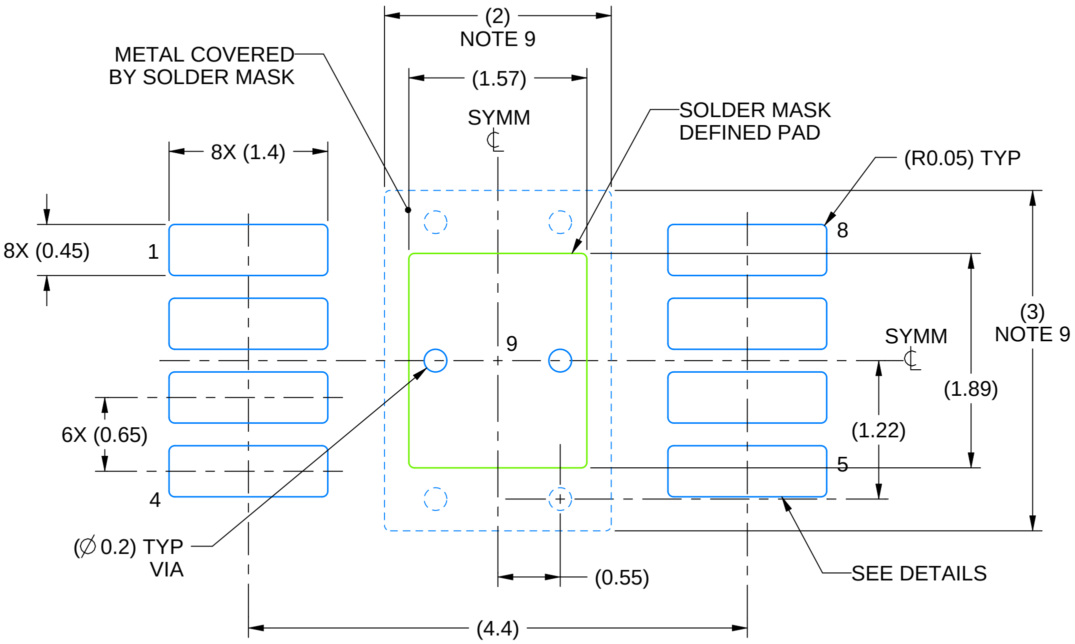


4225481/A 11/2019

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

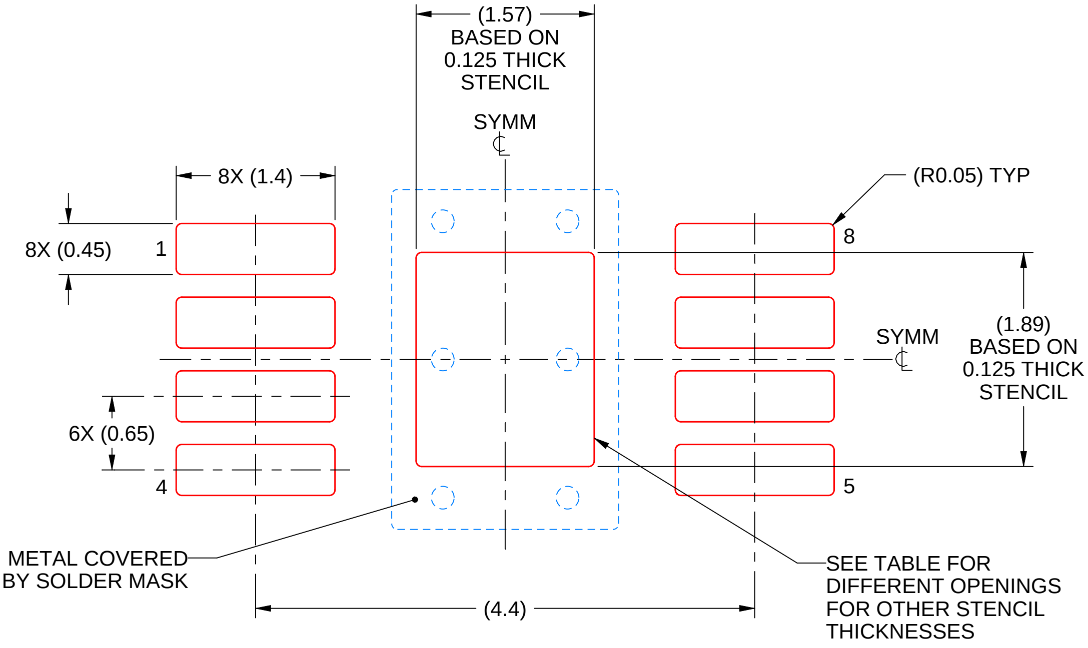
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN



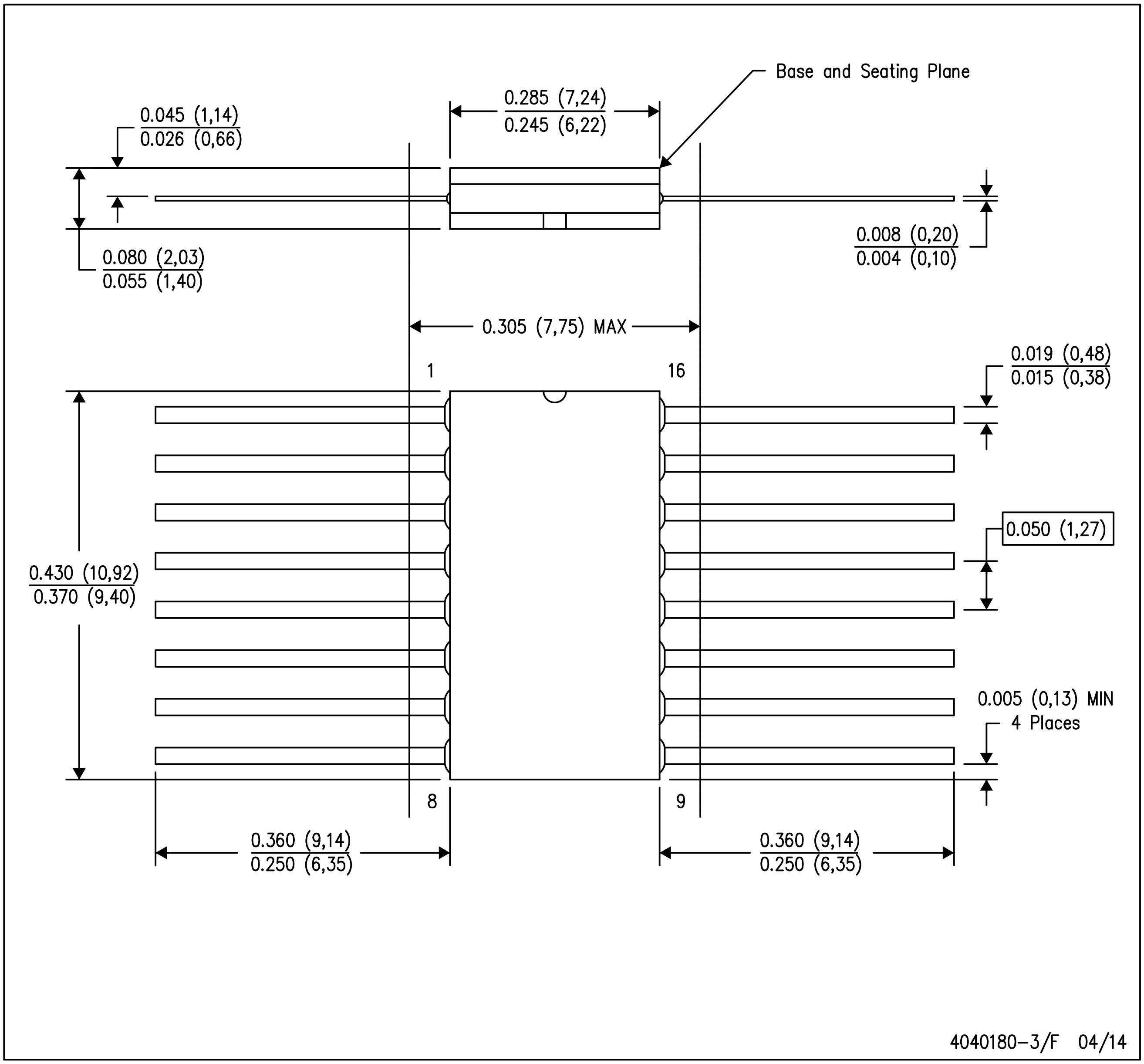
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

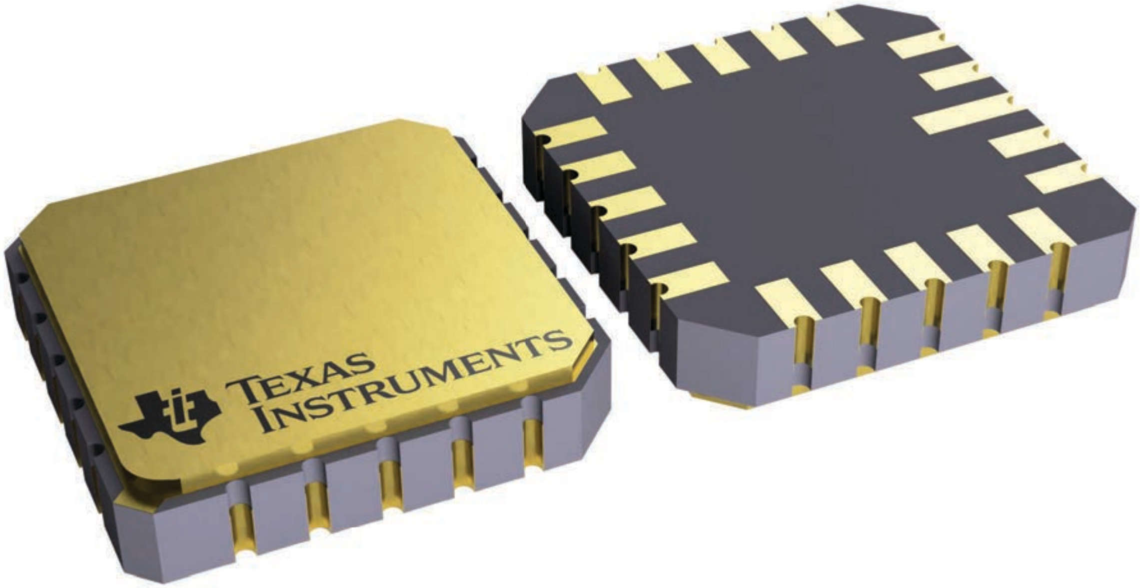
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

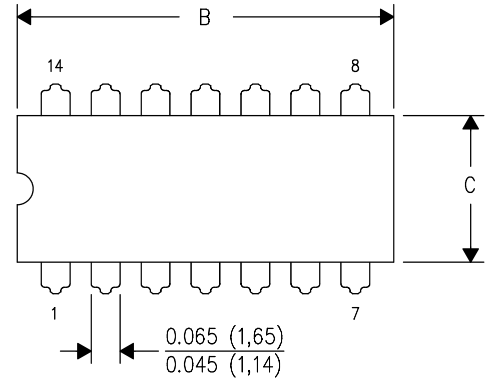
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

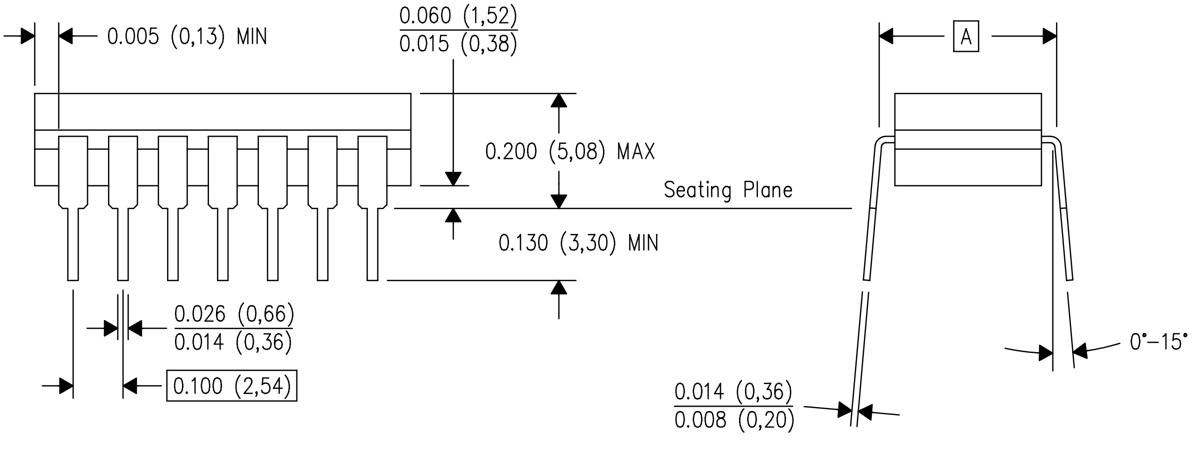


J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN

PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



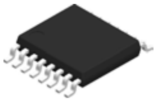


4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

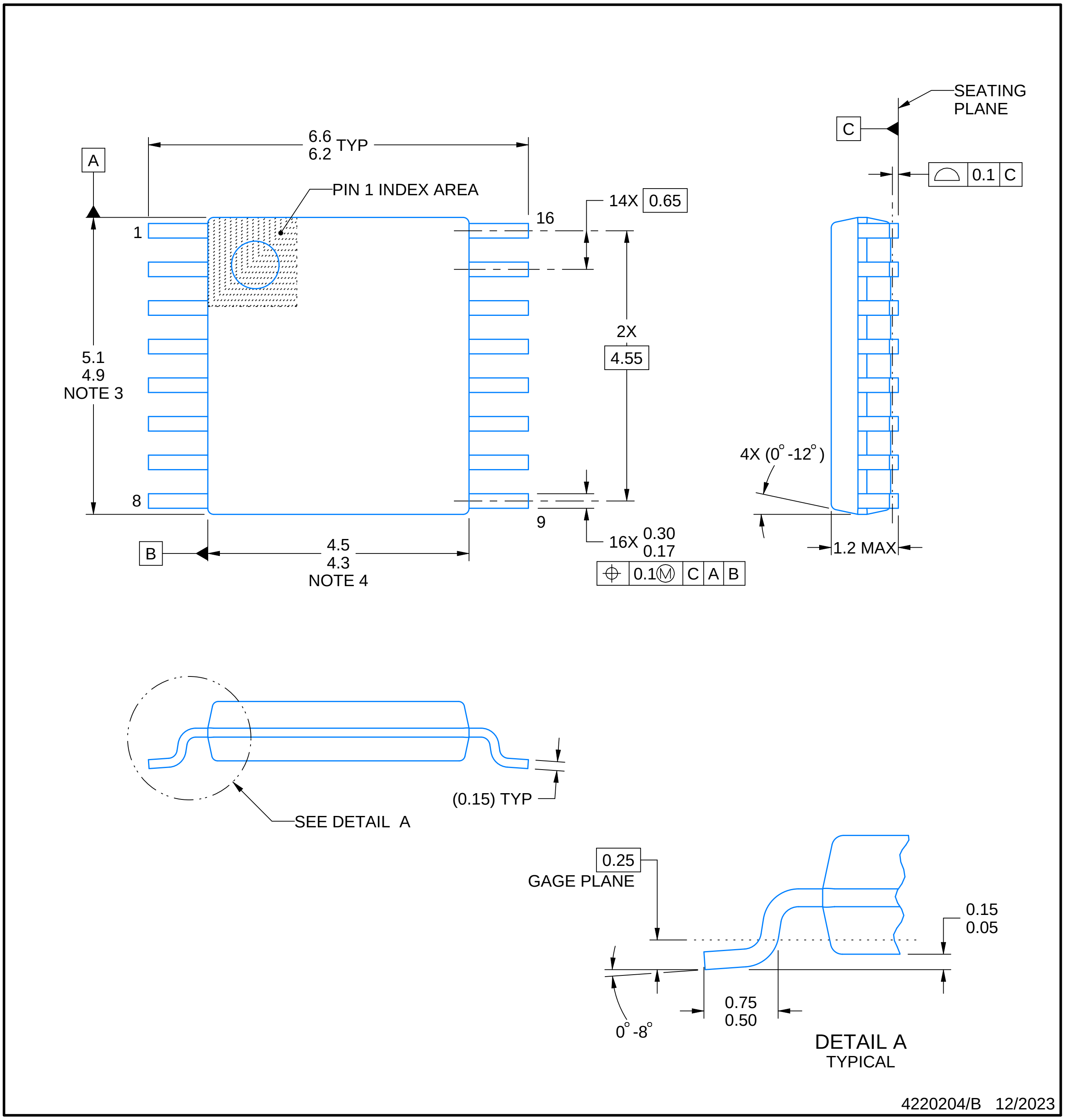
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

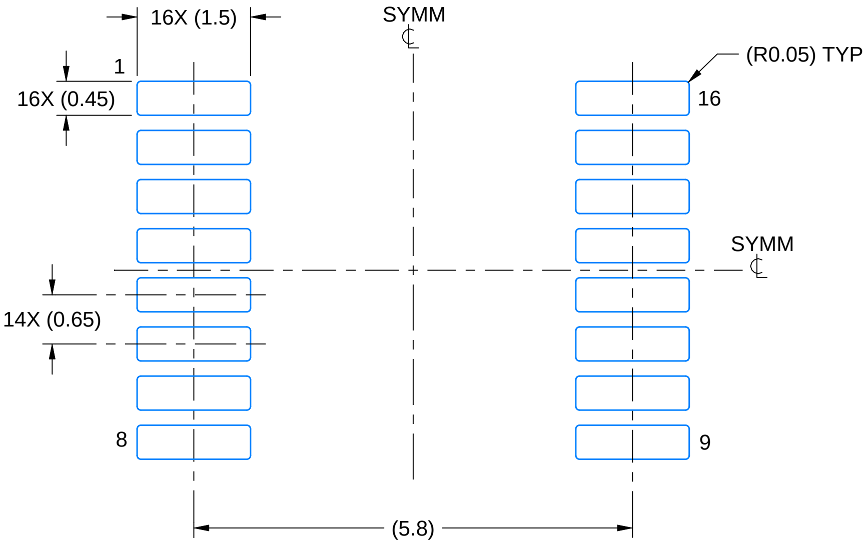
SMALL OUTLINE PACKAGE



4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

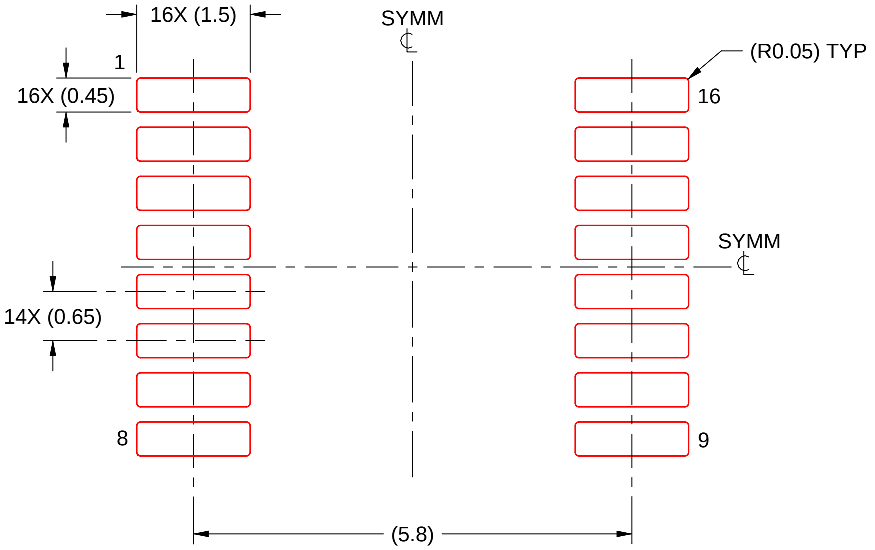
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

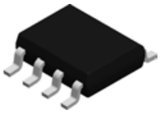


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

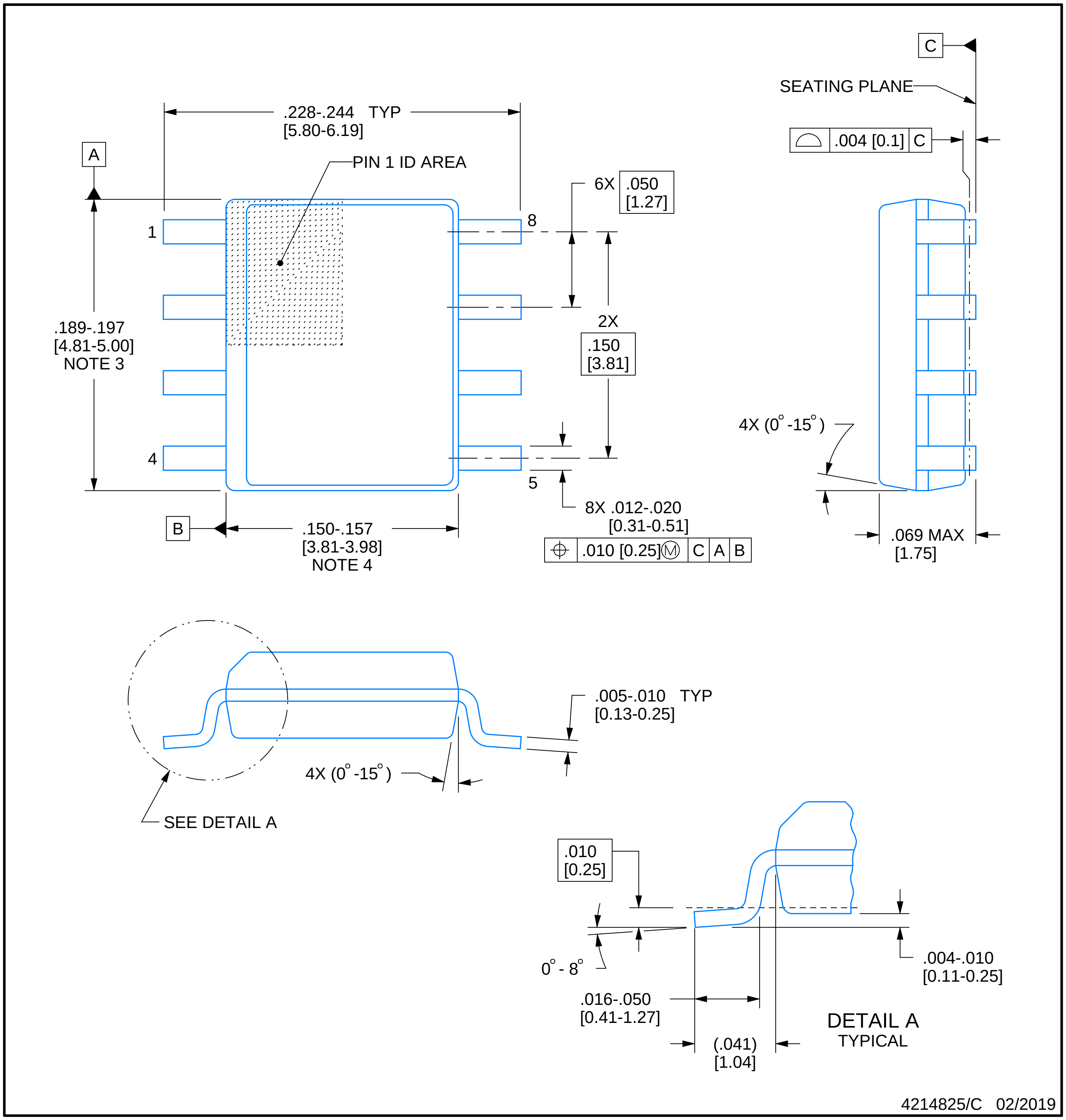


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

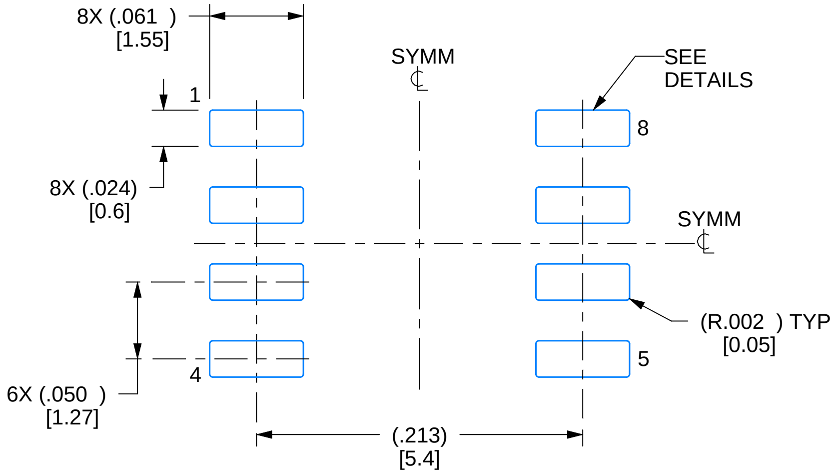
SMALL OUTLINE INTEGRATED CIRCUIT



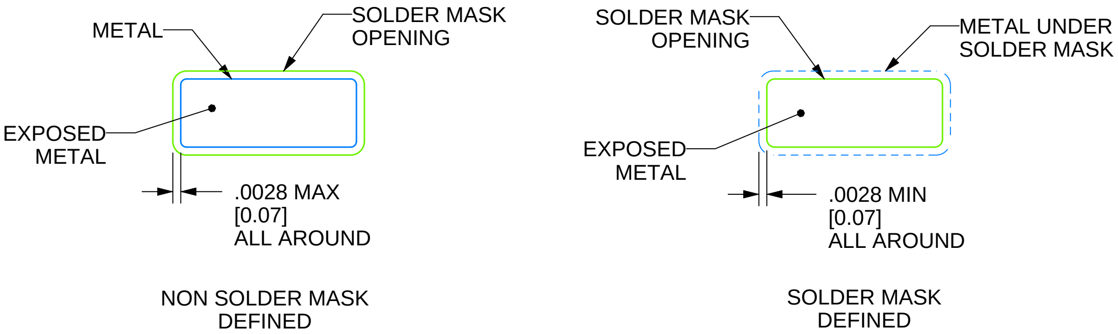
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



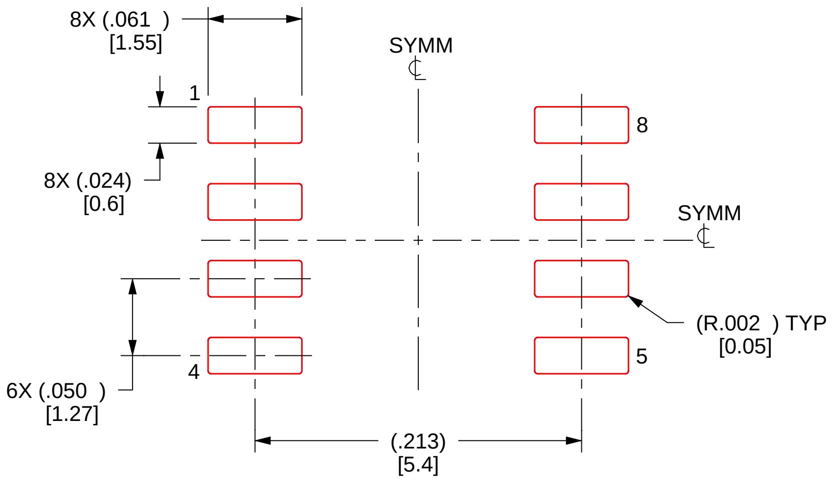
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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