SN65HVD3x、3.3V、全二重 RS-485 ドライバとレシーバ

1 特長

- 1/8 ユニット負荷オプション使用可能 (バス上に最大 256 個のノード)
- 15kV HBM を超えるバス・ピンの ESD 保護
- 1Mbps、5Mbps、26Mbps の信号速度に対応する、オプションのドライバ出力遷移時間
  – ラインの信号レートとは、1 秒あたりの電圧遷移回数を bps (ビット/秒) 単位で表したものです
- 低電流のスタンバイ・モード:1μA 未満
- 電源オンおよび電源オフ時のグリッチ・フリー保護によりホットプラグ・アプリケーションに対応
- 5V 許容の入力
- バス・アイドル、開路、短絡のフェイルセーフ
- ドライバ電流制限および過熱保護
- RS-422 および RS-485 ネットワーク用に設計されています
- 5V デバイスが利用可能、SN65HVD50-55

2 アプリケーション

- ユーティリティ・メーター
- DTE および DCE インターフェイス
- 産業用、プロセス、およびビル・オートメーション
- 販売時点情報管理 (POS) ピンとネットワーク

3 概要

SN65HVD3x デバイスは、3.3V 電源で動作する 3 ステート差動ライン・ドライバおよび差動入力ライン・レシーバです。

各ドライバおよびレシーバは、全二重バス通信設計用に、独立した入力および出力ピンを備えています。これらの製品は、最大
1500m のケーブル長で RS-422 と RS-485 のデータ転送を行うように設計されています。

SN65HVD30、SN65HVD31、SN65HVD32 デバイスは、外部イネーブル・ピンなしで完全にイネーブルになります。

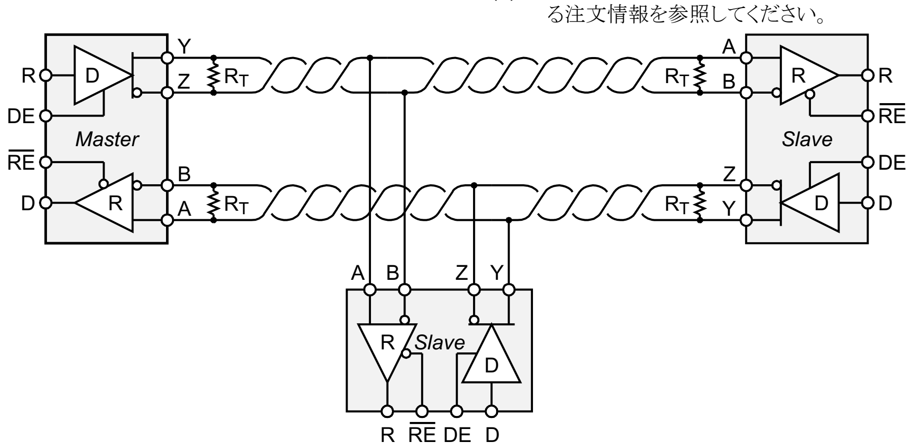
SN65HVD33、SN65HVD34、SN65HVD35 デバイスは、アクティブ HIGH のドライバ・イネーブルと、アクティブ LOW のレシーバ・イネーブルを備えています。ドライバとレシーバの両方をディセーブルにすると、1μA 未満の低いスタンバイ電流が得られます。

すべてのデバイスは、-40℃～85℃の周囲温度で動作が規定されています。消費電力が低いため、パッケージ・オプションに応じて、105℃または 125℃までの温度で動作できます。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN65HVD30	SOIC (8)	4.90mm × 3.91mm
SN65HVD31		
SN65HVD32		
SN65HVD33	SOIC (14)	8.65mm × 3.91mm
	VQFN (20)	4.50mm × 3.50mm
SN65HVD34	SOIC (14)	8.65mm × 3.91mm
SN65HVD35		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision L (January 2017) to Revision M (February 2023)	Page
• Changed the D package values the *Thermal Information*	8

Changes from Revision K (October 2015) to Revision L (January 2017)	Page
• Changed text From: "defaults to Y high and Z low" To: "defaults to Y low and Z high" in the *Low-Power Standby Mode* section	20

Changes from Revision J (July 2015) to Revision K (October 2015)	Page
• 「デバイス情報」の表にあるデバイス・リストを、「パッケージ・オプションの付録」のリストと一致するよう変更。	1
• Changed device listing in the *Pinout Configuration* section to match the *Package Option Addendum* listing	4
• Changed device listing in the Thermal Information table to match the *Package Option Addendum* listing	8

Changes from Revision I (April 2010) to Revision J (July 2015)	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

Changes from Revision H (May 2009) to Revision I (April 2010)	Page
• 「概要」の 3 番目の文の表現を変更	1
• Changed the labels in the *SN65HVD3x Drivers Operate Correctly After Bus Contention Faults* image	22

Changes from Revision G (December 2008) to Revision H (May 2009)	Page
• Added explanatory notes for pin 6 and pin 13 to the 14-Pin SOIC	4
• Added explanatory notes for pin 1 and pin 10 to the 20-Pin VQFN	4

- Added Supply current typical value of 3.8 mA for SN65HVD31, SN65HVD3 in the *Supply Current Characteristics* table....11
- Changed characteristic graph for 図 7-6 13
- Changed characteristic graph for 図 7-7 13
- Added subsection *Safe Operation With Bus Contention* 22

Changes from Revision F (July 2008) to Revision G (December 2008)	Page

- 次のように変更:「特長」で「5V デバイスが利用可能、SN65HVD50-59」から「5V デバイスが利用可能、SN65HVD50-55」へ。....1
- 「概要」から SN65HVD36 および SN65HVD37 を削除....1
- 「概要」から SN65HVD38 および SN65HVD39 を削除....1
- 「概要」の最後の 2 つの段落を削除....1
- Deleted SN65HVD36, SN65HVD37 from the 8-Pin SOIC....4
- Deleted SN65HVD36, SN65HVD37 from the the 14-Pin SOIC....4
- Deleted devices SN65HVD36, SN65HVD38 from the *Recommended Operating Conditions* 8
- Deleted devices SN65HVD37, SN65HVD39 from the *Recommended Operating Conditions* 8
- Deleted all HVD36, HVD38, HVD37, HVD39 from the *Electrical Characteristics: Driver* table....9
- Added added last sentence to note 4 in the *Electrical Characteristics: Driver* table....9
- Deleted all HVD36, HVD38, HVD37, HVD39 from the *Electrical Characteristics: Receiver* table....10
- Deleted all HVD36, HVD38, HVD37, HVD39 rows from the *Supply Current Characteristics* table....11
- Deleted all HVD36, HVD38, HVD37, HVD39 from the *Switching Characteristics: Driver* table....11
- Deleted HVD36, HVD38, HVD37, and HVD39 from the *Switching Characteristics: Receiver* table....11
- Deleted *Receiver Equalization Characteristics* table....13
- Added subsection *Driver Output Current Limiting* 21
- Added subsection *Hot-Plugging* 21
- Added subsection *Receiver Failsafe* 22
- Deleted SN65HVD38 and SN65HVD39 from 表 8-1 title....24
- Deleted SN65HVD38 and SN65HVD39 from 表 8-2 title....24
- Deleted SN65HVD36 and SN65HVD37 from 表 8-3 title....24
- Deleted SN65HVD36 and SN65HVD37 from 表 8-4 title....24
- Deleted SN65HVD36 and SN65HVD37 from first row of 表 8-5 24
- Deleted SN65HVD37, SN65HVD38 and SN65HVD39 from second row of 表 8-5 24

Changes from Revision E (March 2008) to Revision F (July 2008)	Page

- 次のように変更:「特長」で「ANSI TIA/EIA-485-A と RS-422 互換の要件を満たす、または超える性能」から「RS-422 および RS-485 ネットワーク用に設計」へ。....1
- Added Table Note 4 in the *Electrical Characteristics: Driver* table....9

Changes from Revision D (January 2008) to Revision E (March 2008)	Page

- スペルを「termperatures」から「temperatures」に変更....1

5 Device Comparison

表 5-1. Device Features

BASE PART NUMBER	SIGNALING RATE	UNIT LOADS	ENABLES
SN65HVD30	26 Mbps	1/2	No
SN65HVD31	5 Mbps	1/8	No
SN65HVD32	1 Mbps	1/8	No
SN65HVD33	26 Mbps	1/2	Yes
SN65HVD34	5 Mbps	1/8	Yes
SN65HVD35	1 Mbps	1/8	Yes

表 5-2. Improved Replacement for Devices

PART NUMBER	REPLACE WITH	BENEFITS
MAX3491 MAX3490	SN65HVD33 SN65HVD30	Better ESD protection (15 kV versus 2 kV, or not specified) Higher Signaling Rate (26 Mbps versus 10 Mbps) Fractional Unit Load (64 Nodes versus 32)
MAX3491E MAX3490E	SN65HVD33 SN65HVD30	Higher Signaling Rate (26 Mbps versus 12 Mbps) Fractional Unit Load (64 Nodes versus 32)
MAX3076E MAX3077E	SN65HVD33 SN65HVD30	Higher Signaling Rate (26 Mbps versus 16 Mbps) Lower Standby Current (1 µA versus 10 µA)
MAX3073E MAX3074E	SN65HVD34 SN65HVD31	Higher Signaling Rate (5 Mbps versus 500 kbps) Lower Standby Current (1 µA versus 10 µA)
MAX3070E MAX3071E	SN65HVD35 SN65HVD32	Higher Signaling Rate (1 Mbps versus 250 kbps) Lower Standby Current (1 µA versus 10 µA)

6 Pin Configuration and Functions

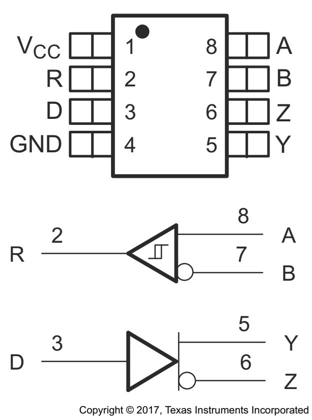
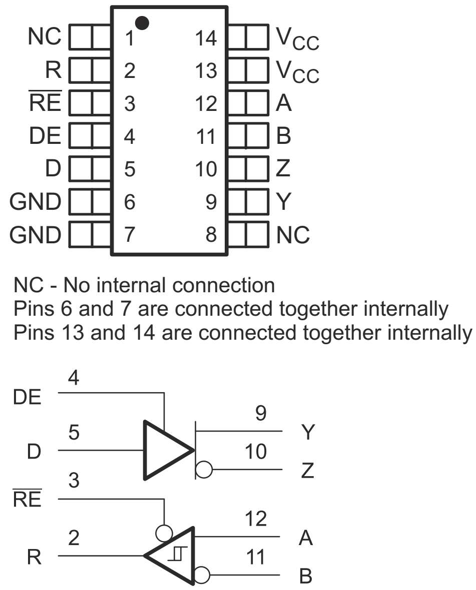
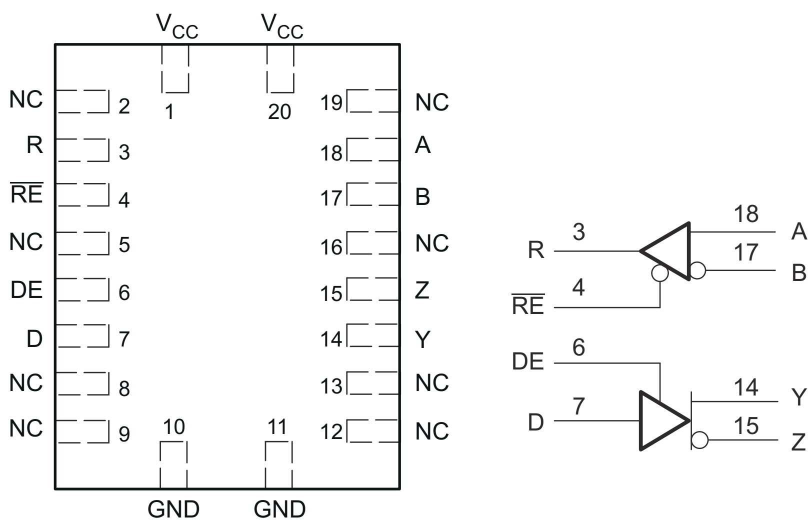


図 6-1. SN65HVD30, SN65HVD31, SN65HVD32, D Package 8-Pin SOIC Top View



NC - No internal connection
Pins 6 and 7 are connected together internally
Pins 13 and 14 are connected together internally

図 6-2. SN65HVD33, SN65HVD34, SN65HVD35 D Package 14-Pin SOIC Top View



NC - No internal connection
Pins 10 and 11 are connected together internally
Pins 1 and 20 are connected together internally

図 6-3. SN65HVD33 RHL Package 20-Pin VQFN Top View

表 6-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	D (8-Pins)	D (14-Pins)	RHL (20-Pins)		
A	8	12	18	Bus input	Receiver input (complementary to B)
B	7	11	17	Bus input	Receiver input (complementary to A)
D	3	5	7	Digital input	Driver data input
DE	—	4	6	Digital input	Driver enable, active high
GND	4	6, 7	10, 11	Reference potential	Local device ground
NC	—	1, 8	2, 5, 8, 9, 12, 13, 16, 19	No connect	No connect; must be left floating
R	2	2	3	Digital output	Receive data output
$\overline{RE}$	—	3	4	Digital output	Receiver enable, active low
V_{CC}	1	13, 14	1, 20	Supply	3-V to 3.6-V supply
Y	5	9	14	Bus output	Driver output (complementary to Z)
Z	6	10	15	Bus output	Driver output (complementary to Y)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted[(1)] [(2)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
$V_{(A)}$, $V_{(B)}$, $V_{(Y)}$, $V_{(Z)}$	Voltage at any bus terminal (A, B, Y, Z)	–9	14	V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 Ω. See 図 8-13 (A, B, Y, Z)[(3)]	–50	50	V
V_I	Input voltage (D, DE, $\overline{RE}$)	–0.5	7	V
I_O	Output current (receiver output only, R)		11	mA
T_{stg}	Storage Temperature		125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 7.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) This tests survivability only and the output state of the receiver is not specified.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	Bus pins and GND	±16000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_I or V_{IC}	Voltage at any bus pin (separately or common mode)		–7[(1)]		12	V
$1/t_{UI}$	Signaling rate	SN65HVD30, SN65HVD33			26	Mbps
		SN65HVD31, SN65HVD34			5	
		SN65HVD32, SN65HVD35			1	
R_L	Differential load resistance		54	60		Ω
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_J	Junction temperature		–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

7.4 Thermal Information

THERMAL METRIC[(1)]		SN65HVD30, SN65HVD31, SN65HVD32	SN65HVD33, SN65HVD34, SN65HVD35	SN65HVD33	UNIT
		D (SOIC)	D (SOIC)	RHL (VQFN)	
		8 PINS	14 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	93.2	73	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	47.5	14	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	49.4	13.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.8	11.2	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.6	48.9	13.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: Driver

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$V_{I(K)}$	Input clamp voltage		I_I = –18 mA	–1.5			V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage		I_O = 0	2.5		V_{CC}	V
			R_L = 54 Ω, See 図 8-2 (RS-485)	1.5	2		
			R_L = 100 Ω, See 図 8-2,[2] (RS-422)	2	2.3		
			V_{test} = –7 V to 12 V, See 図 8-3	1.5			
$\Delta\|V_{OD(SS)}\|$	Change in magnitude of steady-state differential output voltage between states		R_L = 54 Ω, See 図 8-2 and 図 8-3	–0.2		0.2	V
$V_{OD(RING)}$	Differential Output Voltage overshoot and undershoot		R_L = 54 Ω, C_L = 50 pF, See 図 8-6 and 図 8-4			10%[3]	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	SN65HVD30, SN65HVD33	See 図 8-5		0.5		V
		SN65HVD31, SN65HVD34, SN65HVD32, SN65HVD35	See 図 8-5		0.25		
$V_{OC(SS)}$	Steady-state common-mode output voltage		See 図 8-5	1.6		2.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		See 図 8-5	–0.05		0.05	V
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current	SN65HVD30, SN65HVD31, SN65HVD32	V_{CC} = 0 V, V_Z or V_Y = 12 V, Other input at 0 V			90	μA
			V_{CC} = 0 V, V_Z or V_Y = –7 V, Other input at 0 V	–10			
		SN65HVD33, SN65HVD34, SN65HVD35	V_{CC} = 3 V or 0 V, DE = 0 V V_Z or V_Y = 12 V Other input at 0 V			90	
			V_{CC} = 3 V or 0 V, DE = 0 V V_Z or V_Y = –7 V Other input at 0 V	–10			
$I_{Z(S)}$ or $I_{Y(S)}$	Short Circuit output current[4]		V_Z or V_Y = –7 V Other input at 0 V	–250		250	mA
			V_Z or V_Y = 12 V Other input at 0 V	–250		250	
I_I	Input current	D, DE		0		100	μA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		16		pF

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) V_{CC} is 3.3 V_{DC} ± 5%.
(3) 10% of the peak-to-peak differential output voltage swing, per TIA/EIA-485.
(4) Under some conditions of short-circuit to negative voltages, output currents exceeding the ANSI TIA/EIA-485-A maximum current of 250 mA may occur. Continuous exposure can affect device reliability. This applies to the SN65HVD30, SN65HVD31, SN65HVD33, and SN65HVD34.

7.6 Electrical Characteristics: Receiver

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage		I_O = –8 mA			–0.02	V
V_{IT-}	Negative-going differential input threshold voltage		I_O = 8 mA	–0.20			V
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)				50		mV
V_{IK}	Enable-input clamp voltage		I_I = –18 mA	–1.5			V
V_O	Output voltage		V_{ID} = 200 mV, I_O = –8 mA, See 図 8-9	2.4			V
			V_{ID} = –200 mV, I_O = 8 mA, See 図 8-9			0.4	
$I_{O(Z)}$	High-impedance-state output current		V_O = 0 or V_{CC}, $\overline{RE}$ at V_{CC}	–1		1	µA
I_A or I_B	Bus input current	SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35	V_A or V_B = 12 V Other input at 0 V		0.05	0.1	mA
			V_A or V_B = 12 V, V_{CC} = 0 V Other input at 0 V		0.06	0.1	
			V_A or V_B = –7 V Other input at 0 V	–0.10	–0.04		
			V_A or V_B = –7 V, V_{CC} = 0 V Other input at 0 V	–0.10	–0.03		
		SN65HVD30, SN65HVD33	V_A or V_B = 12 V Other input at 0 V		0.20	0.35	mA
			V_A or V_B = 12 V, V_{CC} = 0 V Other input at 0 V		0.24	0.4	
			V_A or V_B = –7 V Other input at 0 V	–0.35	–0.18		
			V_A or V_B = –7 V, V_{CC} = 0 V Other input at 0 V	–0.25	–0.13		
I_{IH}	Input current, $\overline{RE}$		V_{IH} = 0.8 V or 2 V	–60			µA
C_{ID}	Differential input capacitance		V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		15		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

7.7 Device Power Dissipation – P_D

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Power Dissipation (worst case) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: SN65HVD30, SN65HVD33 at 25 Mbps, SN65HVD31, SN65HVD34 at 5 Mbps, SN65HVD32, SN65HVD35 at 1 Mbps	SN65HVD30, SN65HVD33	V_{CC} = 3.6 V, T_J = 140°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)			197	mW
		SN65HVD31, SN65HVD34	V_{CC} = 3.6 V, T_J = 140°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)			213	
		SN65HVD32, SN65HVD35	V_{CC} = 3.6 V, T_J = 140°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)			248	
T_{SD}	Thermal Shut-down Junction Temperature				170		°C

7.8 Supply Current Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	SN65HVD30	D at 0 V or V_{CC} and No Load			2.1	mA
		SN65HVD31, SN65HVD32			3.8	6.4	
		SN65HVD33	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at 0 V, No load (Receiver enabled and driver disabled)			1.8	mA
		SN65HVD34, SN65HVD35				2.2	
		SN65HVD33, SN65HVD34, SN65HVD35	$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load (Receiver disabled and driver disabled)		0.022	1	μA
		SN65HVD33	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at V_{CC}, No load (Receiver enabled and driver enabled)			2.1	mA
		SN65HVD34, SN65HVD35				6.5	
		SN65HVD33	$\overline{RE}$ at V_{CC}, D at 0 V or V_{CC}, DE at V_{CC} No load (Receiver disabled and driver enabled)			1.8	mA
		SN65HVD34, SN65HVD35				6.2	

(1) All typical values are at 25°C and with a 3.3-V supply.

7.9 Switching Characteristics: Driver

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	SN65HVD30, SN65HVD33	R_L = 54 Ω, C_L = 50 pF, See 図 8-6	4	10	18	ns
		SN65HVD31, SN65HVD34		25	38	65	
		SN65HVD32, SN65HVD35		120	175	305	
t_{PHL}	Propagation delay time, high-to-low-level output	SN65HVD30, SN65HVD33		4	9	18	ns
		SN65HVD31, SN65HVD34		25	38	65	
		SN65HVD32, SN65HVD35		120	175	305	
t_r	Differential output signal rise time	SN65HVD30, SN65HVD33		2.5	5	12	ns
		SN65HVD31, SN65HVD34		20	37	60	
		SN65HVD32, SN65HVD35		120	185	300	
t_f	Differential output signal fall time	SN65HVD30, SN65HVD33		2.5	5	12	ns
		SN65HVD31, SN65HVD34		20	35	60	
		SN65HVD32, SN65HVD35		120	180	300	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH}\rvert$)	SN65HVD30, SN65HVD33			0.6		ns
		SN65HVD31, SN65HVD34			2.0		
		SN65HVD32, SN65HVD35			5.1		

7.9 Switching Characteristics: Driver (continued)

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	SN65HVD33	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z See 図 8-7			45	ns
		SN65HVD34				235	
		SN65HVD35				490	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	SN65HVD33				25	ns
		SN65HVD34				65	
		SN65HVD35				165	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	SN65HVD33	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y See 図 8-8			35	ns
		SN65HVD34				190	
		SN65HVD35				490	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	SN65HVD33				30	ns
		SN65HVD34				120	
		SN65HVD35				290	
t_{PZH1}, t_{PZL1}	Driver enable delay with bus voltage offset		V_O= 2 V (Typ)		500	900	ns
t_{PZH2}	Propagation delay time, standby-to-high-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z See 図 8-7			4000	ns
t_{PZL2}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y See 図 8-8			4000	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

7.10 Switching Characteristics: Receiver

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	SN65HVD30, SN65HVD33	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See 図 8-10			26	45	ns
		SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35				47	70	ns
t_{PHL}	Propagation delay time, high-to-low-level output	SN65HVD30, SN65HVD33				29	45	ns
		SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35				49	70	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH}\rvert$)	SN65HVD30, SN65HVD33					7	ns
		SN65HVD31, SN65HVD34, SN65HVD32, SN65HVD35					10	ns
t_r	Output signal rise time						5	ns
t_f	Output signal fall time						6	ns
t_{PHZ}	Output disable time from high level		DE at 3 V	C_L = 15 pF, See 図 8-11			20	ns
t_{PZH1}	Output enable time to high level						20	ns
t_{PZH2}	Propagation delay time, standby-to-high-level output		DE at 0 V				4000	ns
t_{PLZ}	Output disable time from low level		DE at 3 V	C_L = 15 pF, See 図 8-12			20	ns
t_{PZL1}	Output enable time to low level						20	ns
t_{PZL2}	Propagation delay time, standby-to-low-level output		DE at 0 V				4000	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

7.11 Dissipation Ratings

PACKAGE	JEDEC THERMAL MODEL	T_A < 25°C RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C RATING	T_A = 105°C RATING	T_A = 125°C RATING
8-pin D (SOIC)	Low k	625 mW	5 mW/°C	325 mW		
	High k	1000 mW	8 mW/°C	520 mW	360 mW	
14-pin D (SOIC)	Low k	765 mW	6.1 mW/°C	400 mW	275 mW	
	High k	1350 mW	10.8 mW/°C	705 mW	485 mW	270 mW
20-pin RHL (VQFN)	High k	1710 mW	13.7 mW/°C	890 mW	6150 mW	340 mW

7.12 Typical Characteristics

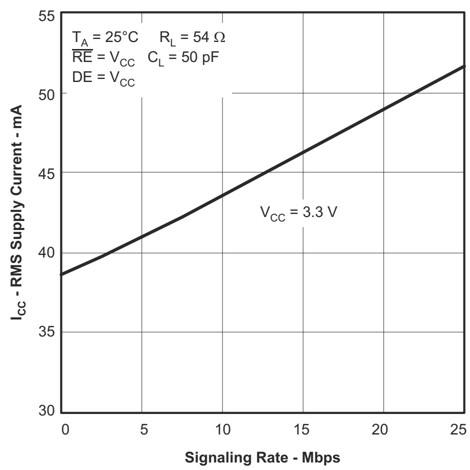


図 7-1. SN65HVD30, SN65HVD33 RMS Supply Current vs Signaling Rate

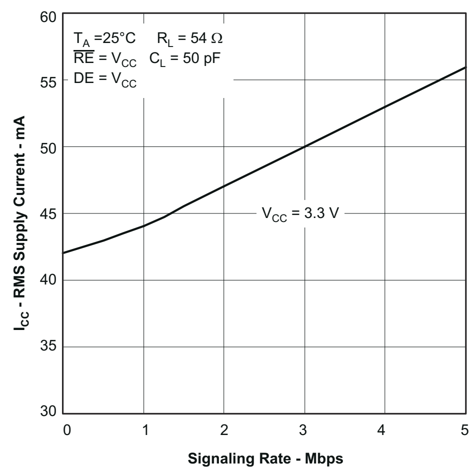


図 7-2. SN65HVD31, SN65HVD34 RMS Supply Current vs Signaling Rate

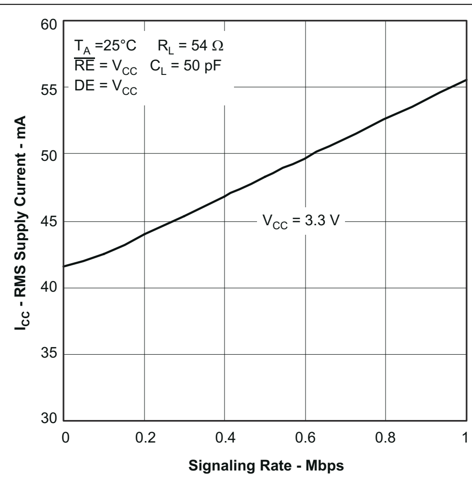


図 7-3. SN65HVD32, SN65HVD35 RMS Supply Current vs Signaling Rate

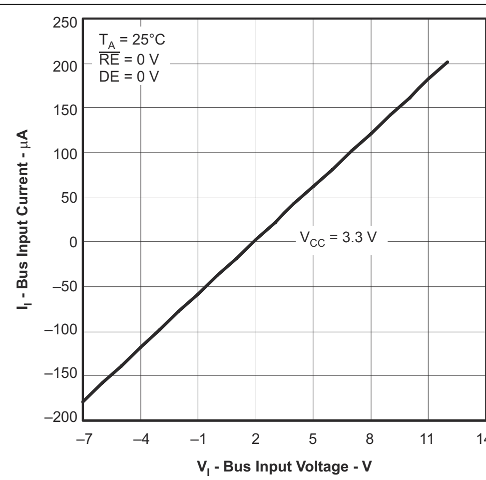


図 7-4. SN65HVD30, SN65HVD33 Bus Input Current vs Input Voltage

7.12 Typical Characteristics (continued)

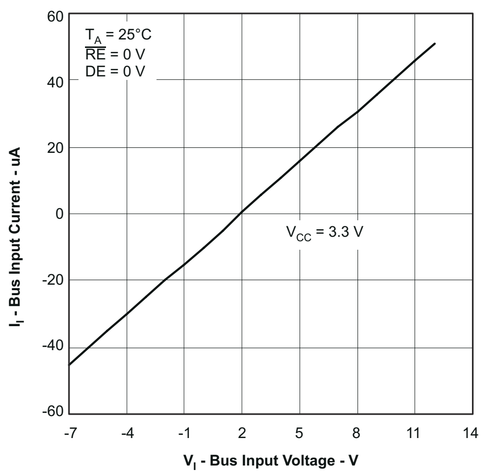


図 7-5. SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35 Bus Input Current vs Input Voltage

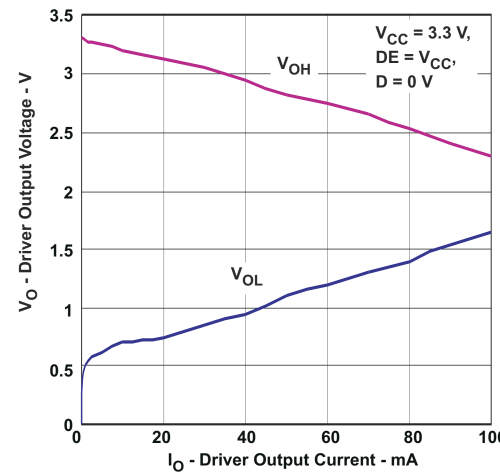


図 7-6. Driver Output Voltage vs Driver Output Current

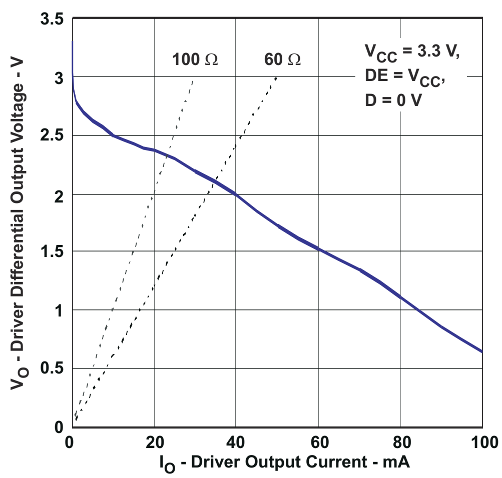


図 7-7. Driver Differential Output Voltage vs Driver Output Current

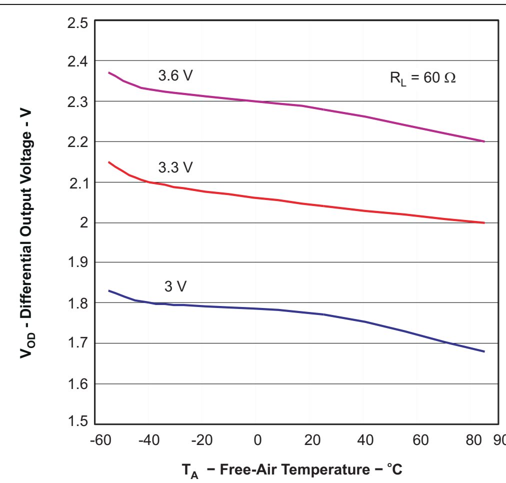


図 7-8. Driver Differential Output Voltage vs Free-Air Temperature

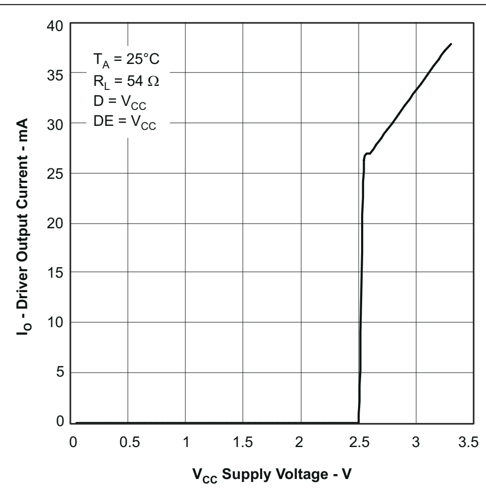


図 7-9. Driver Output Current vs Supply Voltage

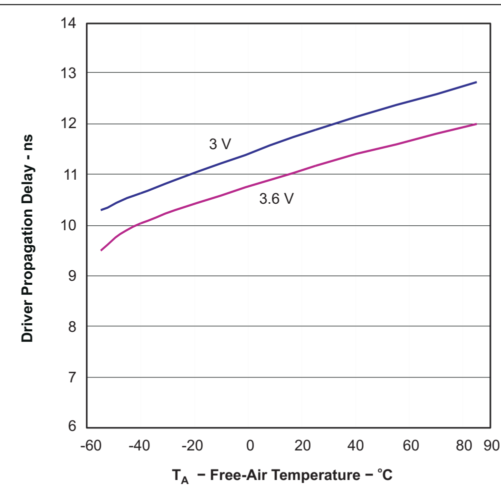


図 7-10. SN65HVD30, SN65HVD33 Driver Propagation Delay vs Free-Air Temperature

7.12 Typical Characteristics (continued)

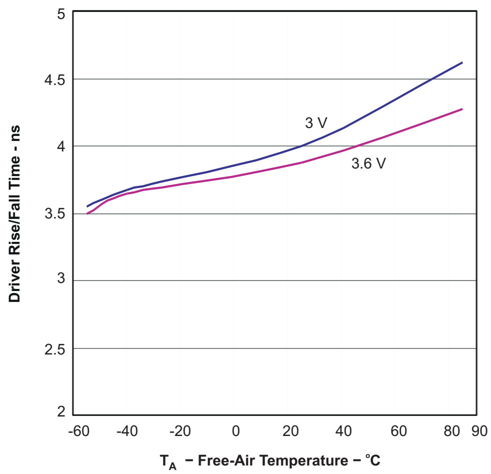


図 7-11. SN65HVD30, SN65HVD33 Driver Rise and Fall Time vs Free-Air Temperature

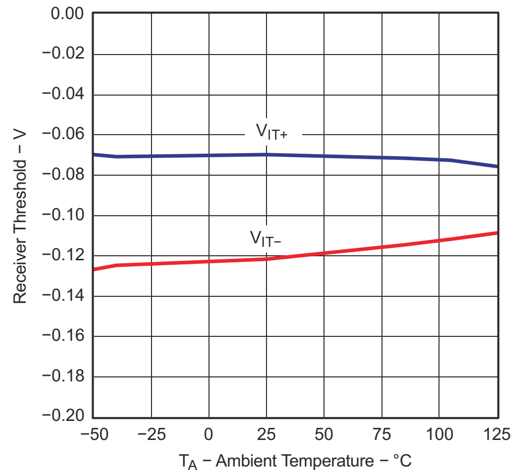


図 7-12. Receiver Threshold vs Ambient Temperature

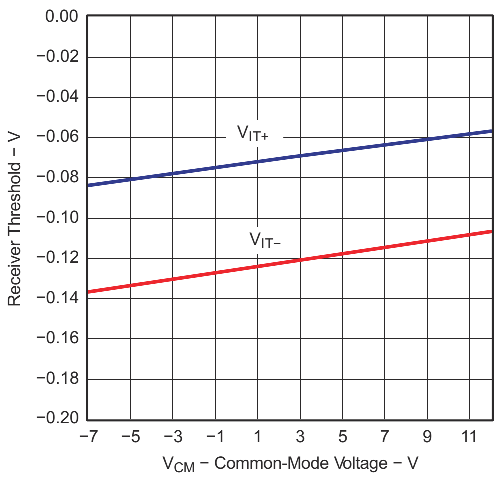


図 7-13. Receiver Threshold vs Common-Mode Voltage

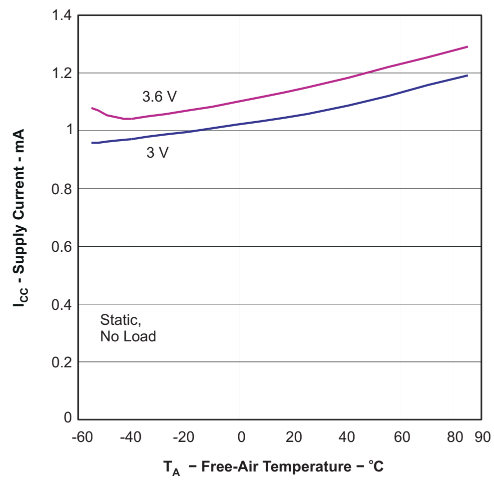


図 7-14. Supply Current vs Free-Air Temperature

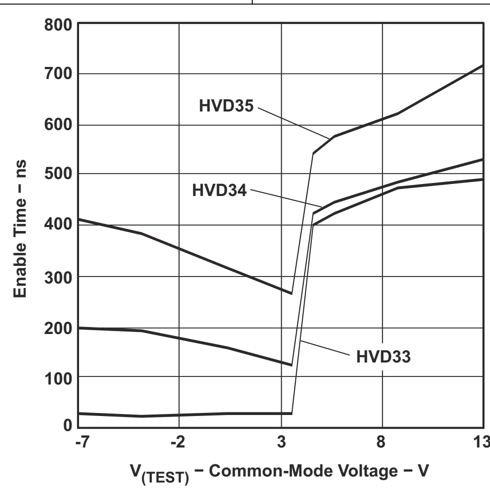
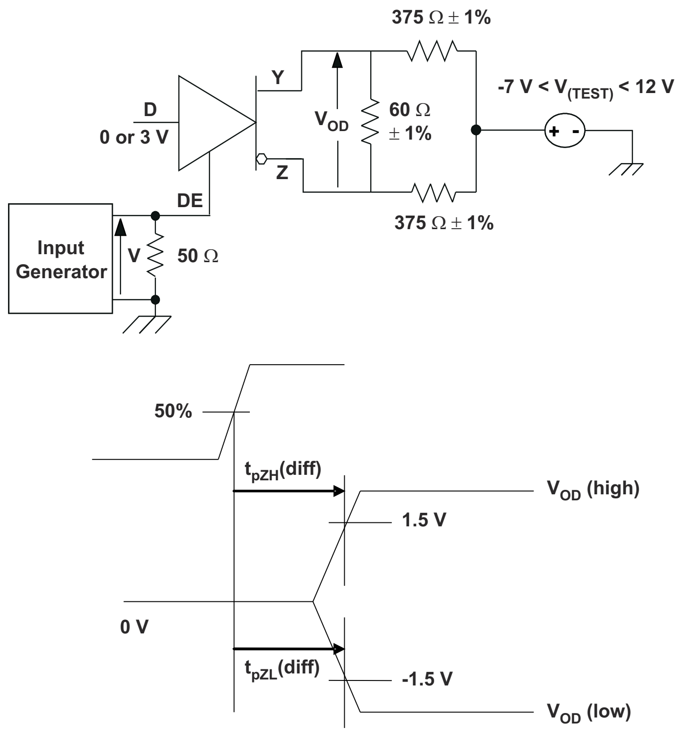


図 7-15. Enable Time vs Common-Mode Voltage (see 図 8-1)

Parameter Measurement Information



The time $t_{pZL}(x)$ is the measure from DE to $V_{OD}(x)$. V_{OD} is valid when it is greater than 1.5 V.

図 8-1. Driver Enable Time From DE to V_{OD}

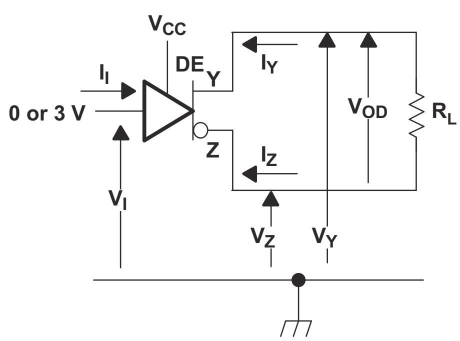


図 8-2. Driver V_{OD} Test Circuit and Voltage and Current Definitions

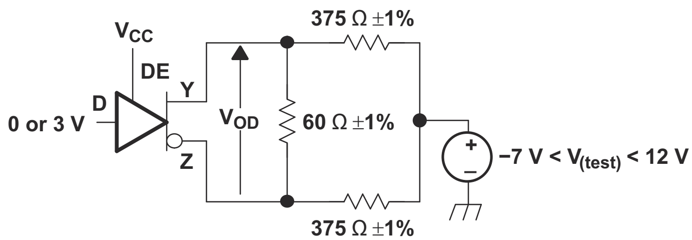


図 8-3. Driver V_{OD} With Common-Mode Loading Test Circuit

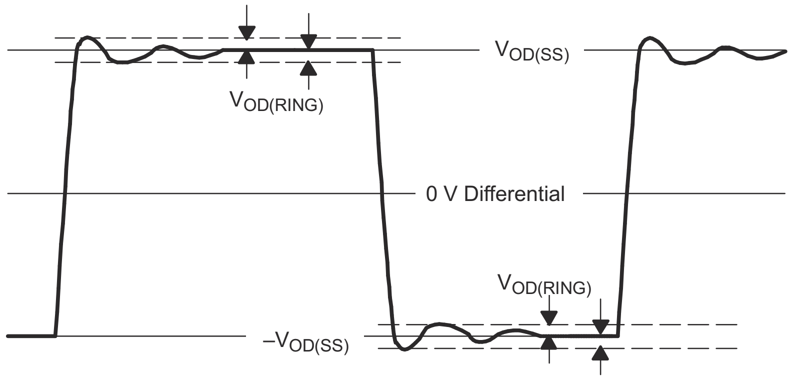


図 8-4. $V_{OD(RING)}$ Waveform and Definitions

$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

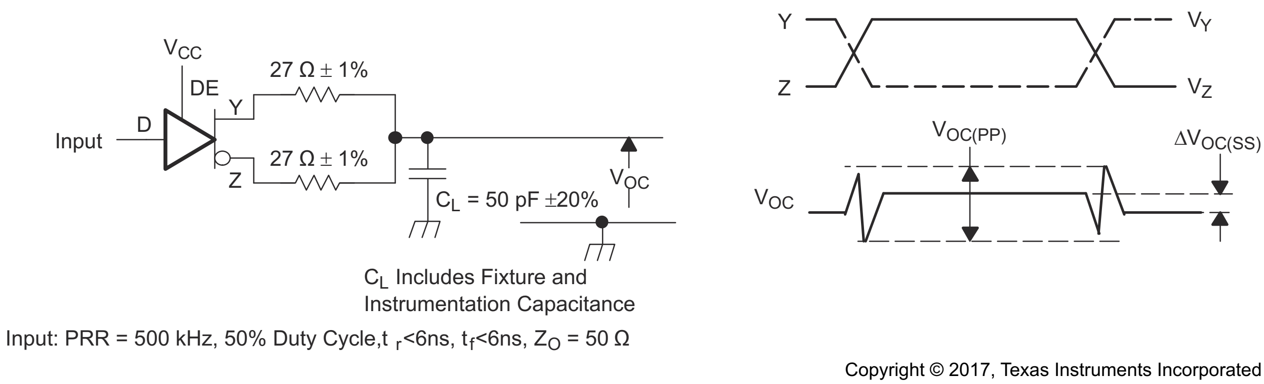


図 8-5. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

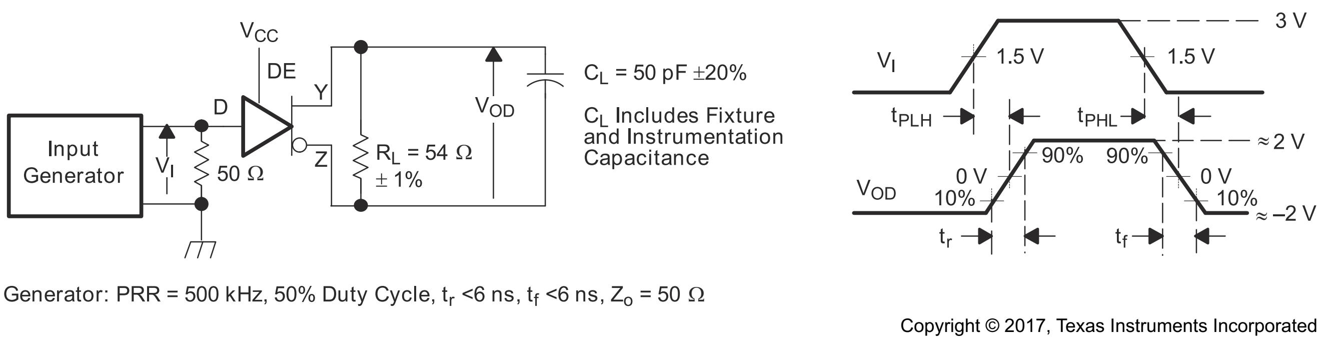
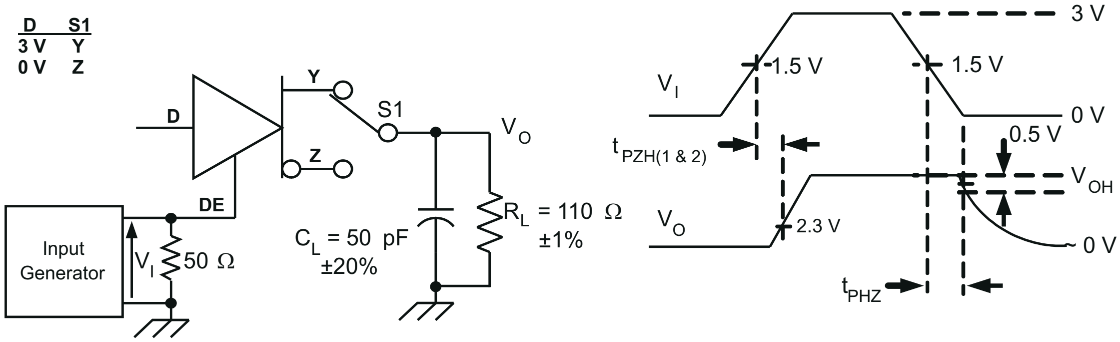
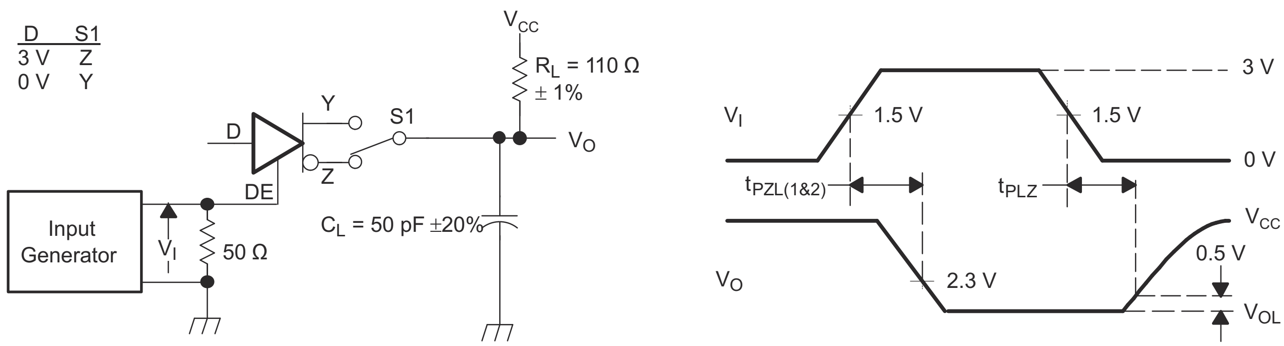


図 8-6. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 50 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_0 = 50 Ω
C_L Includes Fixture and Instrumentation Capacitance

図 8-7. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 50 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_0 = 50 Ω
C_L Includes Fixture and Instrumentation Capacitance

図 8-8. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

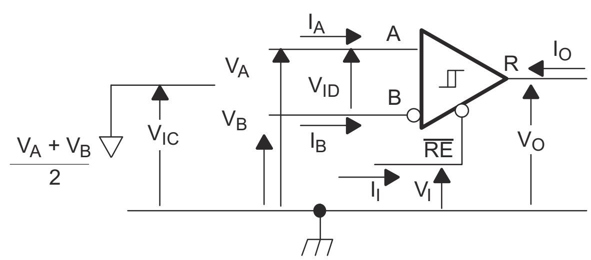
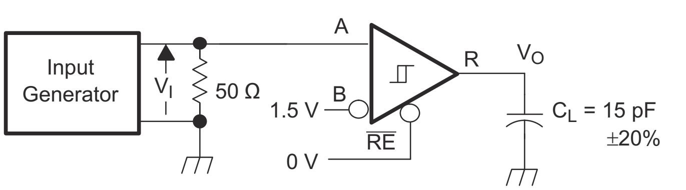


図 8-9. Receiver Voltage and Current Definitions



C_L Includes Fixture and Instrumentation Capacitance

Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

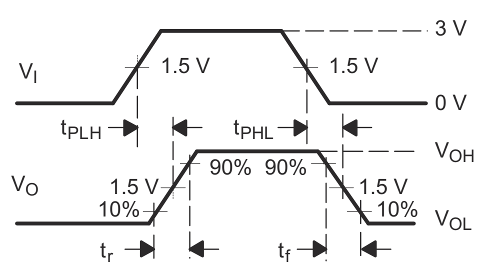


図 8-10. Receiver Switching Test Circuit and Voltage Waveforms

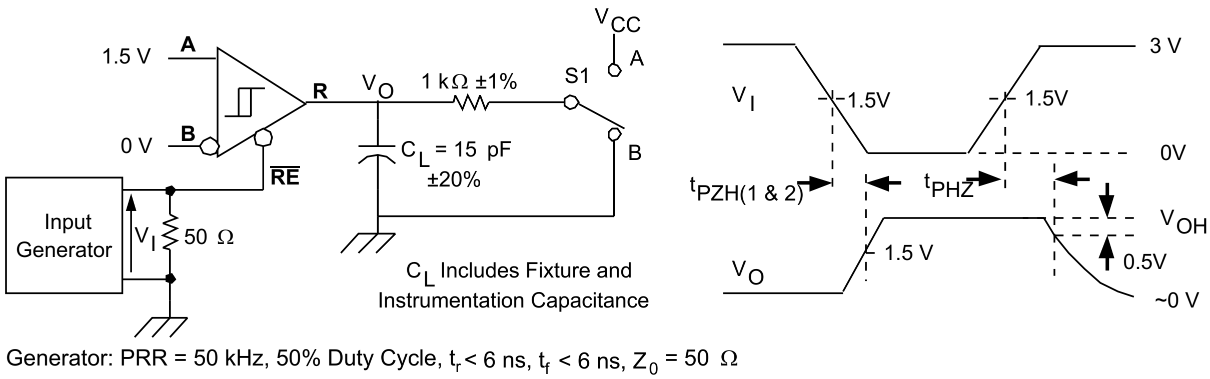


図 8-11. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

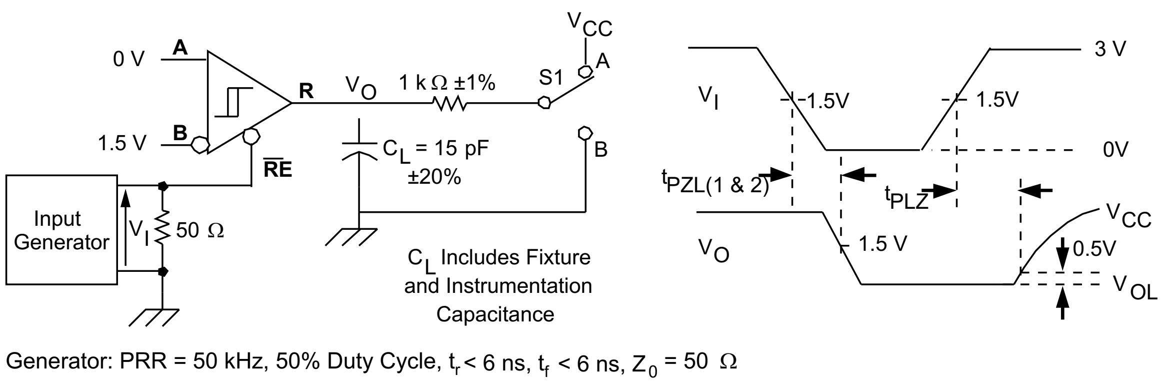


図 8-12. Receiver Enable Time From Standby (Driver Disabled)

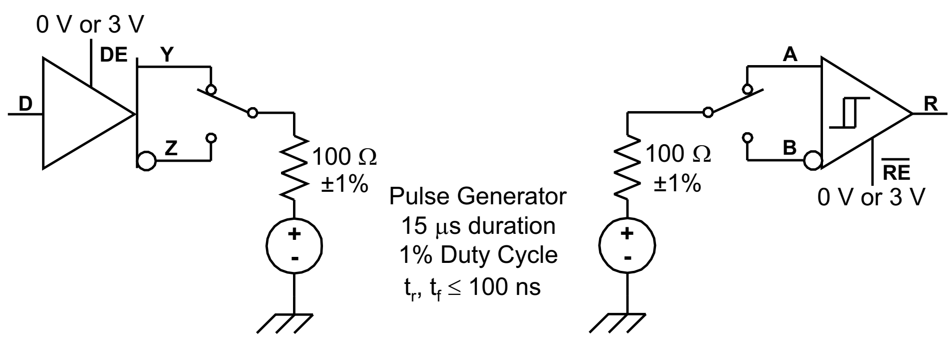


図 8-13. Test Circuit, Transient Over Voltage Test

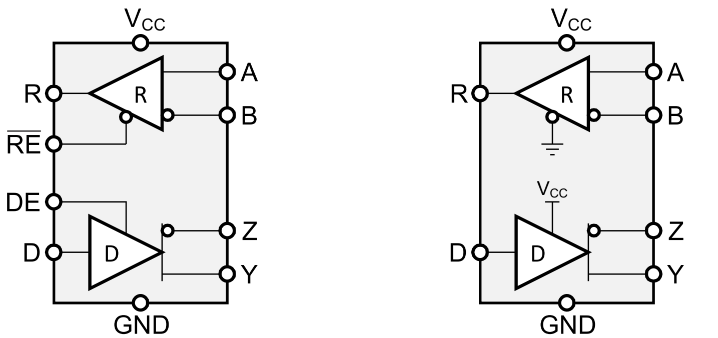
8 Detailed Description

8.1 Overview

The SN65HVD3x devices are low-power, full-duplex RS-485 transceivers available in three speed grades suitable for data transmission of 1 Mbps, 5 Mbps, and 50 Mbps.

The SN65HVD30, SN65HVD31, and SN65HVD32 devices are fully enabled with no external enabling pins. The SN65HVD33, SN65HVD34, and SN65HVD35 devices have active-high driver enables and active-low receiver enables. A standby current of less than 1 µA can be achieved by disabling both driver and receiver.

8.2 Functional Block Diagram



a) SN65HVD33, SN65HVD34, SN65HVD35

b) SN65HVD30, SN65HVD31, SN65HVD32

8.3 Feature Description

8.3.1 Low-Power Standby Mode

When both the driver and receiver are disabled (DE is low and $\overline{RE}$ is high), the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver or receiver enabling. The device in standby mode only when the enable inputs are held in this state for 300 ns or more. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

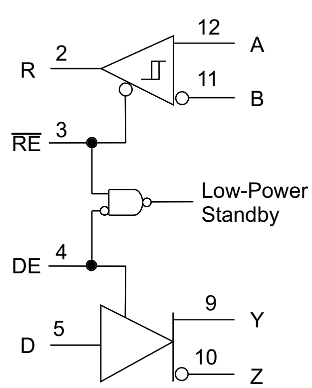


図 8-1. Low-Power Standby Logic Diagram

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by t_{PZH2} and t_{PZL2} in the driver switching characteristics. If the D input is open when the driver is enabled, the driver output defaults to Y low and Z high, in accordance with the driver-failsafe feature.

If only the receiver is re-enabled ($\overline{RE}$ transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by t_{PZH2} and t_{PZL2} in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

8.3.2 Driver Output Current Limiting

The RS-485 standard (ANSI/TIA/EIA-485-A or equivalently ISO 8482) specifies a 250-mA driver output current limit to prevent damage caused by data contention on the bus. That applies in the event that two or more transceivers drive the bus to opposing states at the same time. The SN65HVD3x family of devices includes current-limiting circuitry that prevents damage under these conditions.

注

This current limit prevents damage during the bus contention, but the logic state of the bus can be indeterminate as specified by the standard, so communication errors can occur.

In a specific combination of circumstances, a condition can occur in which current through the bus pin exceeds the 250-mA limit. This combination of conditions is not normally included in RS-485 applications:

- Loading capacitance on the pin is less than 500 pF
- The bus pin is directly connected to a voltage more negative than –1 V
- The device is supplied with V_{CC} equal to or greater than 3.3 V
- The driver is enabled
- The bus pin is driving to the logic high state

In these specific conditions, the normal current-limit circuitry and thermal-shutdown circuitry does not limit or shutdown the current flow. If the current is allowed to continue, the device heats up in a localized area near the driver outputs, and the device can be damaged.

Typical RS-485 twisted-pair cable has a capacitance of approximately 50 pF/meter. Therefore, it is expected that 10 meters of cable can provide sufficient capacitance to prevent this latch-up condition.

The –7 to +12-V common mode range specified by RS-485 is intended to allow communication between transceivers separated by significant distances when ground offsets may occur due to temporary current surges, electrical noise, and so on. Under those circumstances, the inherent cable needed to connect separated transceivers ensures that the conditions previously listed do not occur. For a transceiver separated by only a short cable length or backplane applications, it is unusual for there to be a steady-state negative common-mode voltage. It is possible for a negative power supply to be shorted to the bus lines due to miswiring or cable damage; however, this is a different root cause fault, and robust devices such as the SN65HVD178x family should be used for surviving power supply or miswiring faults.

The 250-mA current limit in the RS-485 standard is intended to prevent damage caused by data contention on the bus; that is, in the event that two or more transceivers drive the bus to different states at the same time. These devices are not damaged under these conditions because all RS-485 drivers have output impedance sufficient to prevent the direct connection condition stated previously. Typical RS-485 driver output impedance is on the order of 10 Ω to 30 Ω.

8.3.3 Hot-Plugging

These devices are designed to operate in *hot swap* or *hot pluggable* applications. Key features for hot-pluggable applications are:

- Power-up
- Power-down glitch-free operation
- Default disabled input/output pins

- Receiver failsafe

As shown in 図 7-9, an internal power-on reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device reliably operates. This ensures that no spurious bits are transmitted on the bus pin outputs as the power supply turns on or turns off.

As shown in the *セクション 8.4*, the enable inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device neither drives the bus nor reports data on the R pin until the associated controller actively drives the enable pins.

8.3.4 Receiver Failsafe

The differential receivers of the SN65HVD3x family are failsafe to invalid bus states caused by:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input indeterminate range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+}, V_{IT-}, and V_{HYS} (the separation between V_{IT+} and V_{IT-}. As shown in the *Electrical Characteristics* table, differential signals more negative than –200 mV always cause a low receiver output, and differential signals more positive than 200 mV always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{IT+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value (V_{HYS}) as well as the value of V_{IT+}.

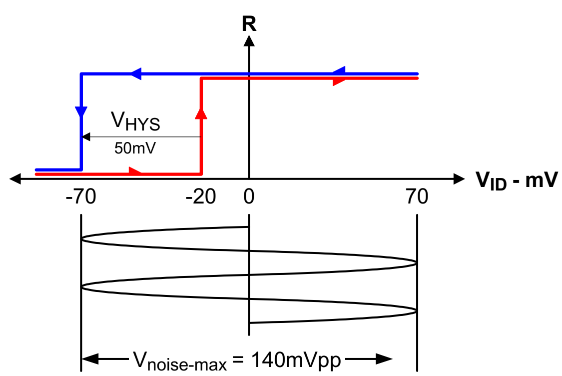


図 8-2. SN65HVD30-35 Noise Immunity Under Bus Fault Conditions

8.3.5 Safe Operation With Bus Contention

These devices incorporate a driver current limit of 250 mA across the RS-485 common-mode range of –7 V to +12 V. As stated in the *Application Guidelines for TIA/EIA-485-A* [1], this sets a practical limitation to prevent damage during bus contention events. Contention can occur during system initialization, during system faults, or whenever two or more drivers are active at the same time.

[1] TIA/EIA Telecommunications System Bulletin TSB89, *Application Guidelines for TIA/EIA-485-A*

図 8-3 shows a 2-node system to demonstrate bus contention by forcing both drivers to be active in opposing states.

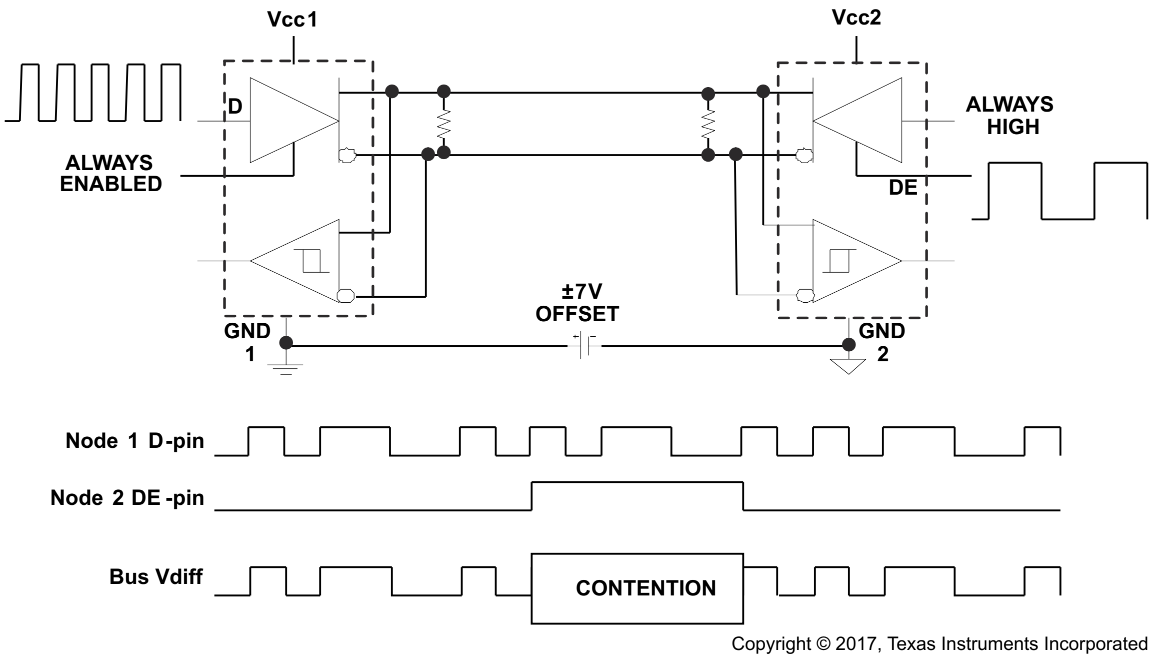


図 8-3. Bus Contention Example

図 8-4 shows typical operation in a bus contention event. The bottom trace illustrates how the SN65HVD33 device at Node 1 continues normal operation after a contention event between the two drivers with a –7-V ground offset on Node 2. This illustrates how the SN65HVD3x family of devices operates robustly in spite of bus contention faults, even with large common-mode offsets.

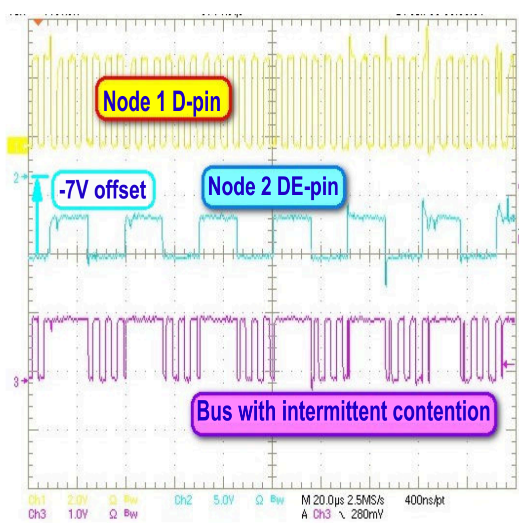


図 8-4. SN65HVD3x Drivers Operate Correctly After Bus Contention Faults

8.4 Device Functional Modes

表 8-1. SN65HVD33, SN65HVD34, SN65HVD35 Driver

INPUTS		OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

表 8-2. SN65HVD33, SN65HVD34, SN65HVD35 Receiver

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \le -0.2$ V	L	L
-0.2 V < V_{ID} < -0.02 V	L	?
-0.02 V ≤ V_{ID}	L	H
X	H or open	Z
Open Circuit	L	H
Idle circuit	L	H
Short Circuit, $V_{(A)} = V_{(B)}$	L	H

表 8-3. SN65HVD30, SN65HVD31, SN65HVD32 Driver

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H
Open	L	H

表 8-4. SN65HVD30, SN65HVD31, SN65HVD32 Receiver

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	OUTPUT R
$V_{ID} \le -0.2$ V	L
-0.2 V < V_{ID} < -0.02 V	?
-0.02 V ≤ V_{ID}	H
Open Circuit	H
Idle circuit	H
Short Circuit, $V_{(A)} = V_{(B)}$	H

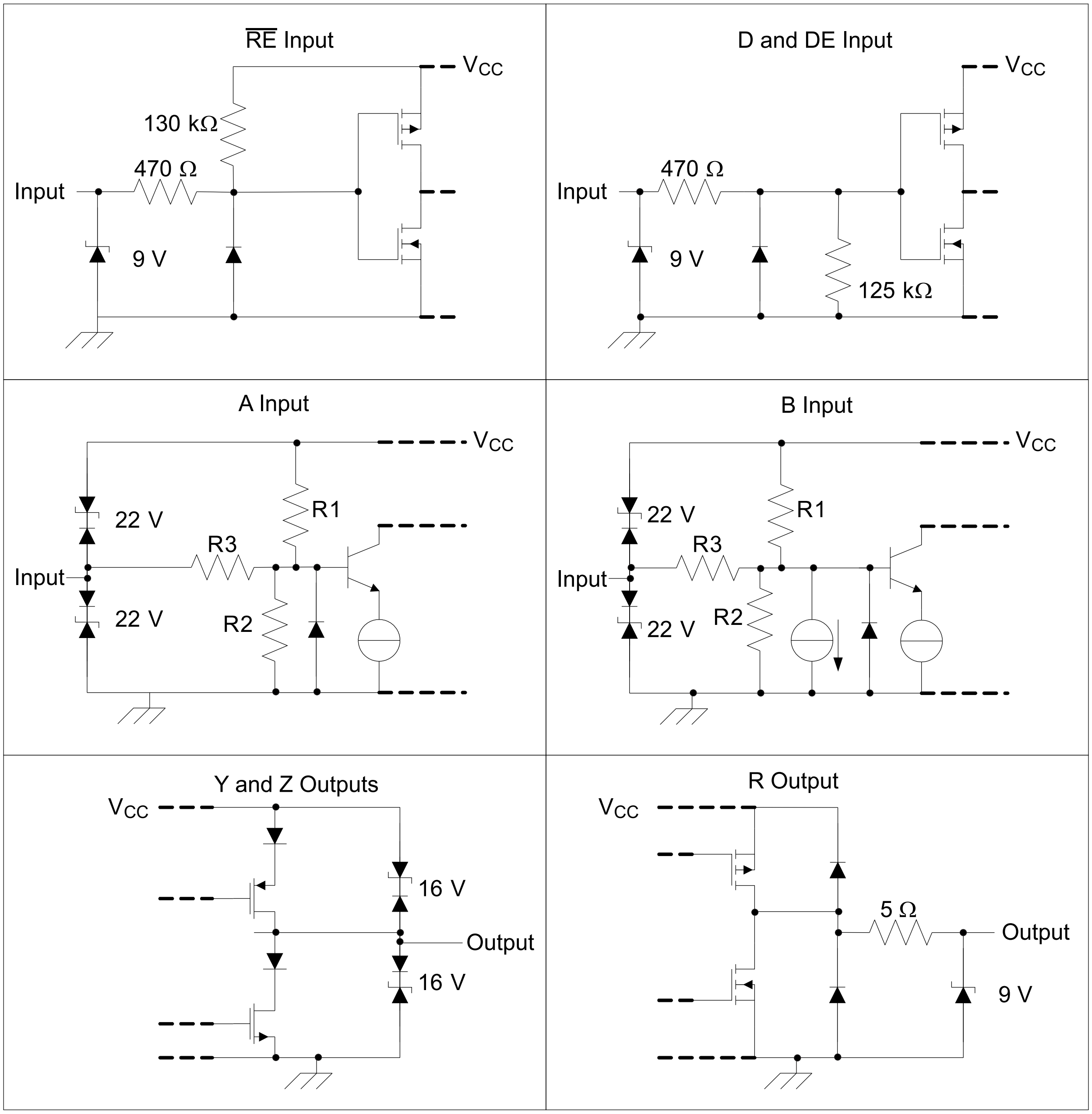


図 8-5. Equivalent Input and Output Schematic Diagrams

表 8-5. Input Attenuator Resistance Values

PART NUMBER	R1, R2	R3
SN65HVD30, SN65HVD33	9 kΩ	45 kΩ
SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35	36 kΩ	180 kΩ

9 Application and Implementation

注

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9.1 Application Information

The SN65HVD3x family consists of full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

To eliminate line reflections, each cable end is terminated with a termination resistor (R_T) whose value matches the characteristic impedance (Z_0) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

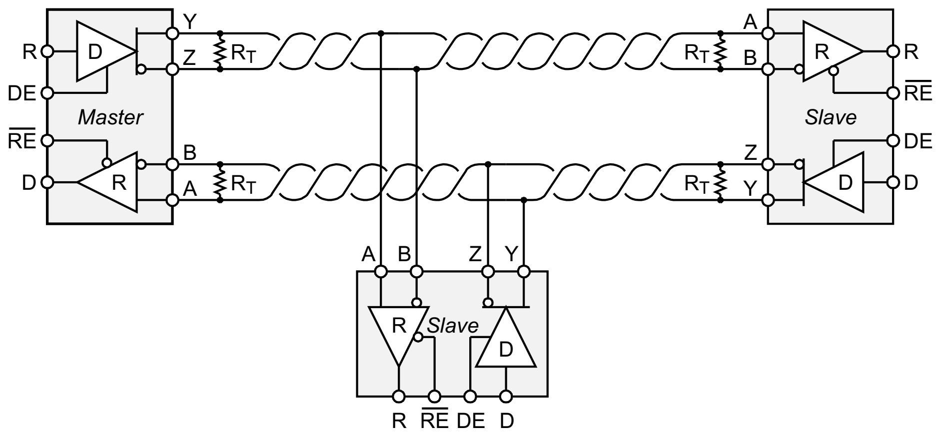


図 9-1. Typical RS-485 Network With Full-Duplex Transceivers

9.2 Typical Application

A full-duplex RS-485 network consists of multiple transceivers connecting in parallel to two bus cables. On one signal pair, a master driver transmits data to multiple slave receivers. The master driver and slave receivers can remain fully enabled at all times. On the other signal pair, multiple slave drivers transmit data to the master receiver. To avoid bus contention, the slave drivers must be intermittently enabled and disabled such that only one driver is enabled at any time, as in half-duplex communication. The master receiver can remain fully enabled at all times.

Because the driver cannot be disabled, only connect one driver to the bus when using the SN65HVD30, SN65HVD31, or SN65HVD32 devices.

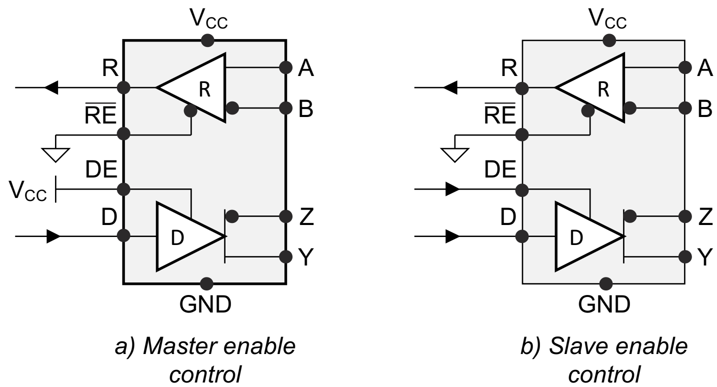


図 9-2. Full-Duplex Transceiver Configurations

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable can be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

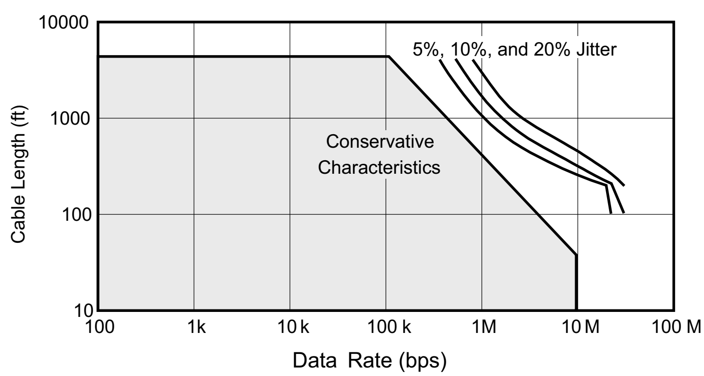


図 9-3. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (such as 26 Mbps for the SN65HVD30 and SN65HVD33 devices) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a nonterminated piece of bus line that can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver; thus giving a maximum physical stub length as shown in 式 1.

$$L_{stub} \le 0.1 \times t_r \times v \times c \tag{1}$$

where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

Per 式 1, 表 9-1 shows the maximum cable-stub lengths for the minimum driver output rise times of the SN65HVD3x full-duplex family of transceivers for a signal velocity of 78%.

表 9-1. Maximum Stub Length

DEVICE	MINIMUM DRIVER OUTPUT RISE TIME (ns)	MAXIMUM STUB LENGTH	
		(m)	(ft)
SN65HVD30	4	0.1	0.3
SN65HVD31	25	0.6	1.9
SN65HVD32	120	2.8	9.2
SN65HVD33	4	0.1	0.3
SN65HVD34	25	0.6	1.9
SN65HVD35	120	2.8	9.2

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD30 and SN65HVD33 devices are 1/2 UL transceivers, it is possible to connect up to 64 receivers to the bus. Likewise, the SN65HVD31, SN65HVD32, SN65HVD34, and SN65HVD35 devices are 1/8 UL transceivers that can support up to 256 receivers.

9.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary (see 図 9-4).

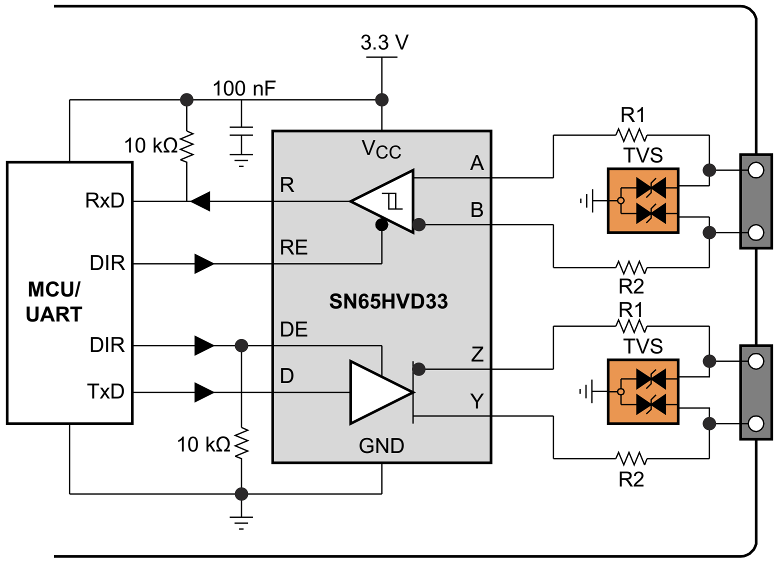
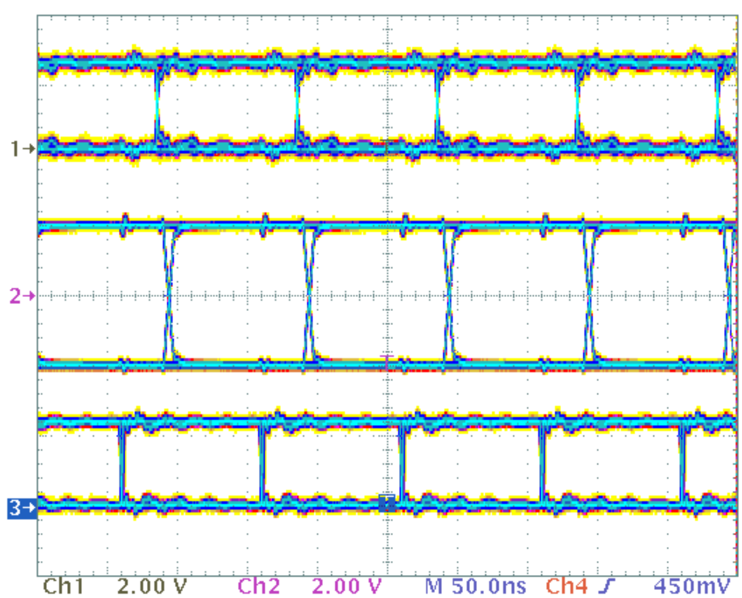


図 9-4. Transient Protection Against ESD, EFT, and Surge Transients

表 9-2. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3-V Full-Duplex RS-485 Transceiver	SN65HVD33	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW060310RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns

9.2.3 Application Curve



Signals from top to bottom: D, Y, Z, VOD

図 9-5. SN65HVD33 Transient Waveform

9.3 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100-nF ceramic capacitor located as close as possible to the supply pins. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps compensate for the resistance and inductance of the PCB power planes.

9.4 Layout

9.4.1 Layout Guidelines

Robust and reliable bus-node design often requires the use of external transient protection devices to protect against EFT and surge transients that can occur in industrial environments. Because these transients have a wide frequency bandwidth (from approximately 3 MHz to 3 GHz), high-frequency layout techniques must be applied during PCB design.

- Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents follow the path of least inductance and not the path of least impedance.
- Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
- Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs), which reduces the transients to a few hundred volts of clamping voltage and transient blocking units (TBUs) that limit transient current to 200 mA.

9.4.2 Layout Example

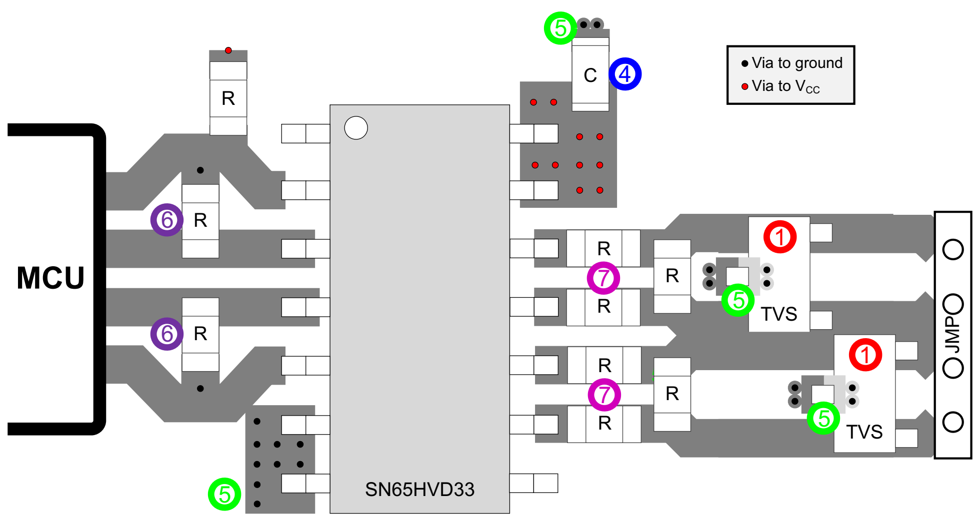


図 9-6. SN65HVD33 Layout Example

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD30D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP30
SN65HVD30DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30
SN65HVD30DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30
SN65HVD30DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30
SN65HVD31D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP31
SN65HVD31DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP31
SN65HVD31DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP31
SN65HVD31DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP31
SN65HVD32DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP32
SN65HVD32DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP32
SN65HVD32DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP32
SN65HVD33DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33
SN65HVD33DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33
SN65HVD33DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33
SN65HVD33RHLR	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65HVD33
SN65HVD33RHLR.A	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65HVD33
SN65HVD33RHLT	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65HVD33
SN65HVD33RHLT.A	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65HVD33
SN65HVD33RHLTG4.A	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65HVD33
SN65HVD34D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	65HVD34
SN65HVD34DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34
SN65HVD34DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34
SN65HVD34DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34
SN65HVD35DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35
SN65HVD35DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35
SN65HVD35DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65HVD30, SN65HVD33 :

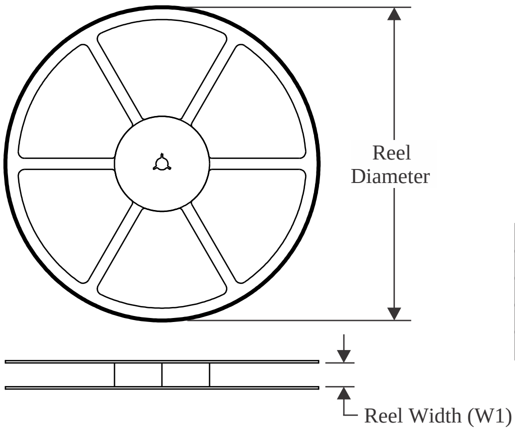
- Enhanced Product : SN65HVD30-EP, SN65HVD33-EP

NOTE: Qualified Version Definitions:

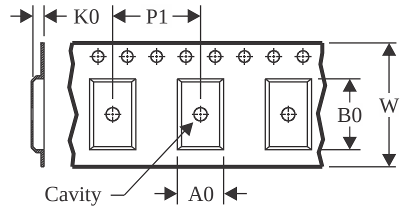
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

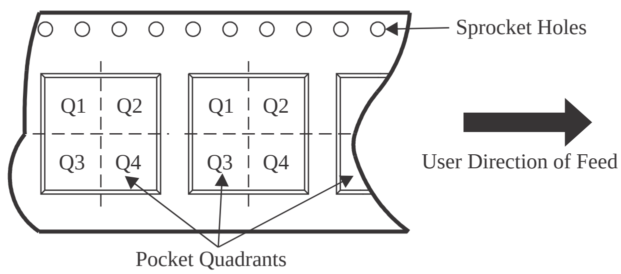


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

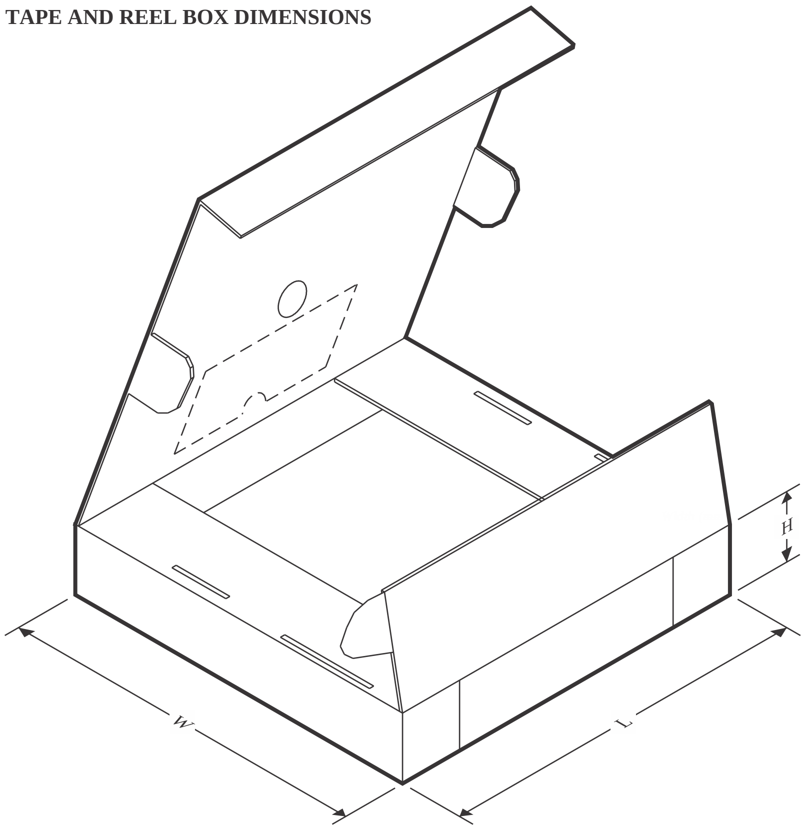
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD31DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD31DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD32DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD32DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD33DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD33RHLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN65HVD33RHLT	VQFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN65HVD34DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD35DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

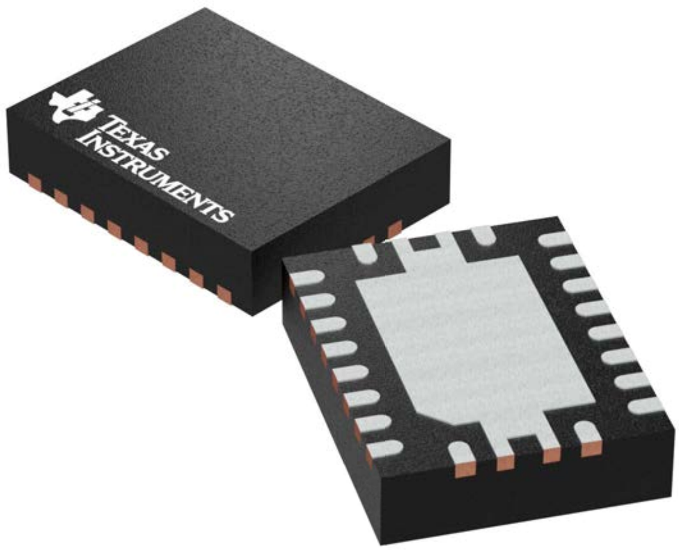
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD30DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD30DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD31DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD31DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD32DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD32DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD33DR	SOIC	D	14	2500	356.0	356.0	35.0
SN65HVD33RHLR	VQFN	RHL	20	3000	356.0	356.0	35.0
SN65HVD33RHLT	VQFN	RHL	20	250	210.0	185.0	35.0
SN65HVD34DR	SOIC	D	14	2500	356.0	356.0	35.0
SN65HVD35DR	SOIC	D	14	2500	356.0	356.0	35.0

RHL 20

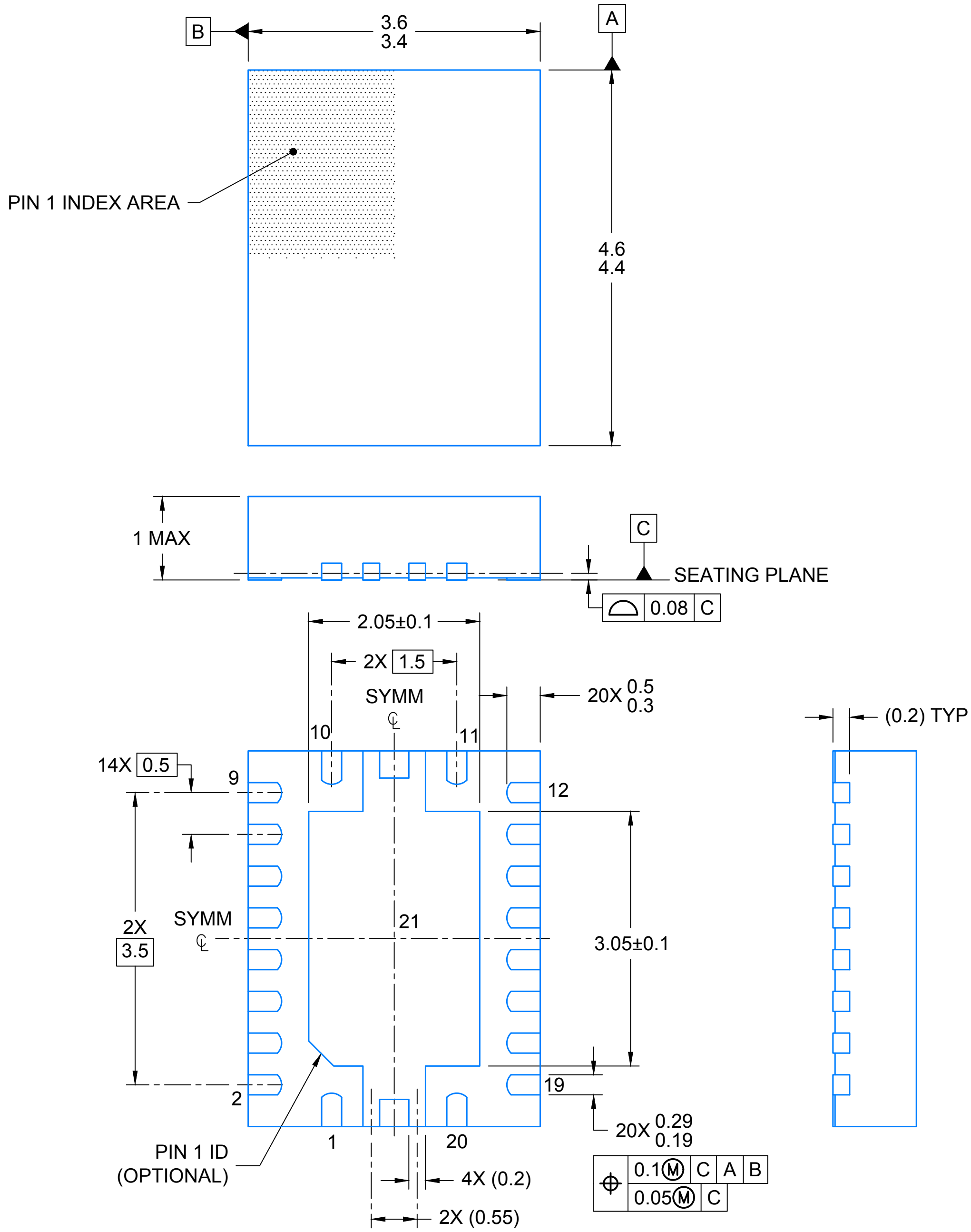
VQFN - 1 mm max height

3.5 x 4.5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



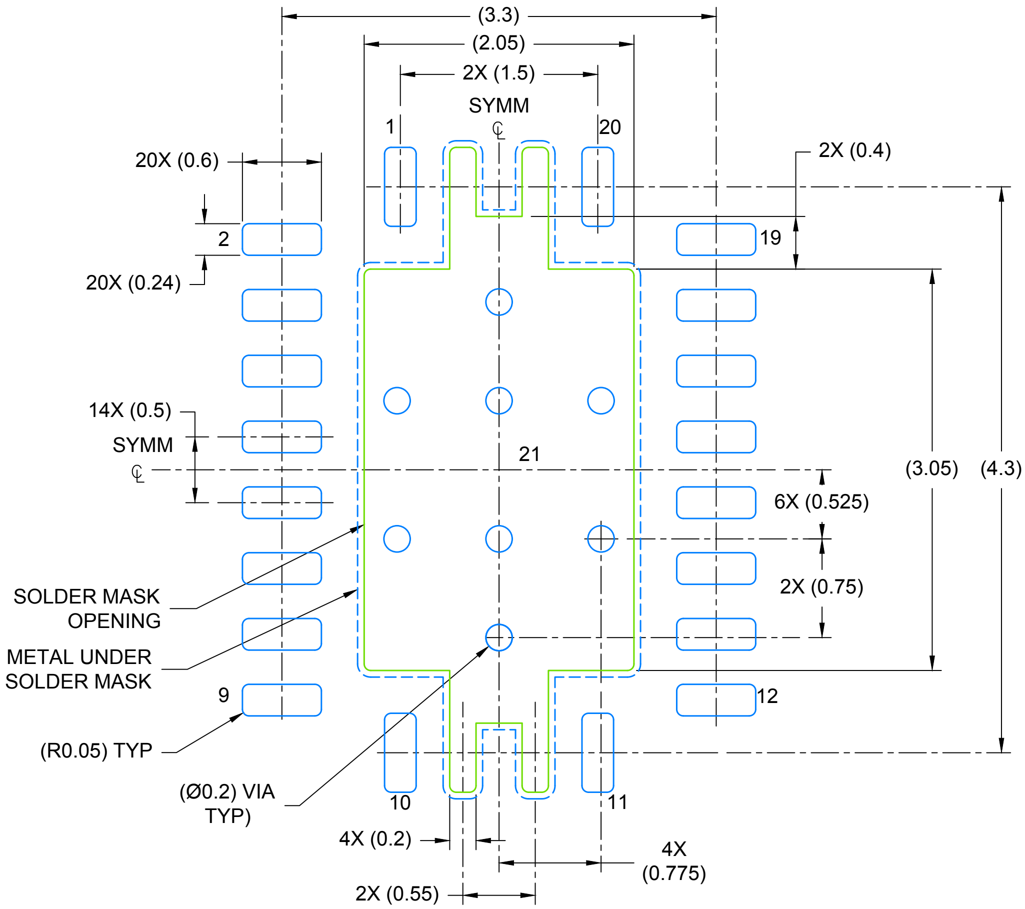
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



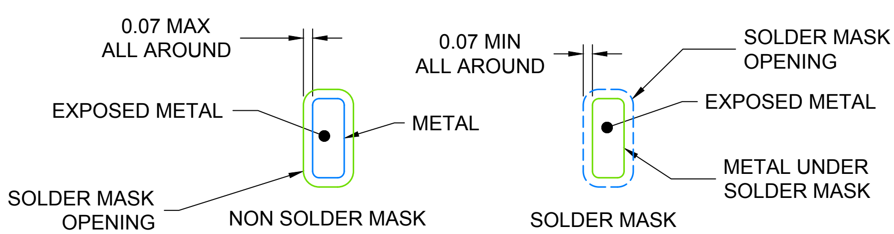
4219071 / A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



NON SOLDER MASK
DEFINED
(PREFERRED)

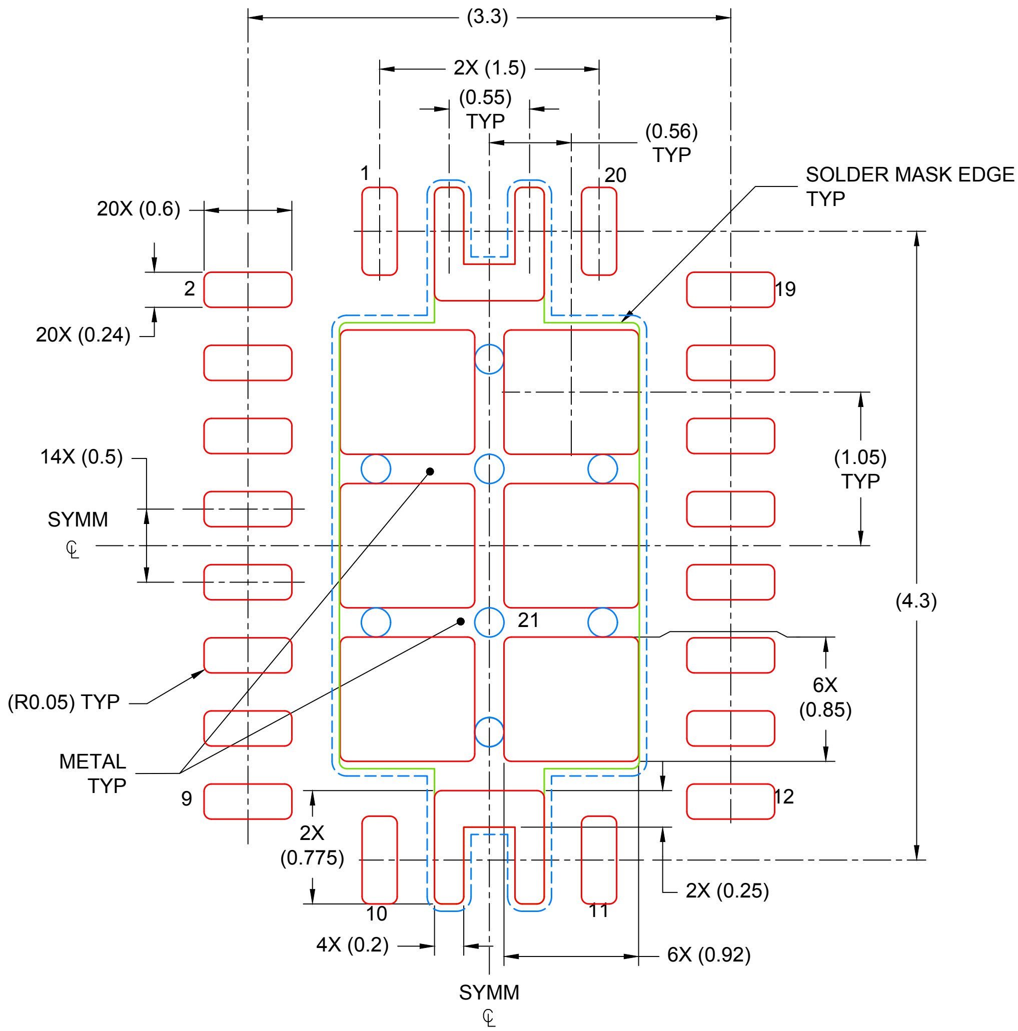
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219071 / A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to theri locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



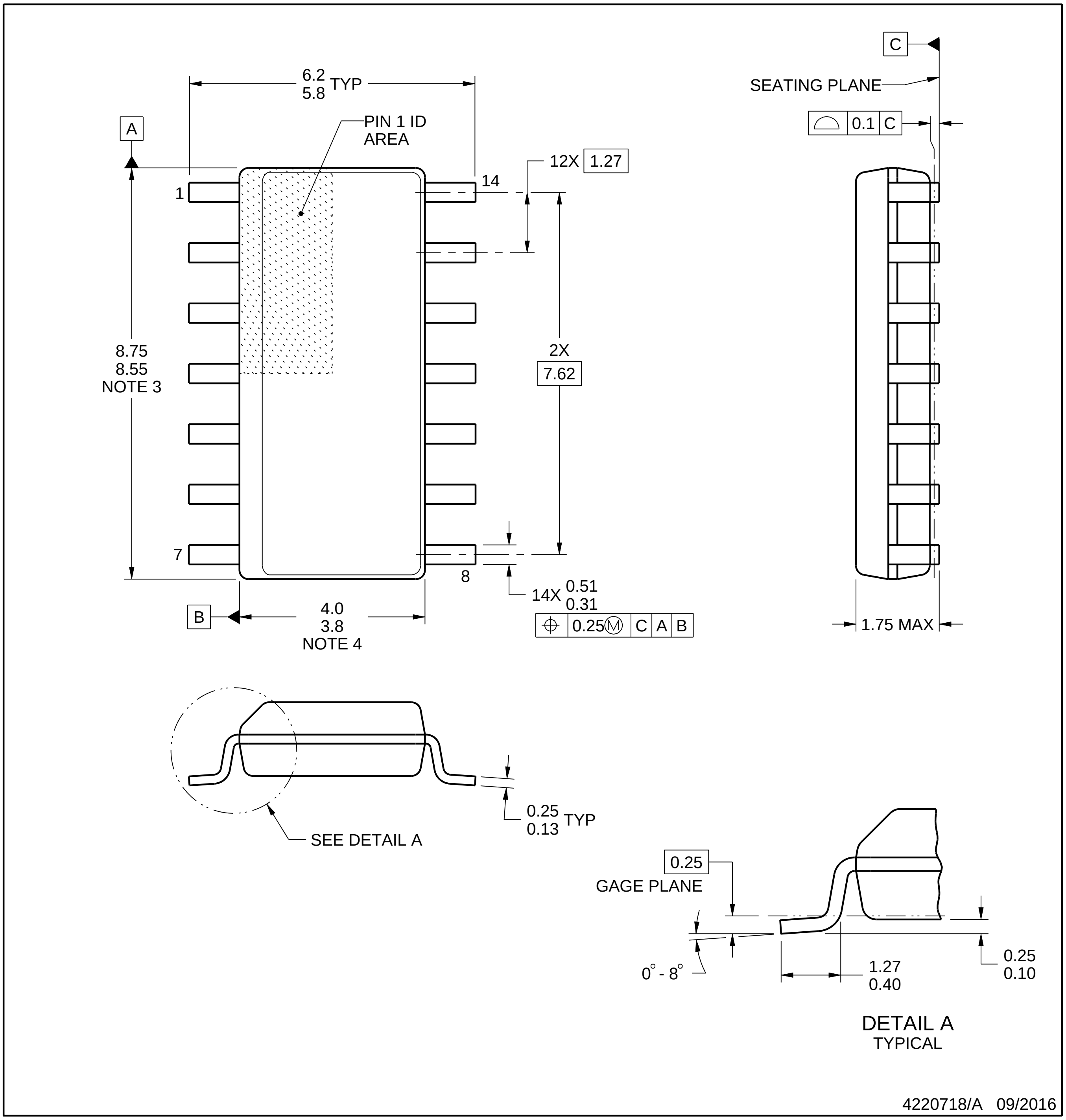
SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 20X

4219071 / A 05/2017

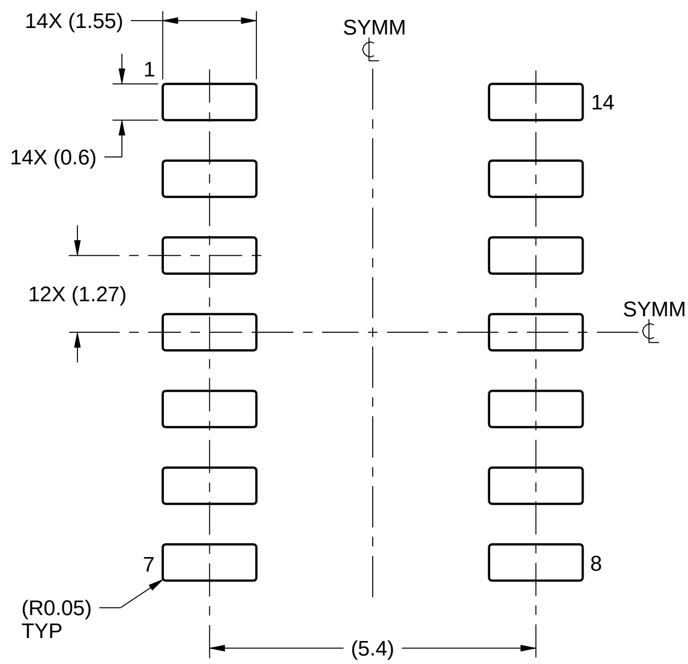
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

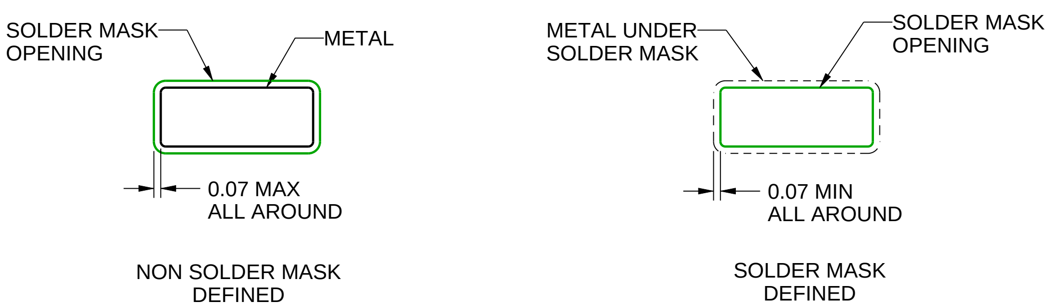


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

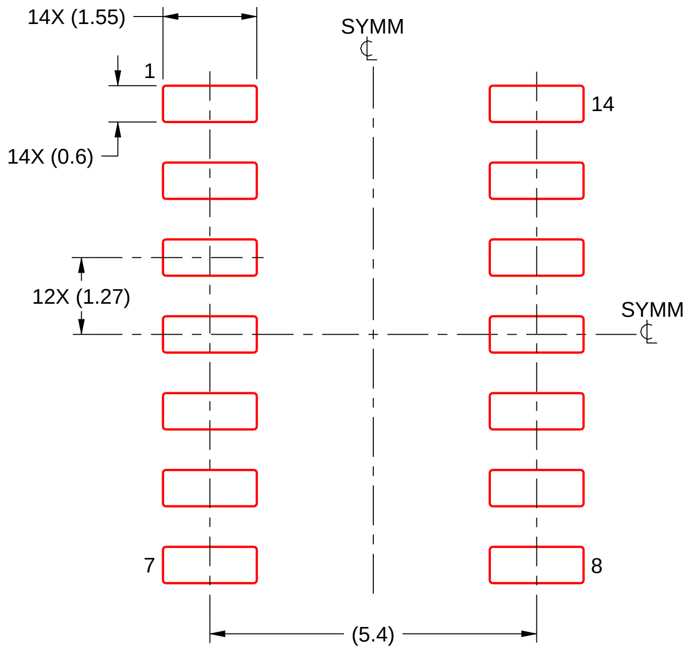


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

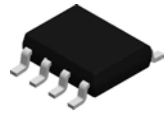


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

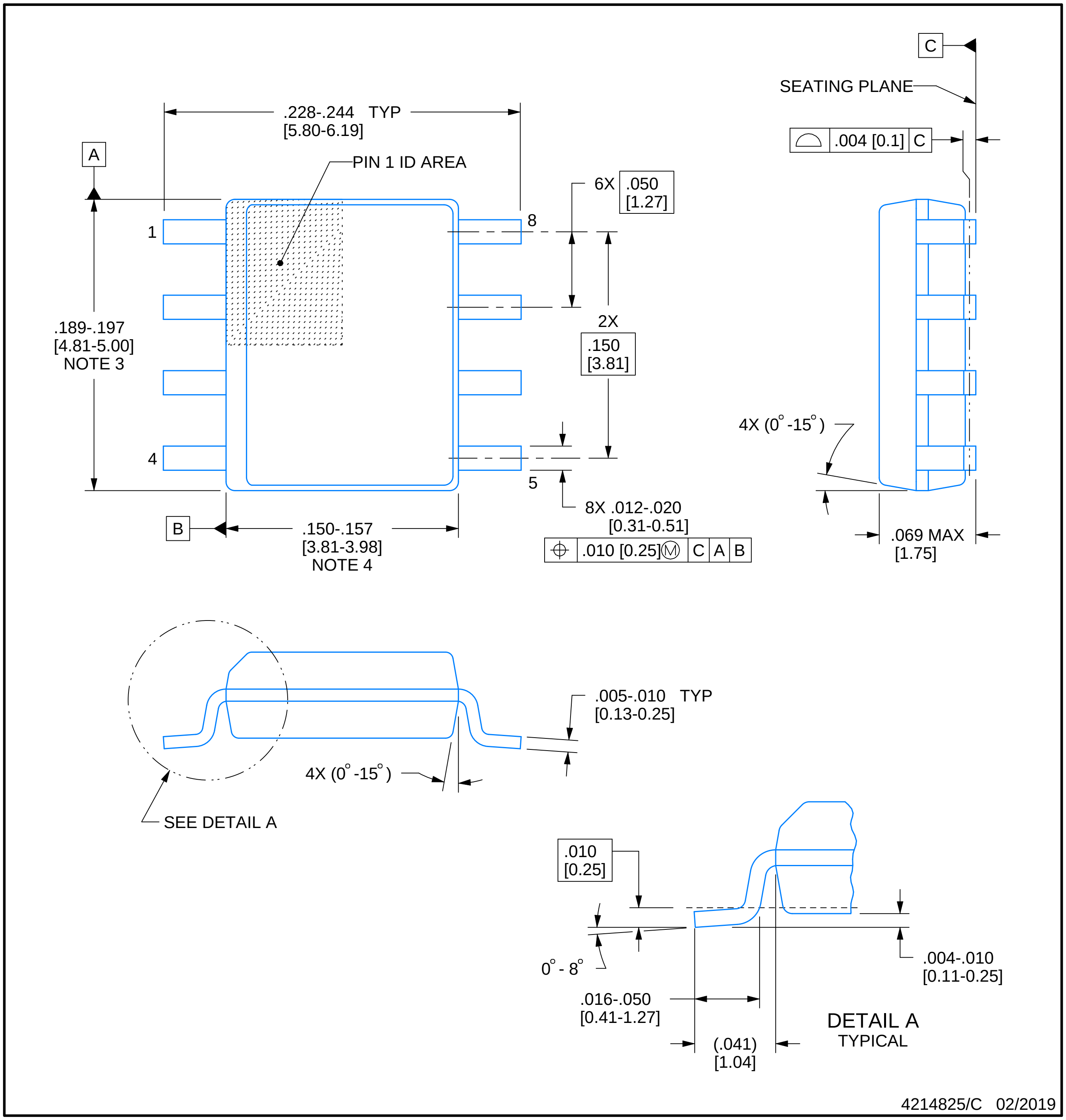
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

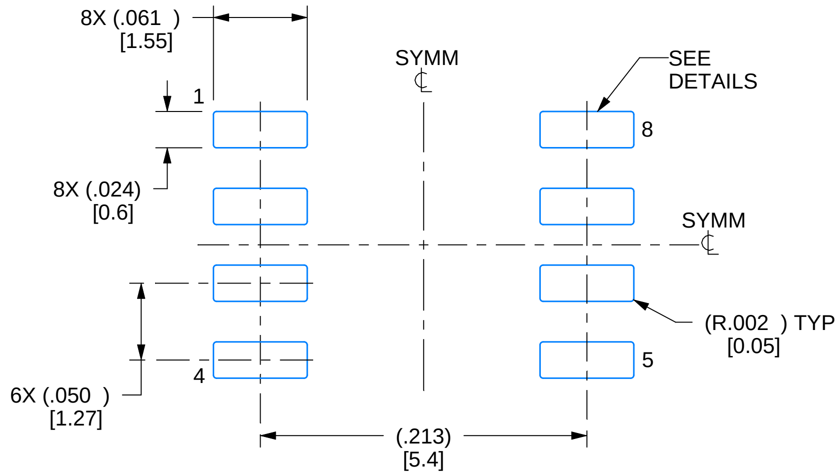
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

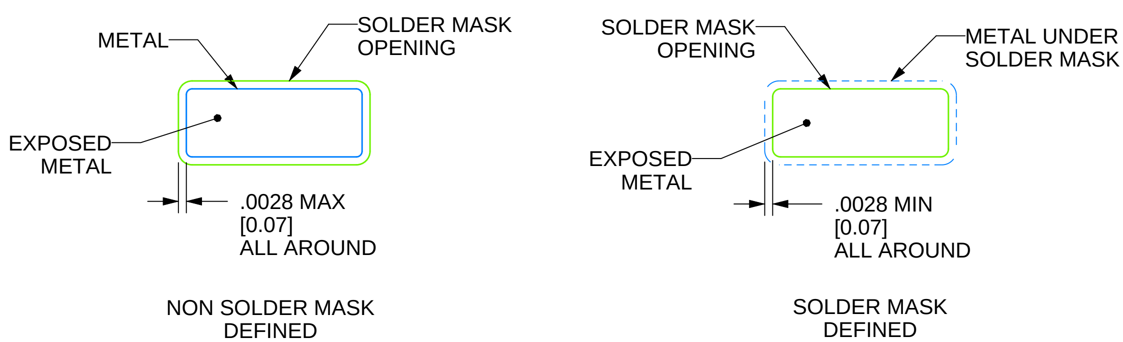


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

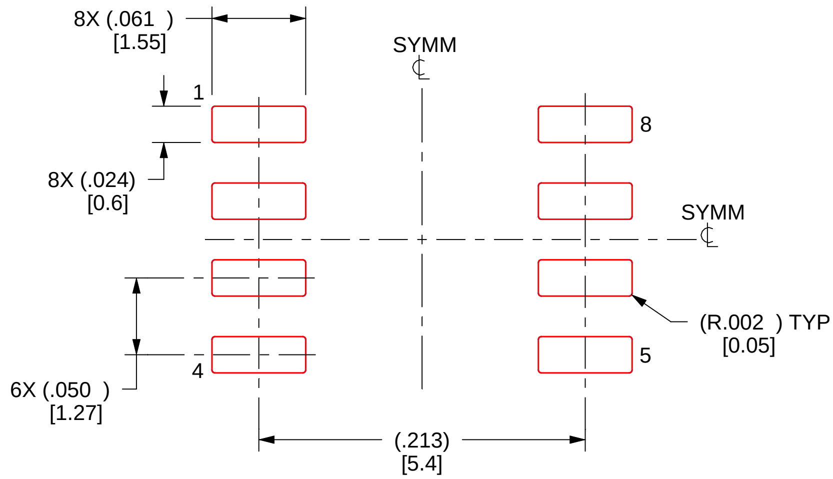


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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