

SN65HVD2x 拡張同相モード RS-485 トランシーバ

1 特長

- 同相電圧範囲 (-20V~25V) が TIA/EIA-485 の要件の 2 倍以上
- レシーバ・イコライゼーションにより、ケーブル長と信号速度を拡大 (SN65HVD2[3, 4])
- ユニット負荷の低減により最大 256 ノードに対応
- 16kV HBM 以上に対するバス I/O 保護
- 開放、短絡、アイドル・バス状況に対してフェイルセーフなレシーバ
- 低いスタンバイ時消費電流 (最大値 1μA)
- 100mV を超えるレシーバのヒステリシス

2 アプリケーション

- ケーブルの長いソリューション
 - ファクトリ・オートメーション
 - セキュリティ・ネットワーク
 - HVAC の構築
- 過酷な電気環境
 - 電力インバータ
 - 産業用ドライブ
 - 航空

3 概要

SN65HVD2x ファミリのトランシーバは、標準の RS-485 デバイスよりもはるかに優れた性能を発揮します。TIA/EIA-485-A 規格のすべての要件を満たすことに加えて、SN65HVD2x ファミリーは拡張同相電圧範囲で動作し、高い ESD 保護、広いレシーバ・ヒステリシス、フェイルセーフ動作などの機能を備えています。このファミリのデバイスは、ケーブル距離の長いアプリケーション、および通常のトランシーバには環境が過酷であるその他のアプリケーション用に設計されています。

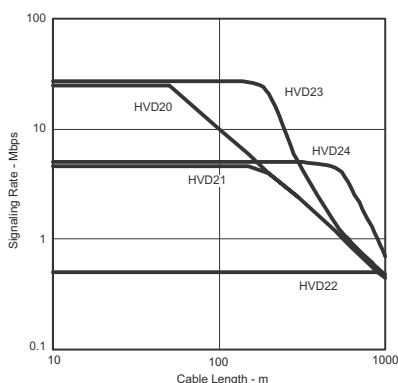
これらのデバイスは、マルチポイントのツイストペア・ケーブルでの双方向データ伝送用に設計されています。アプリケーションの例として、デジタル・モーター・コントローラ、リモート・センサとターミナル、産業用プロセス制御、セキュリティ・ステーション、環境制御システムが挙げられます。

これらの各デバイスは、3 ステートの差動ドライバと差動レシーバを組み合わせたもので、5V の単一電源で動作します。ドライバ差動出力とレシーバ差動入力とは内部で接続され、バスへの負荷を最小限に抑える差動バス・ポートを形成します。このポートは拡張同相電圧範囲に対応しているため、長いケーブルを使用するマルチポイント・アプリケーションに適しています。

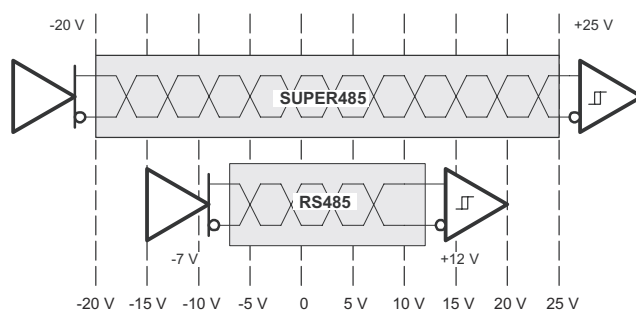
パッケージ情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
SN65HVD2x	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



SN65HVD2x のアプリケーション空間



SN65HVD2x デバイスは広い同相電圧範囲で動作



Table of Contents

1 特長	1	10 Detailed Description	19
2 アプリケーション	1	10.1 Overview.....	19
3 概要	1	10.2 Functional Block Diagram.....	19
4 Revision History	2	10.3 Feature Description.....	19
5 概要 (続き)	4	10.4 Device Functional Modes.....	21
6 Device Comparison	4	11 Application and Implementation	24
7 Pin Configuration and Functions	5	11.1 Application Information.....	24
8 Specifications	6	11.2 Typical Application.....	24
8.1 Absolute Maximum Ratings.....	6	12 Power Supply Recommendations	26
8.2 ESD Ratings.....	6	13 Layout	27
8.3 Recommended Operating Conditions.....	6	13.1 Layout Guidelines.....	27
8.4 Thermal Information.....	8	13.2 Layout Example.....	27
8.5 Driver Electrical Characteristics.....	8	14 Device and Documentation Support	28
8.6 Receiver Electrical Characteristics.....	9	14.1 Receiving Notification of Documentation Updates..	28
8.7 Driver Switching Characteristics.....	9	14.2 サポート・リソース.....	28
8.8 Receiver Switching Characteristics.....	10	14.3 Trademarks.....	28
8.9 Receiver Equalization Characteristics.....	10	14.4 Electrostatic Discharge Caution.....	28
8.10 Power Dissipation.....	11	14.5 Glossary.....	28
8.11 Typical Characteristics.....	12	15 Mechanical, Packaging, and Orderable Information	28
9 Parameter Measurement Information	14		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (November 2016) to Revision G (August 2022)	Page
• Deleted the Available Options table.....	4
• Changed the D (SOIC) values in the <i>Thermal Information</i>	8
Changes from Revision E (May 2010) to Revision F (November 2016)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。.....	1
• 「注文情報」表を削除。データシートの末尾にある POA を参照のこと.....	1
• Added maximum temperature value (150°C) to the Storage temperature, T _{stg} parameter.....	6
Changes from Revision D (April 2005) to Revision E (May 2010)	Page
• Replaced the Dissipation Rating table with the <i>Thermal Information</i> table.....	8
• Changed I _O - Added test condition and values per device number (<i>Driver Electrical Characteristics</i> table).....	8
• Changed the Thermal Characteristics table to <i>Power Dissipation</i> table.....	11
• Added the TEST MODE DRIVER DISABLE section.....	22
Changes from Revision C (September 2003) to Revision D (April 2005)	Page
• Added Receiver output current, I _O to the <i>Absolute Maximum Ratings</i> table.....	6
Changes from Revision B (June 2003) to Revision C (September 2003)	Page
• Added the <i>Thermal Information</i> table.....	8
• Added the Theory of Operation section.....	19
• Added the <i>Noise Considerations for Equalized Receivers</i> section.....	24

Changes from Revision A (March 2003) to Revision B (June 2003)	Page
• Added V_{IK} Typical Value of 0.75 V (<i>Driver Electrical Characteristics</i> table).....	8
• Deleted $V_{IT(F+)} - V_{CM} = -20\text{ V to } 25\text{ V}$ Minimum value (<i>Receiver Electrical Characteristics</i> table).....	9
• Added the <i>Receiver Equalization Characteristics</i> table.....	10
• Added  8-6,  8-7, and  8-8 to the <i>Typical Characteristics</i>	12
• Changed A Input circuit in the <i>Equivalent Input and Output Schematic Diagrams</i>	23
• Changed the Integrated Receiver Equalization Using the SN65HVD23 section.....	25
 Changes from Revision * (December 2002) to Revision A (March 2003)	 Page
• Changed t_{PZH} , t_{PHZ} , t_{PZL} , and t_{PLZ} - From a maximum value of 120 to include typical and maximum values for each entry (<i>Receiver Switching Characteristics</i> table).....	10
• Changed t_{PZH} , t_{PHZ} , t_{PZL} , and t_{PLZ} - From a maximum value of 120 to include typical and maximum values for each entry (<i>Receiver Switching Characteristics</i> table).....	10

5 概要 (続き)

SN65HVD20 デバイスは、最大 25Mbps の高い信号速度で最大 64 ノードのネットワークを相互接続できます。

SN65HVD21 デバイスは、中程度のデータ・レート (最大 5Mbps) で最大 256 のノードを接続できます。ドライバの出力スルーレートは制御されており、成形された遷移により信頼性の高いスイッチングを実現し、高周波のノイズ放射を低減します。

SN65HVD22 デバイスは、放射に敏感なアプリケーションで放射ノイズを低減し、長いスタブで信号品質を向上するよう、ドライバの出力スルーレートを制御します。最大 256 の SN65HVD22 ノードを、最大 500kbps の信号速度で接続できます。

SN65HVD23 デバイスは、レシーバ・イコライゼーション技術を実装しており、差動バス・アプリケーションでジッタ性能が向上するとともに、最長 160m のケーブルで最大 25Mbps のデータ・レートを実現します。

SN65HVD24 デバイスはレシーバ・イコライゼーション技術を実装しており、差動バス・アプリケーションでジッタ性能が向上するとともに、最長 1000m のケーブルで 1Mbps~10Mbps のデータ・レートを実現します。

レシーバにはフェイルセーフ回路が内蔵されており、入力信号が消失すると 250 マイクロ秒以内に高レベル出力を供給します。信号消失の最も一般的な原因は、ケーブルの切断、ラインの短絡、またはバス上にアクティブなトランスミッタが存在しないことです。この機能により、これらの障害条件が発生したときに、ノイズが有効なデータとして受信されることを防止できます。この機能は、有線 OR バスの信号伝達に使用できます。

SN65HVD2x デバイスは、-40°C~85°Cの温度で動作が規定されています。

6 Device Comparison

表 6-1. Product Selection Guide

PART NUMBERS	CABLE LENGTH AND SIGNALING RATE ⁽¹⁾	NODES	MARKING
SN65HVD20	Up to 50 m at 25 Mbps	Up to 64	D: VP20, P: 65HVD20
SN65HVD21	Up to 150 m at 5 Mbps (with slew rate limit)	Up to 256	D: VP21, P: 65HVD21
SN65HVD22	Up to 1200 m at 500 kbps (with slew rate limit)	Up to 256	D: VP22, P: 65HVD22
SN65HVD23	Up to 160 m at 25 Mbps (with receiver equalization)	Up to 64	D: VP23, P: 65HVD23
SN65HVD24	Up to 500 m at 3 Mbps (with receiver equalization)	Up to 256	D: VP24, P: 65HVD24

(1) Distance and signaling rate predictions based upon Belden 3105A cable and 15% eye pattern jitter.

7 Pin Configuration and Functions

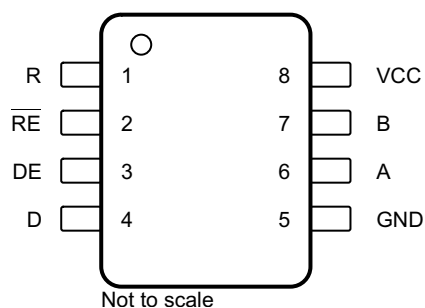


图 7-1. D or P Package, 8-Pin SOIC or PDIP
(Top View)

表 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input and output	Driver output or receiver input (complementary to B)
B	7	Bus input and output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
RE	2	Digital input	Receiver enable, active low
VCC	8	Supply	4.5-V to 5.5-V supply

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
Supply voltage ⁽²⁾			−0.5	7	V
Voltage at any bus I/O terminal			−27	27	V
Voltage input, transient pulse	A, B	(through 100 Ω, see Figure 9-16)	−60	60	V
Voltage input	D, DE, RE		−0.5	V _{CC} + 0.5	V
Receiver output current			−10	10	mA
Continuous total power dissipation			See Power Dissipation Ratings		
Junction temperature, T _J				150	°C
Storage temperature, T _{stg}				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

8.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except 5, 6, and 7	±5000	V
		Pins 5, 6, and 7	±16000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1500	
	Machine Model (MM) ⁽³⁾		±200	

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(2) Tested in accordance with JEDEC Standard 22, Test Method C101.

(3) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
	Voltage at any bus I/O terminal	A, B	−20		25	V
V _{IH}	High-level input voltage	D, DE, RE	2		V _{CC}	V
V _{IL}	Low-level input voltage		0		0.8	V
V _{ID}	Differential input voltage	A with respect to B	−25		25	V
Output current	Driver		−110		110	mA
	Receiver		−8		8	

8.3 Recommended Operating Conditions (continued)

			MIN	NOM	MAX	UNIT
I_{CC}	Supply current	Driver enabled (DE at V_{CC}), Receiver enabled (RE at 0 V), No load, $V_I = 0$ V or V_{CC}	SN65HVD20	6	9	mA
			SN65HVD21	8	12	
			SN65HVD22	6	9	
			SN65HVD23	7	11	
			SN65HVD24	10	14	
	Driver enabled (DE at V_{CC}), Receiver disabled (RE at V_{CC}), No load, $V_I = 0$ V or V_{CC}		SN65HVD20	5	8	
			SN65HVD21	7	11	
			SN65HVD22	5	8	
			SN65HVD23	5	9	
			SN65HVD24	8	12	
	Driver disabled (DE at 0 V), Receiver enabled (RE at 0 V), No load		SN65HVD20	4	7	
			SN65HVD21	5	8	
			SN65HVD22	4	7	
			SN65HVD23	4.5	9	
			SN65HVD24	5.5	10	
	Driver disabled (DE at 0 V), Receiver disabled (RE at V_{CC}) D open	All SN65HVD2x			1	μ A
T_A	Operating free-air temperature ⁽¹⁾		–40		85	°C
T_J	Junction temperature		–40		130	°C

(1) Maximum free-air temperature operation is allowed as long as the device recommended junction temperature is not exceeded.

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN65HVD2x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	110.7	52.5	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	49.9	57.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.7	38.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	6.0	19.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	55.9	31.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

8.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted).⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = −18 mA		−1.5	0.75		V
V _O	Open-circuit output voltage	A or B, No load		0		V _{CC}	V
V _{OD(SS)}	Steady-state differential output voltage	No load (open circuit)		3.3	4.2	V _{CC}	V
		R _L = 54 Ω, See 9-1		1.8	2.5		
		With common-mode loading, See 9-2		1.8			
Δ V _{OD(SS)}	Change in steady-state differential output voltage between logic states	See 9-1 and 9-3		−0.1		0.1	V
V _{OC(SS)}	Steady-state common-mode output voltage	See 9-1		2.1	2.5	2.9	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage, V _{OC(H)} − V _{OC(L)}	See 9-1 and 9-4		−0.1		0.1	V
V _{OC(PP)}	Peak-to-peak common-mode output voltage, V _{OC(MAX)} − V _{OC(MIN)}	R _L = 54 Ω, C _L = 50 pF, See 9-1 and 9-4		0.35			V
V _{OD(RING)}	Differential output voltage over and under shoot	R _L = 54 Ω, C _L = 50 pF, See 9-5				10%	
I _I	Input current	D, DE		−100		100	μA
I _O	Output current with power off. High impedance state output current.	V _O = −7 V to 12 V, Other input = 0 V	SN65HVD2[0,3]	−400		500	μA
			SN65HVD2[1,2,4]	−100		125	
		V _O = −20 V to 25 V, Other input = 0 V	SN65HVD2[0,3]	−800		1000	
			SN65HVD2[1,2,4]	−200		250	
I _{OS}	Short-circuit output current	V _O = −20 V to 25 V, See 9-9		−250		250	mA
C _{OD}	Differential output capacitance					20	pF

(1) All typical values are at V_{CC} = 5 V and 25°C.

8.6 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going differential input voltage threshold	See 9-10	$V_O = 2.4 \text{ V}$, $I_O = -8 \text{ mA}$		60	200	mV
$V_{IT(-)}$	Negative-going differential input voltage threshold		$V_O = 0.4 \text{ V}$, $I_O = 8 \text{ mA}$	-200	-60		
V_{HYS}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			100	130		mV
$V_{IT(F+)}$	Positive-going differential input failsafe voltage threshold	See 9-15	$V_{CM} = -7 \text{ V to } 12 \text{ V}$	40	120	200	mV
			$V_{CM} = -20 \text{ V to } 25 \text{ V}$		120	250	
$V_{IT(F-)}$	Negative-going differential input failsafe voltage threshold	See 9-15	$V_{CM} = -7 \text{ V to } 12 \text{ V}$	-200	-120	-40	mV
			$V_{CM} = -20 \text{ V to } 25 \text{ V}$	-250	-120		
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$		-1.5			V
V_{OH}	High-level output voltage	$V_{ID} = 200 \text{ mV}$, $I_{OH} = -8 \text{ mA}$, See 9-11		4			V
V_{OL}	Low-level output voltage	$V_{ID} = -200 \text{ mV}$, $I_{OL} = 8 \text{ mA}$, See 9-11				0.4	V
$I_{I(BUS)}$	Bus input current (power on or power off)	$V_I = -7 \text{ to } 12 \text{ V}$, Other input = 0 V	SN65HVD2[0,3]	-400		500	μA
			SN65HVD2[1,2,4]	-100		125	
		$V_I = -20 \text{ to } 25 \text{ V}$, Other input = 0 V	SN65HVD2[0,3]	-800		1000	
			SN65HVD2[1,2,4]	-200		250	
I_I	Input current	$\overline{RE}$		-100		100	μA
R_I	Input resistance	SN65HVD2[0,3]		24			k Ω
		SN65HVD2[1,2,4]		96			
C_{ID}	Differential input capacitance	$V_{ID} = 0.5 + 0.4 \text{ sine } (2\pi \times 1.5 \times 10^6 \text{ t})$			20		pF

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and 25°C .

8.7 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Differential output propagation delay, low-to-high and high-to-low	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See 9-3	SN65HVD2[0,3]	6	10	20	ns
			SN65HVD2[1,4]	20	32	60	
			SN65HVD22	160	280	500	
t_r , t_f	Differential output rise time and fall time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See 9-3	SN65HVD2[0,3]	2	6	12	ns
			SN65HVD2[1,4]	20	40	60	
			SN65HVD22	175	400	600	
t_{PZH} , t_{PHZ}	Propagation delay time, high-impedance-to-high-level output and high-level output-to-high-impedance	$\overline{RE}$ at 0 V, See 9-6	SN65HVD2[0,3]			40	ns
			SN65HVD2[1,4]			100	
			SN65HVD22			300	
t_{PZL} , t_{PLZ}	Propagation delay time, high-impedance-to-high-level output and high-level output-to-high-impedance	$\overline{RE}$ at 0 V, See 9-7	SN65HVD2[0,3]			40	ns
			SN65HVD2[1,4]			100	
			SN65HVD22			300	
$t_{d(\text{standby})}$	Time from an active differential output to standby					2	μs
$t_{d(\text{wake})}$	Wake-up time from standby to an active differential output	$\overline{RE}$ at V_{CC} , See 9-8				8	μs
$t_{sk(p)}$	Pulse skew $t_{PLH} - t_{PHL}$	SN65HVD2[0,3]				2	ns
		SN65HVD2[1,4]				6	
		SN65HVD22				50	

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and 25°C .

8.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output and high-to low level output	See 9-11	SN65HVD2[0,3]		16	35	ns
t_{PHL}			SN65HVD2[1,2,4]		25	50	
t_r t_f	Receiver output rise time Receiver output fall time	See 9-11			2	4	ns
t_{PZH} t_{PHZ}	Receiver output enable time to high level and disable time from high level	See 9-12			90 16	120 35	ns
t_{PZL} t_{PLZ}	Receiver output enable time to low level and disable time from low level	See 9-13			90 16	120 35	ns
$t_{r(standby)}$	Time from an active receiver output to standby	See 9-14 , DE at 0 V				2	μ s
$t_{r(wake)}$	Wake-up time from standby to an active receiver output	See 9-14 , DE at 0 V				8	μ s
$t_{sk(p)}$	Pulse skew $ t_{PLH} - t_{PHL} $					5	ns
$t_{p(set)}$	Delay time, bus fail to failsafe set	See 9-15 , pulse rate = 1 kHz			250	350	μ s
$t_{p(reset)}$	Delay time, bus recovery to failsafe reset	See 9-15 , pulse rate = 1 kHz			50		ns

8.9 Receiver Equalization Characteristics

over recommended operating conditions (unless otherwise noted)^{(1) (2)}

PARAMETER		TEST CONDITIONS				TYP	UNIT
$t_{j(pp)}$	Peak-to-peak eye-pattern jitter	Peudo-random NRZ code with a bit pattern length of $2^{16} - 1$, Belden 3105A cable, See 10-2	25 Mbps	0 m	SN65HVD23	2	ns
				100 m	SN65HVD20	6	ns
					SN65HVD23	3	
				150 m	SN65HVD20	15	ns
					SN65HVD23	4	
			200 m	SN65HVD20	27	ns	
					SN65HVD23	8	
			10 Mbps	200 m	SN65HVD20	22	ns
					SN65HVD23	8	
				250 m	SN65HVD20	34	ns
					SN65HVD23	15	
				300 m	SN65HVD20	49	ns
					SN65HVD23	27	
			5 Mbps	500 m	SN65HVD21	128	ns
					SN65HVD24	18	
			3 Mbps	500 m	SN65HVD20	93	ns
					SN65HVD21	103	
					SN65HVD23	90	
					SN65HVD24	16	
			1 Mbps	1000 m	SN65HVD21	216	ns
					SN65HVD24	62	

(1) The SN65HVD20 and SN65HVD21 do not have receiver equalization, but are specified for comparison.

(2) All typical values are at $V_{CC} = 5$ V, and temperature = 25°C.

8.10 Power Dissipation

PARAMETERS		TEST CONDITIONS			VALUE	UNIT
P _D	Device power dissipation	Typical	V _{CC} = 5 V, T _J = 25°C, R _L = 54 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	SN65HVD20: 25 Mbps	295	mW
				SN65HVD21: 5 Mbps	260	
				SN65HVD22: 500 kbps	233	
				SN65HVD23: 25 Mbps	302	
				SN65HVD24: 5 Mbps	267	
		Worst case	V _{CC} = 5.5 V, T _J = 125°C, R _L = 54 Ω, C _L = 50 pF, C _L = 15 pF (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	SN65HVD20: 25 Mbps	408	mW
				SN65HVD21: 5 Mbps	342	
				SN65HVD22: 500 kbps	300	
				SN65HVD23: 25 Mbps	417	
				SN65HVD24: 5 Mbps	352	
T _{SD}	Thermal shut down junction temperature				170	°C

8.11 Typical Characteristics

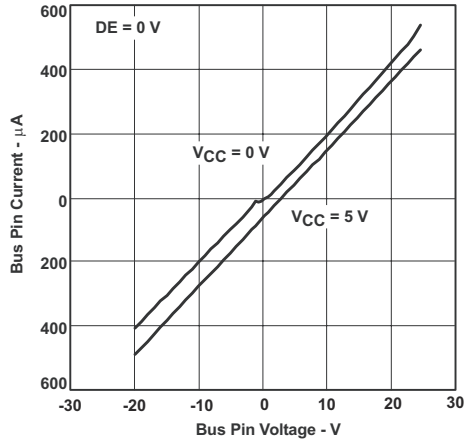


FIG 8-1. SN65HVD20[0,3] Bus Pin Current vs Bus Pin Voltage

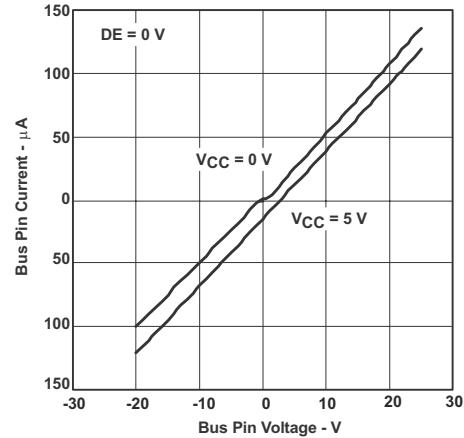


FIG 8-2. SN65HVD2[1,2,4] Bus Pin Current vs Bus Pin Voltage

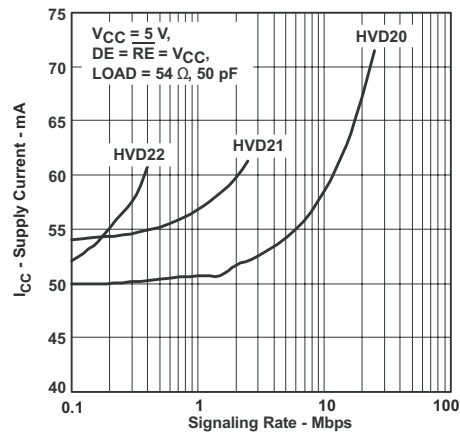


FIG 8-3. Supply Current vs Signaling Rate

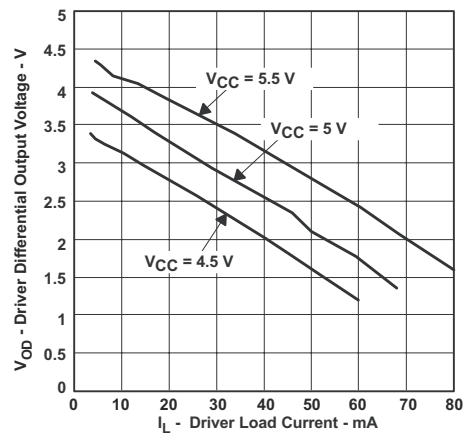


FIG 8-4. Driver Differential Output Voltage vs Driver Load Current

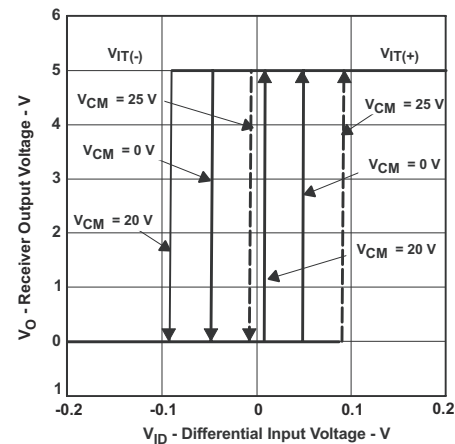


FIG 8-5. Receiver Output Voltage vs Differential Input Voltage

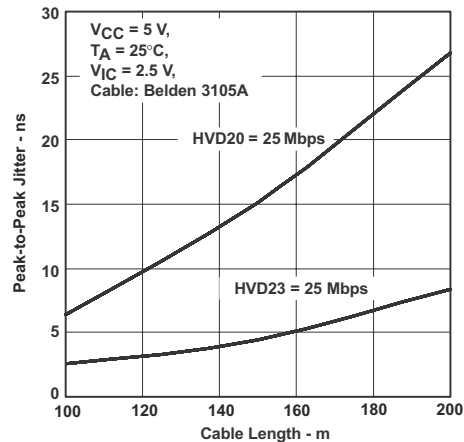


FIG 8-6. SN65HVD2[0,3] Peak-to-Peak Jitter vs Cable Length

8.11 Typical Characteristics (continued)

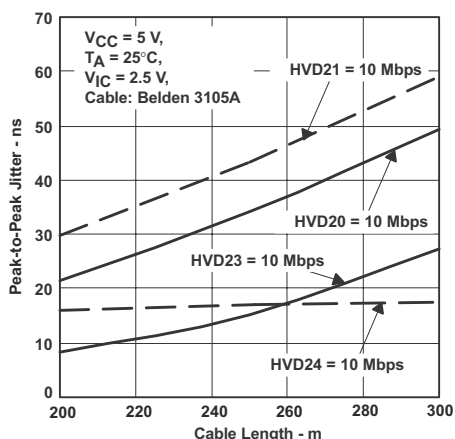


图 8-7. SN65HVD2[0,1,3,4] Peak-to-Peak Jitter vs Cable Length

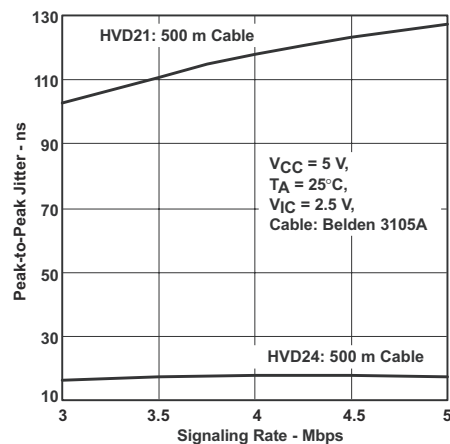


图 8-8. SN65HVD2[1,4] Peak-to-Peak Jitter vs Signaling Rate

9 Parameter Measurement Information

注

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle, $Z_O = 50\ \Omega$ (unless otherwise specified).

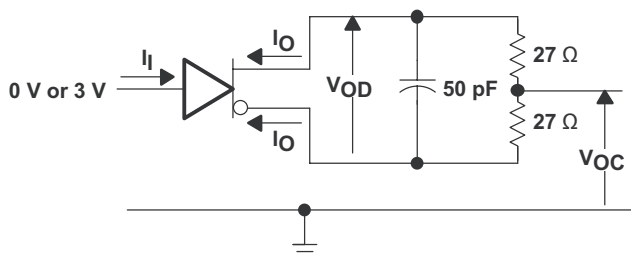


图 9-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

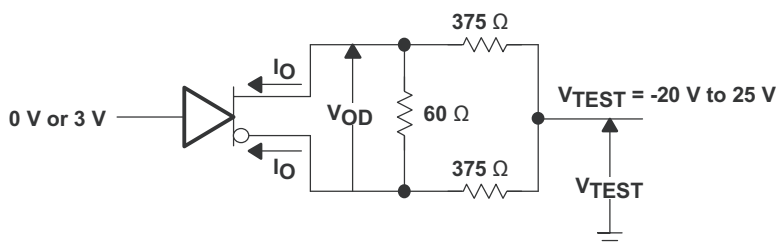


图 9-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

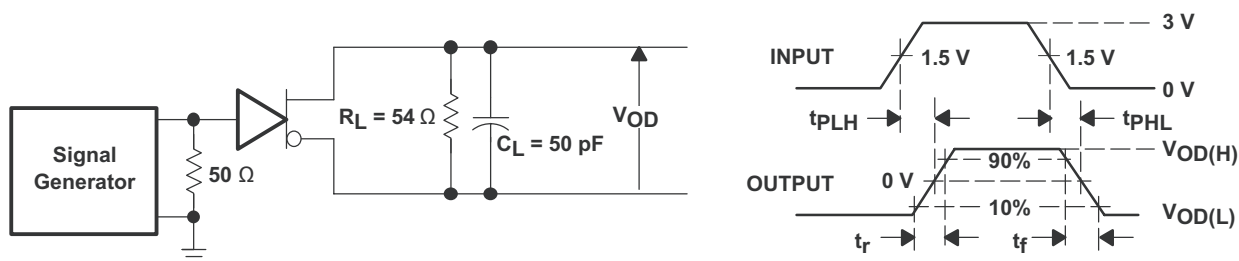


图 9-3. Driver Switching Test Circuit and Waveforms

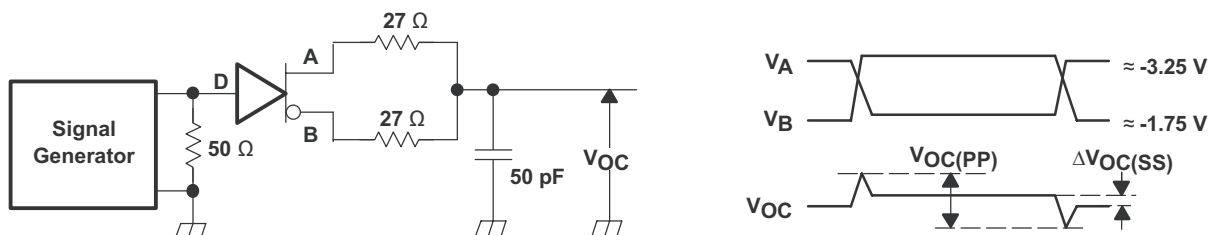
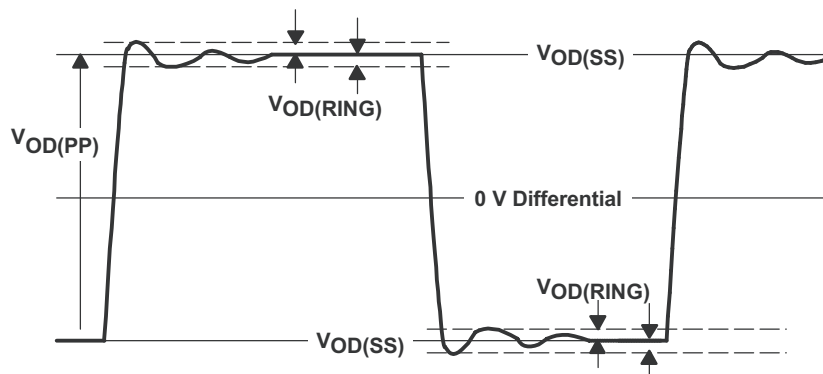
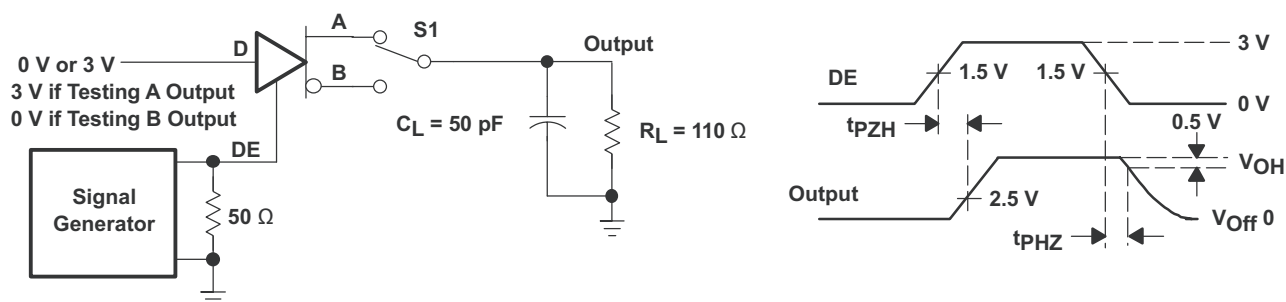


图 9-4. Driver V_{OC} Test Circuit and Waveforms

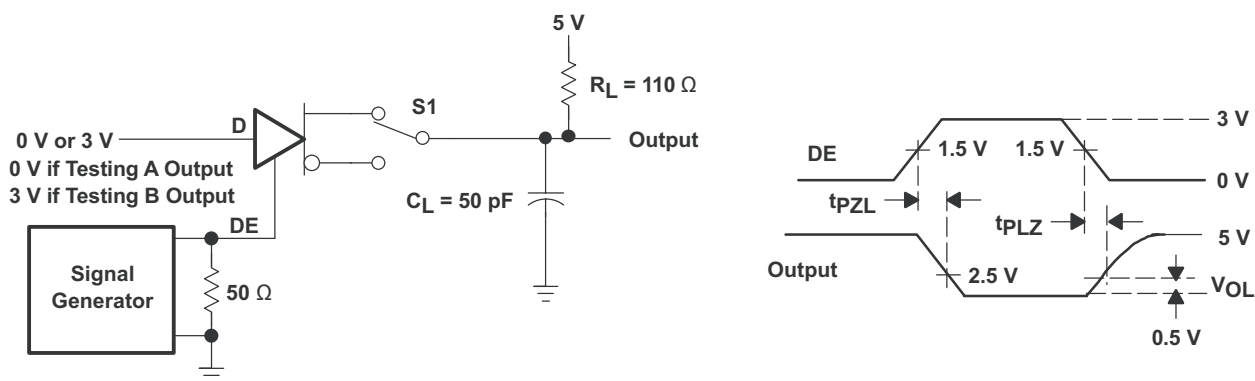


$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

9-5. $V_{OD(RING)}$ Waveform and Definitions



9-6. Driver Enable and Disable Test, High Output



9-7. Driver Enable and Disable Test, Low Output

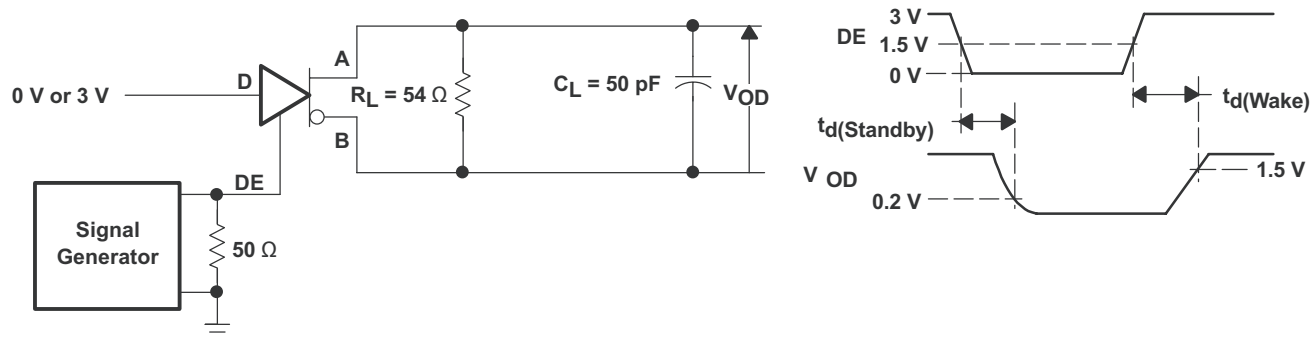


Figure 9-8. Driver Standby and Wake Test Circuit and Waveforms

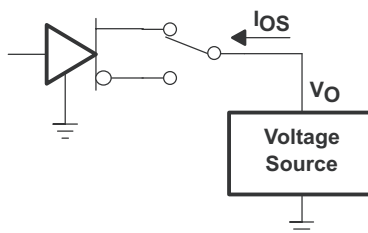


Figure 9-9. Driver Short-Circuit Test

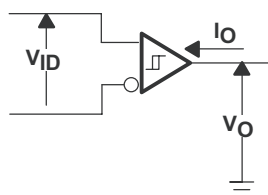


Figure 9-10. Receiver DC Parameter Definitions

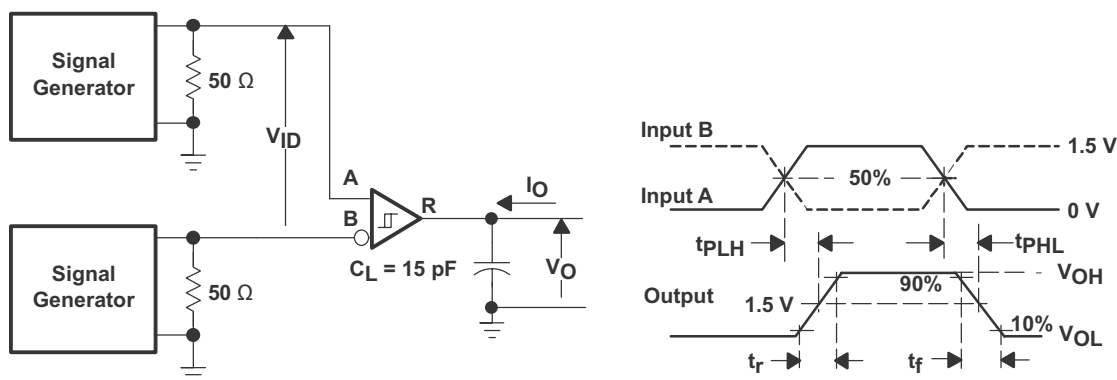
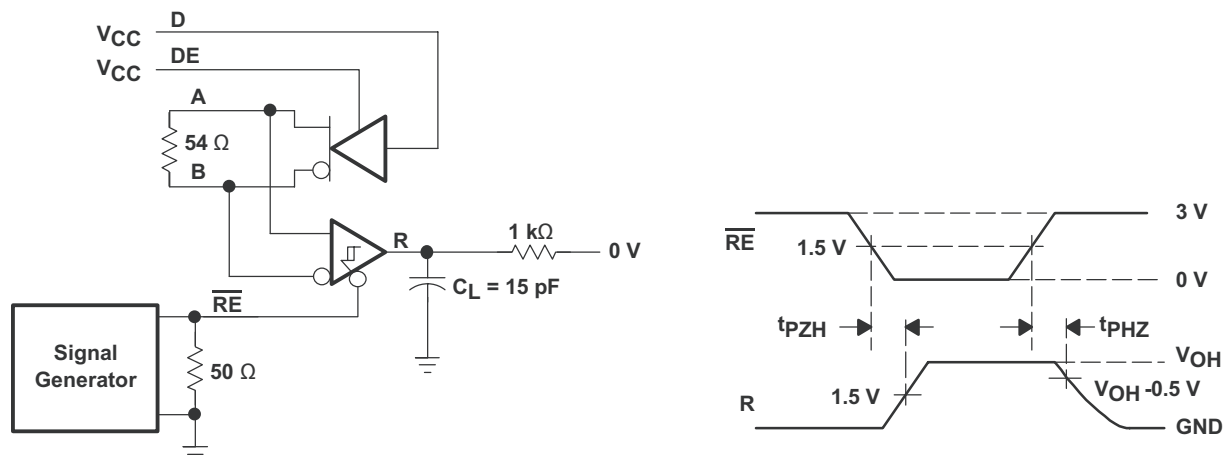
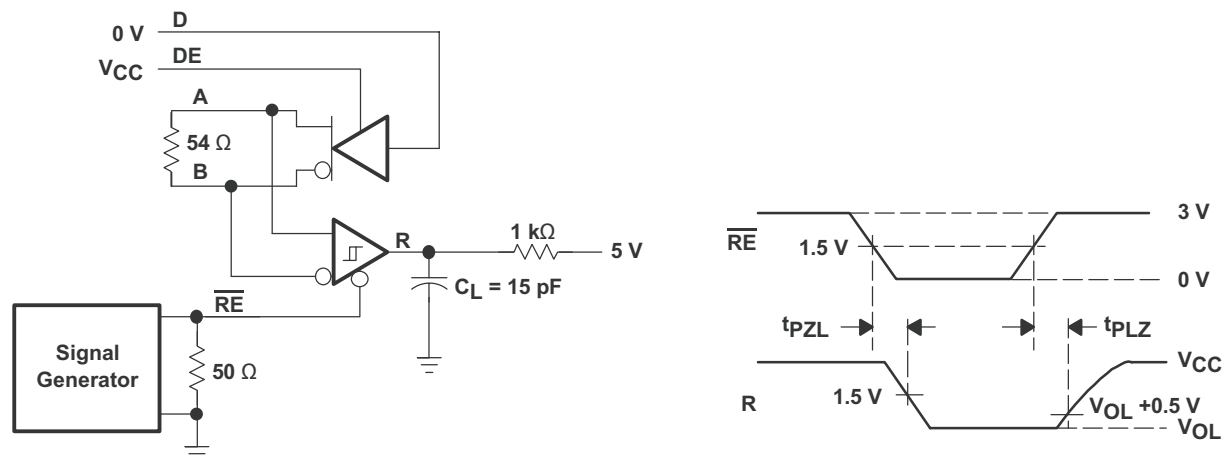


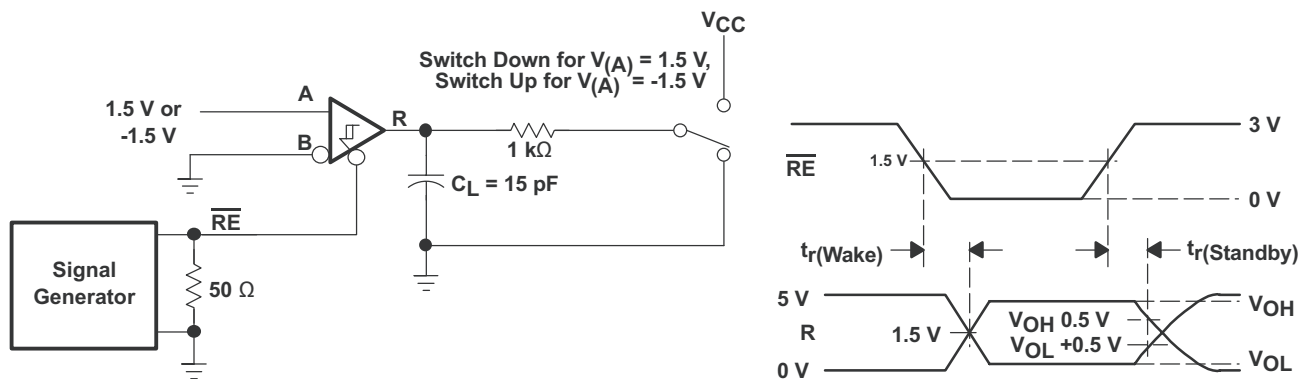
Figure 9-11. Receiver Switching Test Circuit and Waveforms



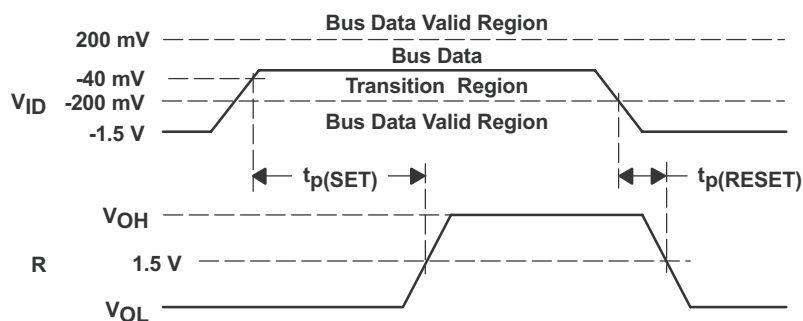
9-12. Receiver Enable Test Circuit and Waveforms, Data Output High



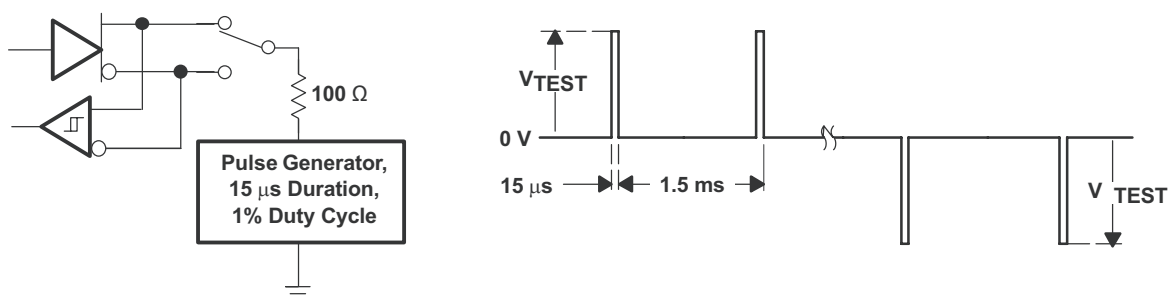
9-13. Receiver Enable Test Circuit and Waveforms, Data Output Low



9-14. Receiver Standby and Wake Test Circuit and Waveforms



9-15. Receiver Active Failsafe Definitions and Waveforms



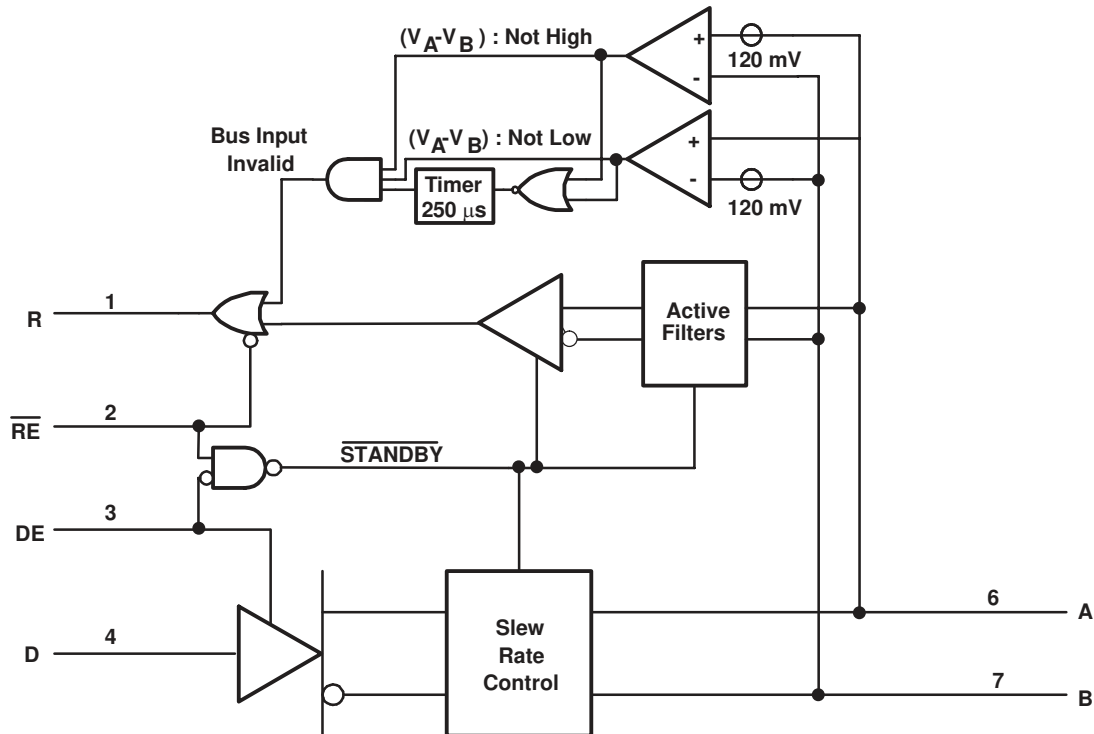
9-16. Test Circuit and Waveforms, Transient Overvoltage Test

10 Detailed Description

10.1 Overview

The SN65HVD2x family of devices are RS-485 compliant half-duplex transceivers designed for communication rates up to 500 kbps (SN65HVD22), 3 Mbps (SN65HVD24), 5 Mbps (SN65HVD21), or 25 Mbps (SN65HVD20 and SN65HVD23). The devices feature extended common-mode range support, which provides immunity to larger ground potential differences that can occur between nodes that communicate over longer distances. The SN65HVD23 and the SN65HVD24 devices feature receiver equalization, which reduces the amount of data-dependent jitter that is introduced by the high-frequency losses associated with long cables.

10.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

10.3 Feature Description

The SN65HVD2x family of devices integrates a differential receiver and differential driver with additional features for improved performance in electrically-noisy, long-cable, or other fault-intolerant applications.

The receiver hysteresis (typically 130 mV) is much larger than found in typical RS-485 transceivers. This helps reject spurious noise signals which would otherwise cause false changes in the receiver output state.

Slew rate limiting on the driver outputs (SN65HVD2[1,2,4]) reduces the high-frequency content of signal edges. This decreases reflections from bus discontinuities, and allows longer stub lengths between nodes and the main bus line. Designers must consider the maximum signaling rate and cable length required for a specific application, and choose the transceiver best matching those requirements.

When DE is low, the differential driver is disabled, and the A and B outputs are in high-impedance states. When DE is high, the differential driver is enabled, and drives the A and B outputs according to the state of the D inputs.

When RE is high, the differential receiver output buffer is disabled, and the R output is in a high-impedance state. When RE is low, the differential receiver is enabled, and the R output reflects the state of the differential bus inputs on the A and B pins.

If both the driver and receiver are disabled, (DE low and RE high) then all nonessential circuitry, including auxiliary functions such as failsafe and receiver equalization is placed in a low-power standby state. This reduces power consumption to less than 5 µW. When either enable input is asserted, the circuitry again becomes active.

In addition to the primary differential receiver, these devices incorporate a set of comparators and logic to implement an active receiver failsafe feature. These components determine whether the differential bus signal is valid. Whenever the differential signal is close to zero volts (neither high nor low), a timer initiates. If the differential input remains within the transition range for more than 250 µs, the timer expires and set the receiver output to the high state. If a valid bus input (high or low) is received at any time, the receiver output reflects the valid bus state, and the timer is reset.

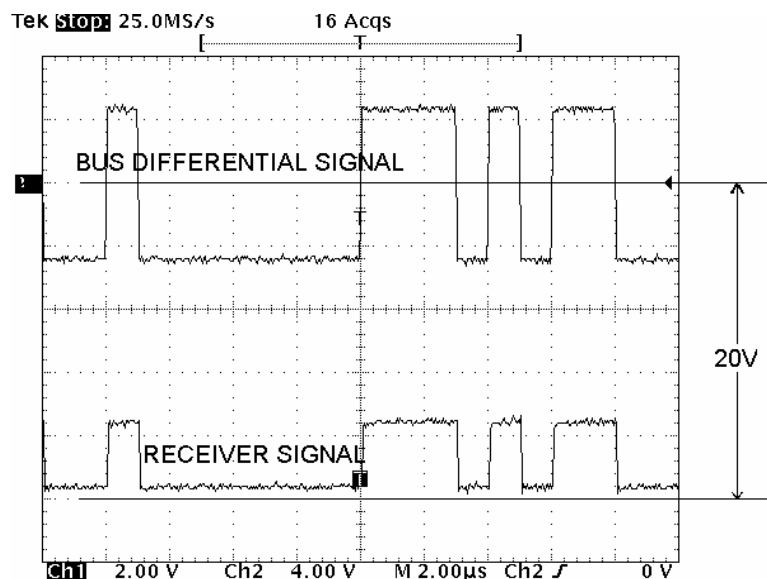


FIG 10-1. SN65HVD22 Receiver Operation With 20-V Offset on Input Signal

$H(s) = k_0 \left[(1-k_1) + \frac{k_1 p_1}{(s + p_1)} \right] \left[(1-k_2) + \frac{k_2 p_2}{(s + p_2)} \right] \left[(1-k_3) + \frac{k_3 p_3}{(s + p_3)} \right]$	k0 (DC loss)	p1 (MHz)	k1	p2 (MHz)	k2	p3 (MHz)	k3
Similar to 160m of Belden 3105A	0.95	0.25	0.3	3.5	0.5	15	1
Similar to 250m of Belden 3105A	0.9	0.25	0.4	3.5	0.7	12	1
Similar to 500m of Belden 3105A	0.8	0.25	0.6	2.2	1	8	1
Similar to 1000m of Belden 3105A	0.6	0.3	1	3	1	6	1

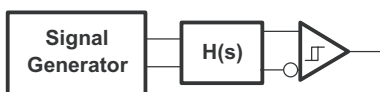


FIG 10-2. Cable Attenuation Model for Jitter Measurements

10.4 Device Functional Modes

The driver and receiver behavior for different input conditions are shown in 表 10-1 and 表 10-2, respectively.

表 10-1. Driver Function Table⁽¹⁾

DEVICE	INPUT	ENABLE	OUTPUTS	
	D	DE	A	B
SN65HVD2[0,1,2]	H	H	H	L
	L	H	L	H
	X	L	Z	Z
	X	OPEN	Z	Z
	OPEN	H	H	L
SN65HVD2[3,4]	H	H	H	L
	L	H	L	H
	X	L	Z	Z
	X	OPEN	Z	Z
	OPEN	H	L	H

(1) Legend: H = high level, L = low level, X = don't care, Z = high impedance (off), ? = indeterminate

表 10-2. Receiver Function Table⁽¹⁾

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE RE	OUTPUT R
$0.2\text{ V} \leq V_{ID}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	H ⁽²⁾
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
X	OPEN	Z
Open circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

(1) H = high level, L = low level, Z = high impedance (off)

(2) If the differential input V_{ID} remains within the transition range for more than 250 μs , the integrated failsafe circuitry detects a bus fault, and set the receiver output to a high state. See 图 9-15.

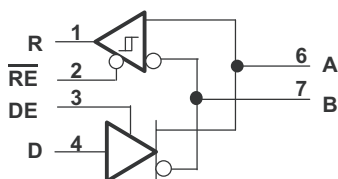


图 10-3. Logic Diagram

10.4.1 Test Mode Driver Disable

If the input signal to the D pin is such that:

1. the signal has signaling rate above 4 Mbps (for the SN65HVD21 and SN65HVD24),
2. the signal has signaling rate above 6 Mbps (for the SN65HVD20 and SN65HVD23),
3. the signal has average amplitude from 1.2 V to 1.6 V ($1.4\text{ V} \pm 200\text{ mV}$), or
4. the average signal amplitude remains in this range for 100 μs or longer,

then the driver may activate a test-mode during which the driver outputs are temporarily disabled. This can cause loss of transmission of data during the period that the device is in the test-mode. The driver is re-enabled and resumes normal operation whenever the above conditions are not true. The device is not damaged by this test mode.

Although rare, there are combinations of specific voltage levels and input data patterns within the operating conditions of the SN65HVD2x family which may lead to a temporary state where the driver outputs are disabled for a period of time.

Observations:

1. The conditions for inadvertently entering the test mode are dependent on the levels, duration, and duty cycle of the logic signal input to the D pin. Operating input levels are specified as greater than 2 V for a logic HIGH input, and less than 0.8 V for a logic LOW input. Therefore, a valid steady-state logic input does not cause the device to activate the test mode
2. Only input signals with frequency content above 2 MHz (4 Mbps) have a possibility of activating the test mode. Therefore, this issue should not affect the normal operation of the SN65HVD22 (500 kbps).
3. For operating signaling rates of 4 Mbps (or above), the conditions stated above must remain true over a period of: $4\text{ Mbps} \times 100\text{ }\mu\text{s} = 400\text{ bits}$. Therefore, a normal short message does not inadvertently activate the test mode.
4. One example of an input signal which may cause the test mode to activate is a clock signal with frequency 3 MHz and 50% duty cycle (symmetric HIGH and LOW half-cycles) with logic HIGH levels of 2.4 V and logic LOW levels of 0.4 V. This signal applied to the D pin as a driver input would meet the criteria listed above, and may cause the test-mode to activate, which would disable the driver. This example situation may occur if the clock signal is generated from a microcontroller or logic chip with a 2.7-V supply.

10.4.2 Equivalent Input and Output Schematic Diagrams

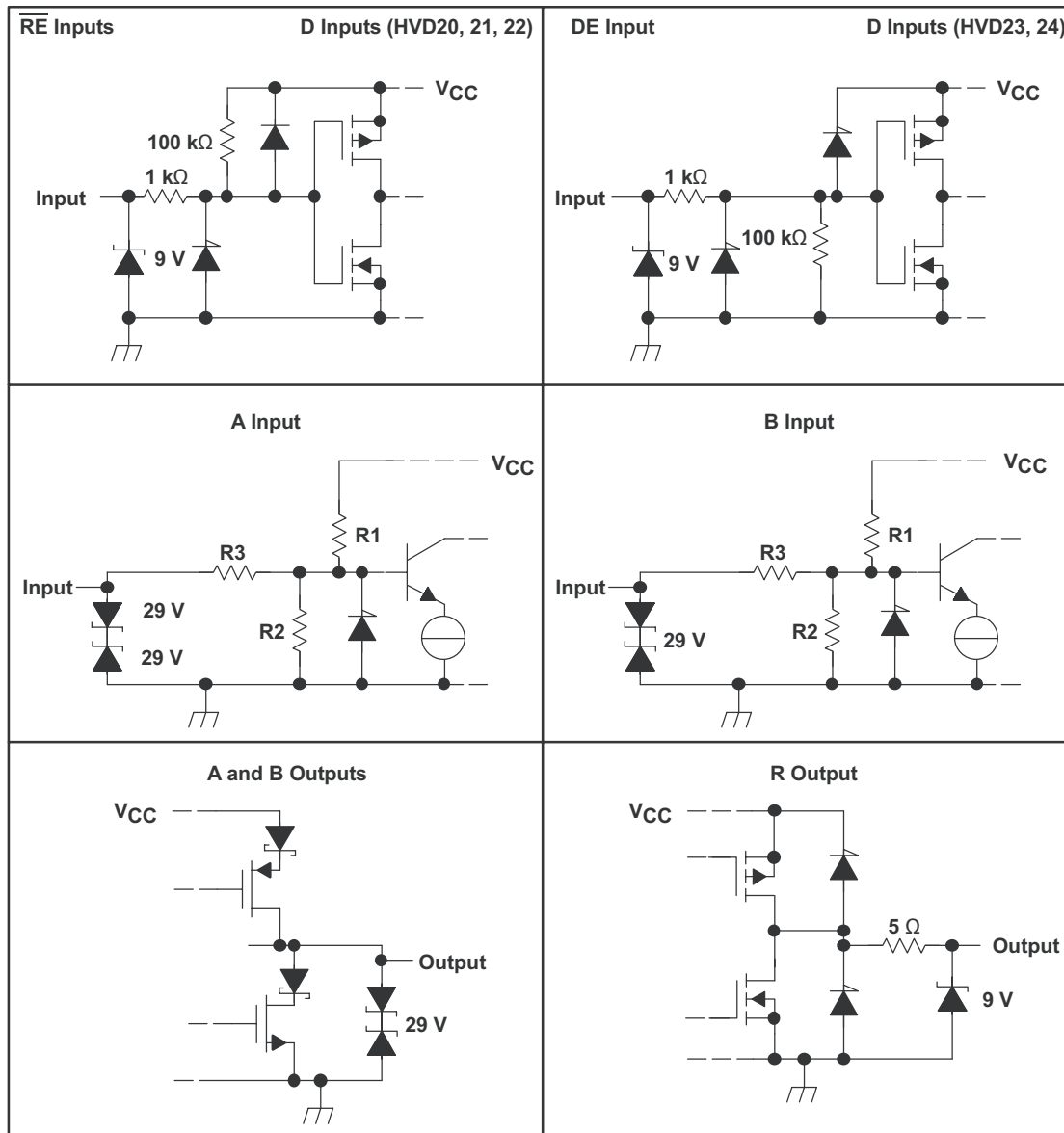


FIG 10-4. Equivalent Input and Output Schematic Diagrams

表 10-3. Input and Output Resistor Values

DEVICE	R1, R2	R3
SN65HVD2[0,3]	9 kΩ	45 kΩ
SN65HVD2[1,2,4]	36 kΩ	180 kΩ

11 Application and Implementation

注

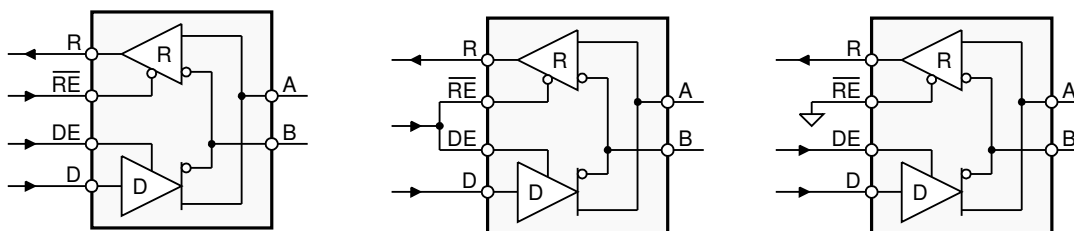
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

11.1 Application Information

The SN65HVD2x devices are half-duplex RS-485 transceivers that can be used for bidirectional, multipoint communication at various data rates over differential transmission lines. These devices support a wide common-mode range, allowing for robust communication even in the presence of voltage differences between the reference potentials of different nodes on a network.

11.2 Typical Application

図 11-1 shows a typical RS-485 application. Transceivers of different nodes are connected to one another over a shared bus. Twisted-pair cabling with a controlled differential impedance is used, and termination resistances are placed at the two ends of the cable to match the transmission line impedance and minimize signal reflections.



Copyright © 2016, Texas Instruments Incorporated

図 11-1. Half-Duplex Transceiver Configurations

11.2.1 Design Requirements

As the distances between nodes in an RS-485 network become greater and greater, it becomes more of a challenge to ensure reliable communication. The increased distance often means that the reference (ground) potentials has more of a difference between nodes. These ground potential differences give rise to differences in the common-mode voltages seen by the various transceivers on the bus. Standard RS-485 transceivers are typically specified to operate over a common-mode voltage from -7 V to 12 V , which may be insufficient for larger distances. The SN65HVD2x family of devices extends this range to -20 V to 25 V , allowing for greater communication distances between nodes.

Increased cable lengths can lead to increased jitter, especially in links operating at high data rates. This increased jitter is due to the attenuation of the cable, which tends to increase with frequency. Having unequal loss between higher and lower frequencies causes the RS-485 signal to distort, adding some timing deviation (jitter) to the edge crossings of the RS-485 data. If the jitter amplitude exceeds the jitter tolerance of the receiving MCU or UART, then bit errors are likely to result in the link. However, jitter can be reduced for a given link through the use of receiver equalization.

11.2.2 Detailed Design Procedure

11.2.2.1 Noise Considerations for Equalized Receivers

The simplest way of overcoming the effects of cable losses is to increase the sensitivity of the receiver. If the maximum attenuation of frequencies of interest is 20 dB , increasing the receiver gain by a factor of ten compensates for the cable. However, this means that signal and noise are amplified. Therefore, the receiver with higher gain is more sensitive to noise and it is important to minimize differential noise coupling to the equalized receiver.

Differential noise is created when conducted or radiated noise energy generates more voltage on one line of the differential pair than the other. For this to occur from conducted or electric far-field noise, the impedance to ground of the lines must differ.

For noise frequency out to 50 MHz, the input traces can be treated as a lumped capacitance if the receiver is approximately 10 inches or less from the connector. Therefore, matching impedance of the lines is accomplished by matching the lumped capacitance of each.

The primary factors that affect the capacitance of a trace are in length, thickness, width, dielectric material, distance from the signal return path, stray capacitance, and proximity to other conductors. It is difficult to match each of the variables for each line of the differential pair exactly, but a reasonable effort to do so keeps the lines balanced and less susceptible to differential noise coupling.

Another source of differential noise is from near-field coupling. In this situation, an assumption of equal noise-source impedance cannot be made as in the far-field. Familiarly known as crosstalk, more energy from a nearby signal is coupled to one line of the differential pair. Minimization of this differential noise is accomplished by keeping the signal pair close together and physical separation from high-voltage, high-current, or high-frequency signals.

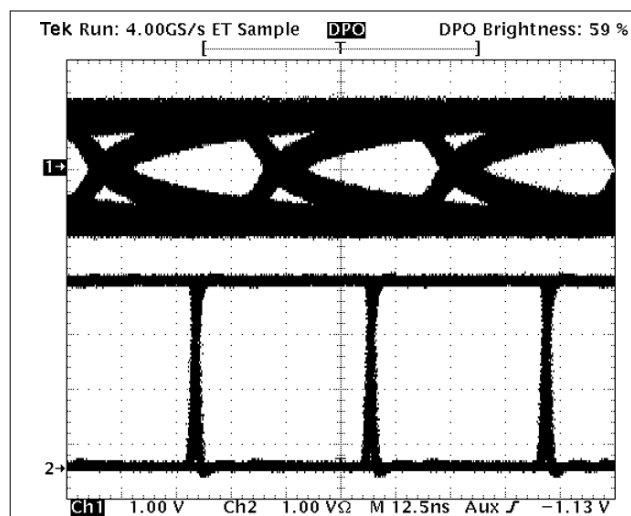
In summary, follow these guidelines in board layout for keeping differential noise to a minimum.

- Keep the differential input traces short.
- Match the length, physical dimensions, and routing of each line of the pair.
- Keep the lines close together.
- Match components connected to each line.
- Separate the inputs from high-voltage, high-frequency, or high-current signals.

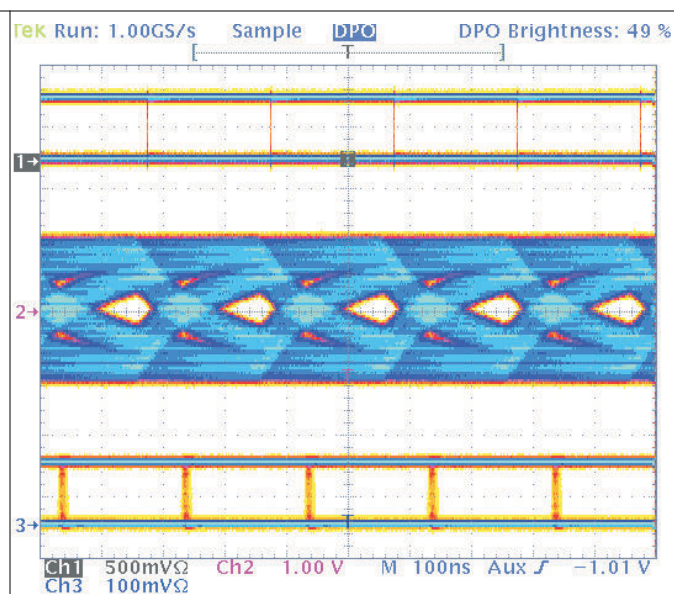
11.2.3 Application Curves

✕ 11-2 illustrates the benefits of integrated receiver equalization as implemented in the SN65HVD23 transceiver. In this test setup, a differential signal generator applied a signal voltage at one end of the cable, which was Belden 3105A twisted-pair shielded cable. The test signal was a pseudo-random bit stream (PRBS) of nonreturn-to-zero (NRZ) data. Channel 1 (top) shows the eye-pattern of the differential voltage at the receiver inputs (after the cable attenuation). Channel 2 (bottom) shows the output of the receiver.

✕ 11-3 illustrates the benefits of integrated receiver equalization as implemented in the SN65HVD24 transceiver. In this test setup, a differential signal generator applied a signal voltage at one end of the cable, which was Belden 3105A twisted-pair shielded cable. The test signal was a pseudo-random bit stream (PRBS) of nonreturn-to-zero (NRZ) data. Channel 1 (top) shows the eye-pattern of the bit stream. Channel 2 (middle) shows the eye-pattern of the differential voltage at the receiver inputs (after the cable attenuation). Channel 3 (bottom) shows the output of the receiver.



11-2. SN65HVD23 Receiver Performance at 25 Mbps Over 150 Meter Cable



11-3. SN65HVD24 Receiver Performance at 5 Mbps Over 500 Meter Cable

12 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100-nF ceramic capacitor placed as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

13 Layout

13.1 Layout Guidelines

In addition to the guidelines on differential trace matching given in [セクション 11.2.2](#), the layout guidelines below must be followed:

- Route power and ground nets as planes rather than traces, and keep their widths as large as possible to minimize resistance and inductance while maximizing parasitic capacitance.
- If external components (like transient voltage suppression diodes) are used for transient protection, place them close to the connector port and within the path of the signal lines. Make sure component capacitances are small enough not to impact the RS-485 signaling at the chosen data rate.
- Small-valued series pulse-proof resistances can be used to provide additional immunity to transients. This is needed to limit input currents if the clamping voltages of external transient protection devices exceed the absolute maximum ratings of the transceiver. These resistances must be less than $10\ \Omega$ so that the RS-485 signal is not overly attenuated.

13.2 Layout Example

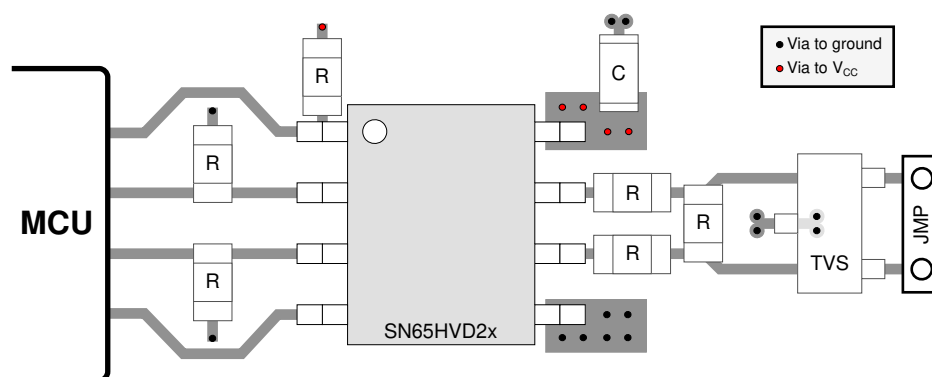


図 13-1. SN65HVD2x Layout Example

14 Device and Documentation Support

14.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

14.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

14.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD20DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP20
SN65HVD20DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP20
SN65HVD20DR1G4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP20
SN65HVD20DR1G4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP20
SN65HVD20P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD20
SN65HVD20P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD20
SN65HVD21D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	VP21
SN65HVD21DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP21
SN65HVD21DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP21
SN65HVD21DRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP21
SN65HVD21DRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP21
SN65HVD21P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD21
SN65HVD21P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD21
SN65HVD22D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	VP22
SN65HVD22DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP22
SN65HVD22DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP22
SN65HVD22DRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP22
SN65HVD22P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD22
SN65HVD22P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD22
SN65HVD23D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	VP23
SN65HVD23DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP23
SN65HVD23DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP23
SN65HVD23DRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP23
SN65HVD23DRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP23
SN65HVD23P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD23
SN65HVD23P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD23
SN65HVD24D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	VP24
SN65HVD24DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP24
SN65HVD24DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP24

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD20DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD20DR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD21DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD21DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD22DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD23DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD23DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD24DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD20DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD20DR1G4	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD21DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD21DRG4	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD22DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD23DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD23DRG4	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD24DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65HVD20P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD20P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD21P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD21P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD22P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD22P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD23P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD23P.A	P	PDIP	8	50	506	13.97	11230	4.32



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

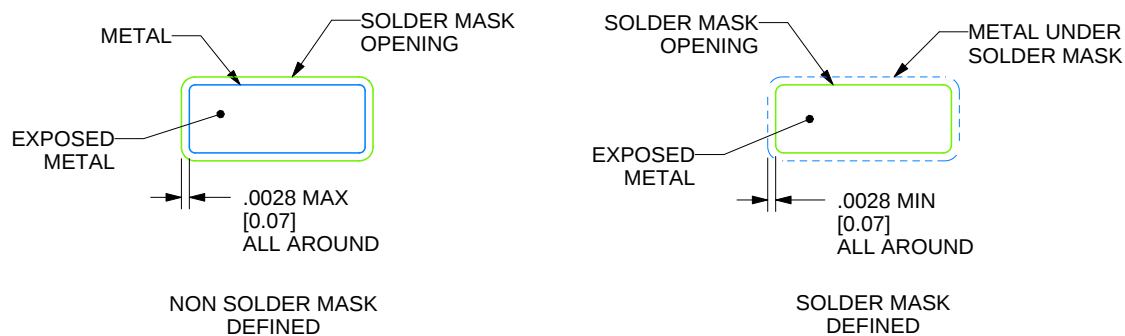
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated