TEXAS INSTRUMENTS
SN65HVD233-Q1, SN65HVD234-Q1, SN65HVD235-Q1
JAJSCG0A – SEPTEMBER 2016 – REVISED NOVEMBER 2016

SN65HVD23x-Q1 3.3V車載用CAN Busトランシーバ

1 特長

- ISO 11898-2と互換
- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード1: 動作時周囲温度範囲 –40°C～125°C
  - デバイスHBM ESD分類レベル
    - Busピン: ±12,000V
    - その他のピン: ±3,000V
  - デバイスCDM ESD分類レベル: ±1,000V
- 3.3V単一電源
- 最高1Mbpsのビット・レート
- 最高±36VのBusピン・フォルト保護
- -7V～12Vの同相範囲
- 高い入力インピーダンスにより120ノードが可能
- LVTTL I/Oは5V許容
- GIFT/ICTに準拠
- ドライバのスルーレートを調整して放射特性を改善可能
- 電力オフのノードはバスに不干渉
- 低電流のスタンバイ・モード: 200µA (標準値)
- 平均消費電力: 36.4mW
- SN65HVD233-Q1: ループバック・モード
- SN65HVD234-Q1: 超低電流スリープ・モード
  - 標準消費電流: 50nA
- SN65HVD235-Q1: オートボー・ループバック・モード
- サーマル・シャットダウン保護機能
- グリッチ・フリーのバス入力および出力による電源オンおよびオフ
  - 高い入力インピーダンスと低いV_{CC}
  - 電源サイクル中の単調出力

2 アプリケーション

- 車内ネットワーキング
- 先進運転支援システム(ADAS)
- 車体エレクトロニクスおよび照明
- インフォテインメントおよびクラスタ
- ハイブリッド車、電気自動車、パワートレイン・システム
- NMEA 2000やSAE J1939などのCAN Bus標準に準拠したアプリケーション

3 概要

SN65HVD233-Q1、SN65HVD234-Q1、SN65HVD235-Q1デバイスは、フォルト保護された3.3V CANトランシーバで、車載アプリケーション用に認定済みです。これらのトランシーバは3.3V電源で動作し、同様に3.3Vのマイクロコントローラを活用するシステムに理想的で、コントローラとCANトランシーバに電力を供給するための追加部品や独立した電源の必要性を減らすことができます。SN65HVD23x-Q1トランシーバはISO-11898-2標準と互換なため、5V CANや3.3V CANトランシーバを採用している混在ネットワークと相互運用が可能です。

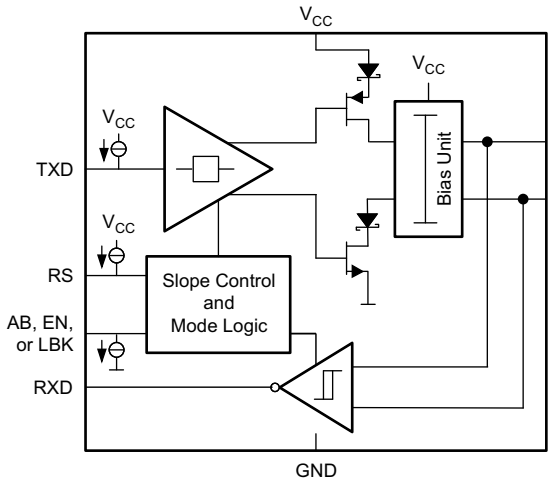
これらのデバイスは特に過酷な環境での動作を想定して設計されており、クロスワイヤ保護、CANHおよびCANLピン上で最高±36Vの過電圧保護、グランド消失保護、過熱(サーマル・シャットダウン)保護、および±100Vの同相過渡保護機能があります。これらのデバイスは、-7V～12Vの広い同相電圧範囲で動作します。これらのトランシーバは、マイクロプロセッサ上のホストCANコントローラと、輸送機関や車載のアプリケーションで使用されている差動CANバスとの間のインターフェイスです。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
SN65HVD233-Q1	SOIC (8)	4.90mm×3.91mm
SN65HVD234-Q1		
SN65HVD235-Q1		

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年9月発行のものから更新 **Page**

- Deleted extra words "all pins except" in the test condition for CANH, CANL pins to GND ... 5
- Added ESD performance information between CANH and CANL pins ... 5

5 概要(続き)

モード: SN65HVD233-Q1、SN65HVD234-Q1、SN65HVD235-Q1デバイスのRSピン(ピン8)には、高速、勾配制御、低消費電力スタンバイ・モードの3つの動作モードがあります。ピン8を直接グランドへ接続すると高速モードの動作が選択され、ドライバ出力トランジスタは立ち上がり/立ち下がり勾配の制限なしに、可能な限り高速にオン/オフのスイッチングを行います。立ち上がり/立ち下がり勾配は、RSピンとグランドとの間に抵抗を接続して調整できます。この勾配は、ピンの出力電流に比例します。抵抗値が10kΩの場合、ドライバのスルーレートは約15V/µsで、値が100kΩなら約2V/µsです。勾配制御の詳細については、*Feature Description*を参照してください。

SN65HVD233-Q1、SN65HVD234-Q1、SN65HVD235-Q1デバイスは、RSピンにHIGHレベルが印加されると、低電流のスタンバイ(リッスンのみ)モードへ移行し、このモードでは、ドライバのスイッチがオフになり、レシーバはアクティブのまま保持されます。ローカル・プロトコル・コントローラがバスへメッセージを送信する必要がある場合は、RSピンによりデバイスを高速モードまたは勾配制御モードに戻す必要があります。

ループバック(SN65HVD233-Q1): SN65HVD233-Q1デバイスのループバック(LBK)ピン(ピン5)がHIGHになると、バス出力とバス入力が高インピーダンス状態になります。内部的に、デバイスのTXD-to-RSパスはアクティブに維持され、ドライバからレシーバへのループバックに利用可能なため、バスに干渉することなく、自己診断ノード機能に使用できます。ループバック・モードの詳細については、*Feature Description*を参照してください。

超低電流スリープ(SN65HVD234-Q1): SN65HVD234-Q1デバイスは、ENピン(ピン5)にLOWレベルが印加されると、超低電流スリープ・モードになり、ドライバとレシーバの両方の回路が非アクティブになります。デバイスは、ピン5にHIGHレベルが印加されて回路が再度アクティブになるまで、このスリープ・モードに維持されます。

オートボー・ループバック(SN65HVD235-Q1): SN65HVD235-Q1デバイスのABピン(ピン5)にはバス・リッスンのみのループバック機能が実装されており、ローカル・ノード・コントローラのボーレートをCANバスのものと同期できます。オートボー・モードでは、ドライバのバス出力は高インピーダンス状態になり、レシーバのバス入力はアクティブ状態に維持されます。コントローラのボーレート検出やオートボー機能を補助するため、内部的にTXDピンからRSピンへのループバックがあります。オートボー・モードの詳細については、*Feature Description*を参照してください。

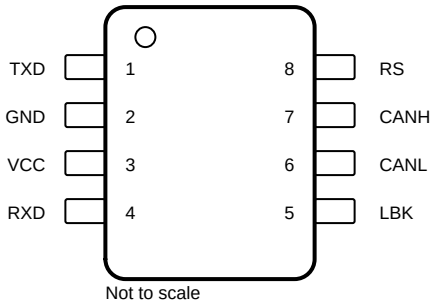
6 Device Comparison Table

PART NUMBER(1)	LOW-POWER MODE	SLOPE CONTROL	DIAGNOSTIC LOOPBACK	AUTOBAUD LOOPBACK
SN65HVD233-Q1	200-µA standby mode	Adjustable	Yes	No
SN65HVD234-Q1	200-µA standby mode or 50-nA sleep mode	Adjustable	No	No
SN65HVD235-Q1	200-µA standby mode	Adjustable	No	Yes

(1) For the most-current package and ordering information, see the orderable addendum at the end of the data sheet, or see the TI Web site at www.ti.com.

7 Pin Configuration and Functions

D Package
8-Pin SOIC
SN65HVD233-Q1 Top View



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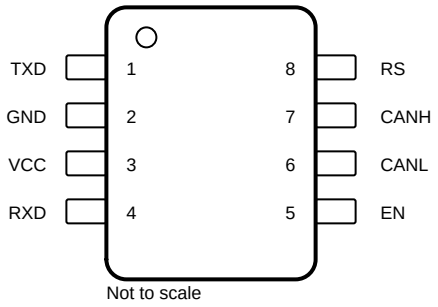
D Package
8-Pin SOIC
SN65HVD234-Q1 Top View



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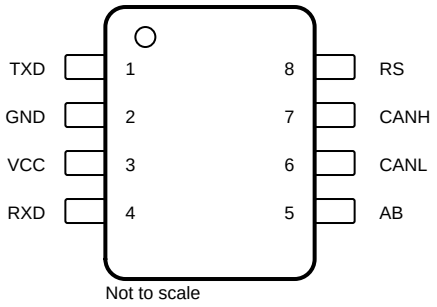
D Package
8-Pin SOIC
SN65HVD235-Q1 Top View



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Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	'233-Q1	'234-Q1	'235-Q1		
AB	—	—	5	I	SN65HVD235-Q1 device: Autobaud loopback mode-input pin (AB). Can be tied to ground if not used. Can also be left open if unused because the internal pulldown biases this toward ground.
CANH	7	7	7	I/O	High-level CAN bus line
CANL	6	6	6	I/O	Low-level CAN bus line
EN	—	5	—	I	SN65HVD234-Q1 device: Enable input pin. Logic high for enabling a normal mode (high-speed or slope-control mode). Logic low for sleep mode. (EN)
GND	2	2	2	—	Ground connection
LBK	5	—	—	I	SN65HVD233-Q1 device: Loopback-mode input pin (LBK). Can be tied to ground if not used. Can also be left open if unused because the internal pulldown biases this toward ground.
RS	8	8	8	I	Mode-select pin: strong pulldown to GND = high-speed mode, strong pullup to V_{CC} = low-power mode, 10-kΩ to 100-kΩ pulldown to GND = slope-control mode
RXD	4	4	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
TXD	1	1	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
V_{CC}	3	3	3	I	Transceiver 3.3-V supply voltage

8 Specifications

8.1 Absolute Maximum Ratings

over operating ambient temperature range unless otherwise noted(1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	7	V
	Voltage at any bus terminal (CANH or CANL)	–36	36	V
	Voltage input, transient pulse, CANH and CANL, through 100 Ω (see Figure 18)	–100	100	V
V_I	Input voltage, (AB, EN, LBK, RS, TXD)	–0.5	7	V
V_O	Output voltage (RXD)	–0.5	7	V
I_O	Receiver output current	–10	10	mA
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to the network ground pin.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	CANH, CANL to GND	±12 000	V
			Between CANH and CANL	±16 000	
			All pins	±3 000	
		Charged-device model (CDM), per AEC Q100-011		±1 000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
	Voltage at any bus terminal (separately or common mode)		–7	12	V
V_{IH}	High-level input voltage	EN, AB, LBK, TXD	2	5.5	V
V_{IL}	Low-level input voltage	EN, AB, LBK, TXD	0	0.8	V
V_{ID}	Differential input voltage between CANH and CANL		–6	6	V
	Resistance from RS to ground		0	100	kΩ
$V_{I(Rs)}$	Input voltage at RS for standby		0.75 V_{CC}	5.5	V
I_{OH}	High-level output current	Driver	–50		mA
		Receiver	–10		
I_{OL}	Low-level output current	Driver		50	mA
		Receiver		10	
T_A	Operating ambient temperature(1)		–40	125	°C

(1) Maximum ambient temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

8.4 Thermal Information

THERMAL METRIC[1]		SN65HVD23x-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics: Driver

over operating ambient temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$V_{O(D)}$	Bus output voltage (dominant)	CANH	TXD at 0 V, RS at 0 V, see Figure 12 and Figure 13	2.45		V_{CC}	V
		CANL		0.5		1.25	
V_O	Bus output voltage (recessive)	CANH	TXD at 3 V, RS at 0 V, see Figure 12 and Figure 13		2.3		V
		CANL			2.3		
$V_{OD(D)}$	Differential output voltage (dominant)		TXD at 0 V, RS at 0 V, see Figure 12 and Figure 13	1.5	2	3	V
			TXD at 0 V, RS at 0 V, see Figure 13 and Figure 14	1.2	2	3	
V_{OD}	Differential output voltage (recessive)		TXD at 3 V, RS at 0 V, see Figure 12 and Figure 13	–120		12	mV
			TXD at 3 V, RS at 0 V, no load	–0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 21		1		V
I_{IH}	High-level input current	AB, EN, LBK, TXD	TXD = 2 V or EN = 2 V or LBK = 2 V or AB = 2 V	–30		30	µA
I_{IL}	Low-level input current	AB, EN, LBK, TXD	TXD = 0.8 V or EN = 0.8 V or LBK = 0.8 V or AB = 0.8 V	–30		30	µA
I_{OS}	Short-circuit output current		V_{CANH} = –7 V, CANL open, see Figure 26	–250			mA
			V_{CANH} = 12 V, CANL open, see Figure 26			1	
			V_{CANL} = –7 V, CANH open, see Figure 26	–1			
			V_{CANL} = 12 V, CANH open, see Figure 26			250	
C_O	Output capacitance		See C_I, Input capacitance in Electrical Characteristics: Receiver				
$I_{IRs(s)}$	RS input current for standby		RS at 0.75 V_{CC}	–10			µA
I_{CC}	Supply current	Sleep	EN at 0 V, TXD at V_{CC}, RS at 0 V or V_{CC}		0.05	2	µA
		Standby	RS at V_{CC}, TXD at V_{CC}, AB at 0 V, LBK at 0 V, EN at V_{CC}		200	600	
		Dominant	TXD at 0 V, no load, AB at 0 V, LBK at 0 V, RS at 0 V, EN at V_{CC}			6	mA
		Recessive	TXD at V_{CC}, no load, AB at 0 V, LBK at 0 V, RS at 0 V, EN at V_{CC}			6	
$P_{(AVG)}$	Average power dissipation		R_L = 60 Ω, R_S at 0 V, input to D a 1-MHz 50% duty cycle square wave V_{CC} at 3.3 V, T_A = 25°C		36.4		mW

(1) All typical values are at 25°C and with a 3.3-V supply.

8.6 Electrical Characteristics: Receiver

over operating ambient temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		AB at 0 V, LBK at 0 V, EN at V_{CC}, see Table 1			750	900	mV
V_{IT-}	Negative-going input threshold voltage				500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					100		mV
V_{OH}	High-level output voltage		I_O = –4 mA, See Figure 17		0.8 × V_{CC}			V
V_{OL}	Low-level output voltage		I_O = 4 mA, See Figure 17				0.4	V
I_I	Bus input current		CANH or CANL at 12 V	Other bus pin at 0 V, TXD at 3 V, AB at 0 V, LBK at 0 V, RS at 0 V, EN at V_{CC}	150		500	µA
			CANH or CANL at 12 V, V_{CC} at 0 V		200		600	
			CANH or CANL at –7 V		–610		–150	
			CANH or CANL at –7 V, V_{CC} at 0 V		–450		–130	
C_I	Input capacitance (CANH or CANL)		Pin-to-ground, V_I = 0.4 sin (4E6πt) + 0.5 V, TXD at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}			40		pF
C_{ID}	Differential input capacitance		Pin-to-pin, V_I = 0.4 sin (4E6πt) + 0.5 V, TXD at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}			20		pF
R_{ID}	Differential input resistance		TXD at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}		40		100	kΩ
R_{IN}	Input resistance (CANH or CANL) to ground				20		50	kΩ
I_{CC}	Supply current	Sleep	EN at 0 V, TXD at V_{CC}, RS at 0 V or V_{CC}			0.05	2	µA
		Standby	RS at V_{CC}, TXD at V_{CC}, AB at 0 V, LBK at 0 V, EN at V_{CC}			200	600	
		Dominant	TXD at 0 V, no load, RS at 0 V, LBK at 0 V, AB at 0 V, EN at V_{CC}				6	mA
		Recessive	TXD at V_{CC}, no load, RS at 0 V, LBK at 0 V, AB at 0 V, EN at V_{CC}				6	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.7 Switching Characteristics: Driver

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	RS at 0 V, see Figure 15		35	85	ns
		RS with 10 kΩ to ground, see Figure 15		70	125	
		RS with 100 kΩ to ground, see Figure 15		500	870	
t_{PHL}	Propagation delay time, high-to-low-level output	RS at 0 V, see Figure 15		70	120	ns
		RS with 10 kΩ to ground, see Figure 15		130	180	
		RS with 100 kΩ to ground, see Figure 15		870	1200	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	RS at 0 V, see Figure 15		35		ns
		RS with 10 kΩ to ground, see Figure 15		60		
		RS with 100 kΩ to ground, see Figure 15		370		
t_r	Differential output signal rise time	RS at 0 V, see Figure 15	20		70	ns
		RS with 10 kΩ to ground, see Figure 15	30		135	
		RS with 100 kΩ to ground, see Figure 15	350		1400	
t_f	Differential output signal fall time	RS at 0 V, see Figure 15	20		70	ns
		RS with 10 kΩ to ground, see Figure 15	30		135	
		RS with 100 kΩ to ground, see Figure 15	350		1400	
$t_{en(s)}$	Enable time from standby to dominant	See Figure 19 and Figure 20		0.6	1.5	µs
$t_{en(z)}$	Enable time from sleep to dominant			1	5	µs

(1) All typical values are at 25°C and with a 3.3-V supply.

8.8 Switching Characteristics: Receiver

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, CANH input low to RXD output high	See Figure 17		35	60	ns
t_{PHL}	Propagation delay time, CANH input high to RXD output low			35	60	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			7		ns
t_r	Output signal rise time			2	5	ns
t_f	Output signal fall time			2	5	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

8.9 Switching Characteristics: Device

over operating ambient temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	'HVD233-Q1	See Figure 23		7.5	12	ns
$t_{(AB1)}$	Loopback delay, driver input to receiver output	'HVD235-Q1	See Figure 24		10	20	ns
$t_{(AB2)}$	Loopback delay, bus input to receiver output	'HVD235-Q1	See Figure 25		35	60	ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant		RS at 0 V, see Figure 22		70	135	ns
			RS with 10 kΩ to ground, see Figure 22		105	190	
			RS with 100 kΩ to ground, see Figure 22		535	1000	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive		RS at 0 V, see Figure 22		70	135	ns
			RS with 10 kΩ to ground, see Figure 22		105	190	
			RS with 100 kΩ to ground, see Figure 22		535	1000	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.10 Typical Characteristics

RS = LBK = AB = 0 V; EN = V_{CC}

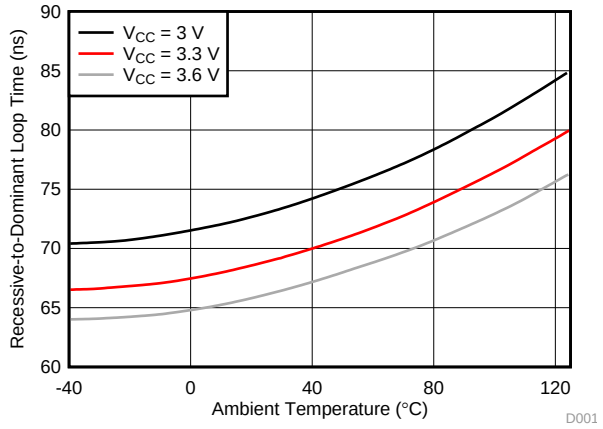


Figure 1. Recessive-to-Dominant Loop Time vs Ambient Temperature

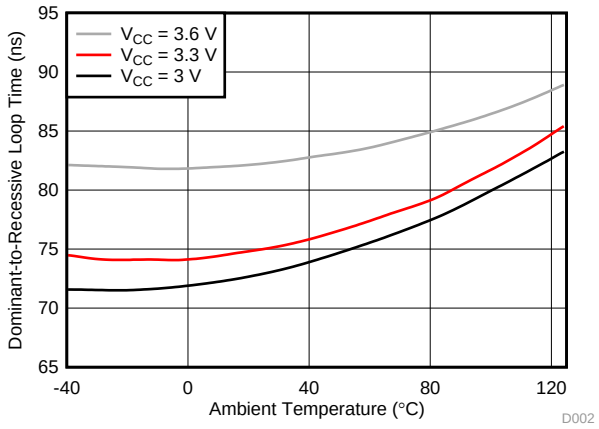


Figure 2. Dominant-to-Recessive Loop Time vs Ambient Temperature

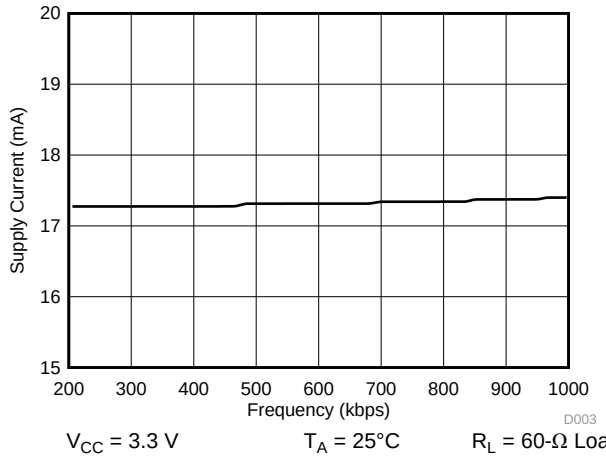


Figure 3. Supply Current vs Frequency

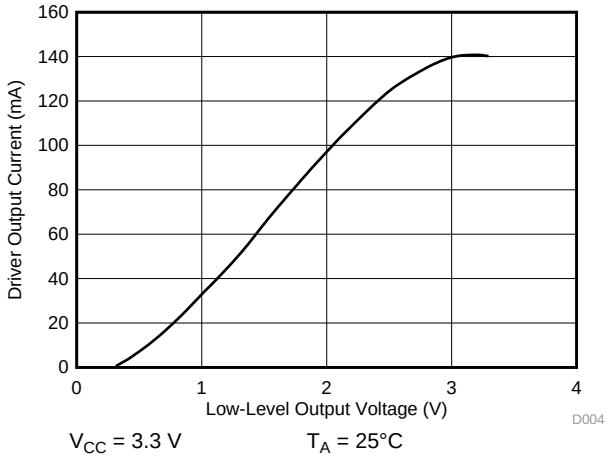


Figure 4. Driver Low-Level Output Current vs Low-Level Output Voltage

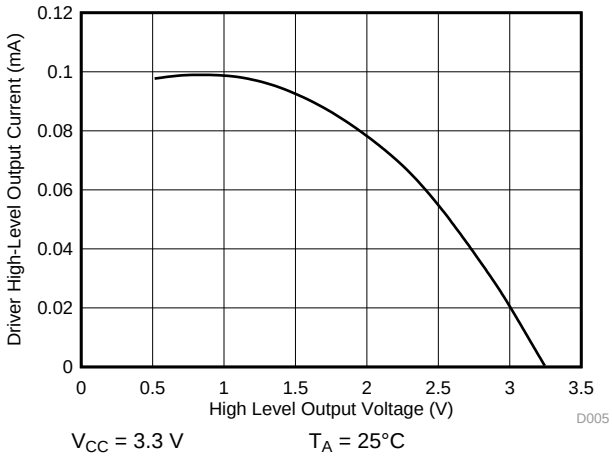


Figure 5. Driver High-Level Output Current vs High-Level Output Voltage

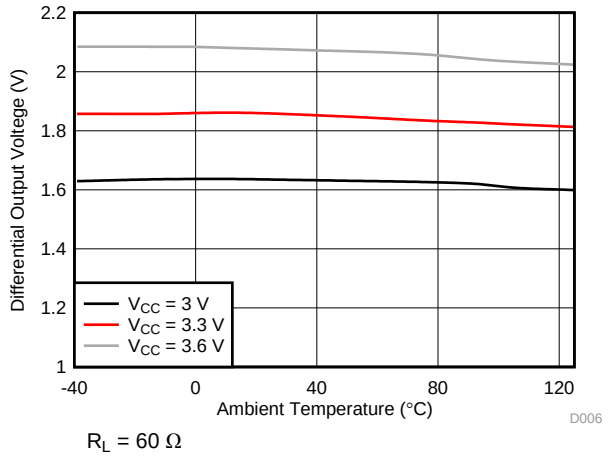
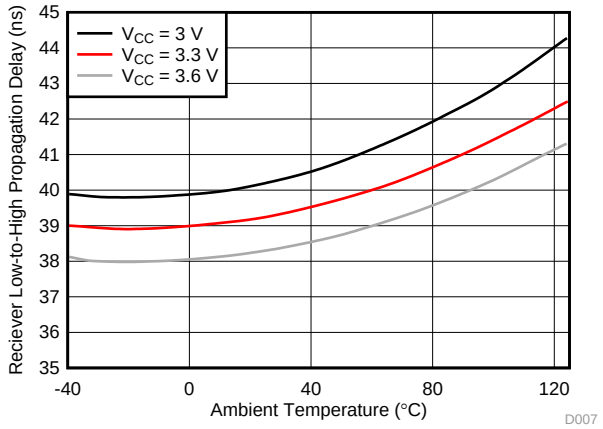


Figure 6. Differential Output Voltage vs Ambient Temperature

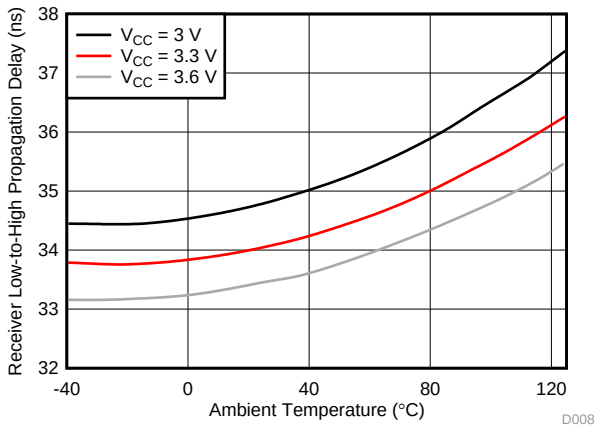
Typical Characteristics (continued)

RS = LBK = AB = 0 V; EN = V_{CC}



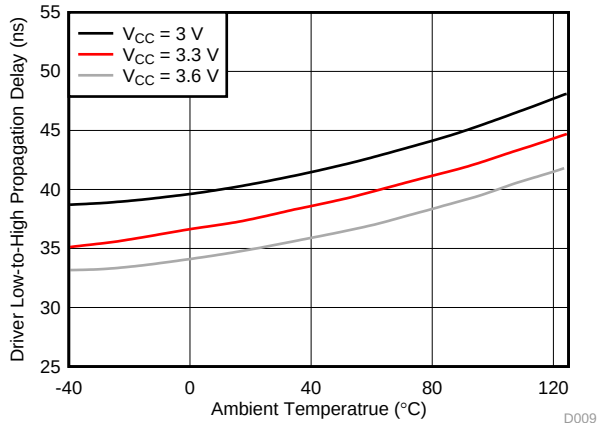
See Figure 3

Figure 7. Receiver Low-to-High Propagation Delay vs Ambient Temperature



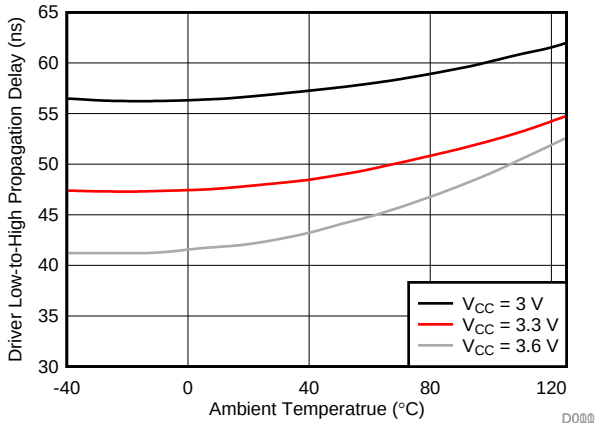
See Figure 3

Figure 8. Receiver High-to-Low Propagation Delay vs Ambient Temperature



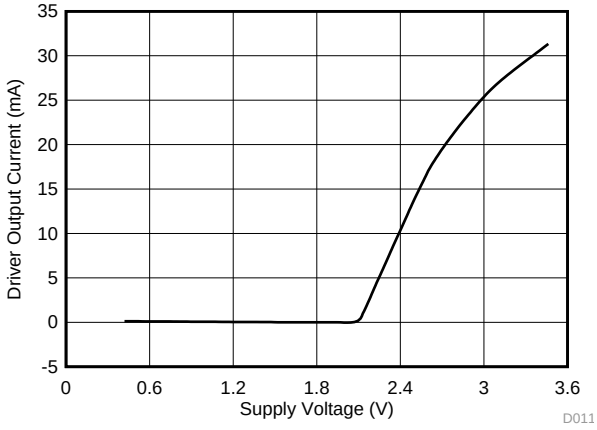
See Figure 1

Figure 9. Driver Low-to-High Propagation Delay vs Ambient Temperature



See Figure 1

Figure 10. Driver High-to-Low Propagation Delay vs Ambient Temperature



T_A = 25°C R_L = 60 Ω

Figure 11. Driver Output Current vs Supply Voltage

9 Parameter Measurement Information

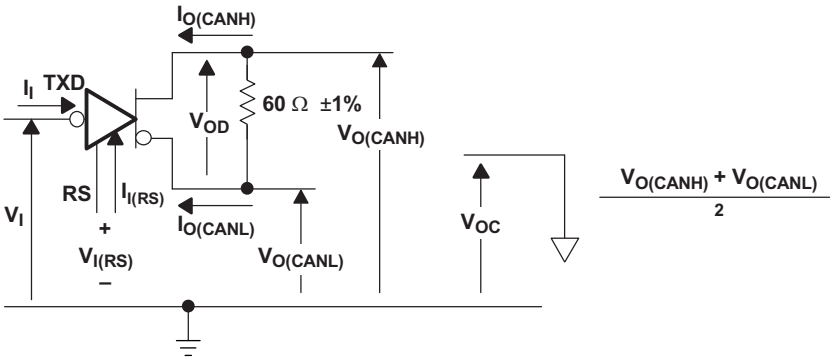


Figure 12. Driver Voltage, Current, and Test Definition

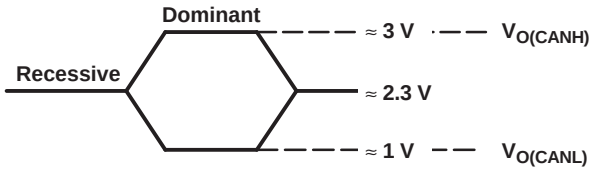


Figure 13. Bus Logic State Voltage Definitions

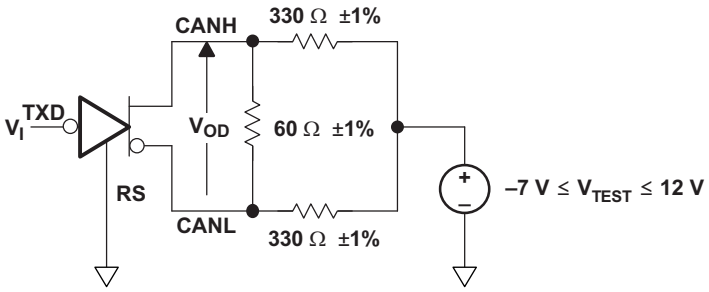
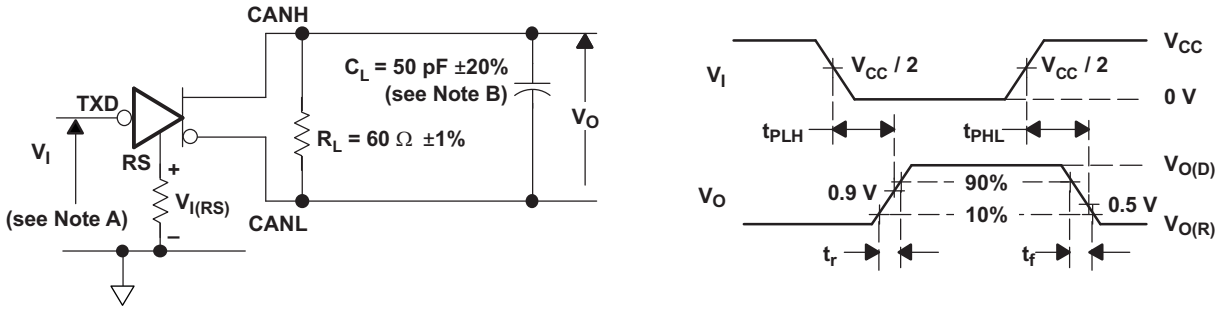


Figure 14. Driver V_{OD}



A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes fixture and instrumentation capacitance.

Figure 15. Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

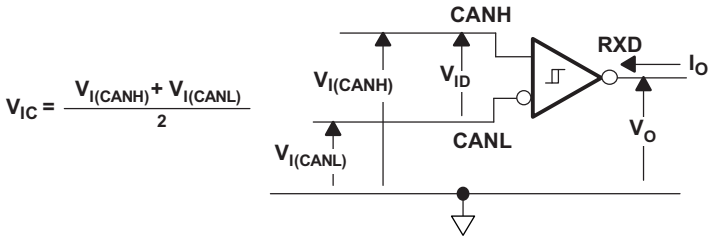
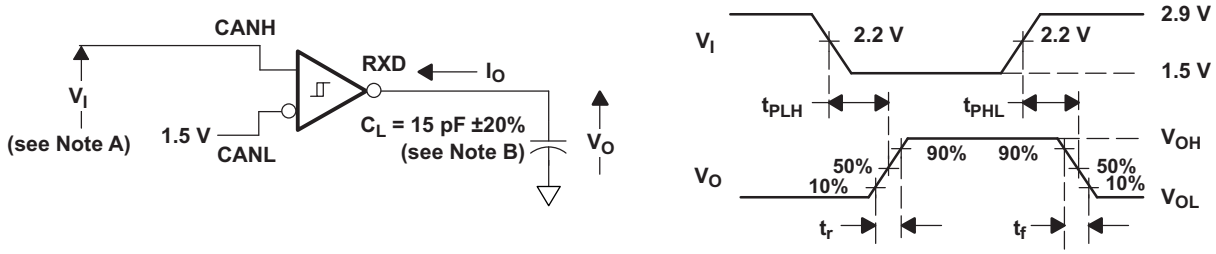


Figure 16. Receiver Voltage and Current Definitions



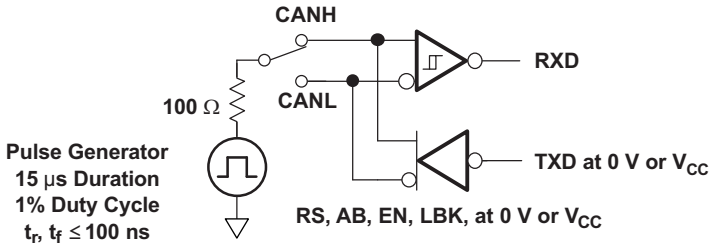
A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes fixture and instrumentation capacitance.

Figure 17. Receiver Test Circuit and Voltage Waveforms

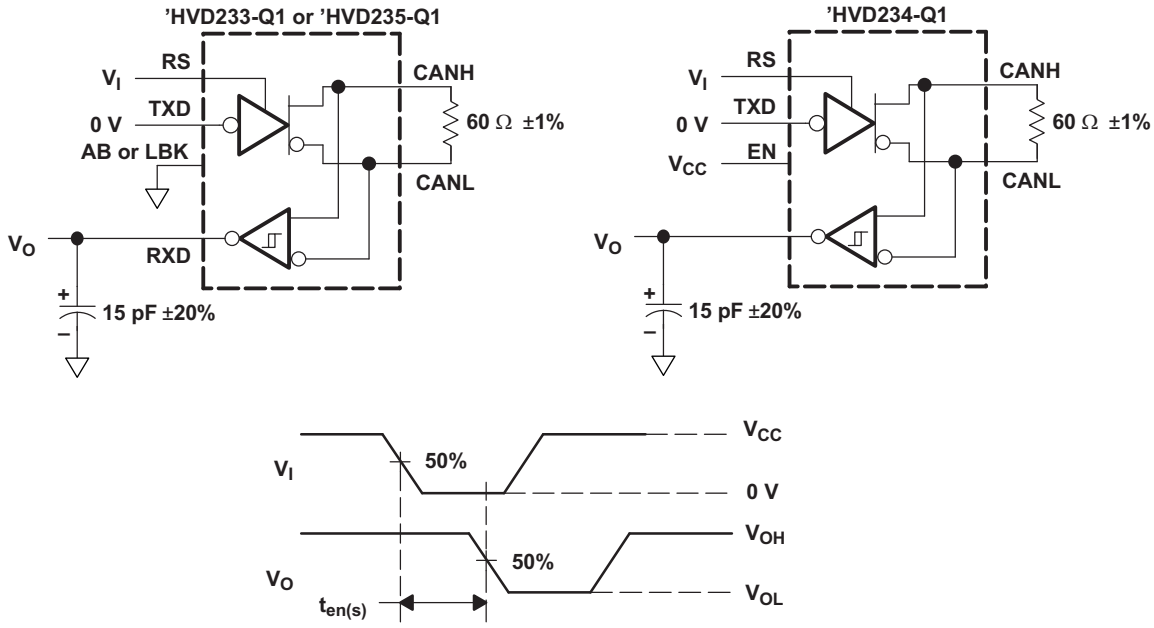
Table 1. Differential Input Voltage Threshold Test

INPUT		OUTPUT		MEASURED
V_{CANH}	V_{CANL}	RXD		$\lvert V_{ID}\rvert$
–6.1 V	–7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
–1 V	–7 V	L		6 V
12 V	6 V	L		6 V
–6.5 V	–7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
–7 V	–1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X



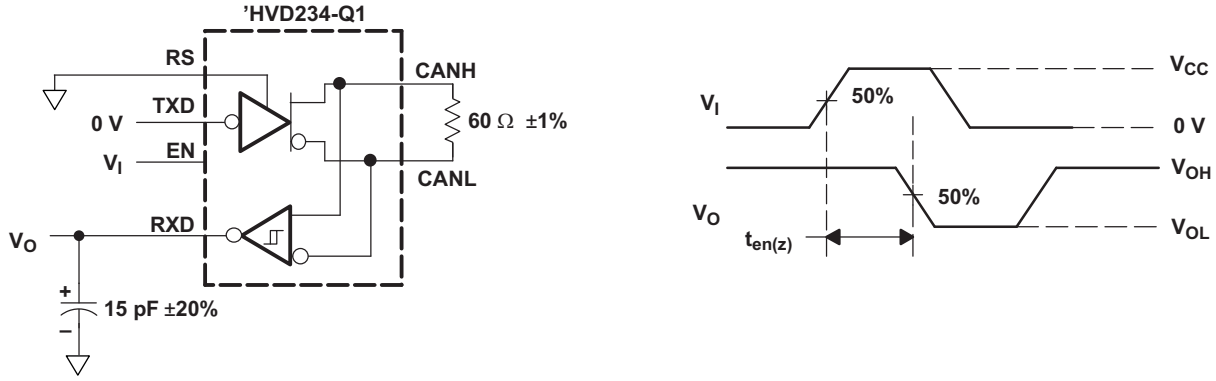
NOTE: This test is conducted to test survivability only. Data stability at the RXD output is not specified.

Figure 18. Test Circuit, Transient Overvoltage Test



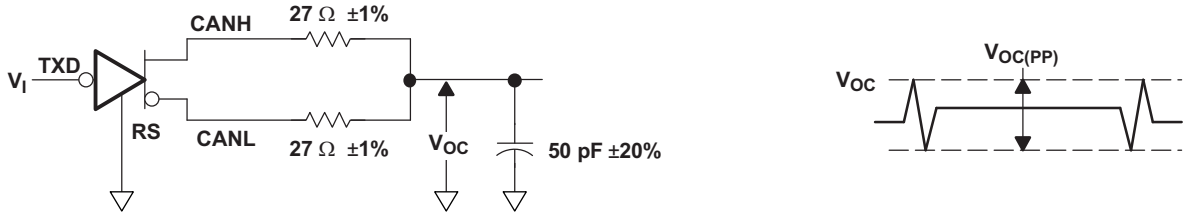
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 19. $t_{en(s)}$ Test Circuit and Voltage Waveforms



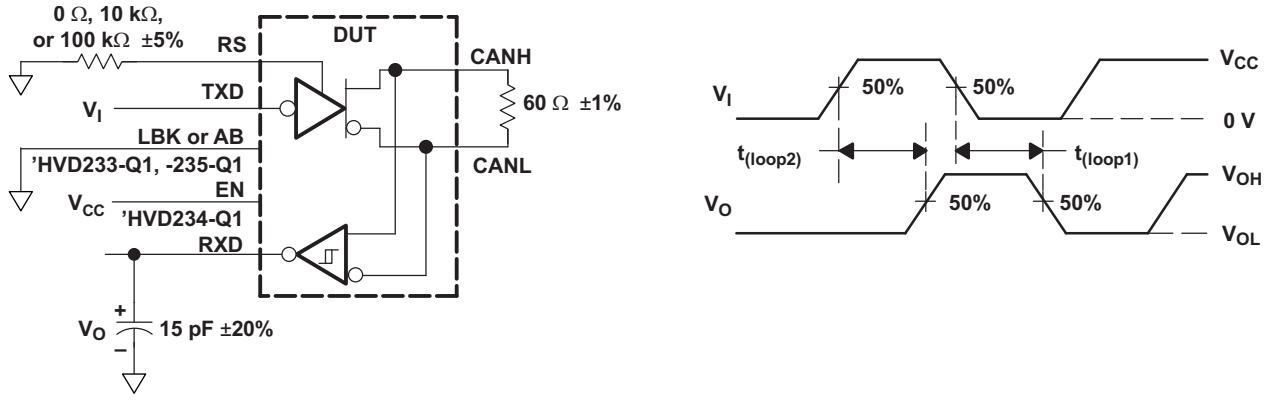
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 50 kHz, 50% duty cycle.

Figure 20. $t_{en(z)}$ Test Circuit and Voltage Waveforms



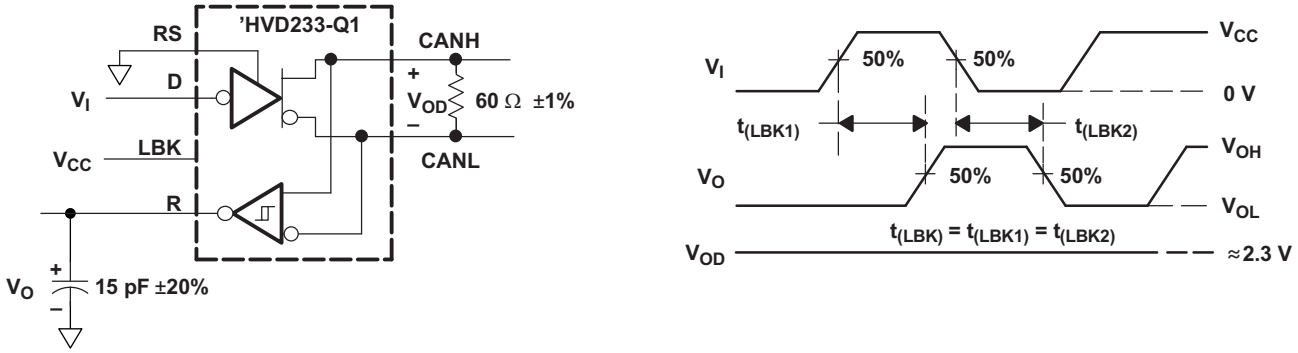
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 21. $V_{OC(pp)}$ Test Circuit and Voltage Waveforms



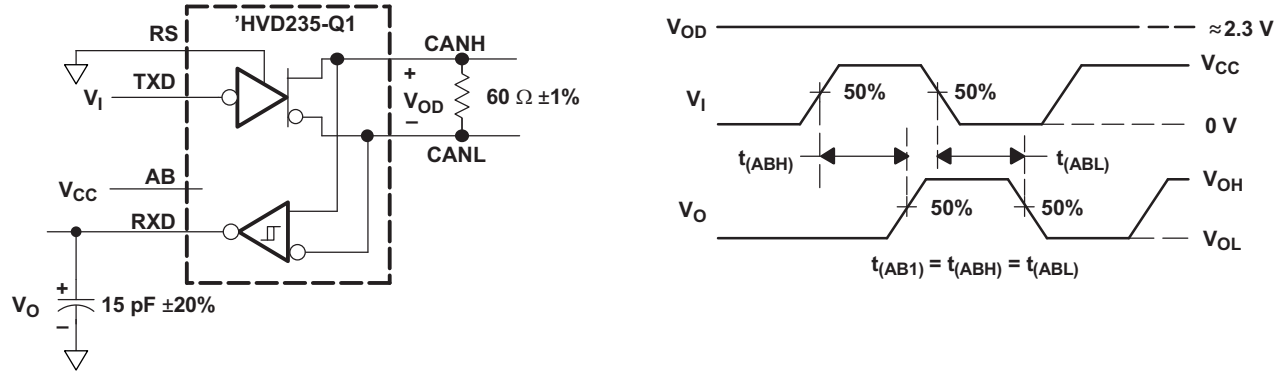
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 22. $t_{(loop)}$ Test Circuit and Voltage Waveforms



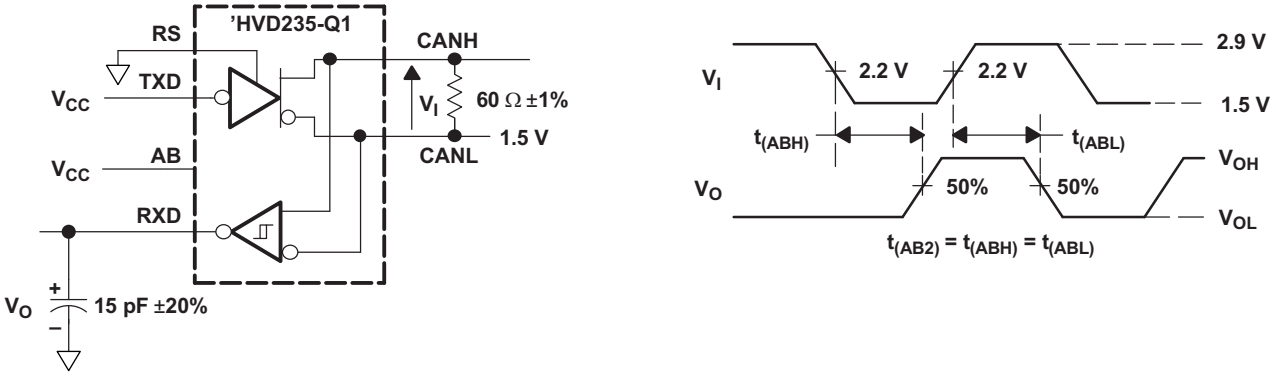
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 23. $t_{(LBK)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 24. $t_{(AB1)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 25. $t_{(AB2)}$ Test Circuit and Voltage Waveforms

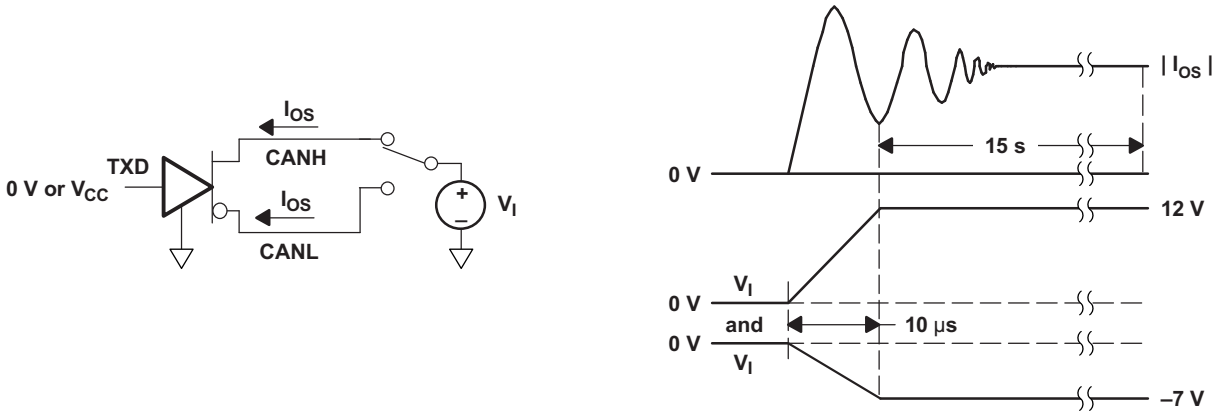
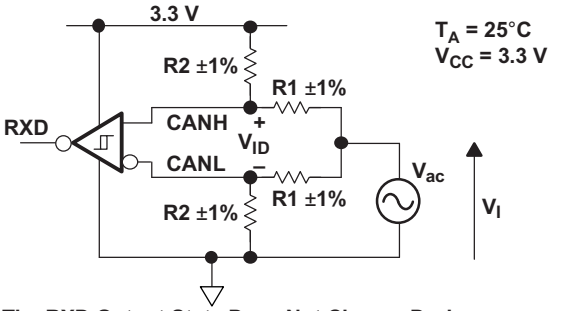


Figure 26. I_{OS} Test Circuit and Waveforms



The RXD Output State Does Not Change During Application of the Input Waveform.

V_{ID}	R1	R2
500 mV	50 Ω	280 Ω
900 mV	50 Ω	130 Ω

NOTE: All input pulses are supplied by a generator with f ≤ 1.5 MHz.

Figure 27. Common-Mode Voltage Rejection

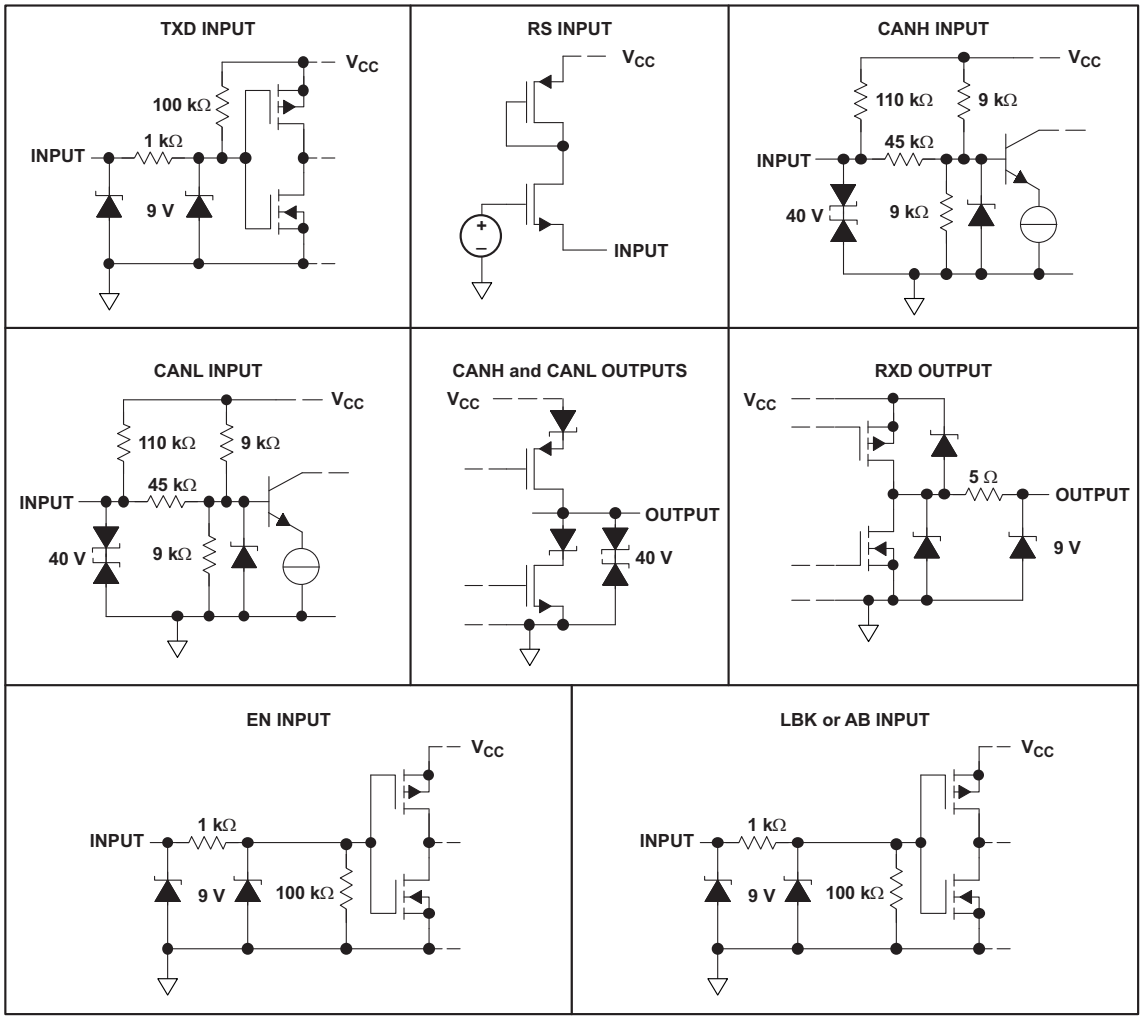


Figure 28. Equivalent Input and Output Schematic Diagrams

10 Detailed Description

10.1 Overview

This family of CAN transceivers is compatible with the ISO 11898-2 high-speed controller-area-network (CAN) physical layer standard. These devices are designed to interface between the differential bus lines in CAN and the CAN protocol controller at data rates up to 1 Mpbs.

10.2 Functional Block Diagrams

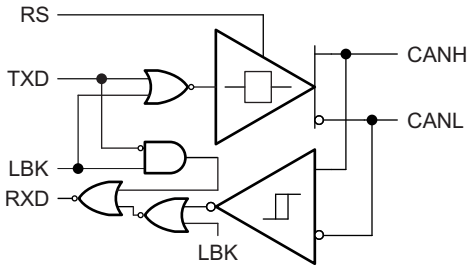


Figure 29. SN65HVD233-Q1 Functional Block Diagram

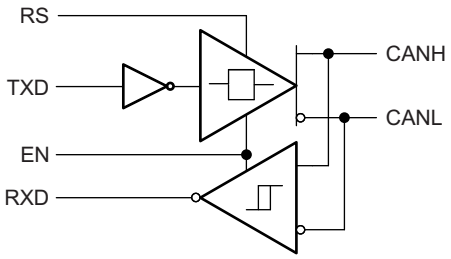


Figure 30. SN65HVD234-Q1 Functional Block Diagram

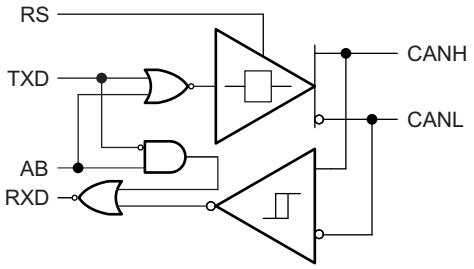


Figure 31. SN65HVD235-Q1 Functional Block Diagram

10.3 Feature Description

10.3.1 Diagnostic Loopback (SN65HVD233-Q1)

The diagnostic loopback or internal loopback function of the SN65HVD233-Q1 device is enabled with a high-level input on pin 5, LBK. This mode disables the driver output while keeping the bus pins biased to the recessive state. This mode also redirects the TXD data input (transmit data) through logic to the received data output pin, thus creating an internal loopback of the transmit-to-receive data path. This mimics the loopback that occurs normally with a CAN transceiver, because the receiver loops back the driven output to the RXD (receive data) pin. This mode allows the host protocol controller to input and read back a bit sequence or CAN messages to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in Figure 37.

Feature Description (continued)

If the LBK pin is not used, it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

10.3.2 Autobaud Loopback (SN65HVD235-Q1)

The autobaud loopback mode of the SN65HVD235-Q1 device is enabled by placing a high-level input on pin 5, AB. In autobaud mode, the driver output is disabled, thus blocking the TXD pin-to-bus path and the bus transmit function of the transceiver. The bus pins remain biased to recessive. The receiver-to-RXD pin path of the device remains operational, allowing bus activity to be monitored. In addition, the autobaud mode includes an internal logic loopback path from the TXD pin to the RXD pin so the local node can transmit to itself in sync with bus traffic while not disturbing messages on the bus. Thus if the CAN controller of the local node generates an error frame, it is not transmitted to the bus, but is detected only by the local CAN controller. This is especially helpful to determine if the local node is set to the same baud rate as the network, and if not, to adjust it to the network baud rate (autobaud detection).

Autobaud detection is best suited to applications that have a known selection of baud rates. For example, if an application has optional settings of 125 kbps, 250 kbps, or 500 kbps. Once the SN65HVD235-Q1 device is placed into autobaud loopback mode, the application software could assume the first baud rate of 125 kbps. It then waits for a message to be transmitted by another node on the bus. If the wrong baud rate has been selected, an error message is generated by the local CAN controller because the sample times will not be at the correct time. However, because the bus-transmit function of the device has been disabled, no other nodes receive the error frame generated by the local CAN controller of this node.

The application would then make use of the status register indications of the local CAN controller for message-received and error-warning status to determine if the set baud rate is correct or not. The warning status indicates that the CAN controller error counters have been incremented. A message received status indicates that a good message has been received. If an error is generated, the application then sets the CAN controller to the next possibly valid baud rate, and waits to receive another message. This pattern is repeated until an error-free message has been received, thus the correct baud rate has been selected. At this point, the application places the SN65HVD235-Q1 device in a normal transmitting mode by setting pin 5 to a low level, thus enabling bus-transmit and bus-receive functions to normal operating states for the transceiver.

If the AB pin is not used, it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

10.3.3 Slope Control

The rise and fall slope of the SN65HVD233-Q1, SN65HVD234-Q1, and SN65HVD235-Q1 driver output can be adjusted by connecting a resistor from RS (pin 8) to ground (GND) as shown in Figure 32, or to a low level input voltage as shown in Figure 33.

The slope of the driver output signal is proportional to the output current of the pin. This slope control is implemented with an external resistor value of 10 kΩ to achieve an approximately 15-V/µs slew rate, and up to 100 kΩ to achieve an approximately 2-V/µs slew rate. A typical slew-rate versus pulldown-resistance graph is shown in Figure 34. Typical driver output waveforms with slope control are displayed in Figure 40.

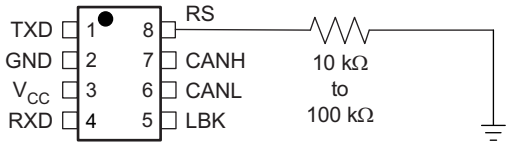


Figure 32. Ground Connection for Selecting Slope-Control or Standby Mode

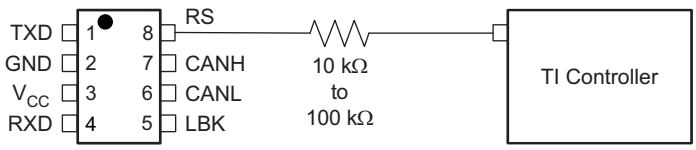


Figure 33. DSP Connection for Selecting Slope-Control or Standby Mode

Feature Description (continued)

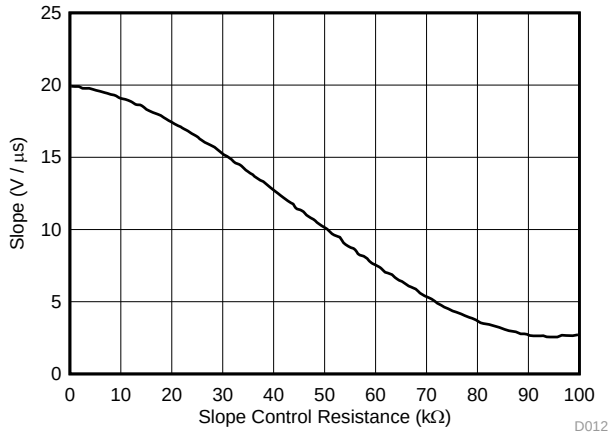


Figure 34. SN65HVD233-Q1 Driver Output-Signal Slope vs Slope-Control Resistance Value

10.3.4 Standby

If a high-level input (> 0.75 V_{CC}) is applied to RS (pin 8), the circuit enters a low-current, *listen only* standby mode during which the driver is switched off and the receiver remains active. If using this mode to save system power while waiting for bus traffic, the local controller can monitor the RXD output pin for a falling edge which indicates that a dominant signal was driven onto the CAN bus. The local controller can then drive the RS pin low to return to slope-control mode or high-speed mode.

10.3.5 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold, the device turns off the CAN driver circuits, thus blocking the TXD pin-to-bus transmission path. The shutdown condition is cleared when the junction temperature drops sufficiently below the thermal shutdown temperature of the device. The CAN bus pins are high-impedance and biased to the recessive level during a thermal shutdown, and the receiver-to-RXD pin path remains operational.

10.4 Device Functional Modes

Table 2. Driver (SN65HVD233-Q1 or SN65HVD235-Q1)

INPUTS			OUTPUTS		
TXD	LBK or AB	RS	CANH	CANL	BUS STATE
X	X	> 0.75 V_{CC}	Z	Z	Recessive
L	L or open	≤ 0.33 V_{CC}	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	≤ 0.33 V_{CC}	Z	Z	Recessive

Table 3. Driver (SN65HVD234-Q1)

INPUTS			OUTPUTS		
TXD	EN	RS	CANH	CANL	BUS STATE
L	H	≤ 0.33 V_{CC}	H	L	Dominant
H	X	≤ 0.33 V_{CC}	Z	Z	Recessive
Open	X	X	Z	Z	Recessive
X	X	> 0.75 V_{CC}	Z	Z	Recessive
X	L or open	X	Z	Z	Recessive

Table 4. Receiver (SN65HVD233-Q1)(1)

INPUTS				OUTPUT
BUS STATE	**$V_{ID} = V_{(CANH)} - V_{(CANL)}$**	**LBK**	**TXD**	**RXD**
Dominant	$V_{ID} \geq 0.9$ V	L or open	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	L or open	H or open	H
?	0.5 V < V_{ID} < 0.9 V	L or open	H or open	?
X	X	H	L	L
X	X	H	H	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

Table 5. Receiver (SN65HVD235-Q1)(1)

INPUTS				OUTPUT
BUS STATE	**$V_{ID} = V_{(CANH)} - V_{(CANL)}$**	**AB**	**TXD**	**RXD**
Dominant	$V_{ID} \geq 0.9$ V	L or open	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	L or open	H or open	H
?	0.5 V < V_{ID} <0.9 V	L or open	H or open	?
Dominant	$V_{ID} \geq 0.9$ V	H	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	H	H	H
Recessive	$V_{ID} \leq 0.5$ V or open	H	L	L
?	0.5 V < V_{ID} <0.9 V	H	L	L

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

Table 6. Receiver (SN65HVD234-Q1)(1)

INPUTS			OUTPUT
BUS STATE	**$V_{ID} = V_{(CANH)} - V_{(CANL)}$**	**EN**	**RXD**
Dominant	$V_{ID} \geq 0.9$ V	H	L
Recessive	$V_{ID} \leq 0.5$ V or open	H	H
?	0.5 V < V_{ID} < 0.9 V	H	?
X	X	L or open	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The CAN bus has two states during powered operation of the device, *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD pins. A recessive bus state is when the bus is biased to V_{CC} / 2 via the high-resistance internal resistors R_{IN} and R_{ID} of the receiver, corresponding to a logic high on the TXD and RXD pins. See *Figure 35* and *Figure 36*.

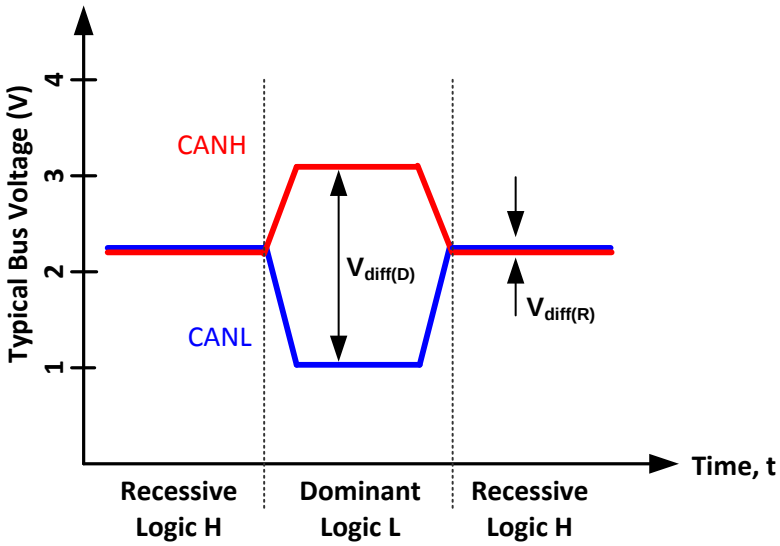


Figure 35. Bus States (Physical Bit Representation)

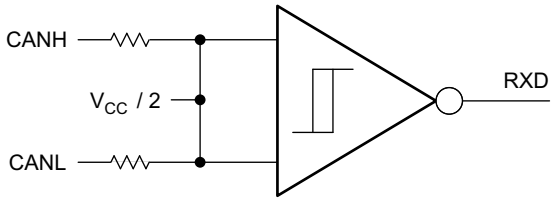


Figure 36. Simplified Recessive Common-Mode Bias and Receiver

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. The different nodes on the network are typically connected through the use of a 120-Ω characteristic impedance twisted-pair cable with termination on both ends of the bus.

11.2 Typical Application

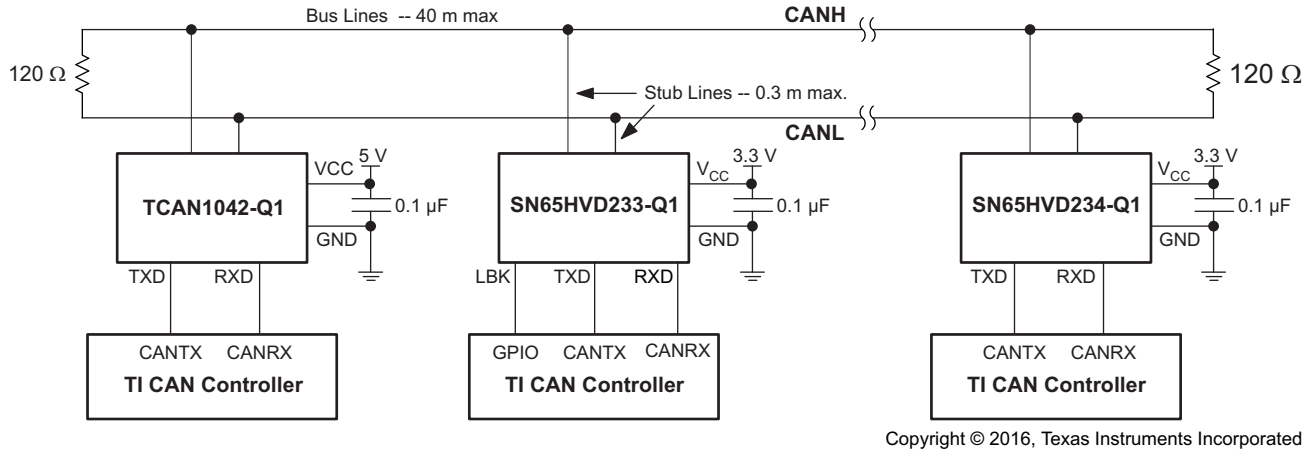


Figure 37. Typical SN65HVD233-Q1 Application

11.2.1 Design Requirements

11.2.1.1 Bus Loading, Length and Number of Nodes

The ISO 11898 standard specifies a data rate of up to 1 Mbps, maximum CAN bus cable length of 40 m, maximum drop line (stub) length of 0.3 m and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet and NMEA200.

A high number of nodes requires a transceiver with high input impedance and wide common-mode range, such as the SN65HVD23x-Q1 CAN family. ISO 11898-2 specifies the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The SN65HVD23x-Q1 devices are specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common mode range of –2 V to 7 V through a 330-Ω coupling network. This network represents the bus loading of 120 SN65HVD23x-Q1 transceivers based on their minimum differential input resistance of 40 kΩ. Therefore, the SN65HVD23x-Q1 devices support up to 120 transceivers on a single bus segment with margin to the 1.2-V minimum differential input-voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity. Thus, a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system-design and data-rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, fewer than 64 nodes, and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

11.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Typical Application (continued)

11.2.2 Detailed Design Procedure

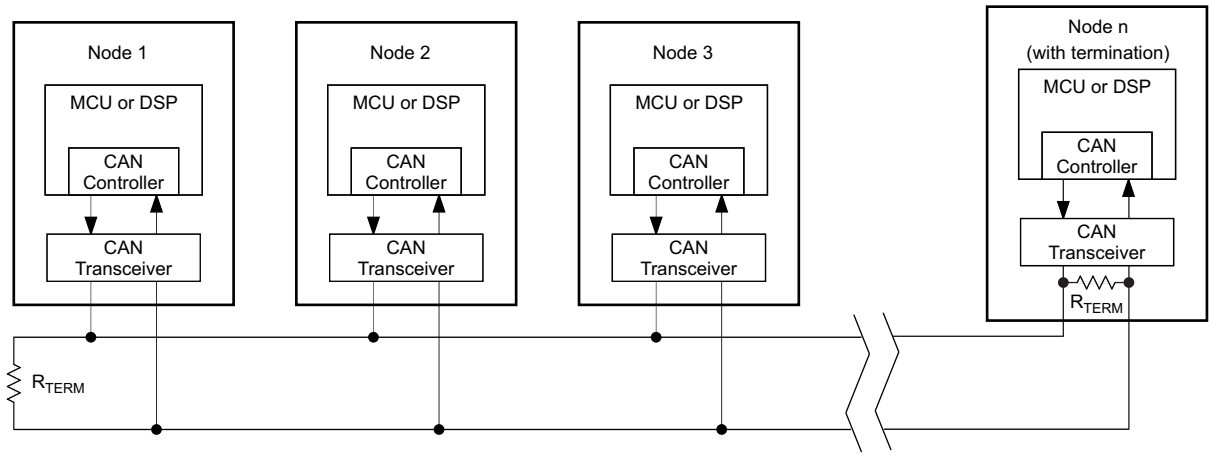


Figure 38. Typical CAN Bus

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used (see Figure 39). Split termination uses two 60-Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

Care should be taken in the power ratings of the termination resistors used. Typically, the worst-case condition would be if the system power supply is shorted across the termination resistance to ground. In most cases, the current flow through the resistor in this condition would be much higher than the transceiver current limit.

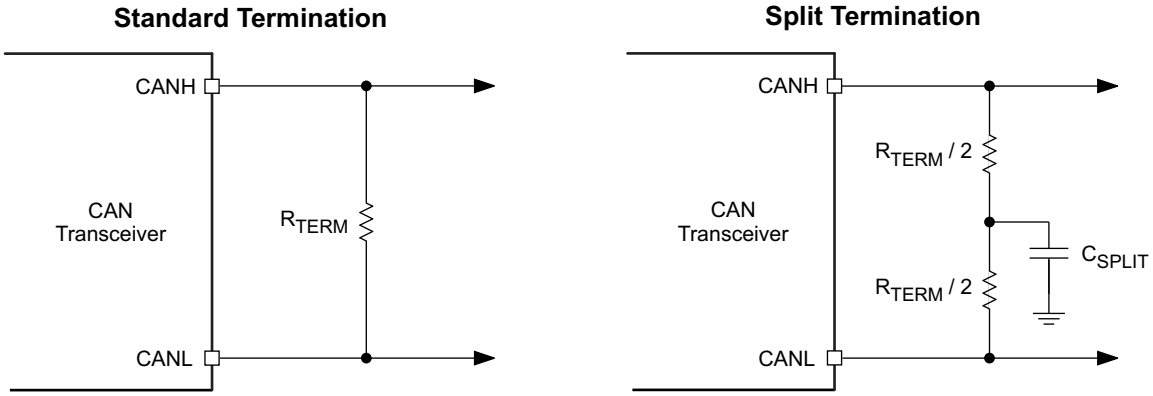


Figure 39. CAN Bus Termination Concepts

11.2.3 Application Curve

Figure 40 shows three typical output waveforms for the SN65HVD233-Q1 device with three different connections made to the RS pin. The top waveform shows the typical differential signal when transitioning from a recessive level to a dominant level on the CAN bus with RS tied to GND through a 0-Ω resistor. The second waveform shows the same signal for the condition with a 10-kΩ resistor tied from RS to ground. The bottom waveform shows the typical differential signal for the case where a 100-kΩ resistor is tied from the RS pin to ground.

Typical Application (continued)

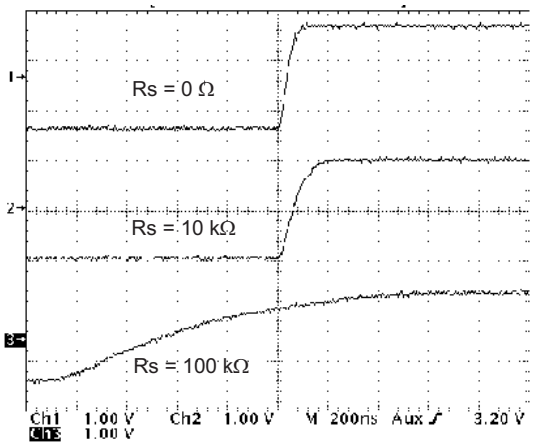


Figure 40. Typical SN65HVD233-Q1 Output Waveforms With Different Slope-Control Resistor Values

11.3 System Example

11.3.1 ISO 11898 Compliance of SN65HVD23x-Q1 Family of 3.3-V CAN Transceivers

11.3.1.1 Introduction

Many users value the low power consumption of operating their CAN transceivers from a 3.3-V supply. However, some are concerned about the interoperability with 5-V-supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

11.3.1.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single-ended logic-level output signal.

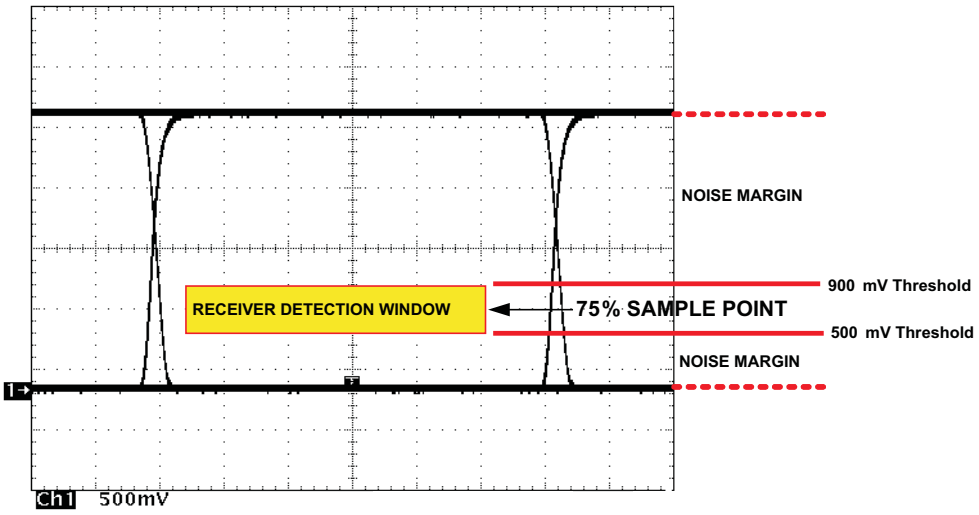


Figure 41. Typical Differential-Output-Voltage Waveform

System Example (continued)

The CAN driver creates the differential voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD23x-Q1 device is greater than 1.5 V and less than 3 V across a 60-Ω load as defined by the ISO 11898 standard. These are the same limiting values as for 5-V-supplied CAN transceivers. The bus termination resistors, and not the CAN driver, drive the bus to the recessive state.

A CAN receiver is required to output a recessive state when less than 500 mV of differential voltage exists on the bus, and a dominant state when more than 900 mV of differential voltage exists on the bus. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V. The SN65HVD23x-Q1 family of receivers meets these same input specifications as 5-V-supplied receivers do.

11.3.1.3 Common-Mode Signal

The differential receiver rejects the common-mode signal, which is the average of the two CAN signals. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Because the bias voltage of the recessive state of the device is dependent on V_{CC}, any noise present or any variation of V_{CC} has an effect on this bias voltage seen by the bus. The SN65HVD23x-Q1 family has the recessive bias voltage set higher than 0.5 × V_{CC} to comply with the ISO 11898-2 CAN standard. The caveat to this is that the common-mode voltage drops by a approximately 200 millivolts when driving a dominant bit on the bus. This means that there is a common-mode shift between the dominant-bit and recessive-bit states of the device. Although this is not ideal, this small variation in the driver common-mode output is rejected by differential receivers and does not affect data, signal noise margins, or error rates.

11.3.1.4 Interoperability of 3.3-V CAN in 5-V CAN Systems

The 3.3-V-supplied SN65HVD23x-Q1 family of CAN transceivers is fully compatible with 5-V CAN transceivers. The differential output voltage is the same, the recessive common-mode output bias is the same, and the receivers have the same input specifications. The only slight difference is in the dominant common-mode output voltage, which is aapproximately 200 millivolts lower for a 3.3-V CAN transceiver than for a 5-V-supplied transceiver.

To help ensure the widest interoperability possible, the SN65HVD23x-Q1 family has successfully passed the internationally recognized GIFT/ICT conformance and interoperability testing for CAN transceivers. Electrical interoperability does not always assure interchangeability, however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure full interchangeability. This comes only with thorough equipment testing.

12 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the V_{CC} supply pins as possible. The TPS76333-Q1 is a linear voltage regulator suitable for the 3.3 V supply.

13 Layout

13.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. On-chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use V_{CC} and ground planes to provide low inductance.

Layout Guidelines (continued)

NOTE

High-frequency current follows the path of least inductance and not the path of least resistance.

Design bus protection by placing the protective components in the signal path. Do not force the transient current to divert from the signal path to reach the protection device.

An example placement of the transient-voltage-suppression (TVS) device indicated as D1 (either bidirectional diode or varistor solution) and bus filter capacitors C8 and C9 is shown in Figure 42.

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 42 shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground via capacitor C7. Split termination provides common-mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus, as there are signal integrity issues if the bus is not properly terminated on both ends. See the Detailed Design Procedure section for information on power ratings needed for the termination resistor(s).

Bypass and bulk capacitors should be placed as close as possible to the supply pins of the transceiver, as in the example of C2 and C3 on V_{CC}.

Use at least two vias for the V_{CC} and ground connections of the bypass capacitors and protection devices to minimize trace and via inductance.

To limit current on the digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4.

To filter noise on the digital I/O lines, a capacitor may be used close to the input side of the I/O as shown by C1 and C4.

Because the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-kΩ to 10-kΩ pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open-drain host processor is used to drive the TXD pin of the device, an external pullup resistor between 1 kΩ and 10 kΩ to V_{CC} should be used to drive the recessive input state of the device.

Pin 8: The mode pin, RS, is shown, assuming that it is used in the application. If the device is only to be used in normal mode or slope-control mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

13.2 Layout Example

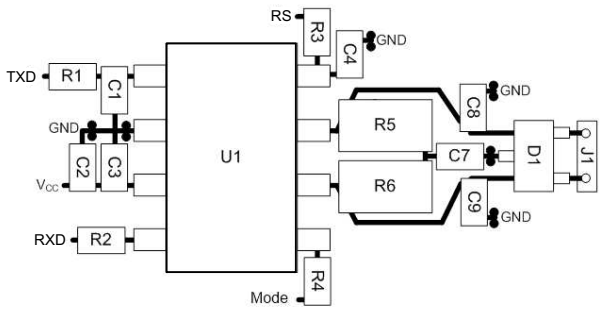


Figure 42. Layout Example Diagram

14 デバイスおよびドキュメントのサポート

14.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 7. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
SN65HVD233-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
SN65HVD234-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
SN65HVD235-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

14.2 ドキュメントの更新通知を受け取る方法

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14.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.4 商標

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14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD233QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	233Q
SN65HVD233QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	233Q
SN65HVD234QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	234Q
SN65HVD234QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	234Q
SN65HVD235QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	235Q
SN65HVD235QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	235Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN65HVD233-Q1, SN65HVD234-Q1, SN65HVD235-Q1 :

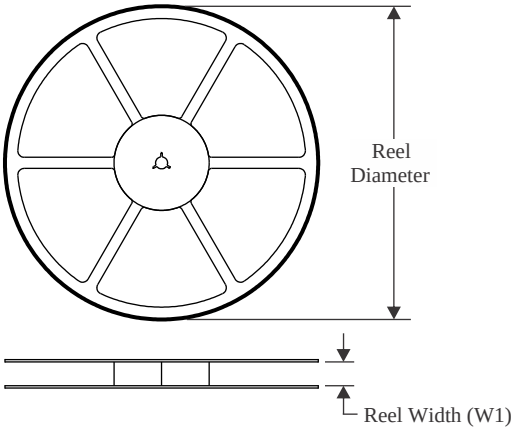
- Catalog : SN65HVD233, SN65HVD234, SN65HVD235
- Enhanced Product : SN65HVD233-EP

NOTE: Qualified Version Definitions:

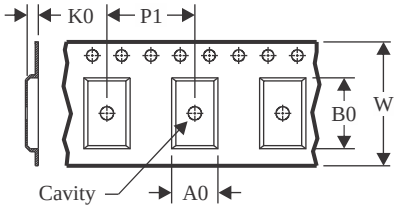
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

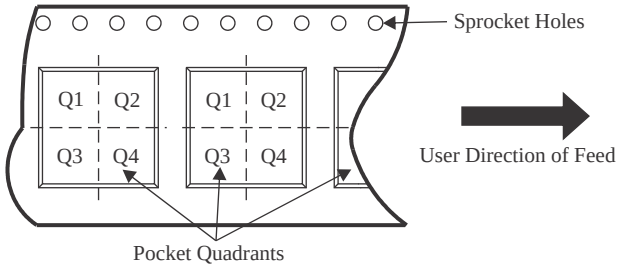


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

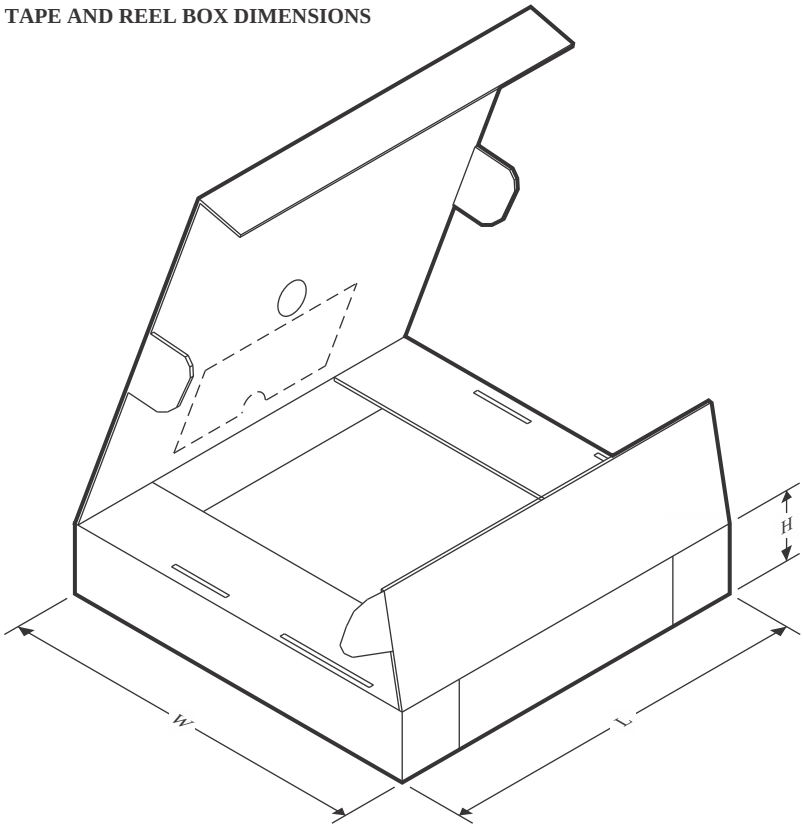
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

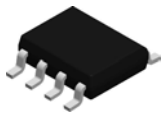
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD233QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD234QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD235QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD233QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD234QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD235QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

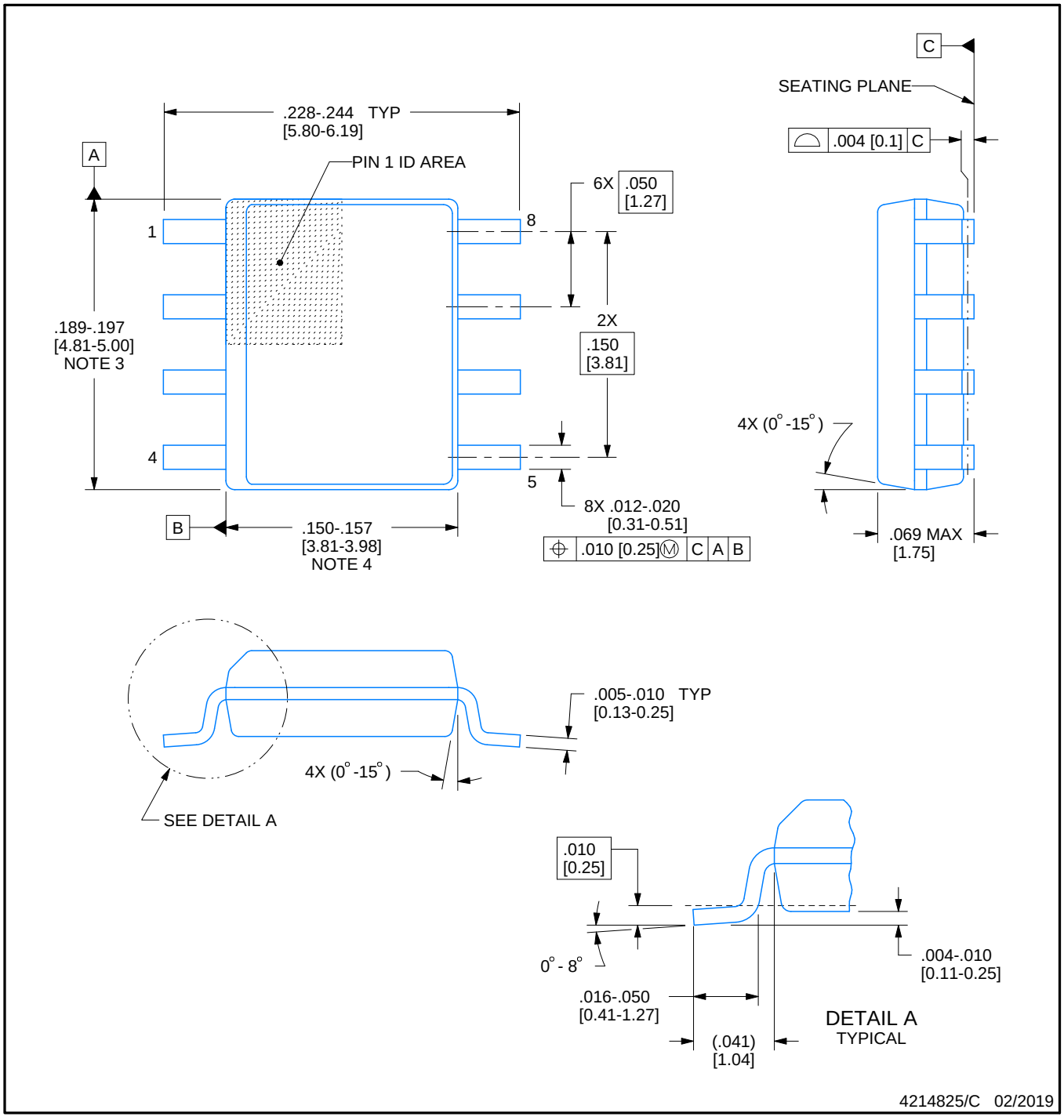


PACKAGE OUTLINE

D0008A

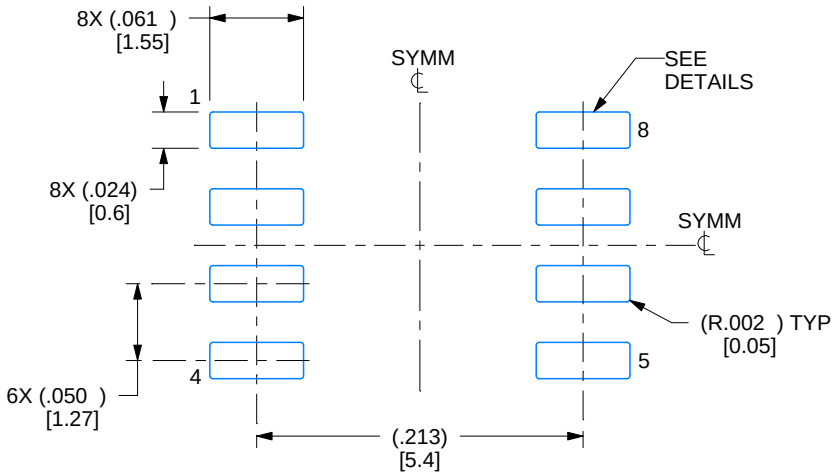
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

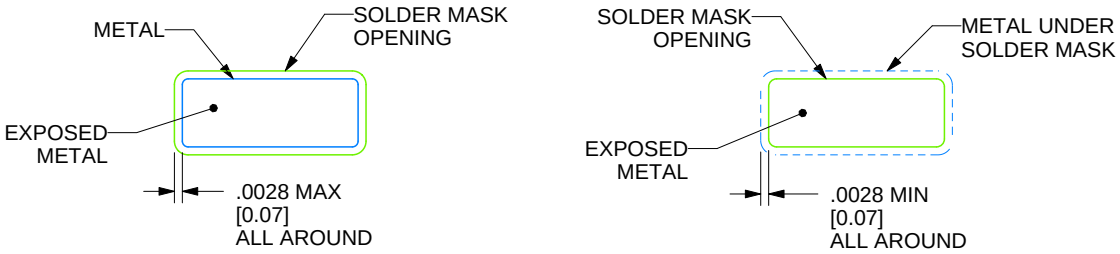


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

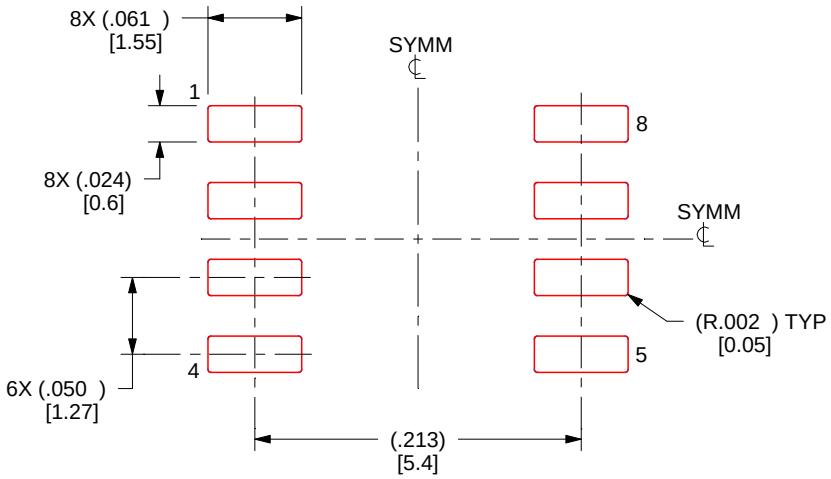
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月