

SN65HVD178x-Q1 3.3V～5V 動作、故障保護機能搭載 RS-485 トランシーバ

1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み
 - デバイス温度グレード 1:
 - -40°C ～ 125°C の周囲動作温度範囲
 - デバイス HBM ESD 分類レベル H2
 - デバイス CDM ESG 分類レベル C3B
- バスピンのフォルト保護:
 - $> \pm 70\text{V}$ ('HVD1780-Q1, 'HVD1781-Q1)
 - $> \pm 30\text{V}$ ('HVD1782-Q1)
- 3.3V～5V の電源電圧範囲で動作
- バスピンの $\pm 16\text{kV}$ HBM 保護
- ユニット負荷の低減により最大 320 ノードに対応
- 開放、短絡、アイドル バス状況に対してフェイルセーフなレシーバ
- 低消費電力
 - 低いスタンバイ時消費電流: $1\mu\text{A}$ 以下
 - 動作時の静止電流 I_{CC} : 4mA
- 業界標準の SN75176 とピン互換
- 信号速度: 115kbps、1Mbps、最大 10Mbps

2 アプリケーション

車載データリンク

3 概要

これらのデバイスは、電源への直接短絡、誤配線フォルト、コネクタ障害、ケーブルのクラッシュ、ツールの誤用などの過電圧フォルトに耐えられるよう設計されています。また、ESD イベントにも高い耐性を持ち、人体モデル仕様に対して高いレベルの保護を実現しています。

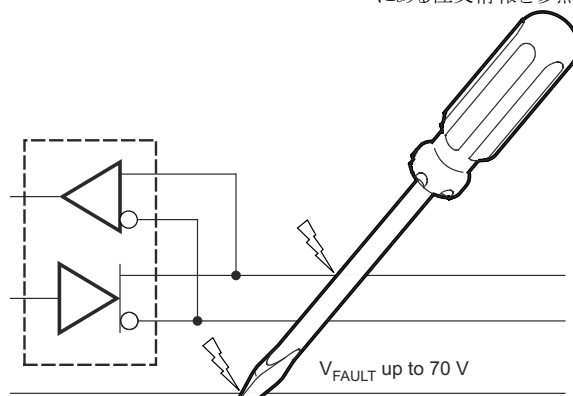
これらのデバイスは、差動ドライバと差動レシーバを組み合わせたもので、単一電源で動作します。'HVD1782 では、ドライバの差動出力とレシーバの差動入力が入内部的に接続され、半二重 (2 線式バス) 通信に適したバスポートを形成しています。このポートは広い同相電圧範囲を持つため、これらのデバイスは長いケーブルを使用するマルチポイントアプリケーションに適しています。これらのデバイスは、 -40°C ～ 125°C で仕様が規定されています。これらのデバイスは、業界標準の SN75176 トランシーバとピン互換であるため、ほとんどのシステムでそのまま置き換えるだけで性能を向上させることができます。

これらのデバイスは 5V 電源において ANSI TIA/EIA 485A に完全準拠しており、低消費電力のアプリケーションではドライバの出力電圧を落として、3.3V 電源で動作可能です。拡張同相電圧範囲での動作が必要なアプリケーションについては、SN65HVD1785 (SLLS872) のデータシートを参照してください。

製品情報

部品番号	信号速度 ⁽¹⁾	ノード数
SN65HVD1780-Q1	最大 115kbps	最大 320
SN65HVD1781-Q1	最大 1Mbps	最大 320
SN65HVD1782-Q1	最大 10Mbps	最大 64

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



Copyright © 2016, Texas Instruments Incorporated

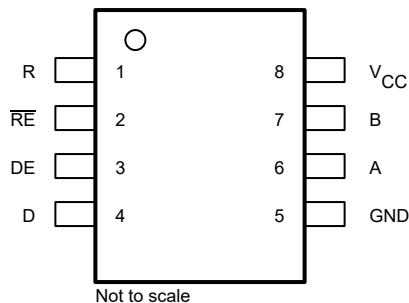
概略回路図



Table of Contents

1 特長	1	7.3 Feature Description.....	13
2 アプリケーション	1	7.4 Device Functional Modes.....	14
3 概要	1	8 Application and Implementation	16
4 Pin Configuration and Functions	3	8.1 Application Information.....	16
5 Specifications	4	8.2 Typical Application.....	16
5.1 Absolute Maximum Ratings.....	4	8.3 Power Supply Recommendations.....	20
5.2 ESD Ratings—AEC.....	4	8.4 Layout.....	20
5.3 ESD Ratings—IEC.....	4	9 Device and Documentation Support	21
5.4 Recommended Operating Conditions.....	4	9.1 Device Support.....	21
5.5 Thermal Information.....	5	9.2 Documentation Support.....	21
5.6 Electrical Characteristics.....	5	9.3 ドキュメントの更新通知を受け取る方法.....	21
5.7 Power Dissipation Ratings.....	6	9.4 サポート・リソース.....	21
5.8 Switching Characteristics.....	7	9.5 Trademarks.....	21
5.9 Package Dissipation Ratings.....	7	9.6 静電気放電に関する注意事項.....	21
5.10 Typical Characteristics.....	8	9.7 用語集.....	21
6 Parameter Measurement Information	9	10 Revision History	22
7 Detailed Description	13	11 Mechanical, Packaging, and Orderable Information	22
7.1 Overview.....	13		
7.2 Functional Block Diagram.....	13		

4 Pin Configuration and Functions



**図 4-1. D Package, 8-Pin SOIC
(Top View)**

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO		
A	6	Bus I/O	Driver output or receiver input (complementary to B)
B	7	Bus I/O	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
RE	2	Digital input	Receiver enable, active low
V _{CC}	8	Supply	3.15V to 5.5V supply

5 Specifications

5.1 Absolute Maximum Ratings

See Note (1).

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	7	V
Voltage range at bus pins	'HVD1780-Q1, 'HVD1781-Q1	A, B pins	−70	70	V
	'HVD1782-Q1	A, B pins	−70	30	
Input voltage range at any logic pin			−0.3	V _{CC} + 0.3	V
Transient overvoltage pulse through 100 Ω per TIA-485			−70	70	V
Receiver output current			−24	24	mA
Continuous total power dissipation			See Power Dissipation Ratings		
T _J	Junction temperature			170	°C
T _{stg}	Storage temperature		−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings—AEC

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	Bus terminals and GND	±16000
			All pins	±4000
		Charged-device model (CDM), per AEC Q100-011		±2000
		Machine Model (MM), AEC-Q100-003		±400

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings—IEC

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per IEC 60749-26	Bus terminals and GND	±16000

5.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3.15	5	5.5	V
V _I	Input voltage at any bus terminal (separately or common mode) ⁽¹⁾		−7		12	V
V _{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V _{CC}	V
V _{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V _{ID}	Differential input voltage		−12		12	V
I _O	Output current, driver		−60		60	mA
	Output current, receiver		−8		8	mA
R _L	Differential load resistance		54	60		Ω
C _L	Differential load capacitance			50		pF
1/t _{UI}	Signaling rate	SN65HVD1780-Q1			0.115	Mbps
		SN65HVD1781-Q1			1	
		SN65HVD1782-Q1			10	
T _A	Operating free-air temperature (See the Thermal Information table)	5V supply	−40		105	°C
		3.3V supply	−40		125	
T _J	Junction Temperature		−40		150	°C

- (1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾			SN65HVD1780-Q1 SN65HVD1781-Q1 SN65HVD1782-Q1	UNIT
			D (SOIC)	
			8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	JEDEC high-K model	138	°C/W
		JEDIC low-K model	242	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance		61	°C/W
R _{θJB}	Junction-to-board thermal resistance		62	°C/W
ψ _{JT}	Junction-to-top characterization parameter		3.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter		38.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OD}	Driver differential output voltage magnitude	R _L = 60 Ω, 4.75 V ≤ V _{CC} ≤ 375 Ω on each output to –7 V to 12 V, See Figure 6-1	T _A < 85°C	1.5			V
			T _A < 125°C	1.4			
		R _L = 54 Ω, 4.75 V ≤ V _{CC} ≤ 5.25 V	T _A < 85°C	1.7	2		
			T _A < 125°C	1.5			
		R _L = 54 Ω, 3.15 V ≤ V _{CC} ≤ 3.45 V		0.8	1		
		R _L = 100 Ω, 4.75 V ≤ V _{CC} ≤ 5.25 V	T _A < 85°C	2.2	2.5		
			T _A < 125°C	2			
Δ V _{OD}	Change in magnitude of driver differential output voltage	R _L = 54 Ω		–50	0	50	mV
V _{OC(SS)}	Steady-state common-mode output voltage			1	V _{CC} /2	3	V
ΔV _{OC}	Change in differential driver output common-mode voltage			–50	0	50	mV
V _{OC(PP)}	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 6-2			500		mV
C _{OD}	Differential output capacitance				23		pF
V _{IT+}	Positive-going receiver differential input voltage threshold				–100	–35	mV
V _{IT–}	Negative-going receiver differential input voltage threshold			–180	–150		mV
V _{HYS}	Receiver differential input voltage threshold hysteresis (V _{IT+} – V _{IT–}) ⁽¹⁾			30	50		mV
V _{OH}	Receiver high-level output voltage	I _{OH} = –8 mA		2.4	V _{CC} – 0.3		V
V _{OL}	Receiver low-level output voltage	I _{OL} = 8 mA	T _A < 85°C		0.2	0.4	V
			T _A < 125°C			0.5	
I _{I(LOGIC)}	Driver input, driver enable, and receiver enable input current			–50		50	μA
I _{OZ}	Receiver output high-impedance current	V _O = 0 V or V _{CC} , RE at V _{CC}		–1		1	μA
I _{OS}	Driver short-circuit output current			–200		200	mA

5.6 Electrical Characteristics (続き)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I _{I(BUS)}	Bus input current (disabled driver)	V _{CC} = 3.15 to 5.5 V or V _{CC} = 0 V, DE at 0 V	V _I = 12 V	HVD1780-Q1, HVD1781-Q1		75	100	μA
				HVD1782-Q1		400	500	
			V _I = −7 V	HVD1780-Q1, HVD1781-Q1	−60	−40		
				HVD1782-Q1	−400	−300		
I _{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V _{CC} , RE = GND, no load			4	6	mA
		Driver enabled, receiver disabled	DE = V _{CC} , RE = V _{CC} , no load			3	5	
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load			2	4	
		Driver and receiver disabled, standby mode	DE = GND, D = open, RE = V _{CC} , no load, T _A < 85°C			0.15	1	μA
			DE = GND, D = open, RE = V _{CC} , no load, T _A < 125°C				12	
		Supply current (dynamic)		See the Typical Characteristics section				

(1) Specified by design. Not production tested.

5.7 Power Dissipation Ratings

PARAMETER	TEST CONDITIONS	VALUE	UNIT
P_D Power dissipation	$V_{CC} = 3.6$ V, $T_J = 150^\circ C$, $R_L = 300 \Omega$, $C_L = 50$ pF (driver), $C_L = 15$ pF (receiver) 3.3-V supply, unterminated ⁽¹⁾	75	mW
	$V_{CC} = 3.6$ V, $T_J = 150^\circ C$, $R_L = 100 \Omega$, $C_L = 50$ pF (driver), $C_L = 15$ pF (receiver) 3.3-V supply, RS-422 load ⁽¹⁾	95	
	$V_{CC} = 3.6$ V, $T_J = 150^\circ C$, $R_L = 54 \Omega$, $C_L = 50$ pF (driver), $C_L = 15$ pF (receiver) 3.3-V supply, RS-485 load ⁽¹⁾	115	
	$V_{CC} = 5.5$ V, $T_J = 150^\circ C$, $R_L = 300 \Omega$, $C_L = 50$ pF (driver), $C_L = 15$ pF (receiver) 5-V supply, unterminated ⁽¹⁾	290	
	$V_{CC} = 5.5$ V, $T_J = 150^\circ C$, $R_L = 100 \Omega$, $C_L = 50$ pF (driver), $C_L = 15$ pF (receiver) 5-V supply, RS-422 load ⁽¹⁾	320	
	$V_{CC} = 5.5$ V, $T_J = 150^\circ C$, $R_L = 54 \Omega$, $C_L = 50$ pF (driver), $C_L = 15$ pF (receiver) 5-V supply, RS-485 load ⁽¹⁾	400	
T_{SD} Thermal-shutdown junction temperature		170	$^\circ C$

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: 1 Mbps.

5.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER (SN65HVD1780)							
t_r, t_f	Driver differential output rise/fall time	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, See 6-3	$3.15\ \text{V} < V_{CC} < 3.45\ \text{V}$	0.4	1.4	1.8	μs
			$3.15\ \text{V} < V_{CC} < 5.5\ \text{V}$	0.4	1.7	2.6	μs
t_{PHL}, t_{PLH}	Driver propagation delay	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, See 6-3			0.8	2	μs
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, See 6-3			20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See 6-4 and 6-5			0.1	5	μs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See 6-4 and 6-5		0.2	3	μs
		Receiver disabled			3	12	
DRIVER (SN65HVD1781)							
t_r, t_f	Driver differential output rise/fall time	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, See 6-3		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, See 6-3				200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, See 6-3				25	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See 6-4 and 6-5				3	μs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See 6-4 and 6-5			300	ns
		Receiver disabled				10	μs
DRIVER (SN65HVD1782)							
t_r, t_f	Driver differential output rise/fall time	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$	All V_{CC} and Temp			50	ns
			$V_{CC} > 4.5\text{V}$ and $T < 105^\circ\text{C}$		16		
t_{PHL}, t_{PLH}	Driver propagation delay	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, See 6-3				55	ns
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, See 6-3				10	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See 6-4 and 6-5				3	μs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See 6-4 and 6-5			300	ns
		Receiver disabled				9	μs
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)							
t_r, t_f	Receiver output rise/fall time ⁽¹⁾	$C_L = 15\ \text{pF}$, See 6-6	All devices		4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time	$C_L = 15\ \text{pF}$, See 6-6	HVD1780-Q1, HVD1781-Q1		100	200	ns
			HVD1782-Q1			80	
$t_{SK(P)}$	Receiver output pulse skew, $ t_{PHL} - t_{PLH} $	$C_L = 15\ \text{pF}$, See 6-6	HVD1780-Q1, HVD1781-Q1		6	20	ns
			HVD1782-Q1			5	
t_{PLZ}, t_{PHZ}	Receiver disable time ⁽¹⁾	Driver enabled, See 6-7			15	100	ns
$t_{PZL(1)}, t_{PZH(1)}$ $t_{PZL(2)}, t_{PZH(2)}$	Receiver enable time	Driver enabled, See 6-7			80	300	ns
		Driver disabled, See 6-8			3	9	μs

(1) Specified by design. Not production tested.

5.9 Package Dissipation Ratings

PACKAGE ⁽¹⁾	JEDEC THERMAL MODEL	$T_A < 25^\circ\text{C}$ RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ RATING	$T_A = 105^\circ\text{C}$ RATING	$T_A = 125^\circ\text{C}$ RATING (3.3 V ONLY)
SOIC (D) 8-pin	High-K	905 mW	7.25 mW/ $^\circ\text{C}$	470 mW	325 mW	180 mW
	Low-K	516 mW	4.1 mW/ $^\circ\text{C}$	268 mW	186 mW	103 mW

(1) For the most current package and ordering information, see the [Mechanical, Packaging, and Orderable Information](#) section, or see the TI website at www.ti.com.

5.10 Typical Characteristics

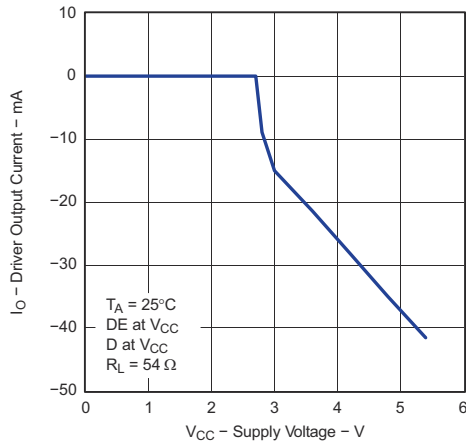


Figure 5-1. Driver Output Current vs Supply Voltage

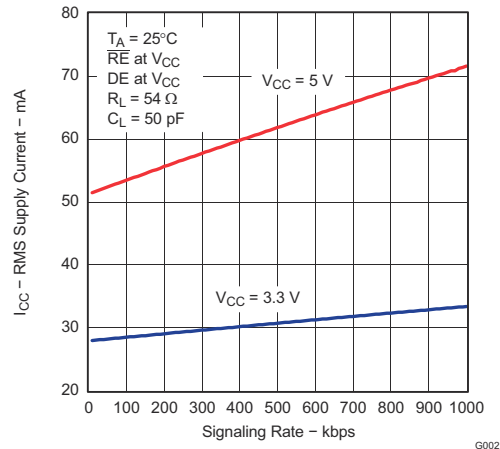


Figure 5-2. RMS Supply Current vs Signaling Rate

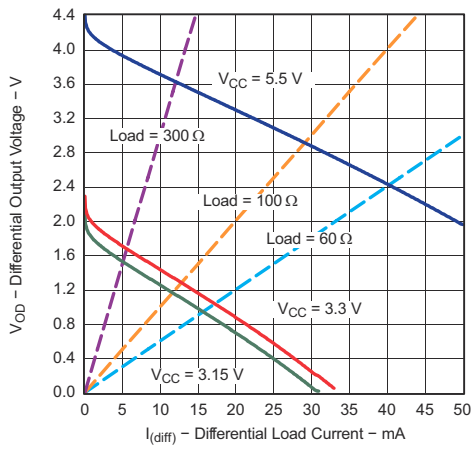


Figure 5-3. Differential Output Voltage vs Differential Load Current

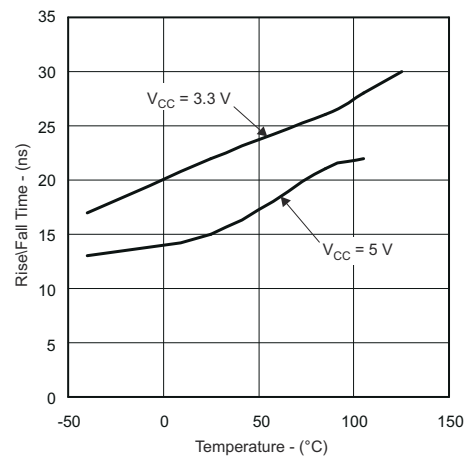


Figure 5-4. SN65HVD1782 Rise and Fall Time

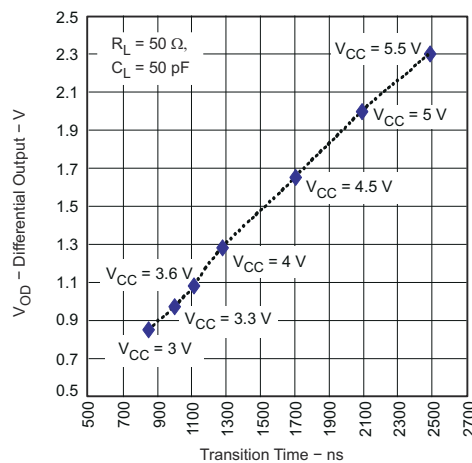
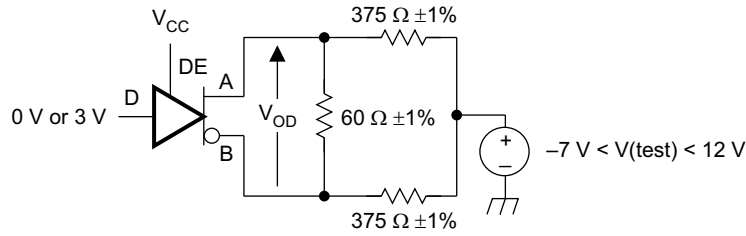


Figure 5-5. SN65HVD1780 Differential Output Amplitude and Transition Time vs Supply Voltage

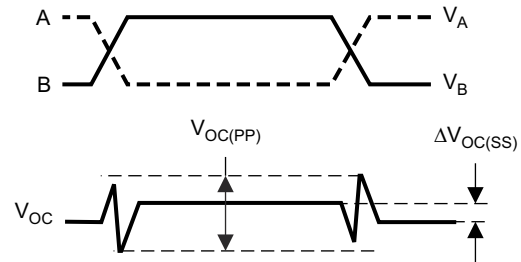
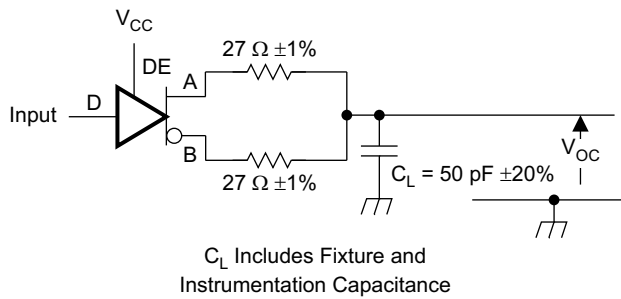
6 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 ns, output impedance 50 Ω .



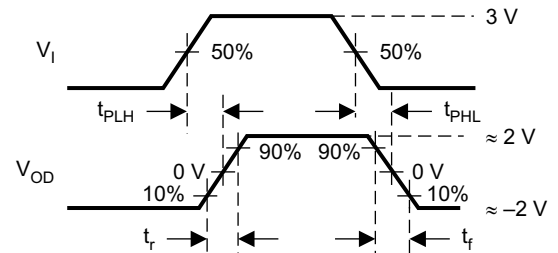
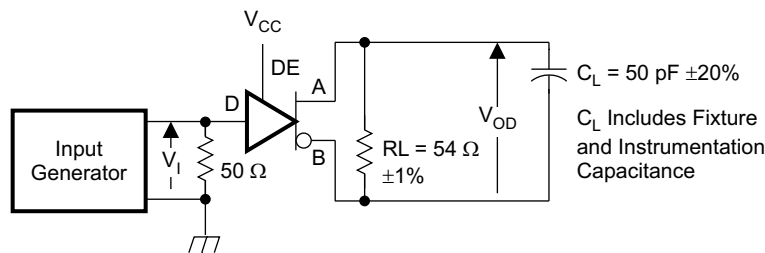
Copyright © 2016, Texas Instruments Incorporated

Figure 6-1. Measurement of Driver Differential Output Voltage With Common-Mode Load



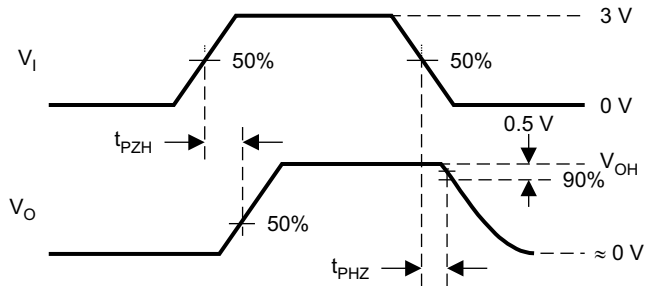
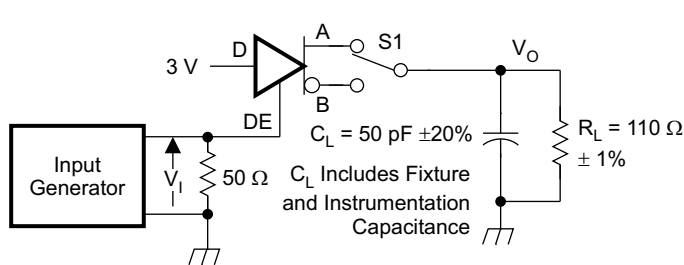
Copyright © 2016, Texas Instruments Incorporated

Figure 6-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



Copyright © 2016, Texas Instruments Incorporated

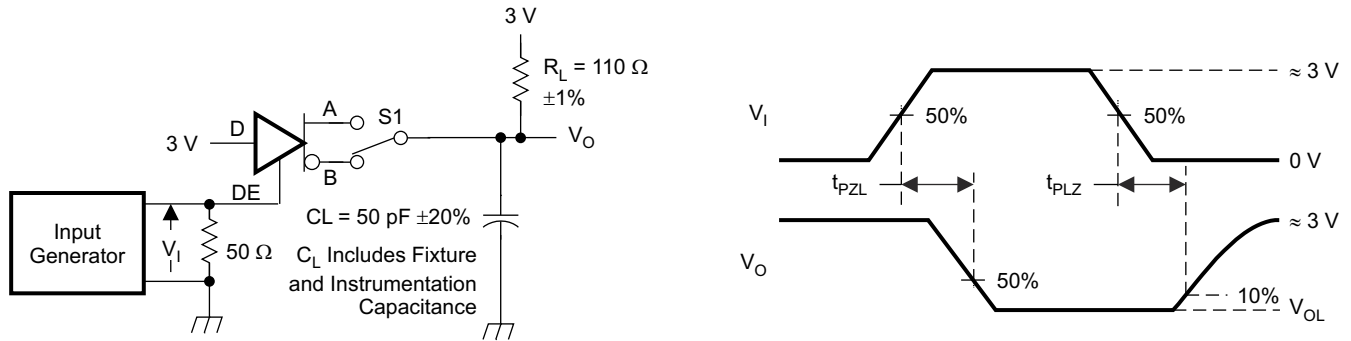
Figure 6-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



Copyright © 2016, Texas Instruments Incorporated

D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 6-4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



D at 0 V to test non-inverting output, D at 3 V to test inverting output.

図 6-5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

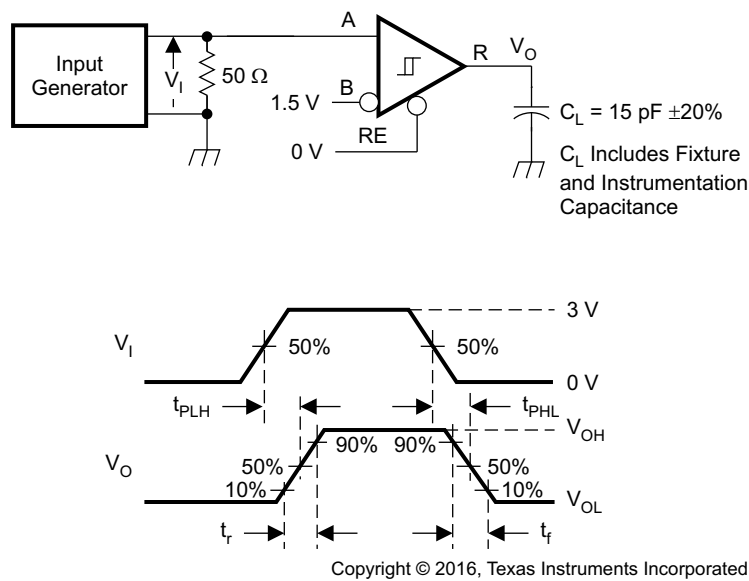


図 6-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

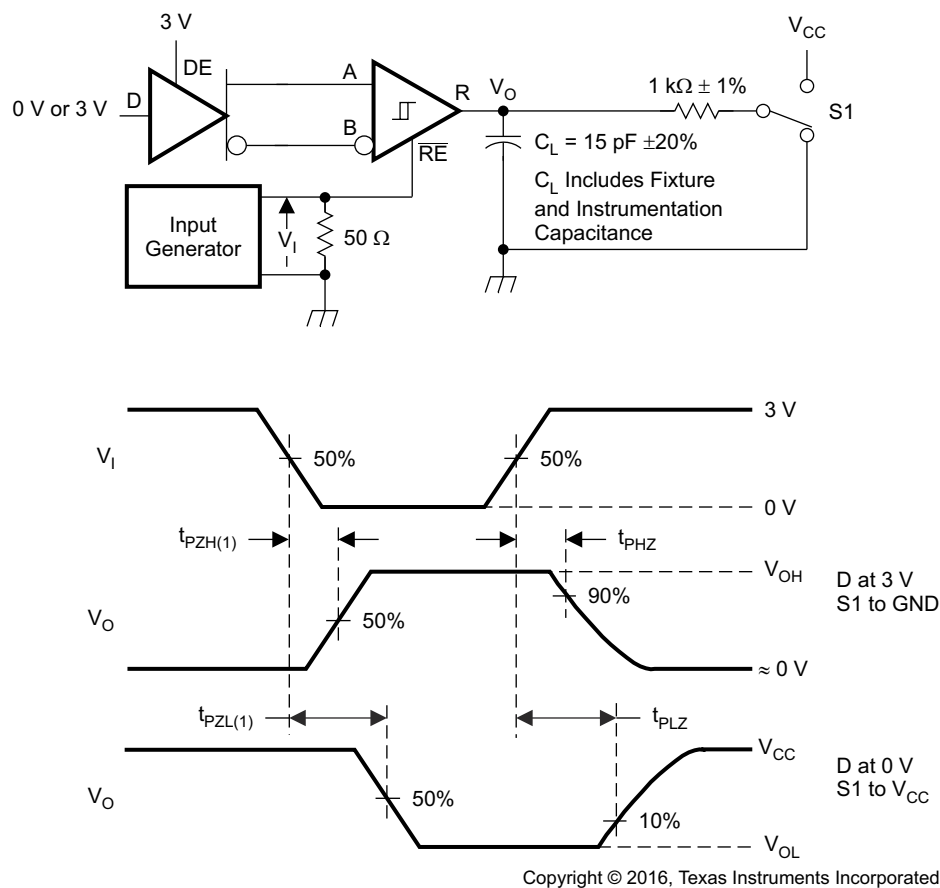


图 6-7. Measurement of Receiver Enable and Disable Times With Driver Enabled

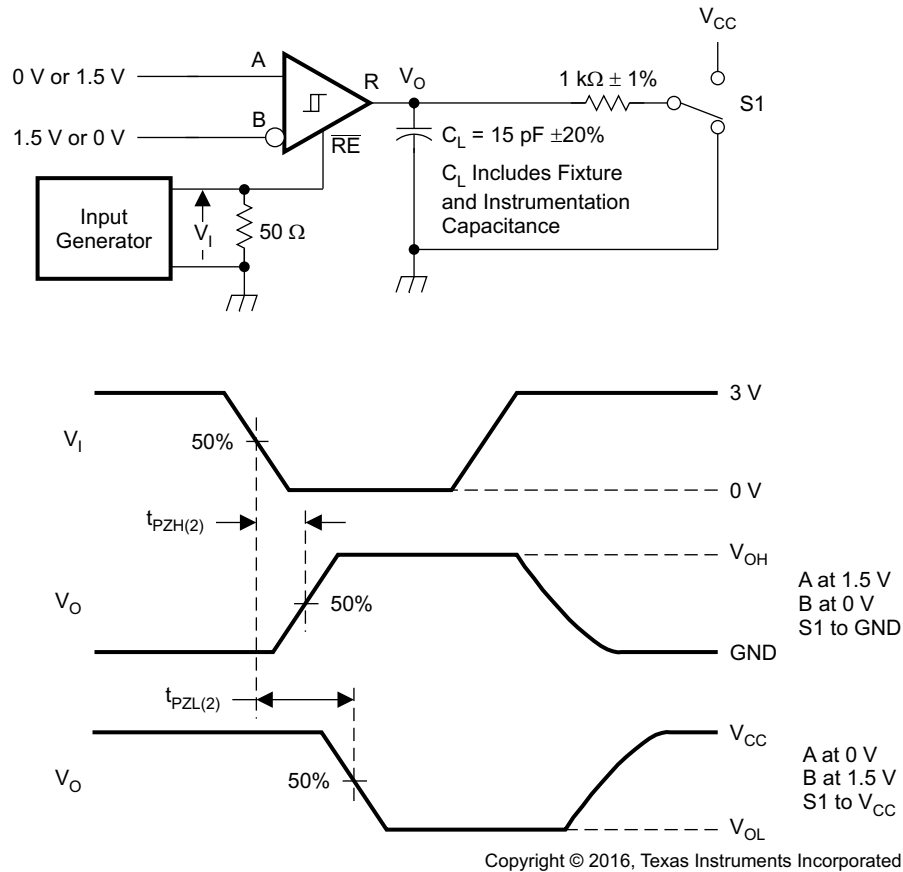


図 6-8. SN65HVD1781 Measurement of Receiver Enable Times With Driver Disabled

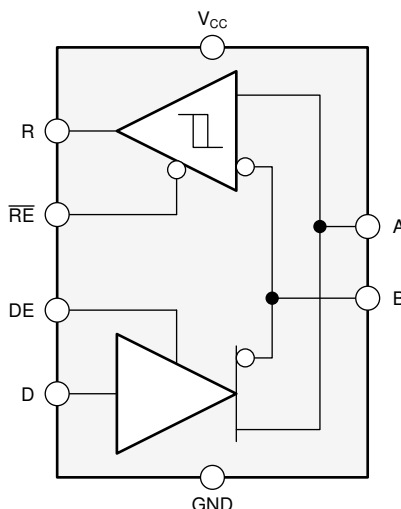
7 Detailed Description

7.1 Overview

The SN65HVD1780-Q1, SN65HVD1781-Q1, and SN65HVD1782-Q1 devices are half-duplex RS-485 transceivers available in three speed grades suitable for data transmission up to 115kbps, 1Mbps, and 10Mbps.

These devices feature a wide common-mode operating range and bus-pin fault protection up to $\pm 70\text{V}$. Each device has an active-high driver enable and active-low receiver enable. A standby current of less than $1\mu\text{A}$ can be achieved by disabling both driver and receiver.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against $\pm 16\text{kV}$ Human Body Model (HBM) electrostatic discharges.

Device operation is specified over a wide temperature range from -40°C to 125°C .

7.3.1 Bus Fault Conditions

The SN65HVD178x-Q1 family of RS-485 transceivers is designed to survive bus pin faults up to $\pm 70\text{V}$. The SN65HVD1782-Q1 device will not survive a bus pin fault with a direct short to voltages above 30V when all of the following occurs:

- The device is powered on
- The driver is enabled ($\text{DE} = \text{HIGH}$), and one of the following is true
 - $\text{D} = \text{HIGH}$ AND the bus fault is applied to the A pin
 - $\text{D} = \text{LOW}$ AND the bus fault is applied to the B pin

Under other conditions, the device survives shorts to bus pin faults up to $\pm 70V$. 表 7-1 summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

表 7-1. Bus Fault Conditions for the HVD1782

POWER	DE	D	A	B	RESULTS
OFF	X	X	$-70V < V_A < 70V$	$-70V < V_B < 70V$	Device survives
ON	LO	X	$-70V < V_A < 70V$	$-70V < V_B < 70V$	Device survives
ON	HI	L	$-70V < V_A < 70V$	$-70V < V_B < 30V$	Device survives
ON	HI	L	$-70V < V_A < 70V$	$30V < V_B$	Damage may occur
ON	HI	H	$-70V < V_A < 30V$	$-70V < V_B < 30V$	Device survives
ON	HI	H	$30V < V_A$	$-70V < V_B < 30V$	Damage may occur

7.3.2 Receiver Failsafe

The SN65HVD178x-Q1 family of half-duplex transceivers provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of $V_{IT+} = -35mV$ and an input hysteresis of $V_{HYS} = 30mV$, the receiver output remains logic high under bus-idle, bus-short, or open bus conditions in the presence of up to $130mV_{PP}$ differential noise without the need for external failsafe biasing resistors.

7.3.3 Hot-Plugging

These devices are designed to operate in *hot swap* or *hot-pluggable* applications. Key features for hot-pluggable applications are power-up and power-down glitch free operation, default disabled input and output pins, and receiver failsafe.

As shown in the [Functional Block Diagram](#), an internal power-on reset circuit keeps the driver outputs in a high impedance state until the supply voltage has reached a level at which the device will reliably operate. This circuit makes sure no problems occur on the bus pin outputs as the power supply turns on or off.

As shown in [Device Functional Modes](#), the driver and receiver enable inputs (DE and $\overline{RE}$) are disabled by default. This default makes sure the device neither drives the bus nor reports data on the R pin until the associated controller actively drives the enable pins.

7.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC} , thus, when left open while the driver is enabled, output A turns high and B turns low.

表 7-2. Driver Function Table

INPUT	ENABLE	OUTPUTS		DRIVER STATE
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+} , the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-} , the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 7-3. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	RECEIVER STATE
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The SN65HVD178x-Q1 family of devices is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

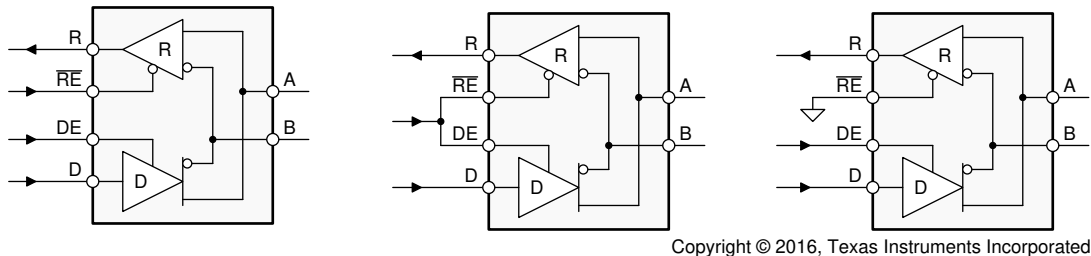


図 8-1. Half-Duplex Transceiver Configurations

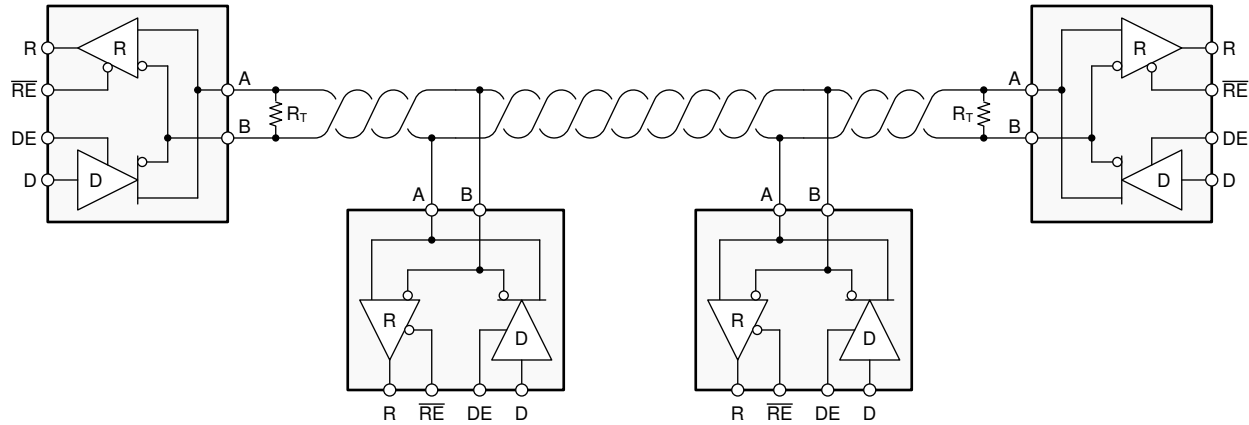
Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.



Copyright © 2016, Texas Instruments Incorporated

図 8-2. Typical RS-485 Network With Half-Duplex Transceivers

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

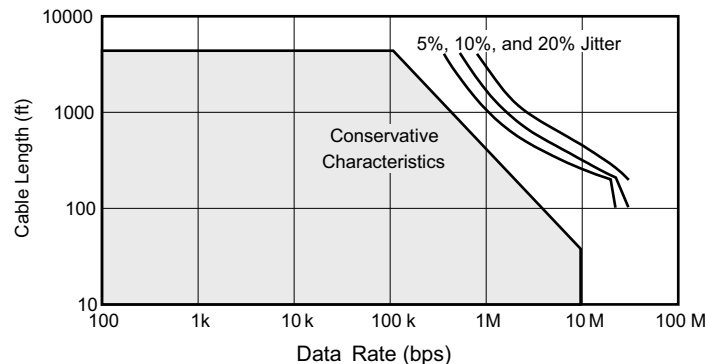


図 8-3. Cable Length vs Data Rate Characteristic

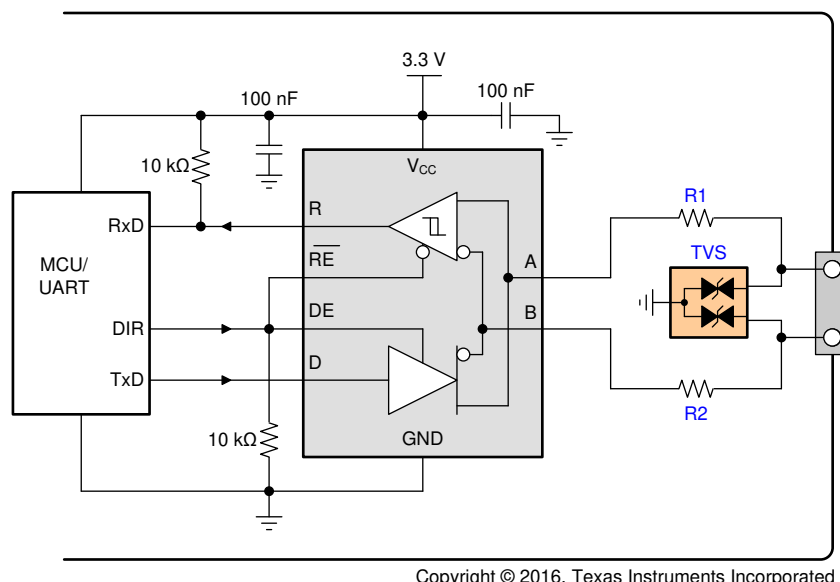
8.2.1.2 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL). Where 1 unit load represents a load impedance of approximately 12kΩ. Because the SN65HVD7x-Q1 family of devices consists of 1/10 UL transceivers, connecting up to 320 receivers to the bus is possible.

8.2.2 Detailed Design Procedure

Although the SN65HVD178x-Q1 family of devices is internally protected against human-body-model ESD strikes up to 16kV, additional protection against higher-energy transients can be provided at the application level by implementing external protection devices.

図 8-4 shows a protection circuit intended to withstand 8kV IEC ESD (per IEC 61000-4-2) as well as 4kV EFT (per IEC 61000-4-4).



Copyright © 2016, Texas Instruments Incorporated

図 8-4. RS-485 Transceiver with External Transient Protection

表 8-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER ⁽¹⁾
XCVR	RS-485 Transceiver	SN65HVD178x-Q1	TI
R1, R2	10Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 600W Transient Suppressor	SMBJ43CA	Littlefuse

(1) See [Third-Party Products Disclaimer](#).

8.2.2.1 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{\text{stub}} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

8.2.2.2 Receiver Failsafe

The differential receivers of the SN65HVD178x-Q1 family have receiver input thresholds that are offset, so the receiver output state is known for the following three fault conditions:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic High state, so the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200mV, and must output a Low when V_{ID} is more negative than –200mV. The receiver parameters which determine the failsafe performance are $V_{IT(+)}$, $V_{IT(-)}$, and V_{HYS} (the separation between $V_{IT(+)}$ and $V_{IT(-)}$). As shown in the [Electrical Characteristics](#) table, differential signals more negative than –200mV always cause a Low receiver output, and differential signals more positive than 200mV always cause a High receiver output.

When the differential input signal is close to zero, the signal is still above the maximum $V_{IT(+)}$ threshold of –35 mV, and the receiver output is High. Only when the differential input is more than V_{HYS} below $V_{IT(+)}$ does the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value, V_{HYS} , as well as the value of $V_{IT(+)}$.

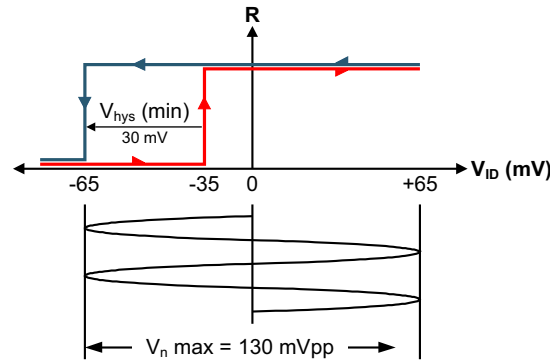
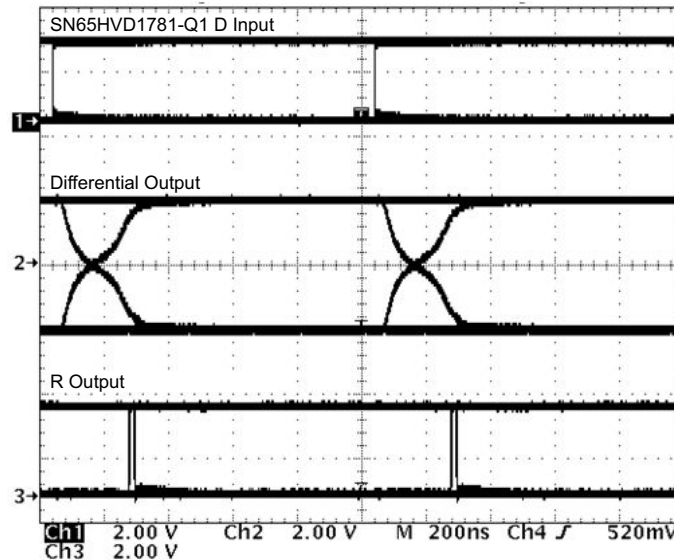


図 8-5. Noise Immunity Under Bus Fault Conditions

8.2.3 Application Curve



1-Mbps Operation

図 8-6. SN65HVD1781-Q1 PRBS Data Pattern

8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be buffered with a 100nF ceramic capacitor located as close to the supply pins as possible. The device is a linear voltage regulator suitable for the 5V supply.

8.4 Layout

8.4.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but often insufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance. High-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100nF to 220nF bypass capacitors as close as possible to the V_{CC} pins of the transceiver, UART, or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
6. Use 1k Ω to 10k Ω pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1mA.

8.4.2 Layout Example

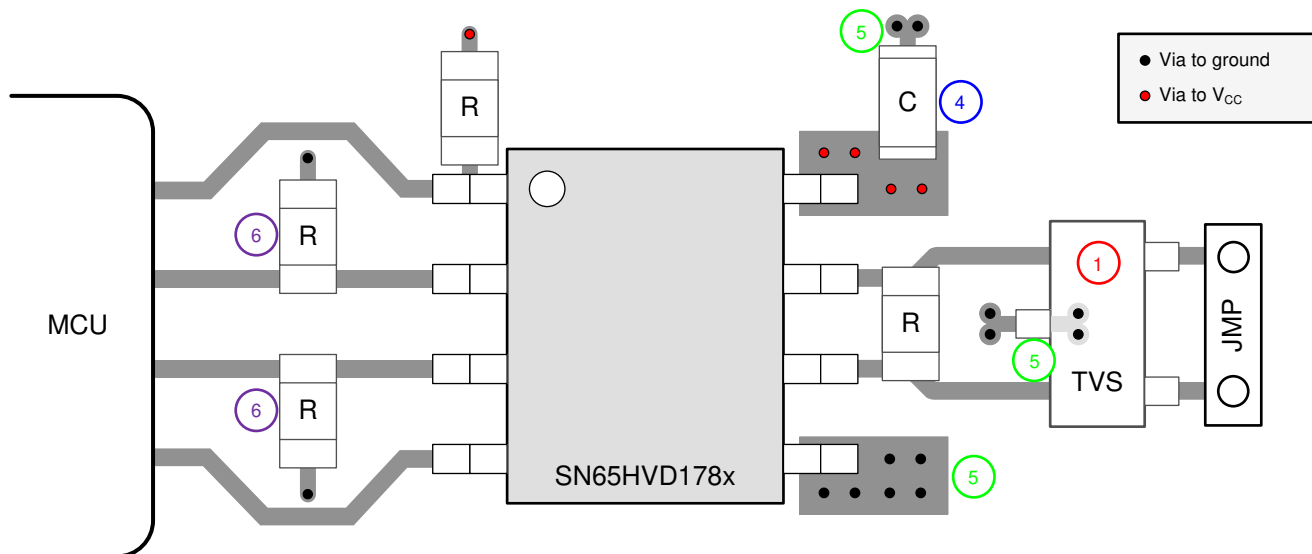


図 8-7. Half-Duplex Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- [RS-485 Half-Duplex Evaluation Module](#)
- [SN65HVD17xx Fault-Protected RS-485 Transceivers With Extended Common-Mode Range](#)
- [TPS7A6xxx-Q1 300-mA 40-V Low-Dropout Regulator With 25-μA Quiescent Current](#)

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

9.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

9.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (July 2017) to Revision E (October 2024) Page

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新..... 1
- Changed the Storage temperature MIN value from -44°C to -55°C in the *Absolute Maximum Ratings*4

Changes from Revision C (April 2016) to Revision D (July 2017) Page

- Changed the differential input to receive a valid bus high from $V_{ID} < V_{IT+}$ to $V_{ID} > V_{IT+}$ in the *Receiver Function Table* 14
- Changed the *Half-Duplex Layout Example* 20
- Added the *Receiving Notification of Documentation Updates* section.....21
- Changed the *Electrostatic Discharge Caution* statement.....21

Changes from Revision B (January 2016) to Revision C (April 2016) Page

- Changed the signaling rate for SN65HVD1780-Q1 from 115 to 0.115 Bin the *Recommended Operating Conditions* table4

Changes from Revision A (August 2015) to Revision B (January 2016) Page

- Changed HBM and CDM back to the AEC specification and split the IEC specification into a separate table . 4
- Added the SN65HVD1780-Q1 and SN65HVD1782-Q1 devices to the *Thermal Information* table.....5

Changes from Revision * (September 2010) to Revision A (August 2015) Page

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加..... 1
- 「特長」に新しい箇条書き項目を追加。2 番目の項目は副箇条書き項目付き..... 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD1780QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1780Q
SN65HVD1780QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1780Q
SN65HVD1781QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1781Q
SN65HVD1781QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1781Q
SN65HVD1782QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1782Q
SN65HVD1782QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1782Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65HVD1780-Q1, SN65HVD1781-Q1, SN65HVD1782-Q1 :

- Catalog : [SN65HVD1780](#), [SN65HVD1781](#), [SN65HVD1782](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1780QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1781QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1782QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1780QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD1781QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD1782QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

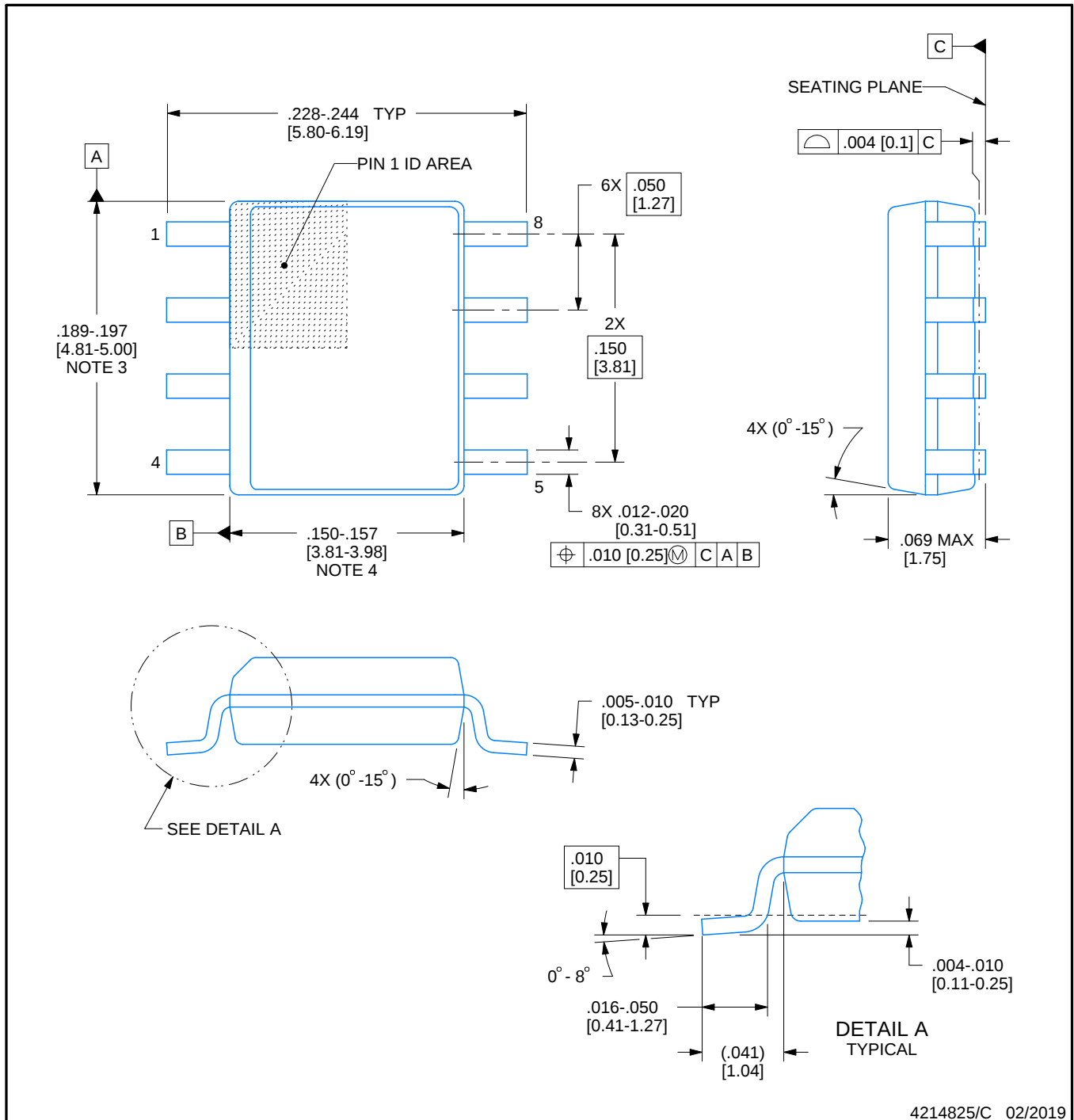


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated