SNx5HVD08 幅広い電源電圧範囲を持つ RS-485 トランシーバ

1 特長

- 3V～5.5V 電源で動作
- 無信号時電流電源の消費電力は 90mW 未満
- 開路、短絡、アイドル・バスのフェイルセーフ・レシーバ
- 1/8 ユニット負荷 (バス上に最大 256 ノード)
- 16kV HBM を超えるバス・ピンの ESD 保護
- 10Mbps で最適な信号品質を実現するためドライバ出力電圧のスルーレートを制限
- ANSI TIA/EIA-485 標準と電気的に互換

2 アプリケーション

- ホストから電力を供給されるリモート・ステーションを使用したデータ転送
- 絶縁型マルチポイント・データ・バス
- 産業用プロセス制御ネットワーク
- 販売時点情報管理ネットワーク
- 電気料金のメーター

3 説明

SN65HVD08 は、平衡データ転送用に設計された 3 ステート差動ライン・ドライバと差動ライン・レシーバを組み合わせており、ANSI TIA/EIA-485-A および ISO-8482E 標準に準拠したデバイスとの相互運用が可能です。

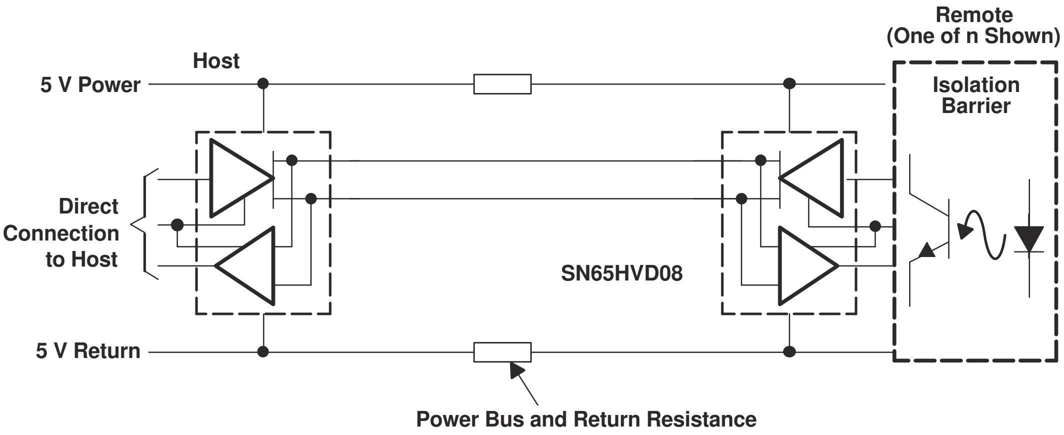
SN65HVD08 は、幅広い電源電圧範囲と低静止時電流要件により、ケーブルの 5V 電源バスから最大 2V のライン電圧降下で動作します。ケーブルで電力を供給することにより、グランド絶縁バスの各接続で絶縁型電源を生成する必要が軽減されます。

ドライバ差動出力とレシーバ差動入力は内部で接続されており、差動入出力 (I/O) バス・ポートを形成しています。この設計により、ドライバが無効になったり、電力が供給されなくなっても、バスへの負荷が最小限になります。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN75HVD08、 SN65HVD08	SOIC (8)	4.90mm x 3.91mm
	PDIP (8)	9.81mm x 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図

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4 Revision History

Changes from Revision D (March 2015) to Revision E (February 2023)	Page
• Changed the *Thermal Information* table	4
• Changed the *Typical Characteristics*	7

Changes from Revision C (July 2006) to Revision D (March 2015)	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

5 Pin Configuration and Functions

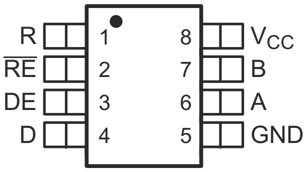


図 5-1. D or P Package, 8-Pin SOIC or PDIP (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input / output	Driver output and receiver input (complementary to B)
B	7	Bus input / output	Driver output and receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable low
V_{CC}	8	Supply	3-V to 5.5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1) (2)

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.3	6	V
Voltage at A or B	–9	14	V
Input voltage at D, DE, R or $\overline{RE}$	–0.5	V_{CC} + 0.5	V
Voltage input, transient pulse, A and B, through 100 Ω	–25	25	V
Receiver output current, I_O	–11	11	mA
Maximum Junction Temperature, T_J		150	°C
Storage Temperature, T_{STG}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A, B, and GND	16000	V
			All pins	4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3		5.5	V
Input voltage at any bus terminal (separately or common mode), V_I (1)		–7		12	V
High-level input voltage, V_{IH}	Driver, driver enable, and receiver enable inputs	2.25		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	
Differential input voltage, V_{ID}		–12		12	
High-level output current, I_{OH}	Driver	–60			mA
	Receiver	–8			
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN75HVD08	0		70	°C
	SN65HVD08	–40		85	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) SN75 Version	D (SOIC) SN65 Version	P (PDIP)	UNIT
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.4	116.7	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	56.3	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.1	63.4	23.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.1	8.8	12.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.4	62.6	23.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L= 60 Ω, 375 Ω on each output to -7 V to 12 V, See 図 7-1	1.5		V_{CC}	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of driver differential output voltage	R_L= 54 Ω	–0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See 図 7-2		0.5		V
V_{IT+}	Positive-going receiver differential input voltage threshold				–10	mV
V_{IT-}	Negative-going receiver differential input voltage threshold		–200			mV
V_{hys}	Receiver differential input voltage threshold hysteresis(V_{IT+} - V_{IT-})			35		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = -8 mA	2.4			V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.4	V
I_{IH}	Driver input, driver enable, and receiver enable high-level input current		–100		100	µA
I_{IL}	Driver input, driver enable, and receiver enable low-level input current		–100		100	µA
I_{OS}	Driver short-circuit output current	7 V < V_O < 12 V	–265		265	mA

6.5 Electrical Characteristics (continued)

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Bus input current (disabled driver)	V_I = 12 V			130	μA
		V_I = -7 V	–100			
		V_I = 12 V, V_{CC} = 0 V			130	
		V_I = -7 V. V_{CC} = 0 V	–100			
I_{CC}	Supply current	Receiver enabled, driver disabled, no load			10	mA
		Driver enabled, receiver disabled, no load			16	
		Both disabled			5	μA
		Both enabled, no load			16	mA

6.6 Driver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Driver high-to-low propagation delay time	R_L = 54 Ω, C_L = 50 pF,See 図 7-3	18		40	ns
t_{PLH}	Driver low-to-high propagation delay time		18		40	
t_r	Driver 10%-to-90% differential output rise time		10		55	
t_f	Driver 90%-to-10% differential output fall time		10		55	
$t_{SK(P)}$	Driver differential output pulse skew, $\lvert t_{PHL} - t_{PLH}\rvert$				2.5	
t_{en}	Driver enable time	Receiver enabled, See Figures 4 and 5			55	ns
		Receiver disabled, See Figures 4 and 5			6	μs
t_{dis}	Driver disable time	Receiver enabled, See Figures 4 and 5			90	ns

6.7 Receiver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Receiver high-to-low propagation delay time	C_L = 15 pF, See 図 7-6			70	ns
t_{PLH}	Receiver low-to-high propagation delay time				70	
t_r	Receiver 10%-to-90% differential output rise time				5	
t_f	Receiver 90%-to-10% differential output fall time				5	
$t_{SK(P)}$	Receiver differential output pulse skew, $\lvert t_{PHL} - t_{PLH}\rvert$				4.5	
t_{en}	Receiver enable time	Driver enabled, See 図 7-7			15	ns
		Driver disabled, See 図 7-8			6	μs
t_{dis}	Receiver disable time	Driver enabled, See 図 7-7			20	ns

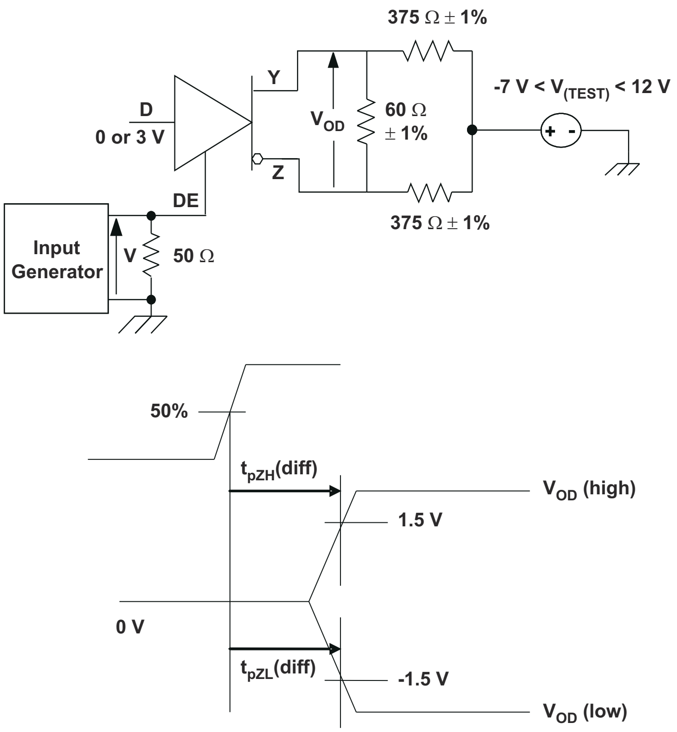


図 6-1. Driver Enable Time From DE to V_{OD}

The time t_{pZL}(x) is the measure from DE to V_{OD}(x). V_{OD} is valid when it is greater than 1.5 V.

6.8 Typical Characteristics

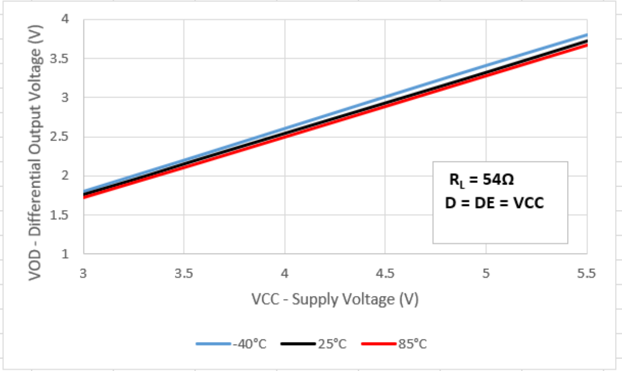


図 6-2. Differential Output Voltage vs Supply Voltage

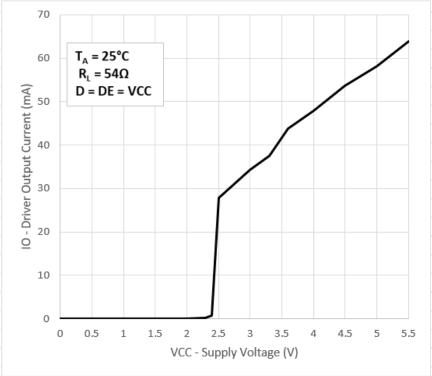


図 6-3. Driver Output Current vs Supply Voltage

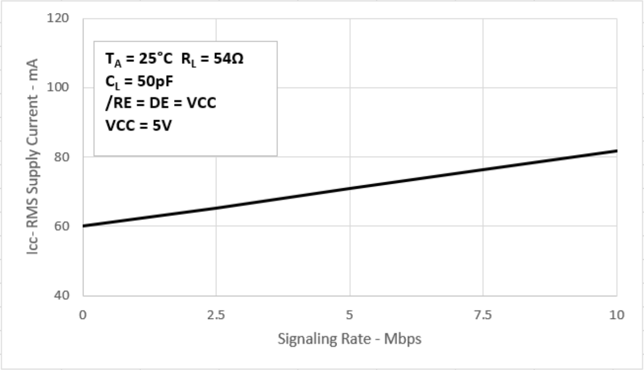


図 6-4. RMS Supply Current vs Signaling Rate

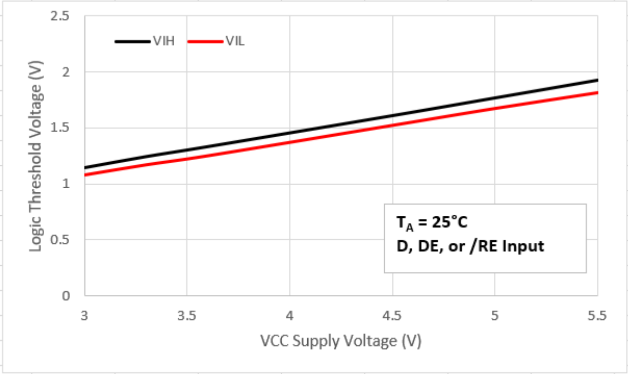


図 6-5. Logic Input Threshold Voltage vs Supply Voltage

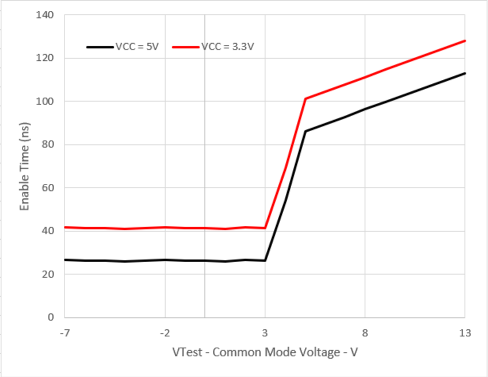


図 6-6. Enable Time vs Common-Mode Voltage (See 図 6-1)

7 Parameter Measurement Information

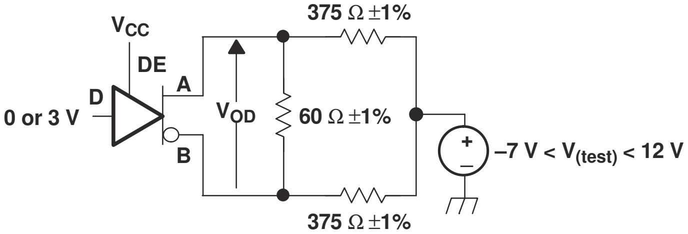
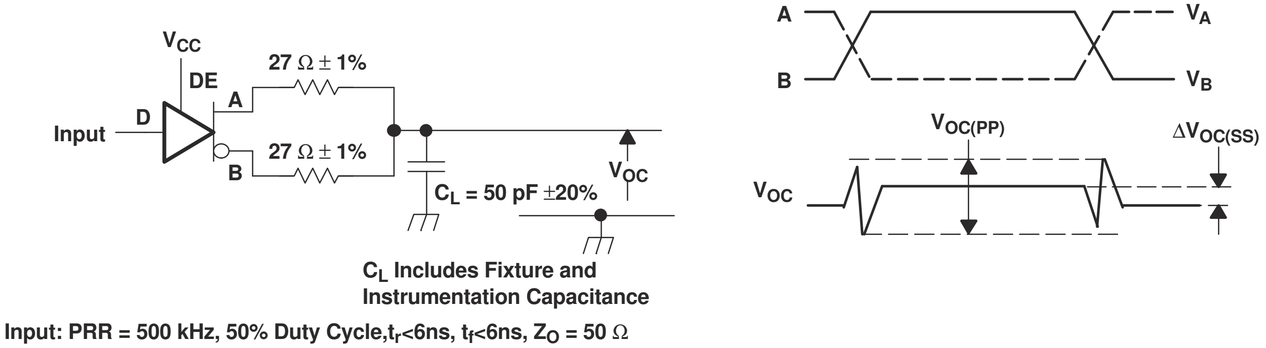
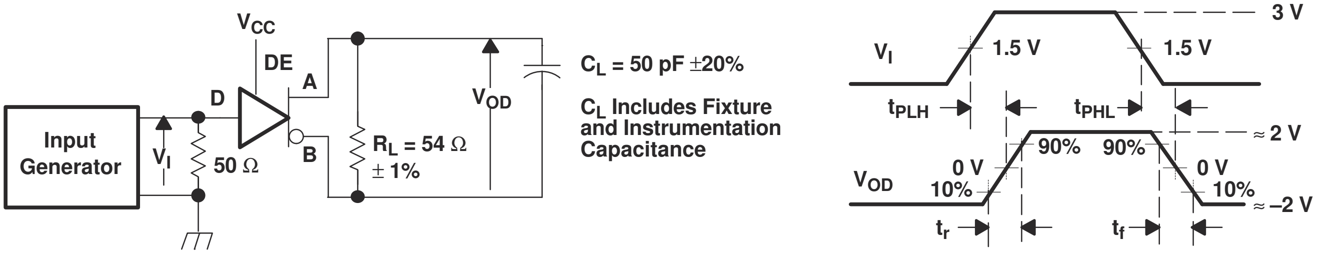


図 7-1. Driver V_{OD} With Common-Mode Loading Test Circuit



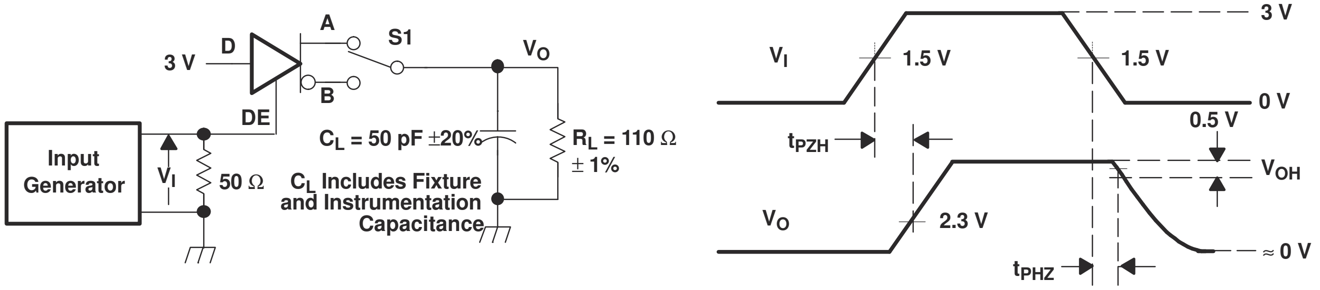
Input: PRR = 500 kHz, 50% Duty Cycle,t_r<6ns, t_f<6ns, Z_O = 50 Ω

図 7-2. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



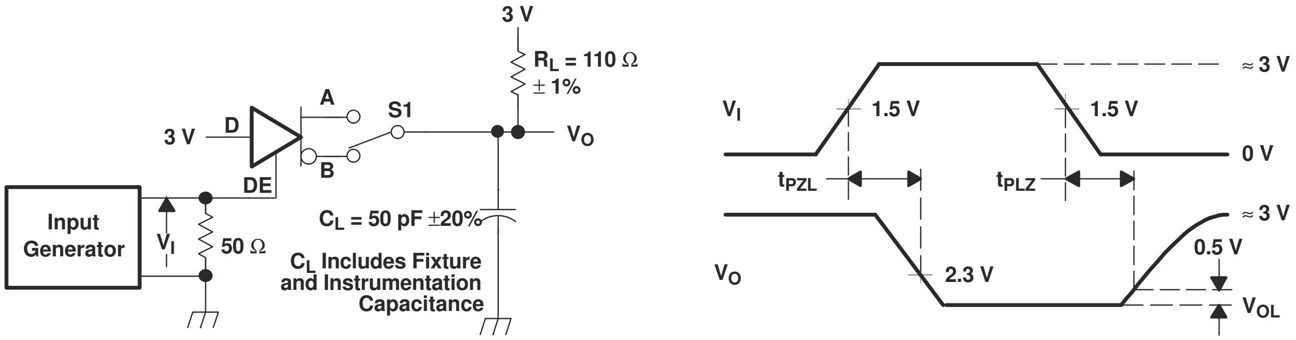
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

図 7-3. Driver Switching Test Circuit and Voltage Waveforms



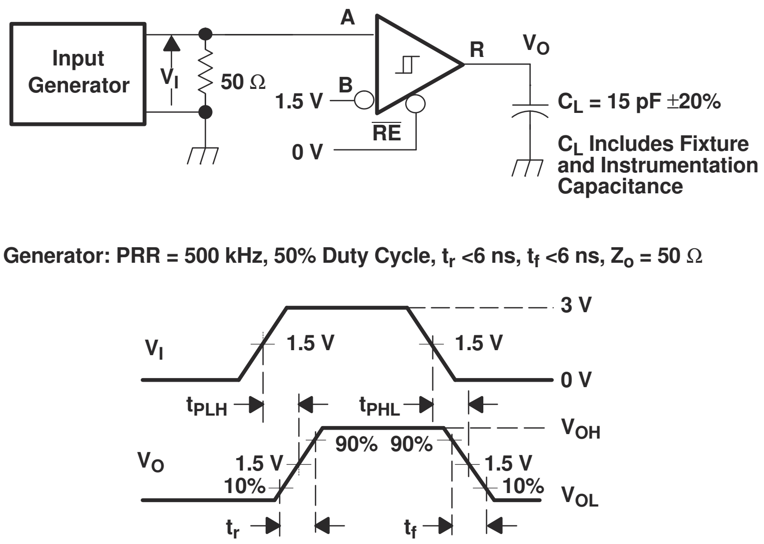
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

図 7-4. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

図 7-5. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

図 7-6. Receiver Switching Test Circuit and Voltage Waveforms

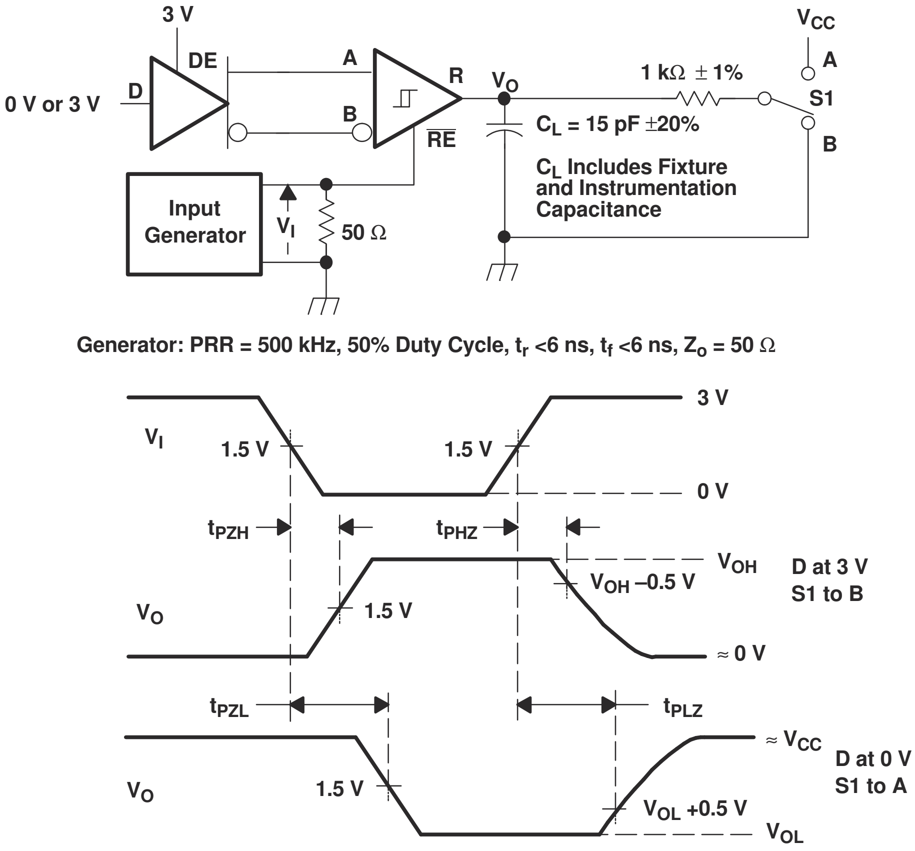


図 7-7. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

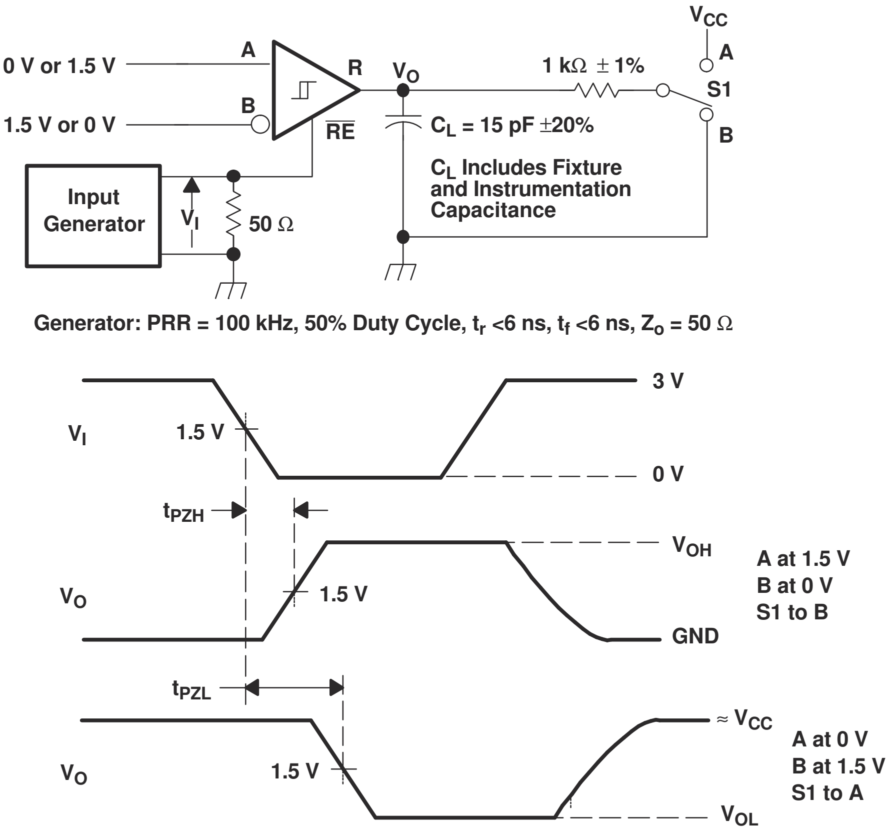


図 7-8. Receiver Enable Time From Standby (Driver Disabled)

8 Detailed Description

8.1 Overview

The SNx5HVD08 is a 3-V to 5.5-V, half-duplex, RS-485 transceiver suitable for data transmission up to 10 Mbps.

This device has an active-high driver enable and active-low receiver enable. A standby current of less than 5 µA can be achieved by disabling both driver and receiver.

Device operation is specified over a wide temperature range from -40°C to +85°C.

8.2 Functional Block Diagram

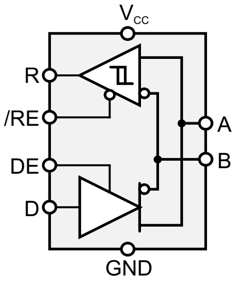


図 8-1. Logic Diagram (Positive)

8.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16 kV Human Body Model (HBM) electrostatic discharges and all other pins up to ±4 kV.

The SNx5HVD08 provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions, and a typical receiver hysteresis of 35 mV.

8.4 Device Functional Modes

表 8-1. Function Table: Driver

INPUT	ENABLE	OUTPUTS	
D	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

表 8-2. Function Table: Receiver

DIFFERENTIAL INPUTS	ENABLE(1)	OUTPUT(1)
$V_{ID} = V_A - V_B$	**$\overline{RE}$**	**R**
$V_{ID} \leq -0.2$ V	L	L
$-0.2\text{ V} < V_{ID} < -0.01$ V	L	?
$-0.01\text{ V} \leq V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

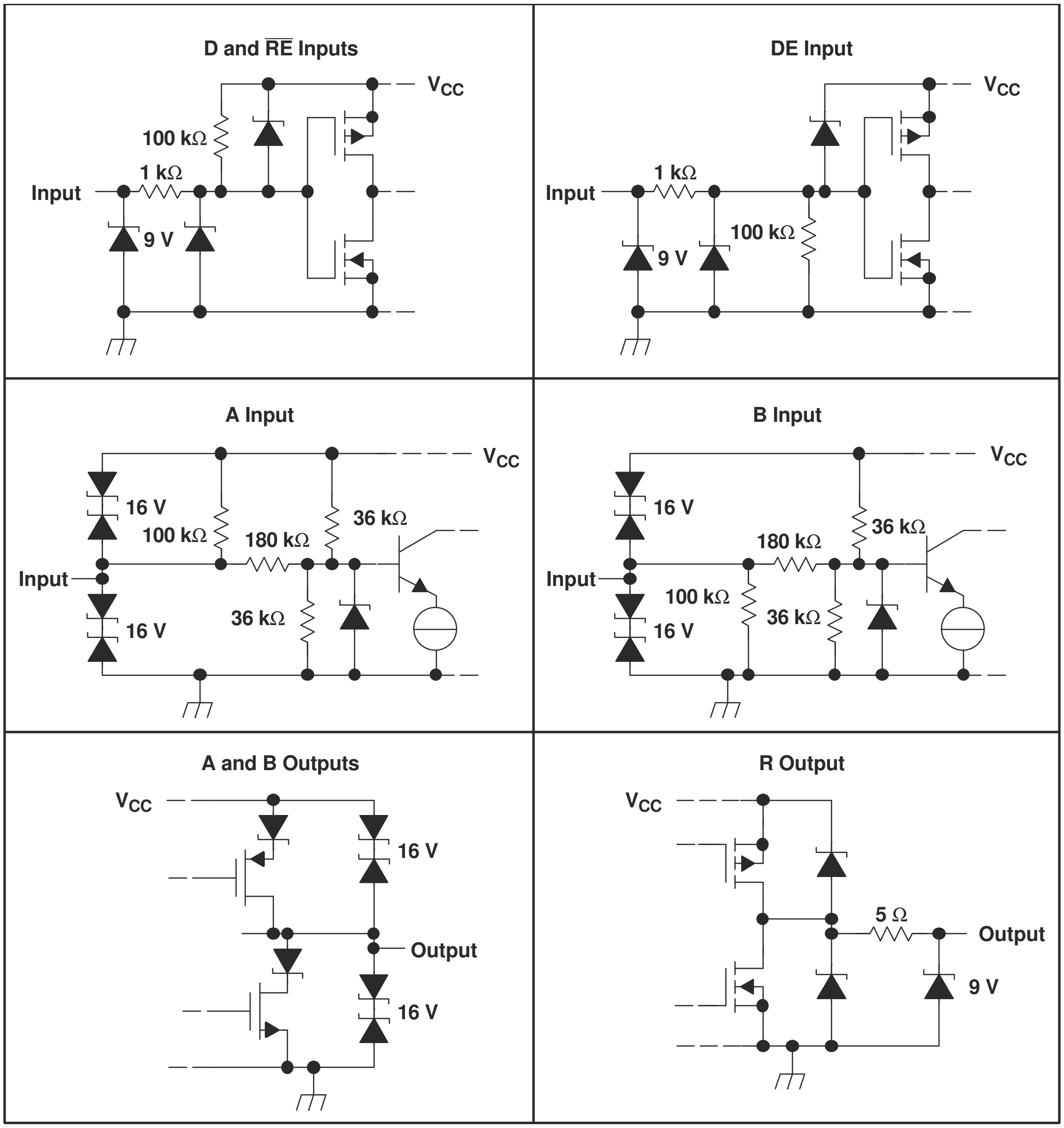


図 8-2. Equivalent Input and Output Schematic Diagrams

9 Application and Implementation

9.1 Application Information

As electrical loads are physically distanced from their power source, the effects of supply and return line impedance and the resultant voltage drop must be accounted. If the supply regulation at the load cannot be maintained to the circuit requirements, it forces the use of remote sensing, additional regulation at the load, bigger or shorter cables, or a combination of these. The SN65HVD08 eases this problem by relaxing the supply requirements to allow for more variation in the supply voltage over typical RS-485 transceivers.

9.1.1 Supply Source Impedance

In the steady state, the voltage drop from the source to the load is simply the wire resistance times the load current as modeled in 図 9-1.

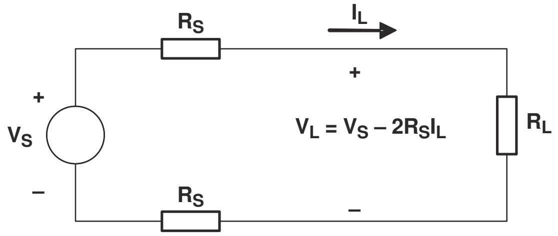


図 9-1. Steady-State Circuit Model

For example, if you were to provide 5-V ±5% supply power to a remote circuit with a maximum load requirement of 0.1 A (one SN65HVD08), the voltage at the load would fall below the 4.5-V minimum of most 5-V circuits with as little as 5.8 m of 28-GA conductors. 表 9-1 summarizes wire resistance and the length for 4.5 V and 3 V at the load with 0.1 A of load current. The maximum lengths would scale linearly for higher or lower load currents.

表 9-1. Maximum Cable Lengths for Minimum Load Voltages at 0.1 A Load

WIRE SIZE	RESISTANCE	4.5-V LENGTH AT 0.1 A	3-V LENGTH AT 0.1 A
28 Gauge	0.213 Ω/m	5.8 m	41.1 m
24 Gauge	0.079 Ω/m	15.8 m	110.7 m
22 Gauge	0.054 Ω/m	23.1 m	162.0 m
20 Gauge	0.034 Ω/m	36.8 m	257.3 m
18 Gauge	0.021 Ω/m	59.5 m	416.7 m

Under dynamic load requirements, the distributed inductance and capacitance of the power lines may not be ignored and decoupling capacitance at the load is required. The amount depends upon the magnitude and frequency of the load current change but, if only powering the SN65HVD08, a 0.1 µF ceramic capacitor is usually sufficient.

9.1.2 Opto-Isolated Data Buses

Long RS-485 circuits can create large ground loops and pick up common-mode noise voltages in excess of the range tolerated by standard RS-485 circuits. A common remedy is to provide galvanic isolation of the data circuit from earth or local grounds.

Transformers, capacitors, or phototransistors most often provide isolation of the bus and the local node. Transformers and capacitors require changing signals to transfer the information over the isolation barrier and phototransistors (opto-isolators) can pass steady-state signals. Each of these methods incurs additional costs and complexity, the former in clock encoding and decoding of the data stream and the latter in requiring an isolated power supply.

Quite often, the cost of isolated power is repeated at each node connected to the bus as shown in 図 9-2. The possibly lower-cost solution is to generate this supply once within the system and then distribute it along with the data line(s) as shown in 図 9-3.

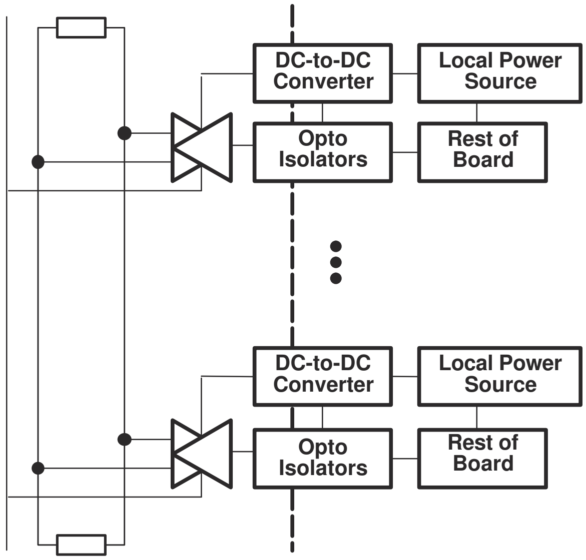


図 9-2. Isolated Power at Each Node

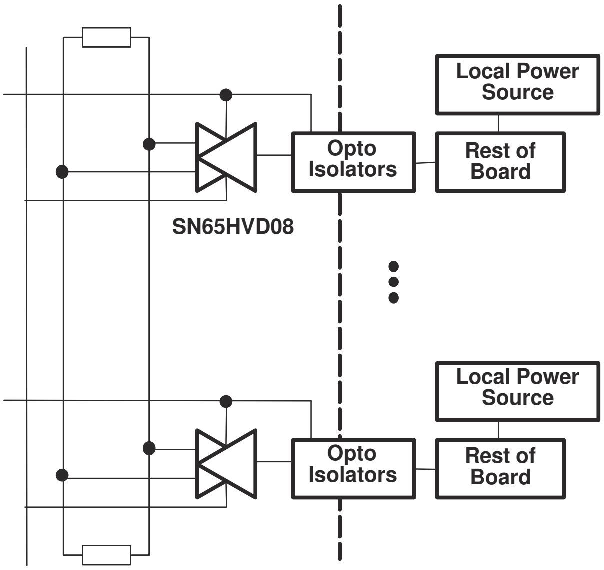


図 9-3. Distribution of Isolated Power

The features of the SN65HVD08 are particularly good for the application of 図 9-3. Due to added supply source impedance, the low quiescent current requirements and wide supply voltage tolerance allow for the poorer load regulation.

9.1.3 Opto Alternative

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80 Mbps. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high-voltage 0.4-pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6 kV/ms.

ISO150 avoids the problems commonly associated with opto-couplers. Optically-isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25 mW per channel with supply voltage range matching that of the SN65HVD08 of 3 V to 5.5 V.

図 9-4 shows a typical circuit.

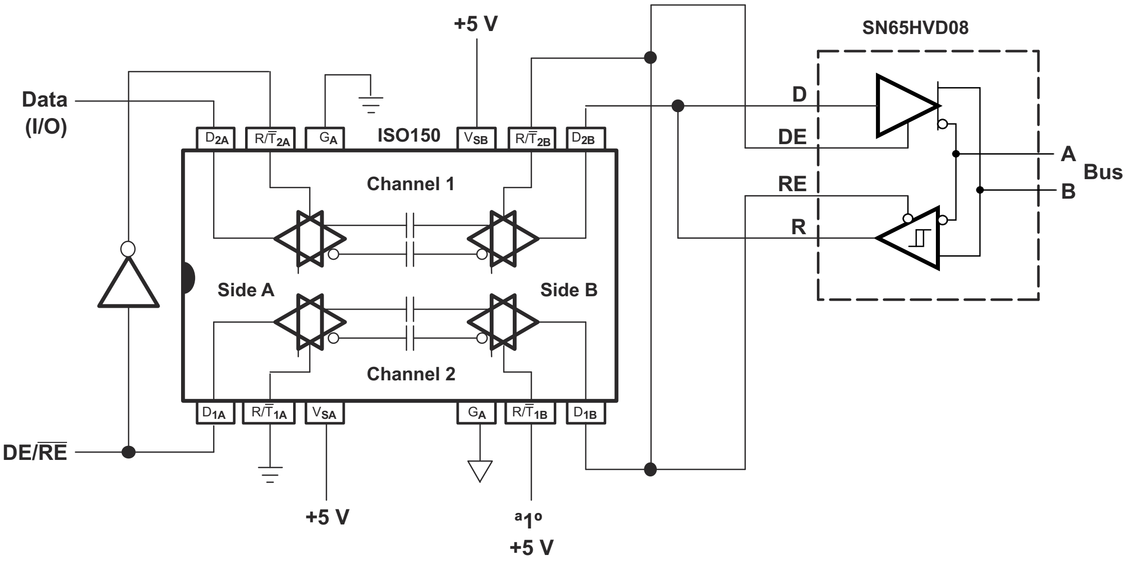


図 9-4. Isolated RS-485 Interface

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

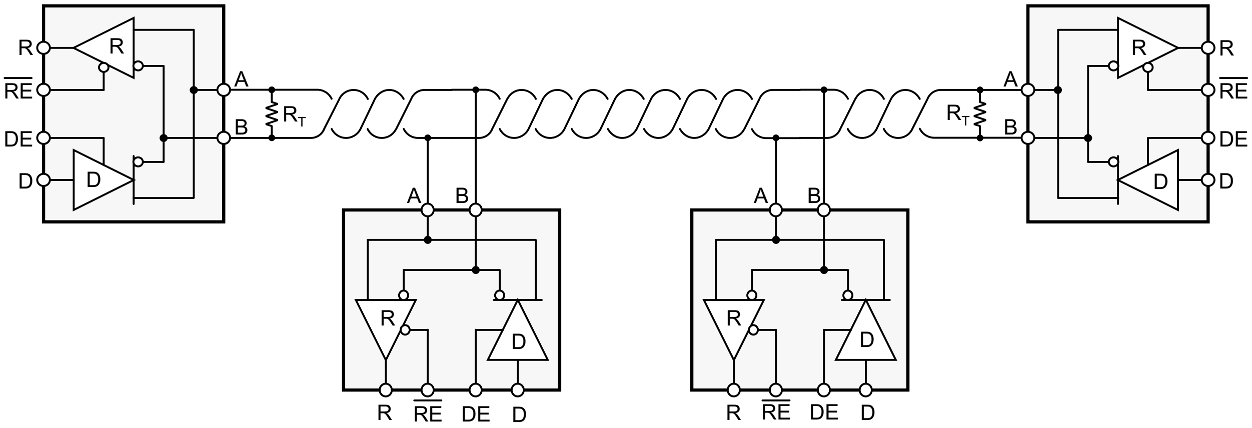


図 9-5. Typical Application Diagram

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

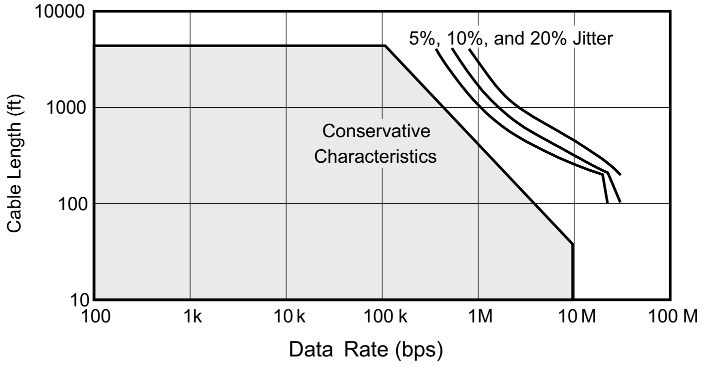


図 9-6. Cable Length vs Data Rate Characteristic

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \tag{1}$$

Where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

Per 式 1, the maximum recommended stub length for the minimum driver output rise time of the SNx5HVD08 for a signal velocity of 78% is 0.23 meters (0.75 feet).

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD08 and SN75HVD08 are each 1/8 UL transceivers, it is possible to connect up to 256 receivers to the bus.

9.2.1.4 Receiver Failsafe

The differential receivers of the SNx5HVD08 family are “failsafe” to invalid bus states caused by:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the “input indeterminate” range does not include zero volts differential.

In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input VID is more positive than +200 mV, and must output a Low when VID is more negative than -200 mV. The receiver parameters which determine the failsafe performance are VIT(+) and VIT(-).

As shown in the Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output, and differential signals more positive than -10 mV will always cause a High receiver output. Thus, when the differential input signal is close to zero, it is still above the maximum VIT(+) threshold of -10 mV, and the receiver output will be High.

9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

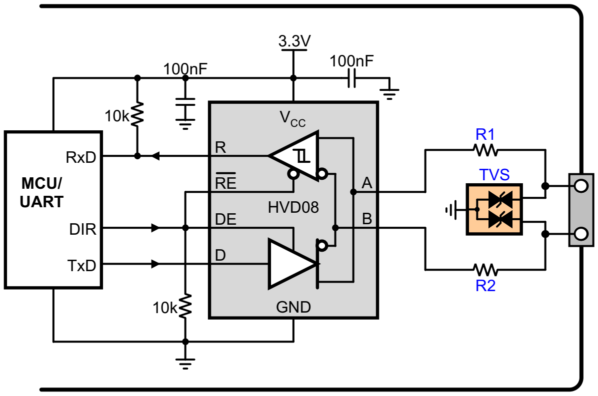


図 9-7. Transient protection against ESD, EFT, and Surge transients

図 9-7 suggests a protection circuit against 10 kV ESD (IEC 61000-4-2), 4 kV EFT (IEC 61000-4-4), and 1 kV surge (IEC 61000-4-5) transients. 表 9-2 shows the associated Bill of Materials.

表 9-2. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3 V to 5 V, 10 Mbps RS-485 Transceiver	SNx5HVD08	TI
R1, R2	10 Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400 W Transient Suppressor	CDSOT23-SM712	Bourns

9.2.3 Application Curve

図 9-8 demonstrates operation of the SN65HVD08 at a signaling rate of 10 Mbps.

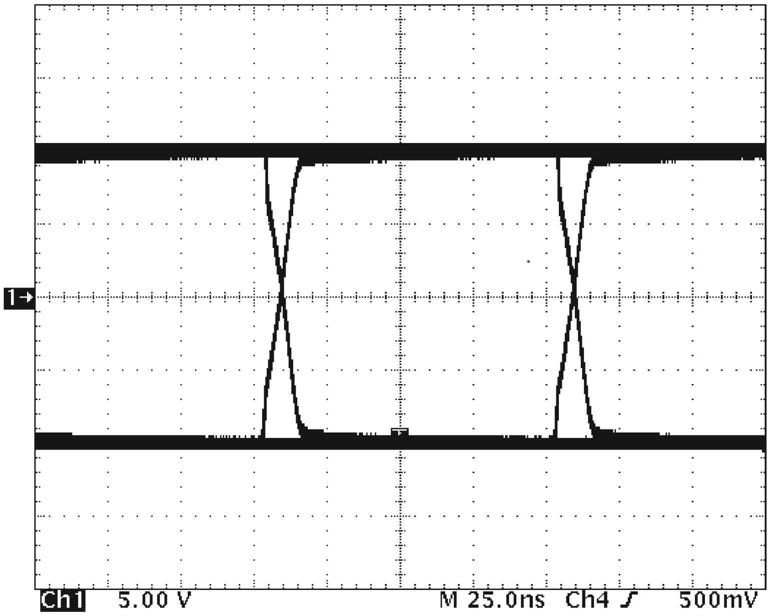


図 9-8. SNx5HVD08 Differential Output Waveform

9.3 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76333 and TPS76350 are linear voltage regulators suitable for 3.3 V and 5 V supplies respectively.

9.4 Layout

9.4.1 Layout Guidelines

On-chip IEC-ESD protection is sufficient for laboratory and portable equipment but insufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use VCC and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC-pins of transceiver, UART, or controller ICs on the board.
5. Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

9.4.2 Layout Example

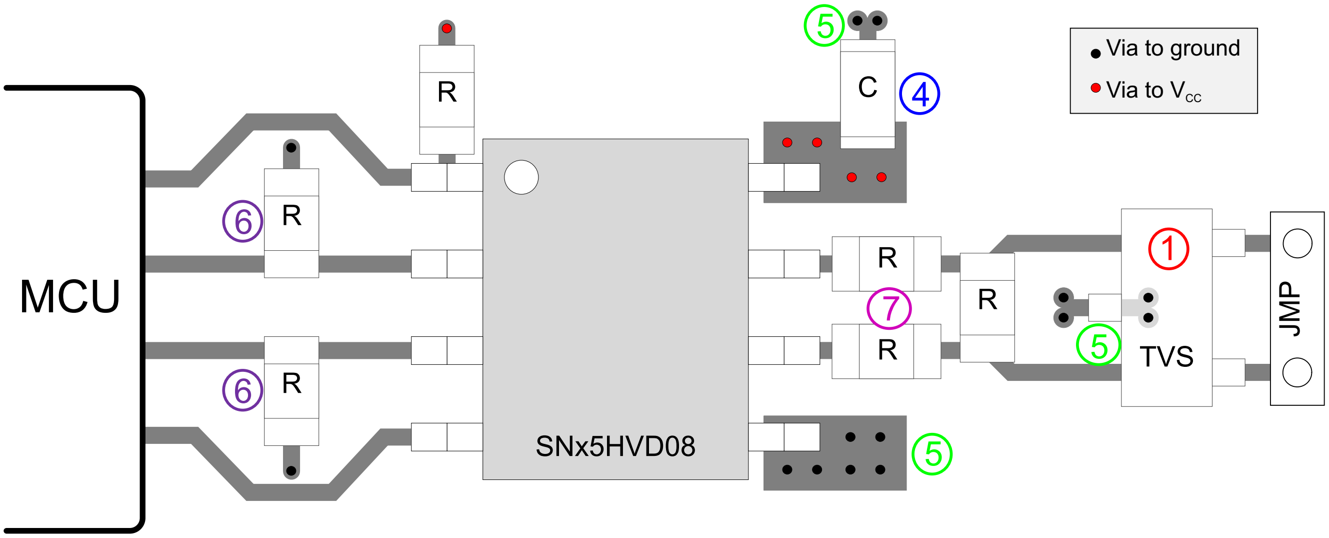


図 9-9. SNx5HVD08 Layout example

10 Device and Documentation Support

10.1 Device Support

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10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD08D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP08
SN65HVD08DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP08
SN65HVD08DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP08
SN65HVD08DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP08
SN65HVD08P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD08
SN65HVD08P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD08
SN75HVD08D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN08
SN75HVD08DR	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN08
SN75HVD08P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75HVD08
SN75HVD08P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75HVD08

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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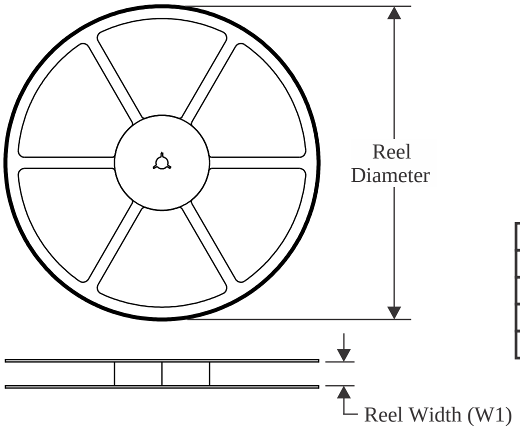
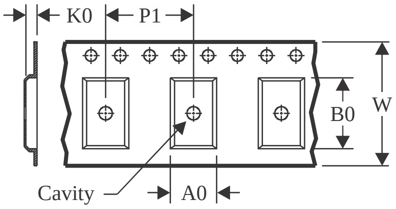
TAPE AND REEL INFORMATION

REEL DIMENSIONS

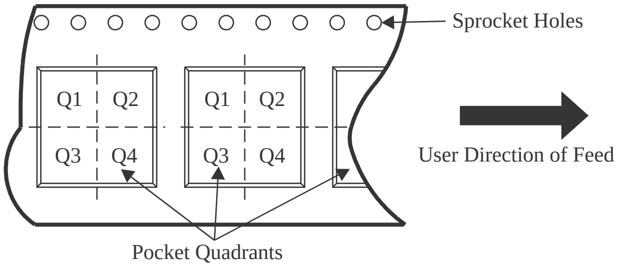


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

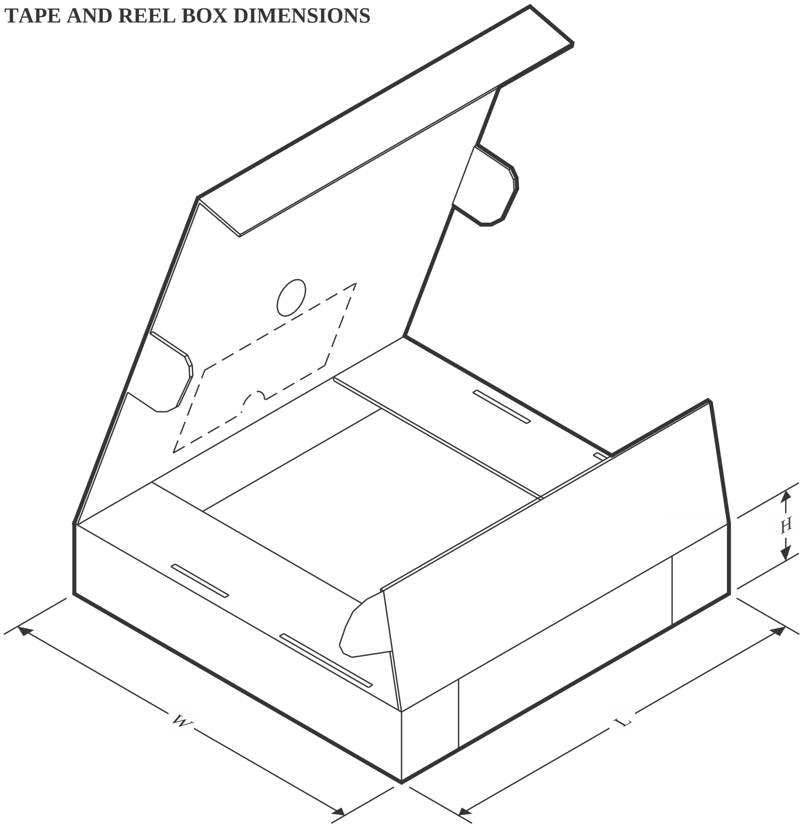
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD08DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

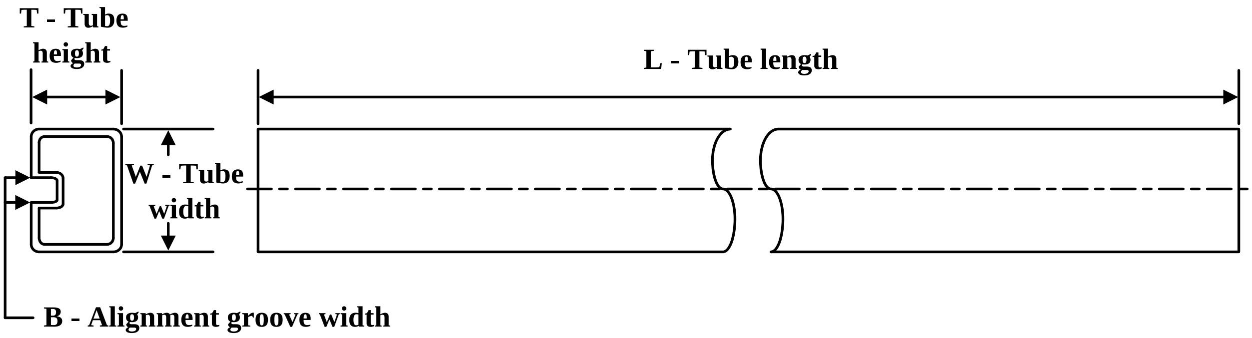
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

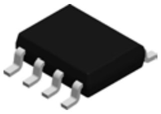
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD08DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD08P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD08P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75HVD08P	P	PDIP	8	50	506	13.97	11230	4.32
SN75HVD08P.A	P	PDIP	8	50	506	13.97	11230	4.32

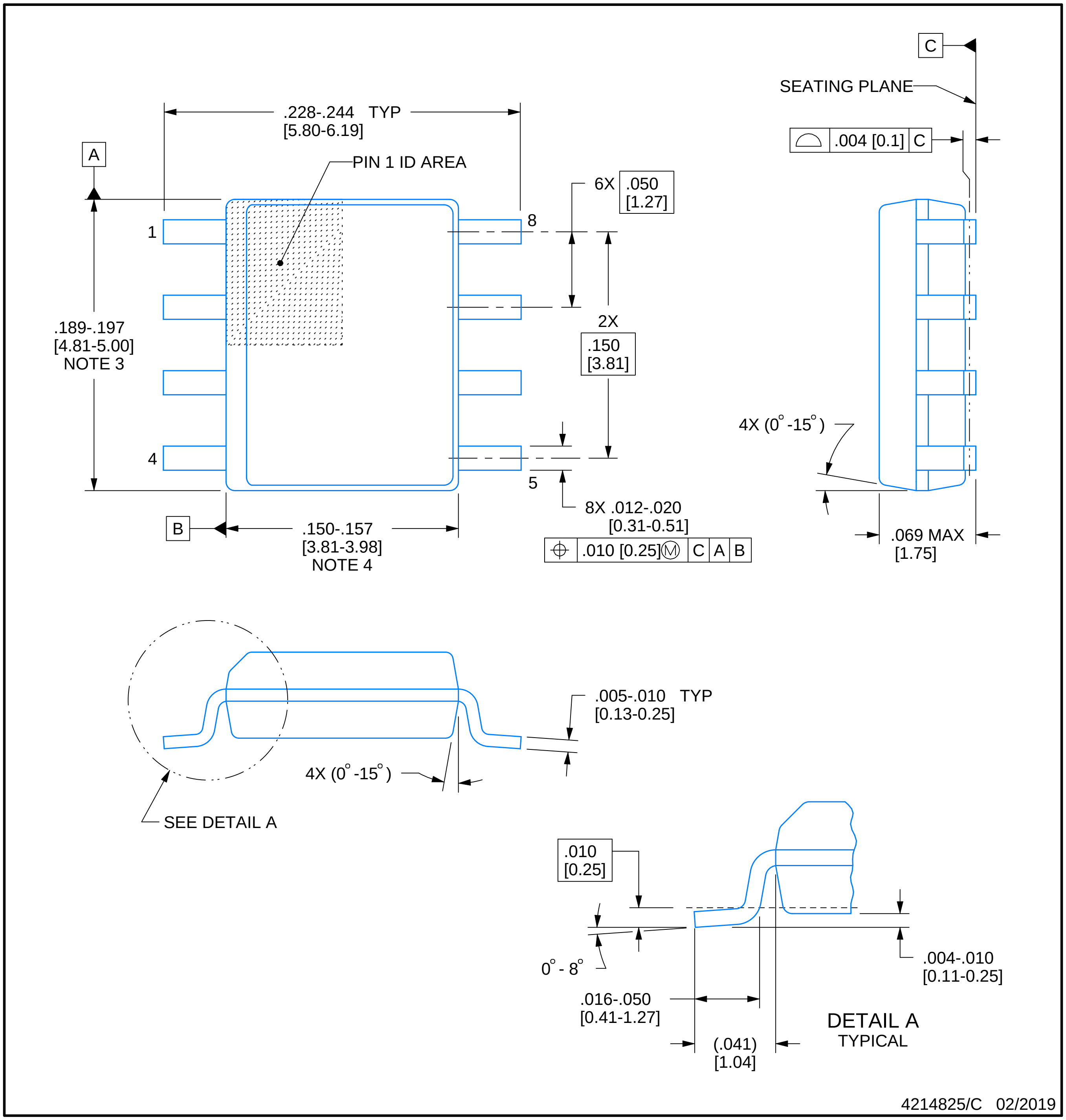


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

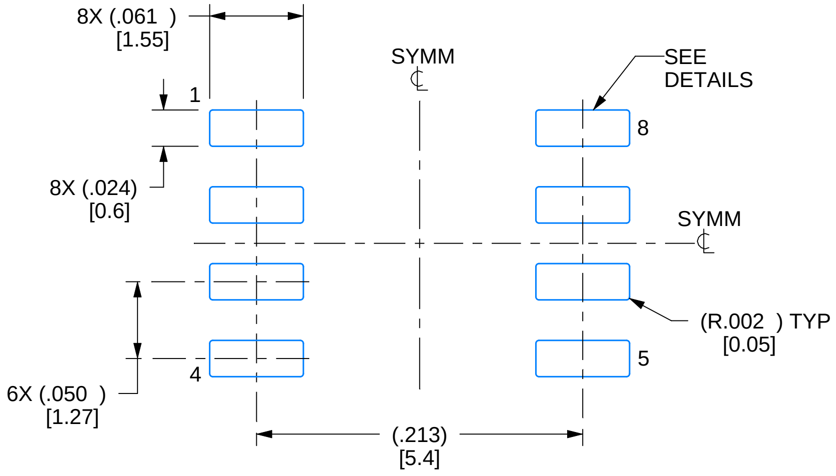
SMALL OUTLINE INTEGRATED CIRCUIT



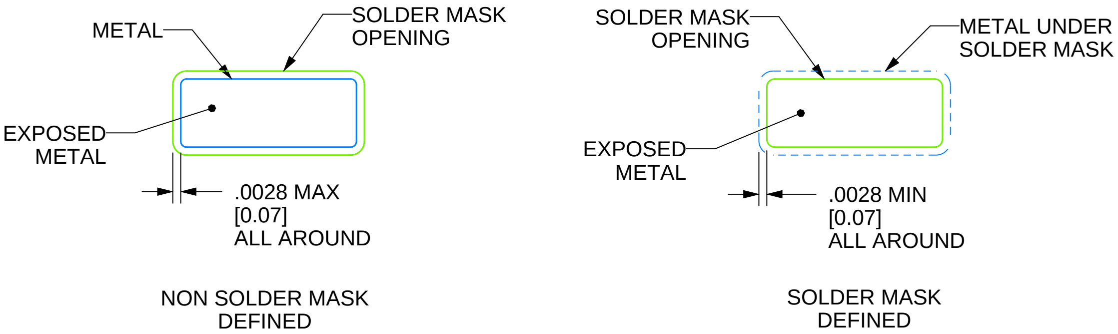
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



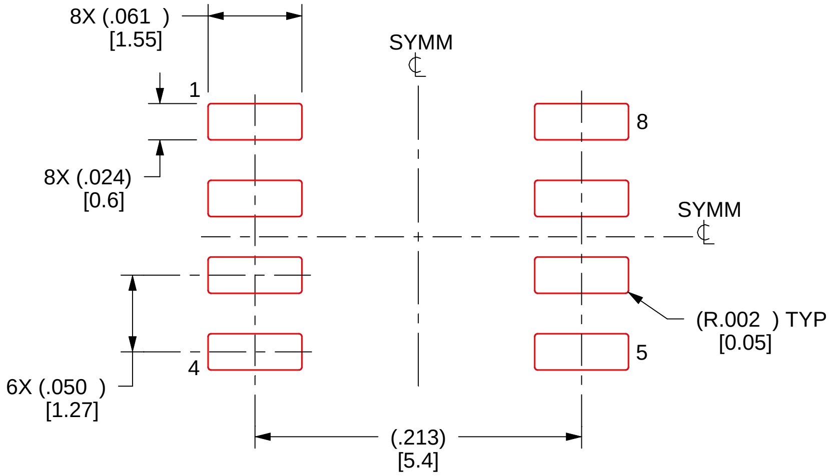
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

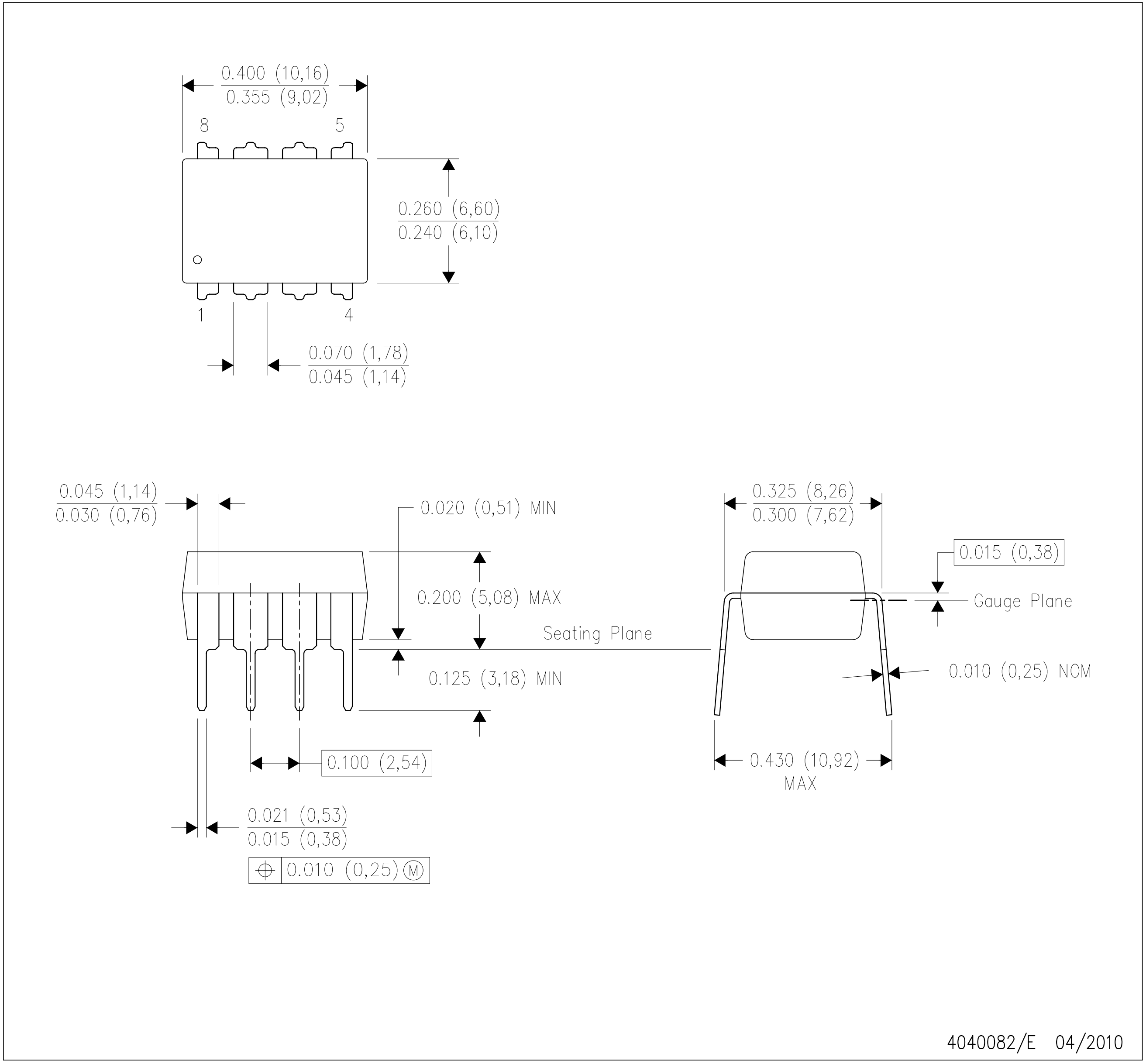


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

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