SN55LVRA4-SEP クワッド チャネル高速差動レシーバ

1 特長

- ベンダー品目の図面利用可能
- 総吸収線量(TID)特性:30krad(Si)
  - ウェハー ロットごとに 30krad (Si) までの累積線量耐性放射線ロット受け入れ試験 (TID RLAT)
- シングル イベント効果 (SEE) 特性:
  - シングル イベント ラッチアップ (SEL) 耐性:線エネルギー付与 (LET) = 43MeV-cm2/mg
  - シングル イベント過渡 (SET) 特性:43MeV-cm2/mg。
- 400Mbps の信号速度
- 3.3V 単一電源電圧で動作
- -4V~5V 拡張同相入力電圧範囲
- 同相入力電圧範囲全体にわたり、差動入力のスレッショルドは±50mV 未満で、ヒステリシスは 50mV です
- TIA/EIA-644(LVDS)に準拠
- アクティブなフェイルセーフにより、入力がなくても高レベル出力が保証され、パワーダウン時には入力がハイインピーダンスに維持されます。
- 15kV HBM を超えるバス ピンの ESD 保護
- TTL 制御入力は 5V 耐圧
- 宇宙向け強化プラスチック (SEP)
  - 管理されたベースライン
  - 金 ワイヤ、NiPdAu リード仕上げ
  - 1 つのアセンブリ / テスト拠点と 1 つの製造拠点
  - 長期にわたる製品ライフ サイクル
  - 軍用温度範囲:-55℃～125℃
  - 製品のトレーサビリティ
  - NASA ASTM E595 アウトガス仕様に適合

2 アプリケーション

- 低軌道 (LEO) 衛星システム
- コマンドとデータの処理 (C&DH)
- 通信ペイロード
- 光学画像処理ペイロード
- レーダー画像処理ペイロード

3 概要

SN55LVRA4-SEP は、業界で最も広い同相入力電圧範囲を提供します。これらのレシーバは、5V の PECL 信号と互換性のある入力電圧範囲仕様と全体的に向上したグランドノイズ耐性を提供します。

SN55LVRA4-SEP にはフェイルセーフ回路が内蔵されており、入力信号が損した後 60ns 以内に高レベル出力を供給します。信号ロスの主な原因は、ケーブルの断線、回線のショート、トランスミッタのパワーダウンです。フェイルセーフ回路により、これらのフォルト状態でノイズが有効なデータとして受信されることを防止します。

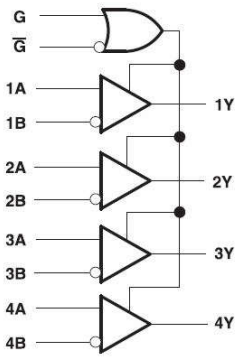
これらのデバイスの意図された用途と信号伝達手法は、約 100Ω の制御されたインピーダンス媒体にわたるポイントツーポイントのベースバンドデータ伝送です。伝送媒体にはプリント基板のトレース、バックプレーン、ケーブルを使用できます。データ転送の最高速度および最大距離は、メディアの減衰特性と周囲からのノイズに依存します。

SN55LVRA4-SEP は、-55℃～125℃の温度範囲の動作で特徴づけられています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
SN55LVRA4-SEP	D (SOIC、16)	9.90mm × 3.91mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)

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4 Pin Configuration and Functions

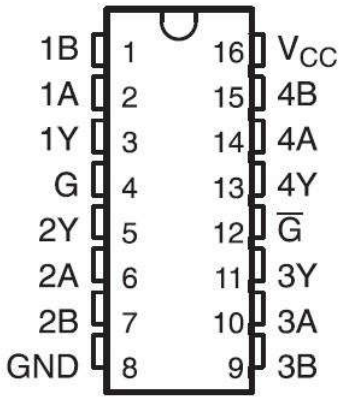

図 4-1. D Package 16-Pin, SOIC (Top View)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	16	P	Supply voltage
GND	8	G	Ground
1A	2	I	Differential (LVDS) non-inverting input
1B	1	I	Differential (LVDS) inverting input
1Y	3	O	LVTTL output signal
2A	6	I	Differential (LVDS) non-inverting input
2B	7	I	Differential (LVDS) inverting input
2Y	5	O	LVTTL output signal
3A	10	I	Differential (LVDS) non-inverting input
3B	9	I	Differential (LVDS) inverting input
3Y	11	O	LVTTL output signal
4A	14	I	Differential (LVDS) non-inverting input
4B	15	I	Differential (LVDS) inverting input
4Y	13	O	LVTTL output signal
G	4	I	Enable (HI = ENABLE)
G/	12	I	Enable (LO = ENABLE)

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage (V_{CC})		–0.5	4	V
Input Voltage (A or B)		–5	6	V
Input Voltage (G, $\overline{G}$)		–0.5	VCC + 0.4	V
Differential Voltage |A - B| for LVDS		0	3	V
Output Voltage (R_{OUT})		–0.5	4	V
Lead Temperature Range Soldering	(4 sec.)		260	°C
Junction Temperature		-55	140	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended* Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, and performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (3.3 V mode)	3.0	3.3	3.6	V
V_{IH}	High-level input voltage (G, $\overline{G}$)	2		5	V
V_{IL}	Low-level input voltage (G, $\overline{G}$)	0		0.8	V
$\|V_{ID}\|$	Magnitude of Receiver input voltage (LVDS)	0.1		3.0	V
V_I or V_{CM}	Voltage at any LVDS terminal (separately or common-mode)	-4		+5	V
T_A	Operating free-air temperature	-55		125	°C
T_{PCB}	PCB temperature (Standard)	-55		128	°C
T_J	Junction temperature (Standard)	-55		135	°C

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT1}	Positive-going differential input voltage threshold	V_{IB} = -4V or 5V, V_{CC} = 3.0V to 3.6V, See 図 6-2			50	mV
V_{IT2}	Negative-going differential input voltage threshold		-50			
V_{IT3}	Differential input failsafe voltage threshold	V_{CC} = 3.0V to 3.6V See 図 6-2 and 図 6-5	–32		–100	mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT1} – V_{IT2}$	V_{CC} = 3.0V to 3.6V		50		mV
V_{CM_RANGE}	Input common mode voltage range	VCC = 3.0V to 3.6V	-4	1.2	5	V
V_{OH}	High-level output voltage	I_{OH} = –4mA, V_{CC} = 3.0V to 3.6V	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA, V_{CC} = 3.0V to 3.6V			0.4	V
I_{CC}	Supply current	G at V_{CC}, No load, Steady-state VID=200mV/-200mV, V_{CC} = 3.0V to 3.6V		16	25	mA
		Disable and in deep sleep (Disable for >100us), G at GND, V_{CC} = 3.0V to 3.6V		1.1	6	
I_I	Input current (A or B inputs)	V_I = 0V, Other input open	-25		25	µA
I_I	Input current (A or B inputs)	V_I = 2.4V, Other input open	-25		25	µA
I_I	Input current (A or B inputs)	V_I = –4V, Other input open	-80		80	µA
I_I	Input current (A or B inputs)	V_I = 5V, Other input open	-45		45	µA
I_{ID}	Differential input current ($I_{IA} – I_{IB}$)	V_{ID} = 100 mV, V_{IC} = –4V or 5V	-5		5	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_A or V_B = –4V or 5V, V_{CC} = 0V	-70		70	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_A or V_B = 0V or 2.4V, V_{CC} = 0V	-25		25	µA
V_{IH}	High-level input voltage (enables)	V_{CC} = 3.0V to 3.6V			2	V
I_{IH}	High-level input current (enables)	V_{IH} = 2V, V_{CC} 3.0V to 3.6V			15	µA
V_{IL}	Low-level input voltage (enables)	V_{CC} = 3.0V to 3.6V	.8			V
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8V, V_{CC} 3.0V to 3.6V			15	µA
I_{OZ}	High-impedance output current		–12		12	µA

(1) All typical values are at 25°C and with a 3.3 V supply.

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5.6 Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1) (2) (3)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
t_{PHL}	Differential Propagation Delay High to Low	V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10%. See 図 6-3	1.8	4	8	ns
t_{PLH}	Differential Propagation Delay Low to High		1.8	4	8	ns
t_{d1}	Delay time, failsafe deactivate time	V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10%. See 図 6-3 and 図 6-6			11	ns
t_{d2}	Delay time, failsafe activate time		0.2		2	ns
$tSK_{(p)}$	Differential Pulse Skew ($t_{PHLD} - t_{PLHD}$) (4)	V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10%. See 図 6-3		200		ps
$t_{SK(o)}$	Differential Channel-to-Channel Skew-same device (5)			150		ps
$t_{SK(pp)}$	Differential Part to Part Skew (6)				1.2	ns
t_{TPHZ}	Propagation delay time, high level-to-high impedance output	V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10% 図 6-4		5.5	12	ns
t_{TPLZ}	Propagation delay time, low level-to-high impedance output			4.4	12	ns
t_{TPZH}	Propagation delay time, high impedance to high level output			3.8	12	ns
t_{TPZL}	Propagation delay time, high impedance to low level output			7.0	12	ns
t_{TLH}	Output Rise Time	V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10%. See 図 6-3		800		ps
t_{THL}	Output Fall Time			800		ps

(1) All typicals are given for: V_{CC} = 3.3V and T_A = +25°C.
(2) C_L includes probe and jig capacitance.
(3) Generator waveform for all tests unless otherwise specified: f = 1MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.
(4) $t_{SK(p)}$ is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(5) $t_{SK(o)}$ is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
(6) $t_{SK(pp)}$, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

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5.7 Typical Characteristics

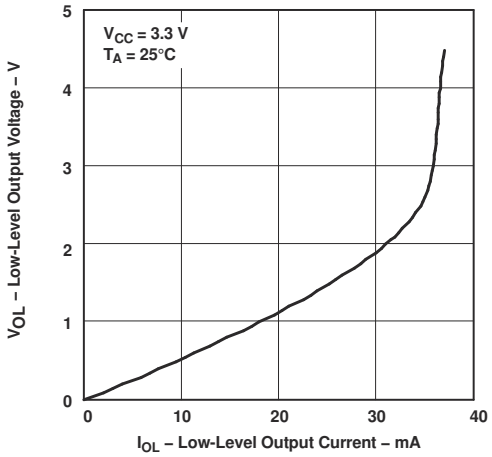

図 5-1. Low-Level Output Voltage vs Low-Level Output Current

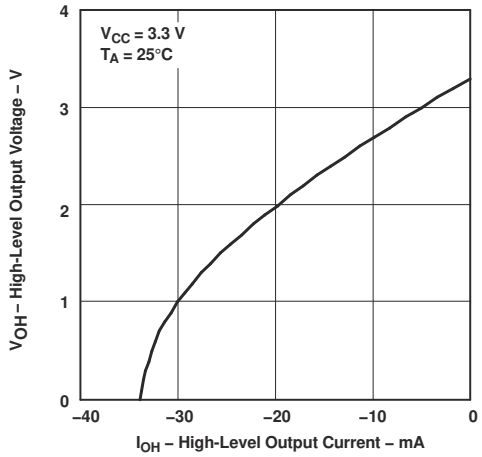

図 5-2. High-Level Output Voltage vs High-Level Output Current

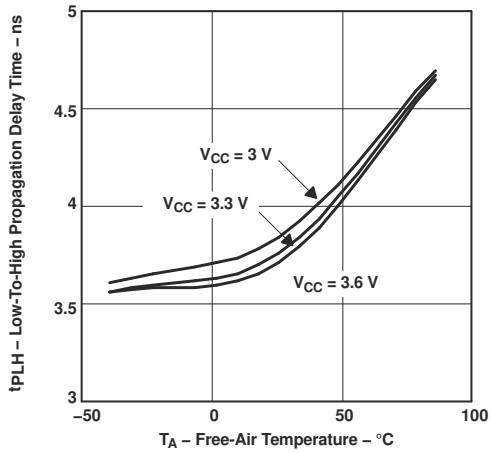

図 5-3. Low-to-High Propagation Delay Time vs Free-Air Temperature

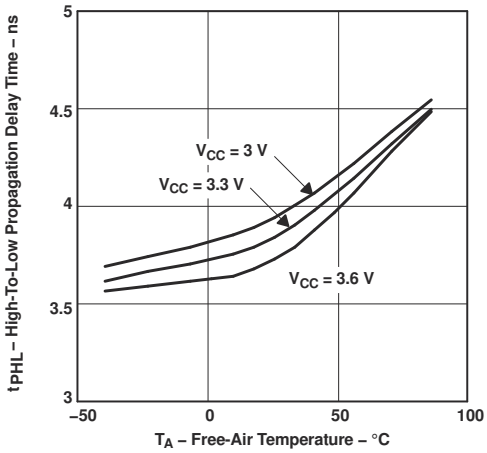

図 5-4. High-to-Low Propagation Delay Time vs Free-Air Temperature

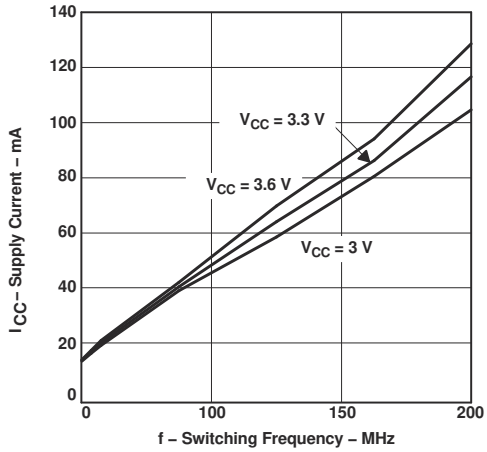

図 5-5. Supply Current vs Frequency

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6 Parameter Measurement Information

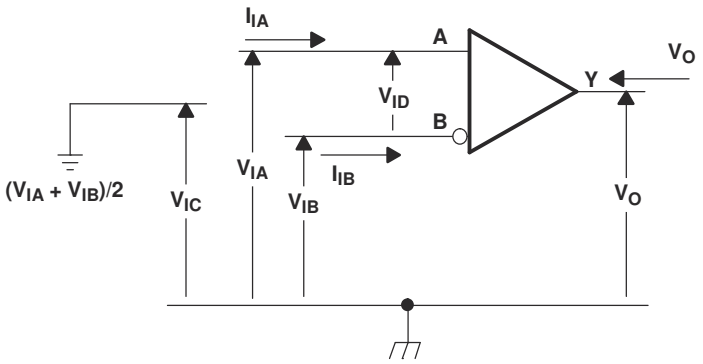
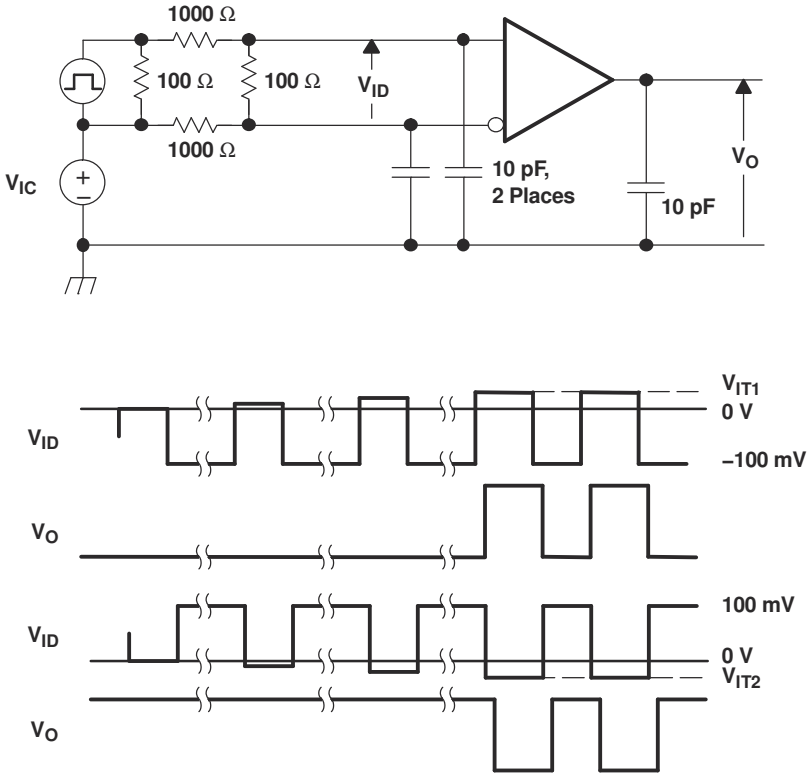
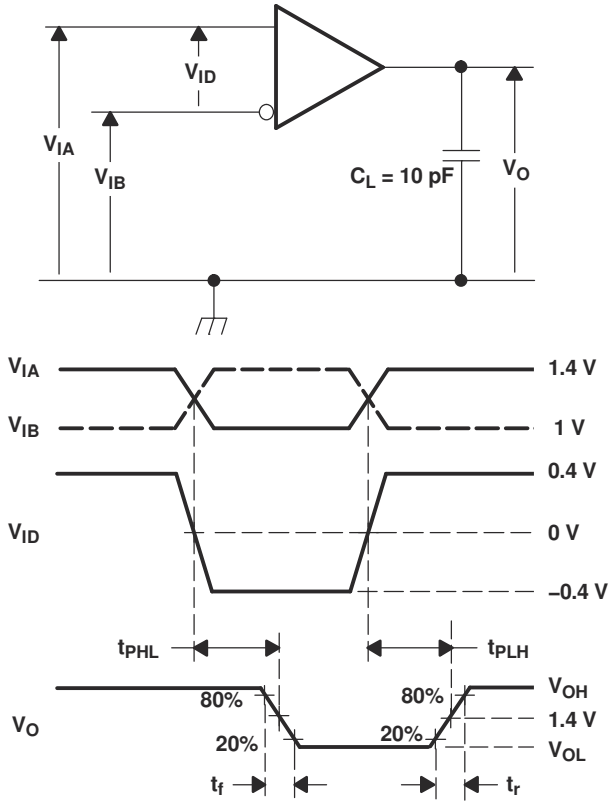


図 6-1. Voltage and Current Definitions



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

図 6-2. V_{IT1} and V_{IT2} Input Voltage Threshold Test Circuit and Definitions



All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1ns, pulse repetition rate (PRR) = 50Mpps [pps : pulse per second], pulse width = 10 ±0.2ns . C_L includes instrumentation and fixture capacitance within 0,06mm of the D.U.T.

図 6-3. Timing Test Circuit and Waveforms

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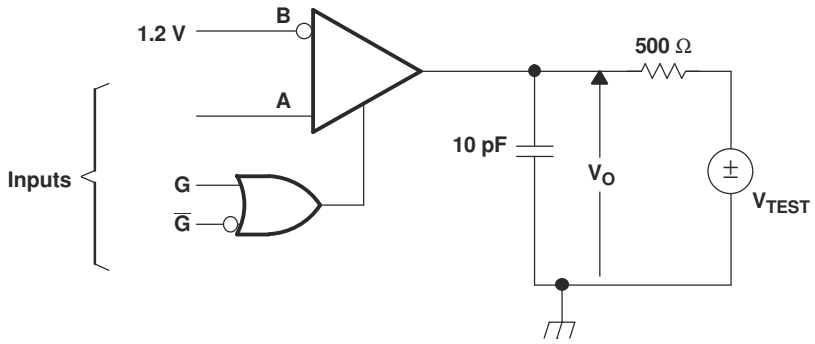

NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

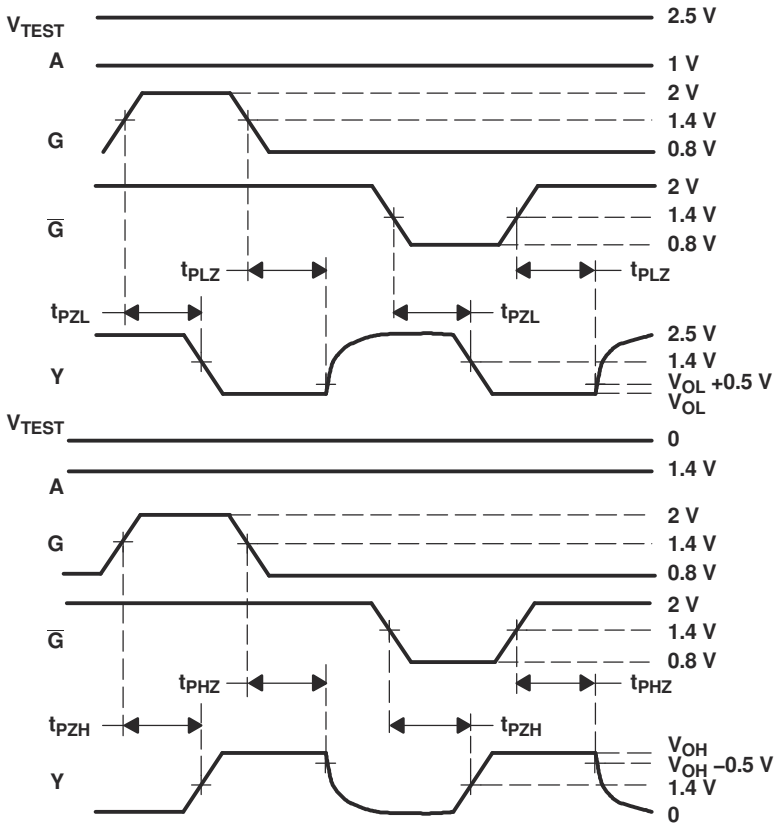

図 6-4. Enable/Disable Time Test Circuit and Waveforms

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表 6-1. Receiver Minimum and Maximum V_{IT3} Input Threshold Test Voltages

APPLIED VOLTAGES(1)		RESULTANT INPUTS		
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	Output
–4000	–3900	–100	–3950	L
–4000	–3968	–32	–3984	H
4900	5000	–100	4950	L
4968	5000	–32	4984	H

(1) These voltages are applied for a minimum of 1.5µs.

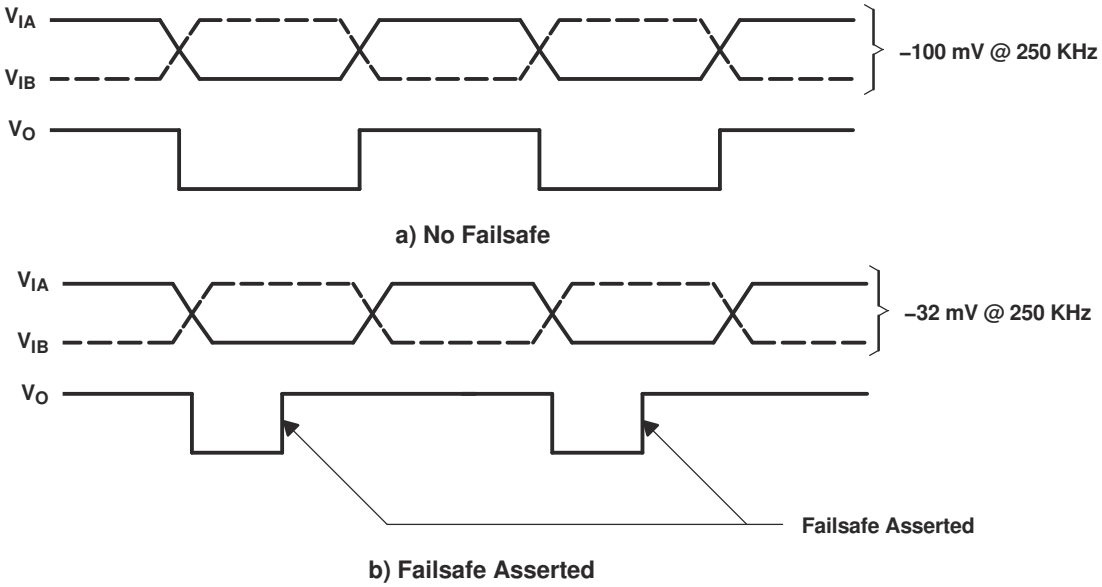

図 6-5. V_{IT3} Failsafe Threshold Test

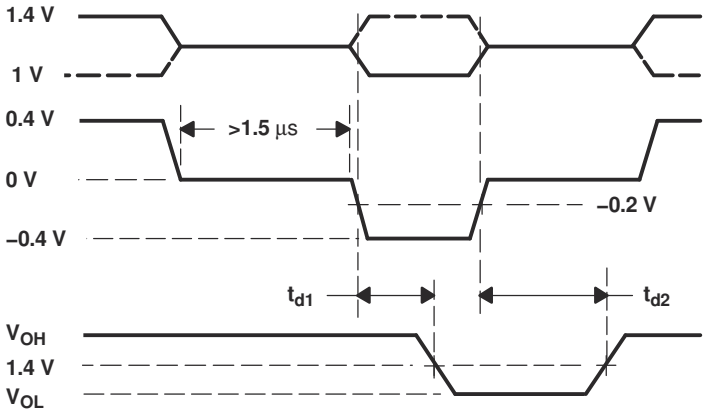

図 6-6. Waveforms for Failsafe Activate and Deactivate

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7 Detailed Description

7.1 Overview

図 7-1 shows how LVDS drivers and receivers are intended to be used primarily in a simple point-to-point configuration. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the source through a impedance controlled 100Ω differential PCB traces. Use a termination resistor of 100Ω and place it as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver.

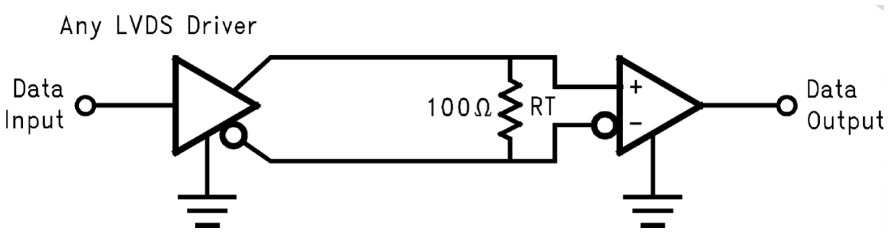
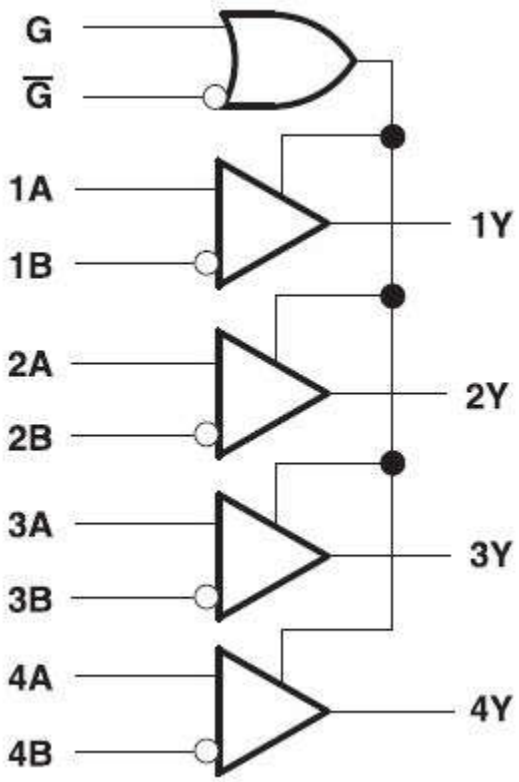


図 7-1. Application Diagram

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Receiver Output States

When the receiver differential input signal is greater than 100mV, the receiver output is high; and when the differential input voltage is below –100mV, the receiver output is low. When the input voltage is between these thresholds (for example, between –100mV and 100mV), the receiver output is indeterminate. The output state can be high or low. A special case occurs when the input to the receiver is open-circuited, which is covered in *セクション 8.3*. When the receiver is disabled, the receiver outputs are high-impedance.

7.3.2 General Purpose Comparator

While the SN55LVRA4-SEP receivers are LVDS standard-compliant receivers, utility and applications extend to a wider range of signals. As long as the input signals are within the required differential and common-mode voltage ranges mentioned above, the receiver output follows a faithful representation of the input signal.

7.3.3 Common-Mode Range vs Supply Voltage

The SN55LVRA4-SEP receivers operate over an input extended common-mode range of -4V to 5V, allowing significant amount of ground shift between transmitter and receiver. If the input common mode is anywhere within this range and has a differential magnitude greater than or equal to 100mV, the receivers correctly output the LVDS bus state.

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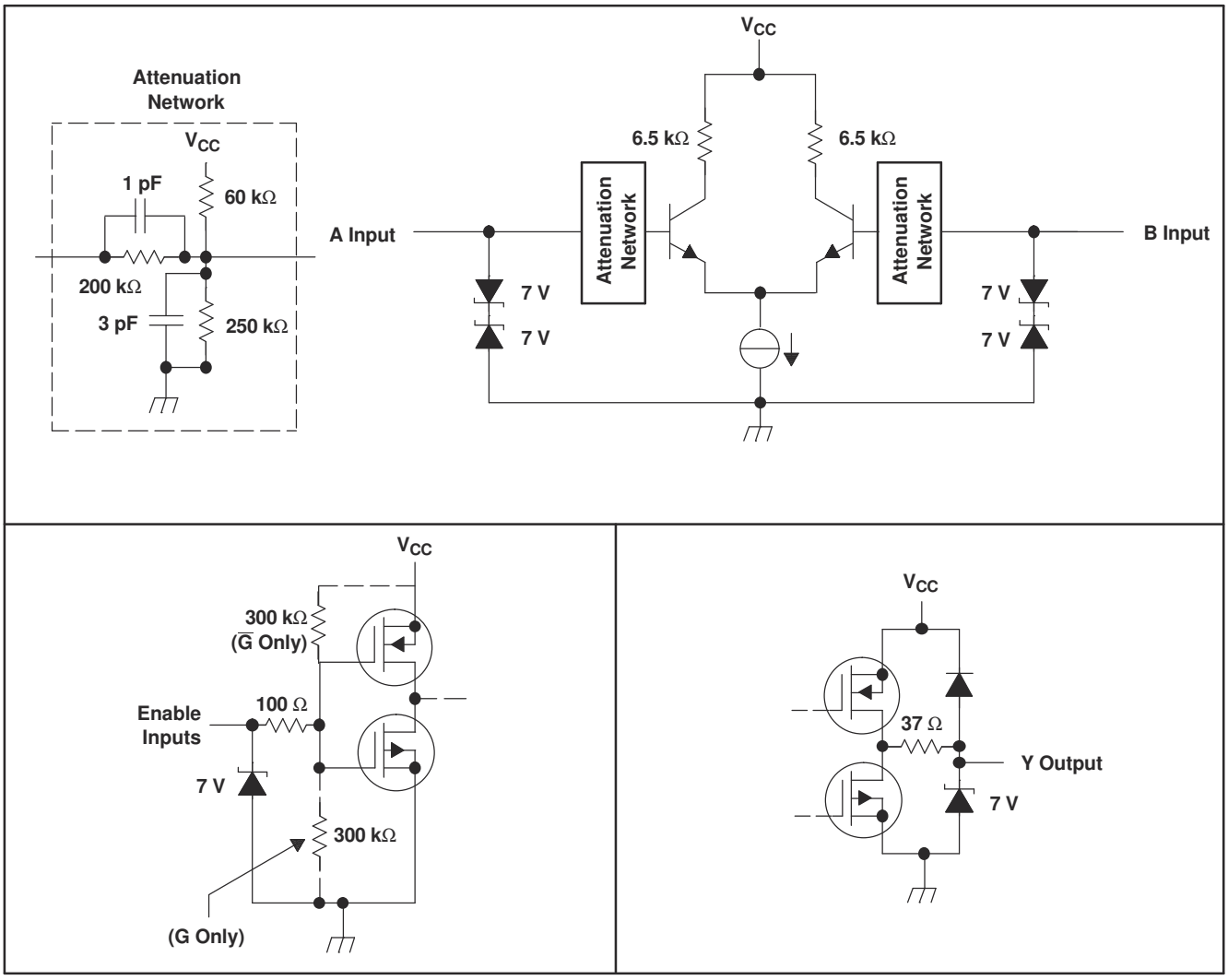
7.4 Equivalent Input and Output Schematic Diagrams



7.5 Device Functional Modes

表 7-1. Function Table

SN55LVRA4-SEP (1)			
DIFFERENTIAL INPUT	ENABLES		OUTPUT
$V_{ID} = V_A - V_B$	G	$\overline{G}$	Y
$V_{ID} \geq -32mV$	H	X	H
	X	L	H
$-100\ mV < V_{ID} \leq -32mV$	H	X	?
	X	L	?
$V_{ID} \leq -100mV$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

8 Application and Implementation

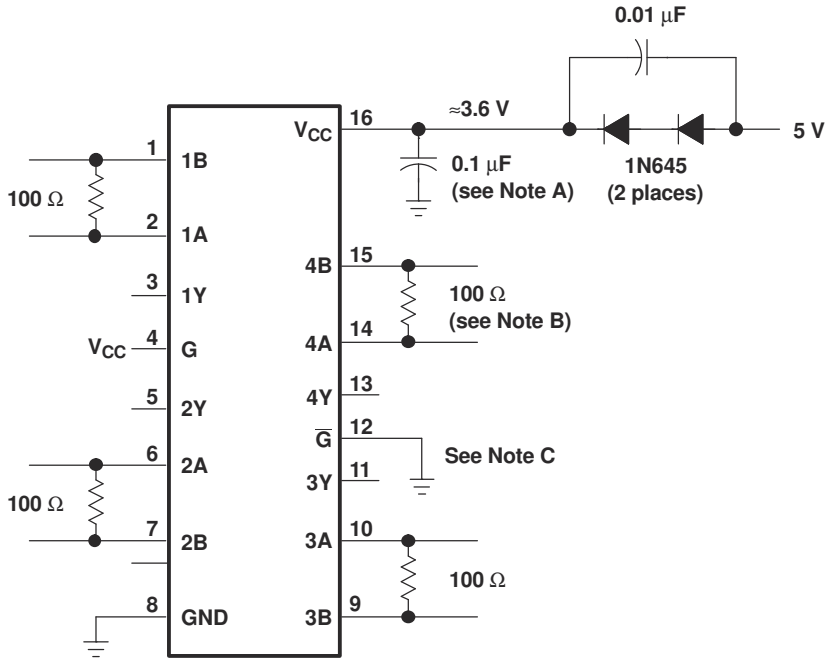
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

For general application guidelines and hints about LVDS drivers and receivers, refer to the *LVDS application notes and design guides*.

8.2 Typical Application



A. Place a 0.1µF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.

B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.

C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

図 8-1. Operation With 5V Supply

8.2.1 Detailed Design Procedure

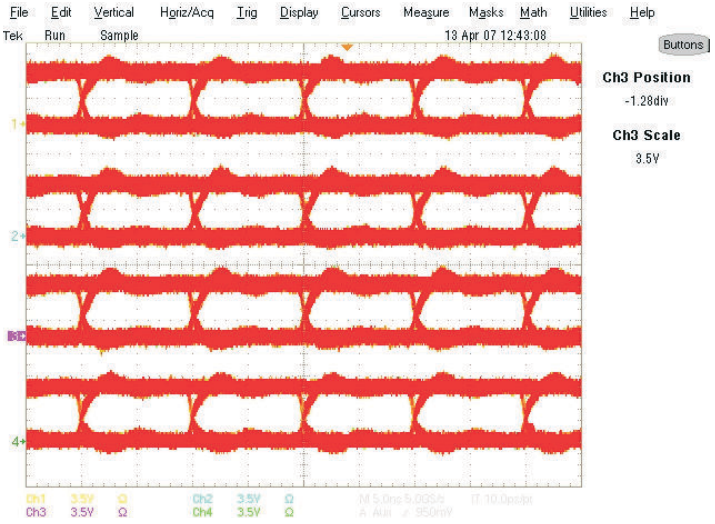
The physical communication channel between the driver and the receiver can be any balanced paired metal conductors meeting the requirements of the LVDS standard. This media can be a twisted pair, twinax, flat ribbon cable, or PCB traces. The nominal characteristic impedance of the interconnect shall be between typical 100Ω with a variation of no more than 10% (90Ω to 110Ω).

ADVANCE INFORMATION

8.2.2 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6V
Driver Input Voltage	0.8 to 3.3V
Driver Signaling Rate	DC to 100Mbps
Interconnect Characteristic Impedance	100Ω
Termination Resistance	100Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6V
Receiver Input Voltage	0 to 24V
Receiver Signaling Rate	DC to 100Mbps
Ground shift between driver and receiver	±1V

8.2.3 Application Performance Plots



All Rx running at 100Mbps; Channel 1: 1Y Channel 2: 2Y Channel 3: 3Y Channel 4: 4Y

T = 25°C V_{CC} = 3.6V PRBS = 2^{23} – 1

図 8-2. Typical Eye Patterns

8.2.4 Cold Sparing

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, V_{CC} must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

ADVANCE INFORMATION

8.3 Active Failsafe Feature

A differential line receiver commonly has a failsafe circuit to prevent the output from switching on input noise. Current LVDS failsafe implementation require either external components with subsequent reductions in signal quality or integrated solutions with limited application. This family of receivers has a new integrated failsafe that solves the limitations seen in present solutions. A detailed theory of operation is presented in the Active Fail-Safe in TI's LVDS Receivers application note.

図 8-3 shows one receiver channel with active failsafe, which consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two failsafe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and the comparator detects when the input differential falls below 80mV. A 600ns failsafe timer filters the window comparator outputs. When failsafe is asserted, the failsafe logic drives the main receiver output to logic high.

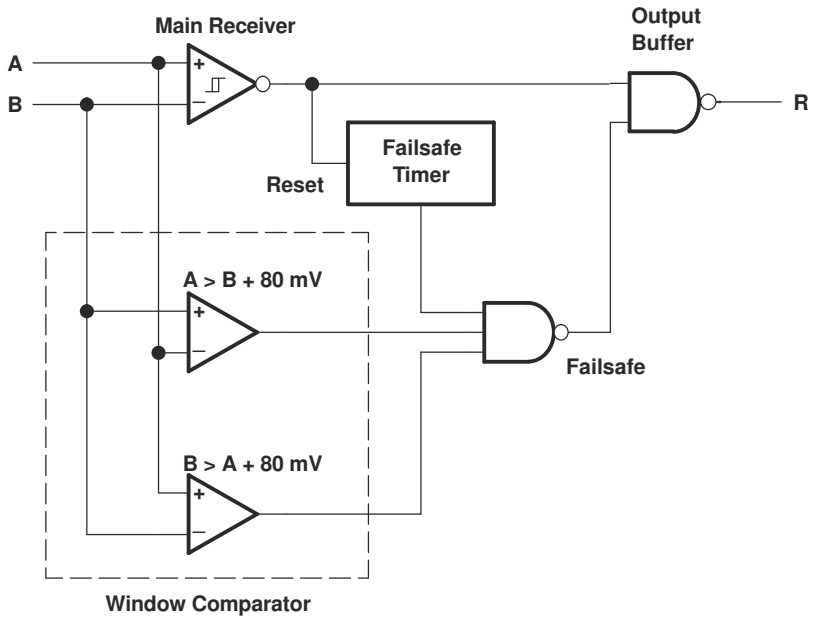


図 8-3. Receiver with active failsafe

8.4 ECL/PECL-to-LVTTL Conversion with TI's LVDS Receiver

The various versions of emitter-coupled logic (for example, ECL, PECL and LVPECL) are often the physical layer of choice for system designers. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS is not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. Texas Instruments has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination (V_{CC} – 2V).

図 8-4 and 図 8-5 show the use of an LV/PECL driver driving five meters of CAT-5 cable and being received by Texas Instruments wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50Ω. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

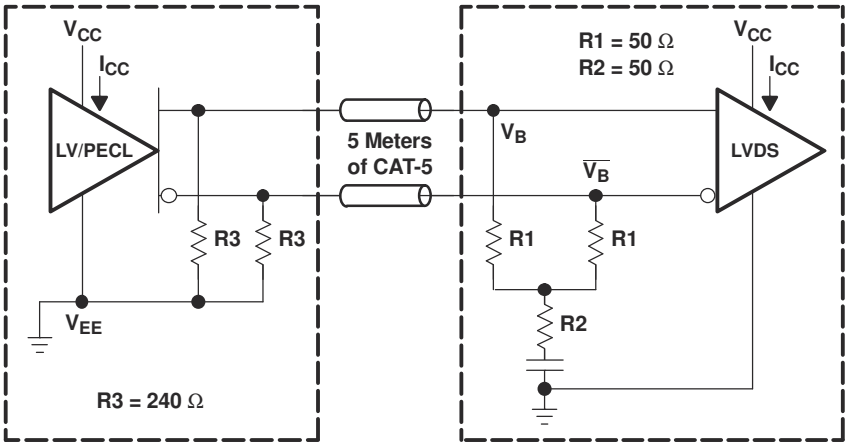


図 8-4. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

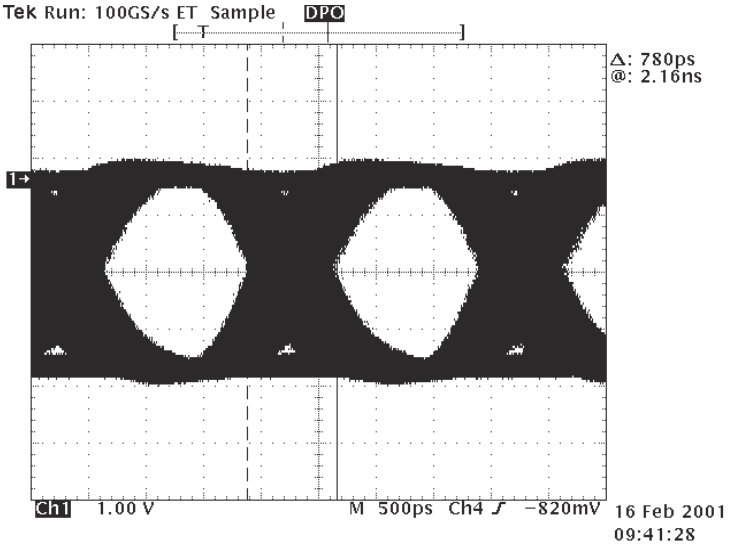


図 8-5. LV/PECL to Remote SN55LVRA4-SEP at 500Mbps Receiver Output (CH1)

ADVANCE INFORMATION

8.5 Test Conditions

- V_{CC} = 3.3 V
- T_A = 25°C (ambient temperature)
- All four channels switching simultaneously with NRZ data. The scope is pulse-triggered simultaneously with NRZ data.

8.6 Equipment

- Tektronix PS25216 programmable power supply
- Tektronix HFS 9003 stimulus system
- Tektronix TDS 784D 4-channel digital phosphor oscilloscope – DPO

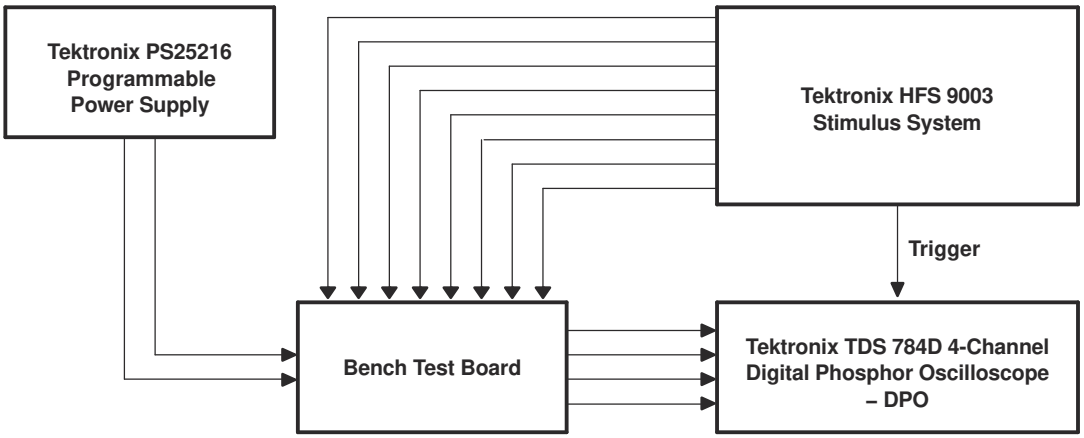


図 8-6. Equipment Setup

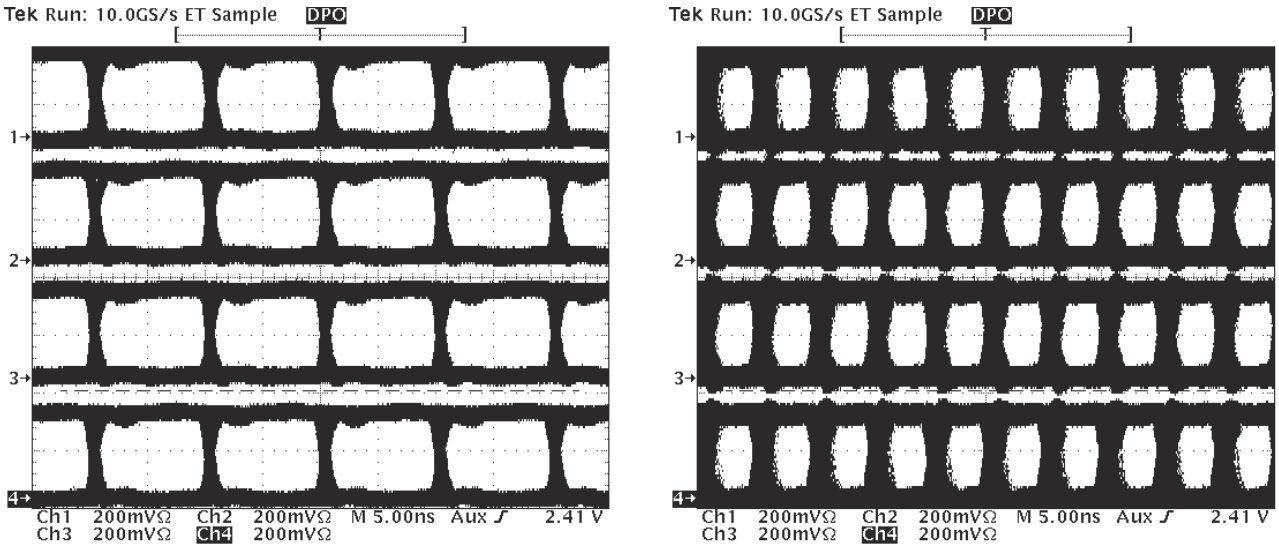


図 8-7. Typical Eye Pattern SN55LVRA4-SEP

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Power Supply Recommendations

9.1 Supply Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, bypass capacitors create low-impedance paths between power and ground at particular frequency depending on the value. At low frequencies, a voltage regulator offers low-impedance paths between the terminal and ground. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10µF to 1000µF) at the board-level do a good job up into the kHz range. Due to the size and length of the leads, large capacitors tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one can resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because the lead inductance is about 1nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula, equations 式 1 to 式 2. A conservative rise time of 200ps and a worst-case change in supply current of 1A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200mV; however, this figure varies depending on the noise budget available in your design.

$$C_{chip} = \left(\frac{\Delta I_{Maximum\ Step\ Change\ Supply\ Current}}{\Delta V_{Maximum\ Power\ Supply\ Noise}}\right) \times T_{Rise\ Time} \quad (1)$$

$$C_{LVDS} = \left(\frac{1A}{0.2V}\right) \times 200\,ps = 0.001\,\mu F \quad (2)$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10µF) and the value of capacitance found above (0.001µF). The smallest value of capacitance shall be as close as possible to the chip.

図 9-1. Recommended LVDS Bypass Capacitor Layout

10 Layout

10.1 Layout Guidelines

10.1.1 Microstrip vs. Stripline Topologies

As per the LVDS Application and Data Handbook, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in 図 10-1.

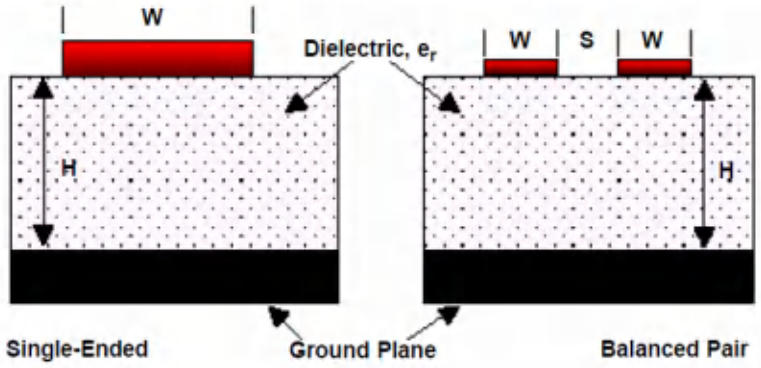


図 10-1. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances.

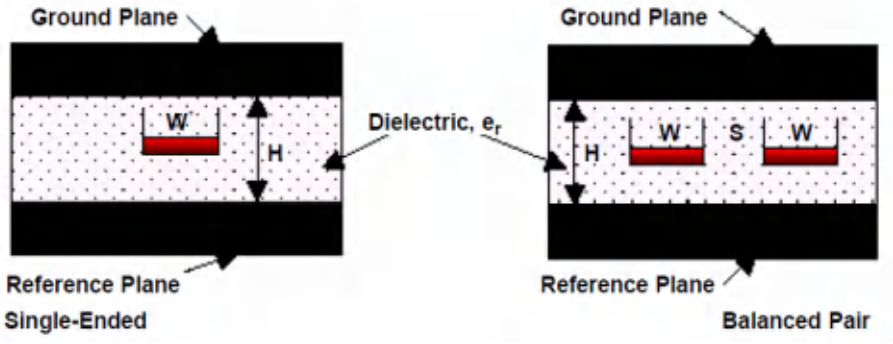


図 10-2. Stripline Topology

10.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

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10.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you should decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in 図 10-3.

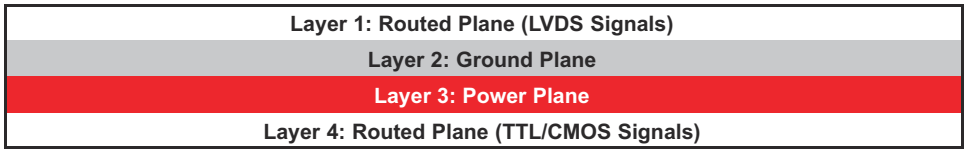

図 10-3. Four-Layer PCB Board

注

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in 図 10-4.

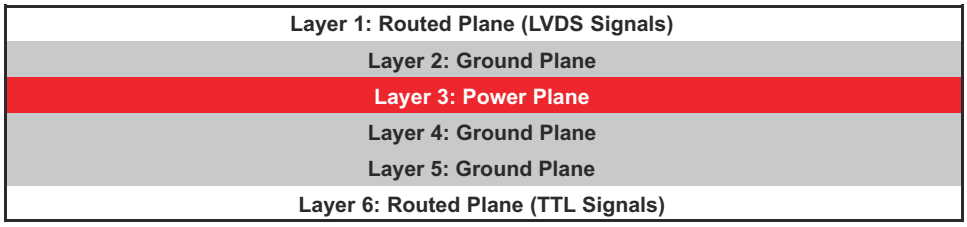

図 10-4. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

10.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces should be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

ADVANCE INFORMATION

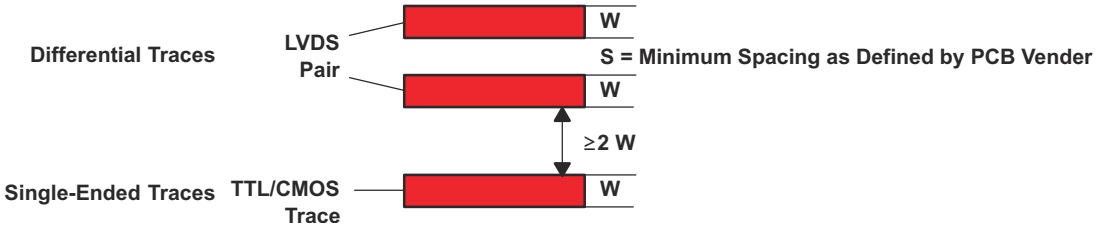

図 10-5. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

10.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

10.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in 図 10-6.

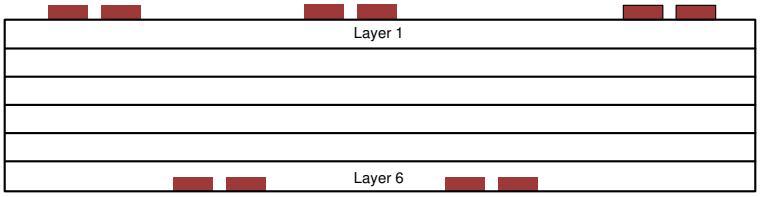

図 10-6. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in 図 10-7. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

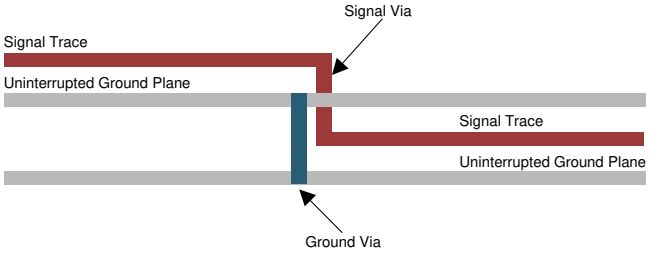

図 10-7. Ground Via Location (Side View)

ADVANCE INFORMATION

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

IBIS modeling is available for this device. Contact the local Texas Instruments sales office or the Texas Instruments Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- Texas Instruments, *Low-Voltage Differential Signalling Design Notes*
- Texas Instruments, *Interface Circuits for TIA/EIA-644* (LVDS)
- Texas Instruments, *Reducing EMI With LVDS*
- Texas Instruments, *Slew Rate Control of LVDS Circuits*
- Texas Instruments, *Using an LVDS Receiver With RS-422 Data*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

DATE	REVISION	NOTES
February 2025	*	Initial APL Release

ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PSN55LVRA4MDTSEP	ACTIVE	SOIC	D	16	250	TBD	Call TI	Call TI	-55 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

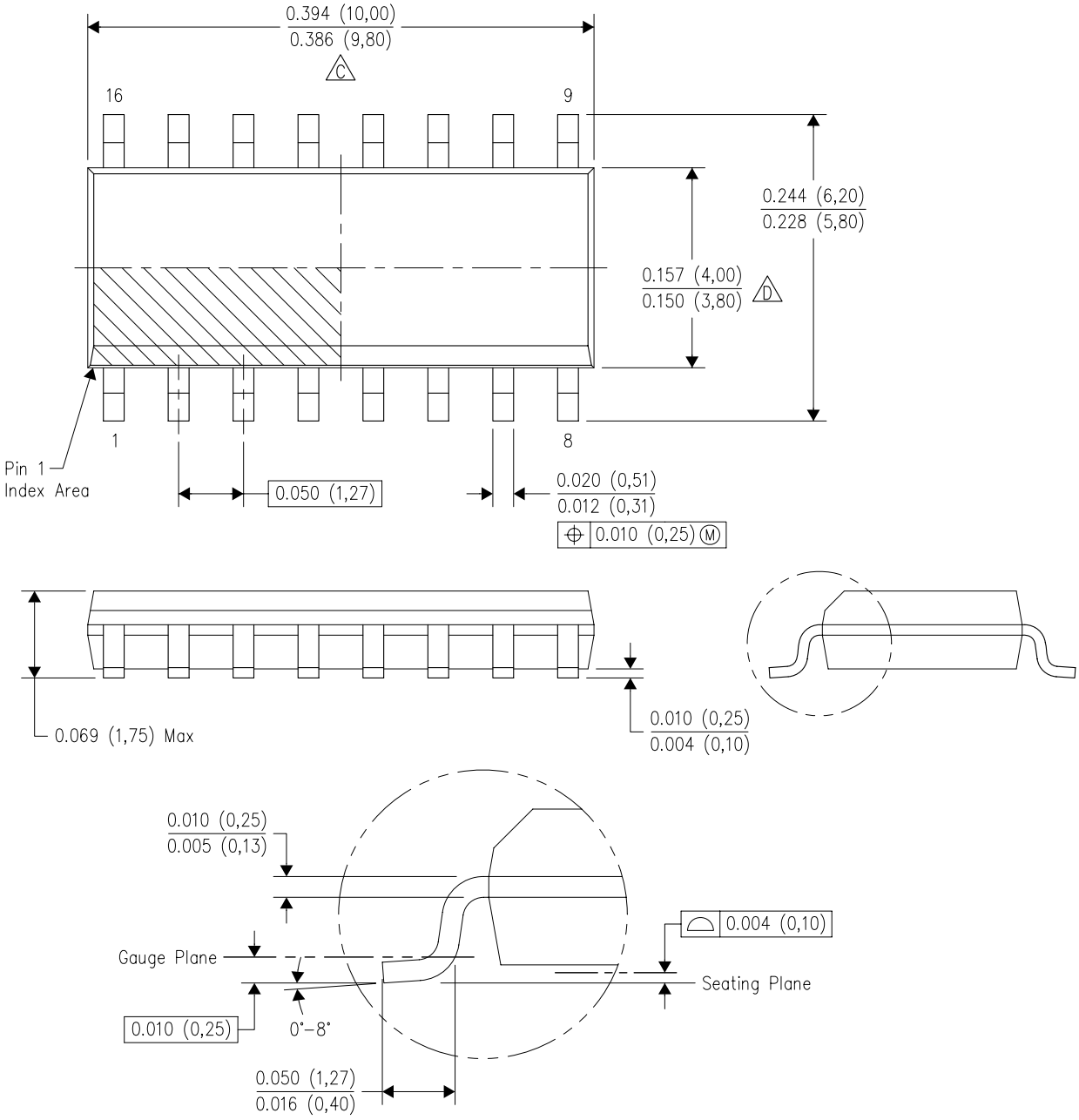
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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