SN55LVCP22A-SP QML Class V、2×2、1Gbps、LVDS クロスポイント・スイッチ

1 特長

- QML Class V、RHA、SMD 5962-11242
- 耐放射線性能
  - 100krad(Si) まで RHA
  - 100krad(Si) まで ELDRS フリー
  - LET = 75MeV×cm^2/mg までの SEL 耐性
  - LET = 75MeV×cm^2/mg までの SEE 特性を規定
- 高速 (最高 1000Mbps)
- 低ジッタの完全差動データ・パス
- PRBS = 2^{23}-1 パターンで 50ps (標準値) のピーク・ツー・ピーク・ジッタ
- 227mW 未満 (標準値)、313mW (最大値) の合計消費電力
- 出力 (チャネル間) スキューは 80ps (標準値)
- 2:1 マルチプレクサ、1:2 デマルチプレクサ、リピータ、または 1:2 信号スプリッタとして構成可能
- 入力は LVDS、LVPECL、CML 信号に対応
- 高速なスイッチ時間:1.7ns (標準値)
- 短い伝搬遅延:0.65ns (標準値)
- TIA/EIA-644-A LVDS 標準と相互動作
- 防衛、航空宇宙、医療アプリケーションをサポート
  - 管理されたベースライン
  - 1 つのアセンブリ / テスト拠点と 1 つの製造拠点
  - 長期間の製品ライフ・サイクルと製品変更通知
  - 製品のトレーサビリティ

2 アプリケーション

- コマンドとデータの処理 (C&DH)
- 通信ペイロード
- レーダー画像処理ペイロード
- 光学画像処理ペイロード
- 衛星用電源システム (EPS)

3 説明

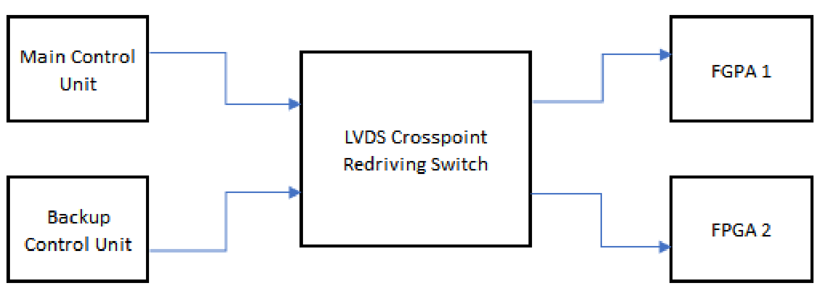
SN55LVCP22A-SP は 2×2 のクロスポイント・スイッチで、パスごとに 1000Mbps を超える速度で動作します。デュアル・チャネルに広い同相 (0V～4V) レシーバが組み込まれており、LVDS、LVPECL、CML 信号を受信できます。デュアル出力は LVDS ドライバで、低消費電力、低 EMI、高速動作を実現します。SN55LVCP22A-SP は単一デバイスで、チャネルごとに 2:2 のバッファリング (反復)、1:2 の分割、2:1 の多重化、2×2 のスイッチング、および LVPECL/CML から LVDS へのレベル変換をサポートします。SN55LVCP22A-SP は柔軟に動作するため、単一のデバイスで、光ネットワーク、ワイヤレス・インフラストラクチャ、データ通信システムに見られるフォルト・トレラント・スイッチ・システムの、冗長シリアル・バス伝送の要求 (動作および保護スイッチング・カード) に対応できます。

SN55LVCP22A-SP は、完全差動データ・パスを使用して、低ノイズの生成、高速スイッチング時間、低パルス幅歪み、低ジッタを保証します。出力のチャネル間スキューは 80ps (標準値) で、すべてのアプリケーションで出力の正確なアライメントを保証します。

デバイス情報

型番	グレード	パッケージ (1)	本体サイズ (公称)
5962R11242 01VFA	QMLV RHA	CFP (16)	6.73mm × 10.3mm
SN55LVCP2 2W/EM	エンジニアリング・サンプル(2)	CFP (16)	6.73mm × 10.3mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) これらのユニットは、技術的な評価のみを目的としています。標準とは異なるフロー (バーンインがないなど) に従って処理され、25℃の温度定格のみがテストされています。これらのユニットは、認定、量産、放射線テスト、航空での使用には適していません。



簡略化されたアプリケーション

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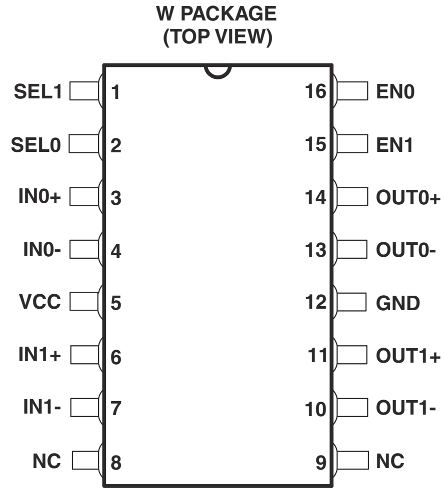
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2021	*	Initial Release

5 Pin Configuration and Functions



NC - No internal connection

表 5-1. Pin Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SEL1	1	Input	Switch Selection Control 1
SEL0	2	Input	Switch Selection Control 2
IN0+	3	Input	LVDS Receiver Positive Input 0
IN0-	4	Input	LVDS Receiver Negative Input 0
VCC	5	Power	3.3V Supply Voltage
IN1+	6	Input	LVDS Receiver Positive Input 1
IN1-	7	Input	LVDS Receiver Negative Input 1
NC	8	N/A	No Internal Connection
NC	9	N/A	No Internal Connection
OUT1-	10	Output	LVDS Driver Negative Output 1
OUT1+	11	Output	LVDS Driver Positive Output 1
GND	12	Ground	Ground
OUT0-	13	Output	LVDS Driver Negative Output 0
OUT0+	14	Output	LVDS Driver Positive Output 0
EN1	15	Input	Output Enable for Driver 1
EN0	16	Input	Output Enable for Driver 0

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted[(1)]

	UNIT
Supply voltage[(2)], V_{CC}	–0.5 V to 4 V
CMOS/TTL input voltage (ENO, EN1, SEL0, SEL1)	–0.5 V to 4 V
LVDS receiver input voltage (IN+, IN–)	–0.7 V to 4.3 V
LVDS driver output voltage (OUT+, OUT–)	–0.5 V to 4 V
Maximum Junction temperature	150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminals.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	-5000	5000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	-500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Receiver input voltage	0		4	V
Operating case (top) temperature, T_C [(1)]	–55		125	°C
Magnitude of differential input voltage, $\|V_{ID}\|$	0.1		3	V

(1) Maximum case temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

6.4 Thermal Information

THERMAL METRIC[(1)]		SN55LVCP22A-SP	UNIT
		W (CFP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	107.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	95.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
CMOS/TTL DC SPECIFICATIONS (EN0, EN1, SEL0, SEL1)					

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IH}	High-level input voltage		2	1.5	V_{CC}	V
V_{IL}	Low-level input voltage		GND	1.5	0.8	V
I_{IH2}	High-level input current	V_{IN} = 3.6 V or 2.0 V, V_{CC} = 0 V	-250	±3	250	μA
I_{IH}	High-level input current	V_{IN} = 3.6 V or 2.0 V, V_{CC} = 3.6 V	-25	±3	25	μA
I_{IL2}	Low-level input current	V_{IN} = 0.0 V or 0.8 V, V_{CC} = 0 V	-150	±1	150	μA
I_{IL}	Low-level input current	V_{IN} = 0.0 V or 0.8 V, V_{CC} = 3.6 V	-15	±1	15	μA
V_{CL}	Input clamp voltage	I_{CL} = –18 mA		-0.8	-1.5	V
LVDS OUTPUT SPECIFICATIONS (OUT0, OUT1)						
$\|V_{OD}\|$	Differential output voltage	R_L = 75 Ω, See 図 7-3	255	390	475	mV
		R_L = 75 Ω, V_{CC} = 3.3 V, T_A = 25°C, See 図 7-3	320	390	430	
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states	V_{ID} = ±100 mV, See 図 7-3	–25		25	mV
V_{OS}	Steady-state offset voltage	See 図 7-4	1	1.2	1.45	V
ΔV_{OS}	Change in steady-state offset voltage between logic states	See 図 7-4	–25		25	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See 図 7-4		50		mV
I_{OZ}	High-impedance output current	V_{OUT} = GND or V_{CC}	-15		15	μA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V, 1.5 V; V_{OUT} = 3.6 V or GND	-15		15	μA
I_{OZH}	High-impedance output current, after HDR 100 krad	V_{OUT} = V_{CC}, T_A = 25°C	-120		350	μA
I_{OFFH}	Power-off leakage current, after after HDR 100 krad	V_{CC} = 0 V, 1.5 V; V_{OUT} = 3.6 V, T_A = 25°C	-50		150	μA
I_{OS}	Output short-circuit current	V_{OUT+} or V_{OUT-} = 0 V			-8	mA
I_{OSB}	Both outputs short-circuit current	V_{OUT+} and V_{OUT-} = 0 V	–8		8	mA
C_O	Differential output capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		3		pF
LVDS RECEIVER DC SPECIFICATIONS (IN0, IN1)						
V_{TH}	Positive-going differential input voltage threshold	See 図 7-2 and 表 7-1			100	mV
V_{TL}	Negative-going differential input voltage threshold	See 図 7-2 and 表 7-1	–100			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis			20	150	mV
V_{CMR}	Common-mode voltage range	V_{ID} = 100 mV, V_{CC} = 3.0 V to 3.6 V	0.05		3.95	V
I_{IN}	Input current	V_{IN} = 4 V, V_{CC} = 3.6 V or 0.0	-18	±1	18	μA
		V_{IN} = 0 V, V_{CC} = 3.6V or 0.0	-18	±1	18	
C_{IN}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
SUPPLY CURRENT						
I_{CCQ}	Quiescent supply current	R_L = 75 Ω, EN0=EN1=High		60	87	mA
I_{CCD}	Total supply current	R_L = 75 Ω, C_L = 5 pF, 500 MHz (1000 Mbps), EN0=EN1=High		63	87	mA
I_{CCZ}	3-state supply current	EN0 = EN1 = Low		25	35	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

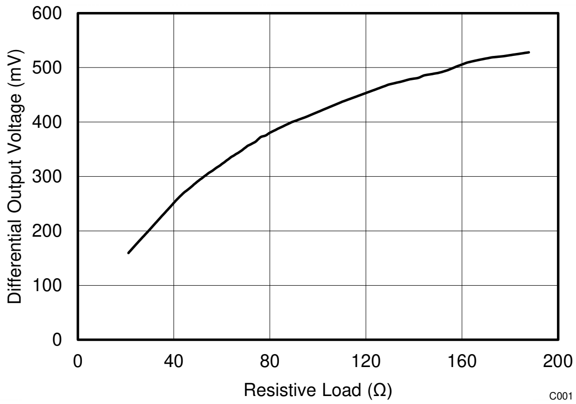
6.6 Switching Characteristics

over recommended operating conditions unless otherwise noted

parameter		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET}	Input to SEL setup time	See 図 7-7		0.8	2.2	ns
t_{HOLD}	Input to SEL hold time	See 図 7-7		1.0	2.2	ns
t_{SWITCH}	SEL to switched output	See 図 7-7		1.7	2.6	ns
t_{PHZ}	Disable time, high-level-to-high-impedance	See 図 7-6		2	8	ns
t_{PLZ}	Disable time, low-level-to-high-impedance	See 図 7-6		2	8	ns
t_{PZH}	Enable time, high-impedance -to-high-level output	See 図 7-6		2	8	ns
t_{PZL}	Enable time, high-impedance-to-low-level output	See 図 7-6		2	8	ns
t_{LHT}	Differential output signal rise time (20%-80%)[1]	C_L = 5 pF, See 図 7-5		280	620	ps
t_{HLT}	Differential output signal fall time (20%-80%)[1]	C_L = 5 pF, See 図 7-5		280	620	ps
t_{JIT}	Added peak-to-peak jitter[3]	V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 50 MHz, C_L = 5 pF		13.7	22.2	ps
		V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 240 MHz, C_L = 5 pF		13.4	24.5	
		V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 500 MHz, C_L = 5 pF		14.4	35.7	
		V_{ID} = 200 mV, PRBS = 2^{15}-1 data pattern, V_{CM} = 1.2 V, 240 Mbps, C_L = 5 pF		68.3	204	ps
		V_{ID} = 200 mV, PRBS = 2^{15}-1 data pattern, V_{CM} = 1.2 V, 1000 Mbps, C_L = 5 pF		73.2	282	
t_{Jrms}	Added random jitter (rms)[3]	V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 50 MHz, C_L = 5 pF		0.97	1.5	ps_{RMS}
		V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 240 MHz, C_L = 5 pF		0.85	1.53	
		V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 500 MHz, C_L = 5 pF		0.86	1.79	
t_{PLHD}	Propagation delay time, low-to-high-level output[1]		200	650	2350	ps
t_{PHLD}	Propagation delay time, high-to-low-level output[1]		200	650	2350	ps
t_{skew} [5]	Pulse skew ($\|t_{PLHD} - t_{PHLD}\|$)[2]	C_L = 5 pF, See 図 7-5		45	160	ps
t_{CCS}	Output channel-to-channel skew, splitter mode	C_L = 5 pF, See 図 7-5		80		ps
f_{MAX} [5]	Maximum operating frequency[4]		1			GHz

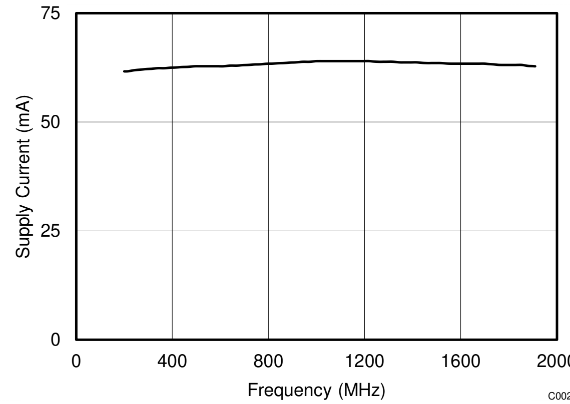
(1) Input: V_{IC} = 1.2 V, V_{ID} = 200 mV, 50% duty cycle, 1 MHz, t_r/t_f = 500 ps
(2) t_{skew} is the magnitude of the time difference between the t_{PLHD} and t_{PHLD} of any output of a single device.
(3) Not production tested.
(4) Signal generator conditions: 50% duty cycle, t_r or $t_f \leq$ 100 ps (10% to 90%), transmitter output criteria: duty cycle = 45% to 55% $V_{OD} \geq$ 300 mV.
(5) t_{skew} and f_{MAX} parameters are guaranteed by characterization, but not production tested.

6.7 Typical Characteristics



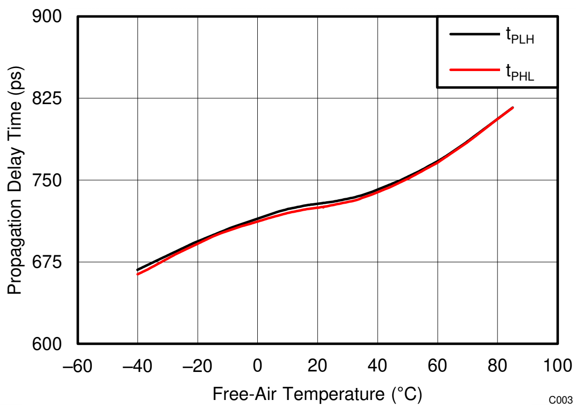
V_{CC} = 3.3 V T_A = 25°C

図 6-1. Differential Output Voltage vs Resistive Load



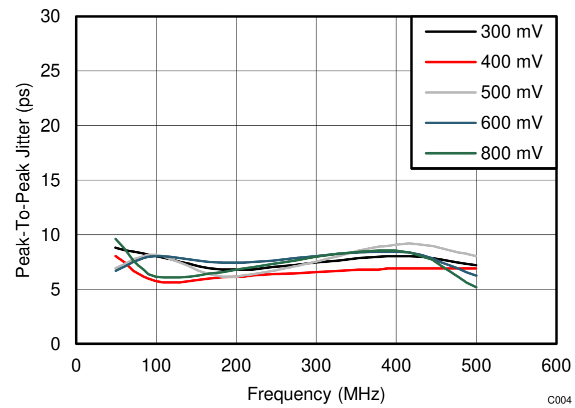
V_{CC} = 3.3 V T_A = 25°C V_{IC} = 1.2 V
$|V_{ID}|$ = 200 mV

図 6-2. Supply Current vs Frequency



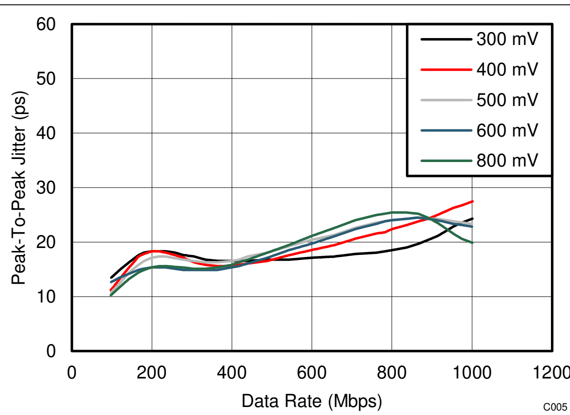
V_{CC} = 3 V - 3.6 V V_{IC} = 1.2 V $|V_{ID}|$ = 300 mV
Input = 1 MHz

図 6-3. Propagation Delay Time bs Ffree-Air Temperature



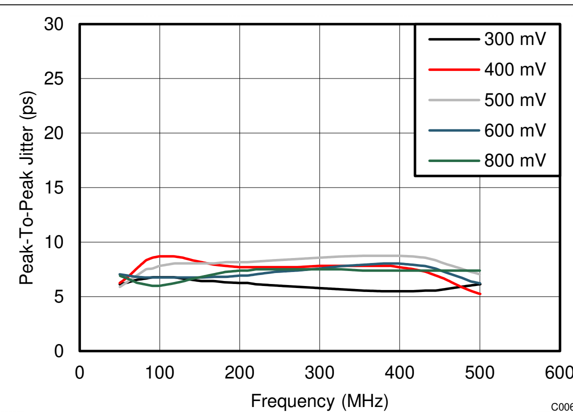
V_{CC} = 3.3 V T_A = 25°C V_{IC} = 400 mV
Input = Clock

図 6-4. Peak-To-Peak Jitter vs Frequency



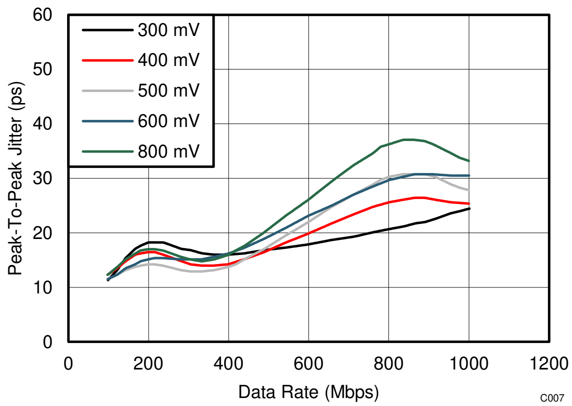
V_{CC} = 3.3 V T_A = 25°C V_{IC} = 400 mV
Input = PRBS 2^{23} −1

図 6-5. Peak-To-Peak Jitter vs Data Rate



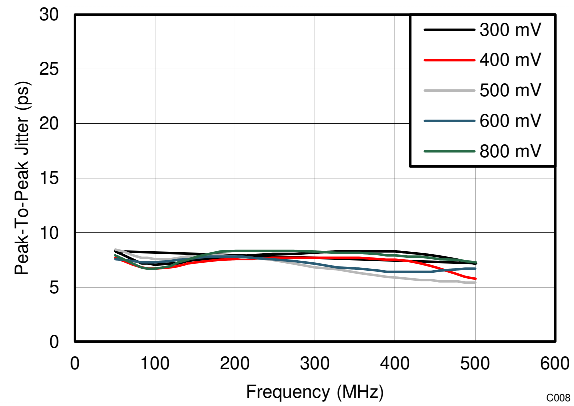
V_{CC} = 3.3 V T_A = 25°C V_{IC} = 1.2 V
Input = Clock

図 6-6. Peak-To-Peak Jitter vs Frequency



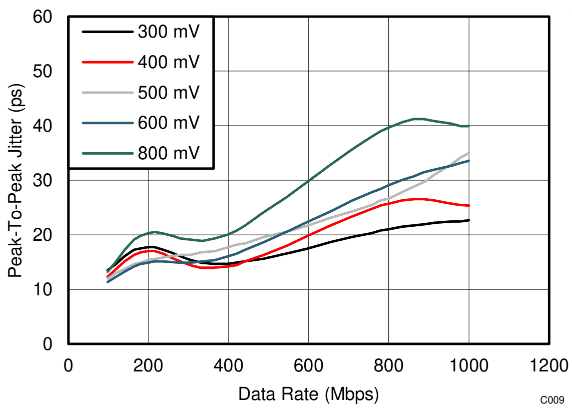
V_{CC} = 3.3 V　T_A = 25°C　V_{IC} = 1.2 V
Input = PRBS 2^{23} −1

図 6-7. Peak-To-Peak Jitter vs Data Rate



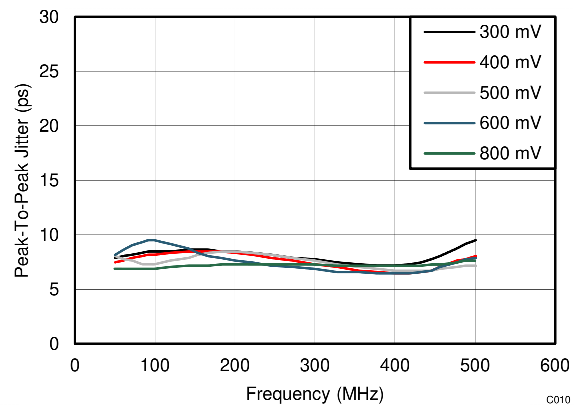
V_{CC} = 3.3 V　T_A = 25°C　V_{IC} = 1.6 V
Input = Clock

図 6-8. Peak-To-Peak Jitter vs Frequency



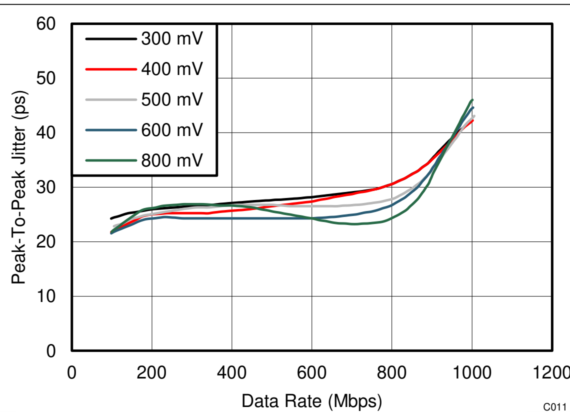
V_{CC} = 3.3 V　T_A = 25°C　V_{IC} = 1.6 V
Input = PRBS 2^{23} −1

図 6-9. Peak-To-Peak Jitter vs Data Rate



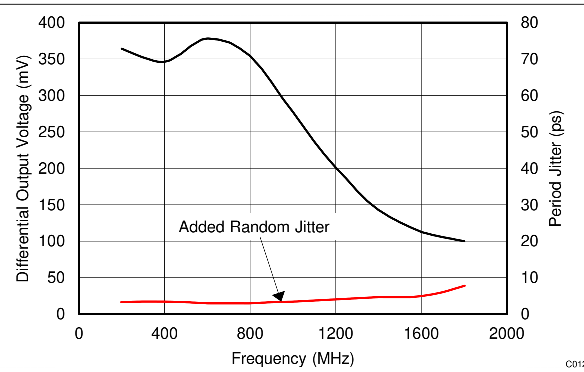
V_{CC} = 3.3 V　T_A = 25°C　V_{IC} = 3.3 V
Input = Clock

図 6-10. Peak-To-Peak Jitter vs Frequency



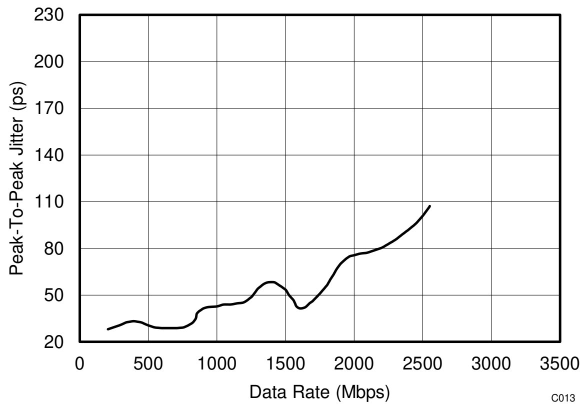
V_{CC} = 3.3 V　T_A = 25°C　V_{IC} = 3.3 V
Input = PRBS 2^{23} −1

図 6-11. Peak-To-Peak Jitter vs Data Rate



V_{CC} = 3.3 V　T_A = 25°C　V_{IC} = 1.2 V
$|V_{ID}|$ = 200 mV

図 6-12. Differential Output Voltage vs Frequency



V_{CC} = 3.3 V　T_A = 25°C　V_{IC} = 1.2 V
$|V_{ID}|$ = 200 mV　Input = PRBS 2^{23} −1

図 6-13. Peak-To-Peak Jitter vs Data Rate

7 Parameter Measurement Information

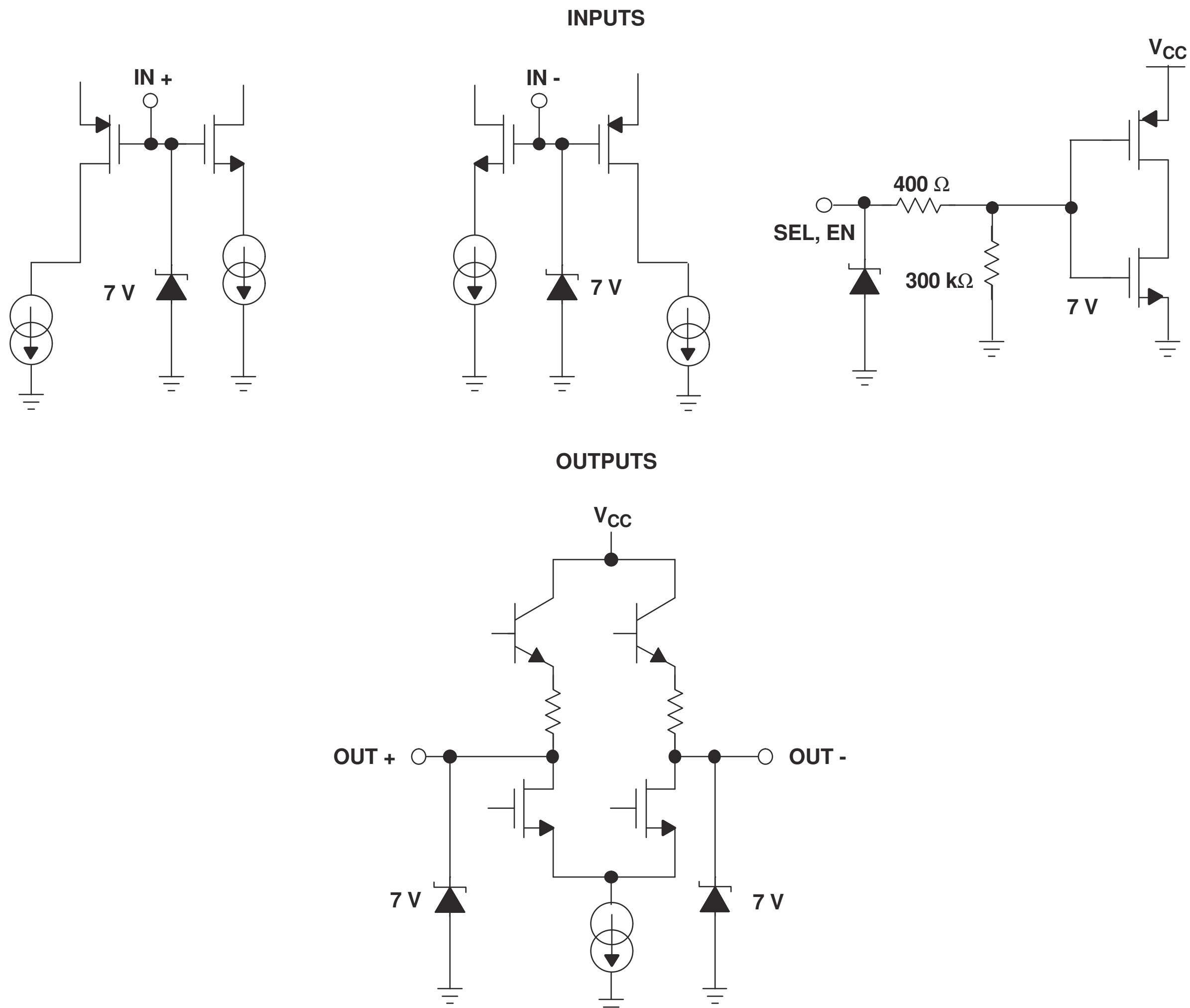


図 7-1. Equivalent Input and Output Schematic Diagrams

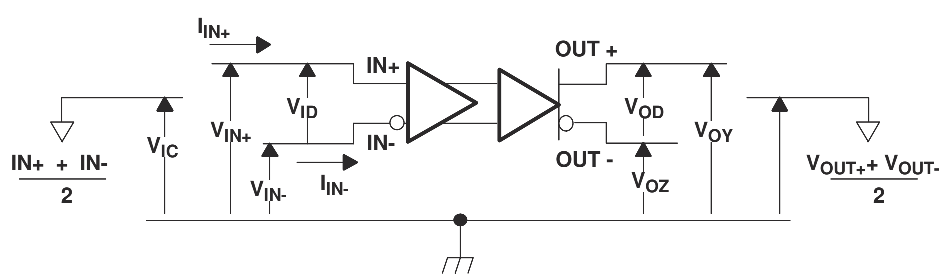


図 7-2. Voltage And Current Definitions

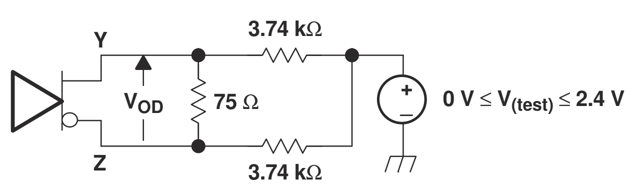
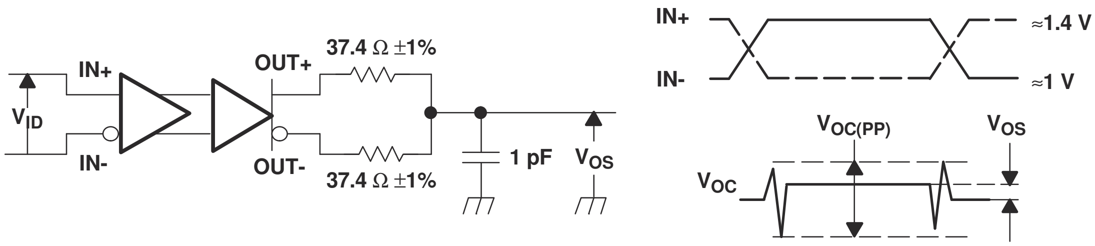
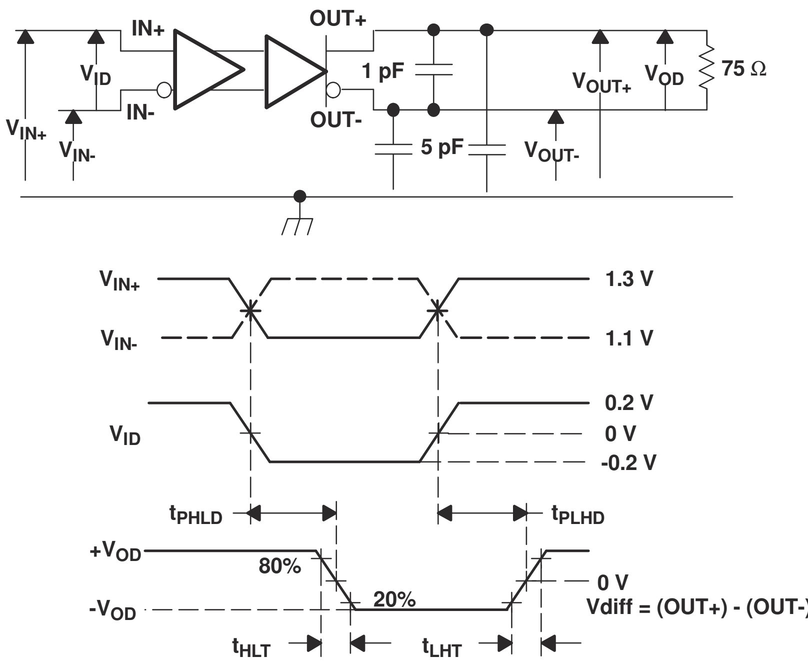


図 7-3. Differential Output Voltage (V_{OD}) Test Circuit



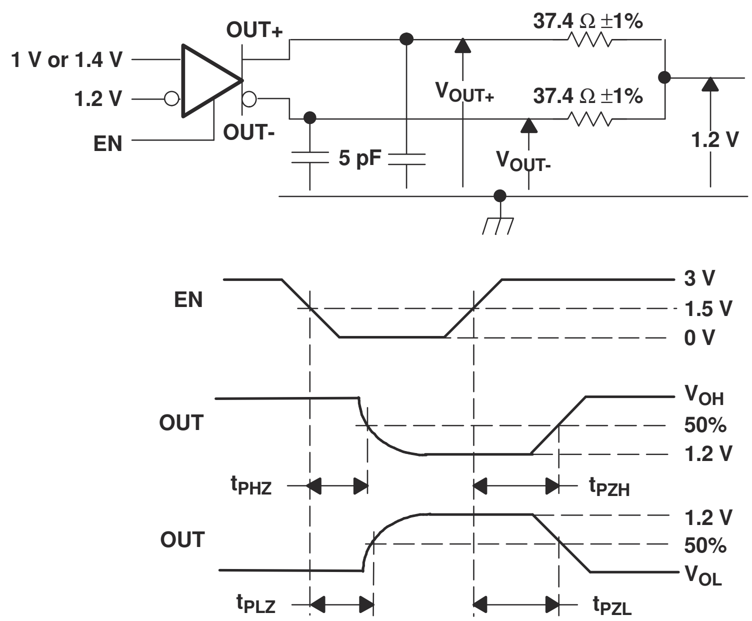
All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns; R_L = 100 Ω; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

図 7-4. Test Circuit And Definitions For The Driver Common-Mode Output Voltage



All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le$ .25 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

図 7-5. Timing Test Circuit And Waveforms



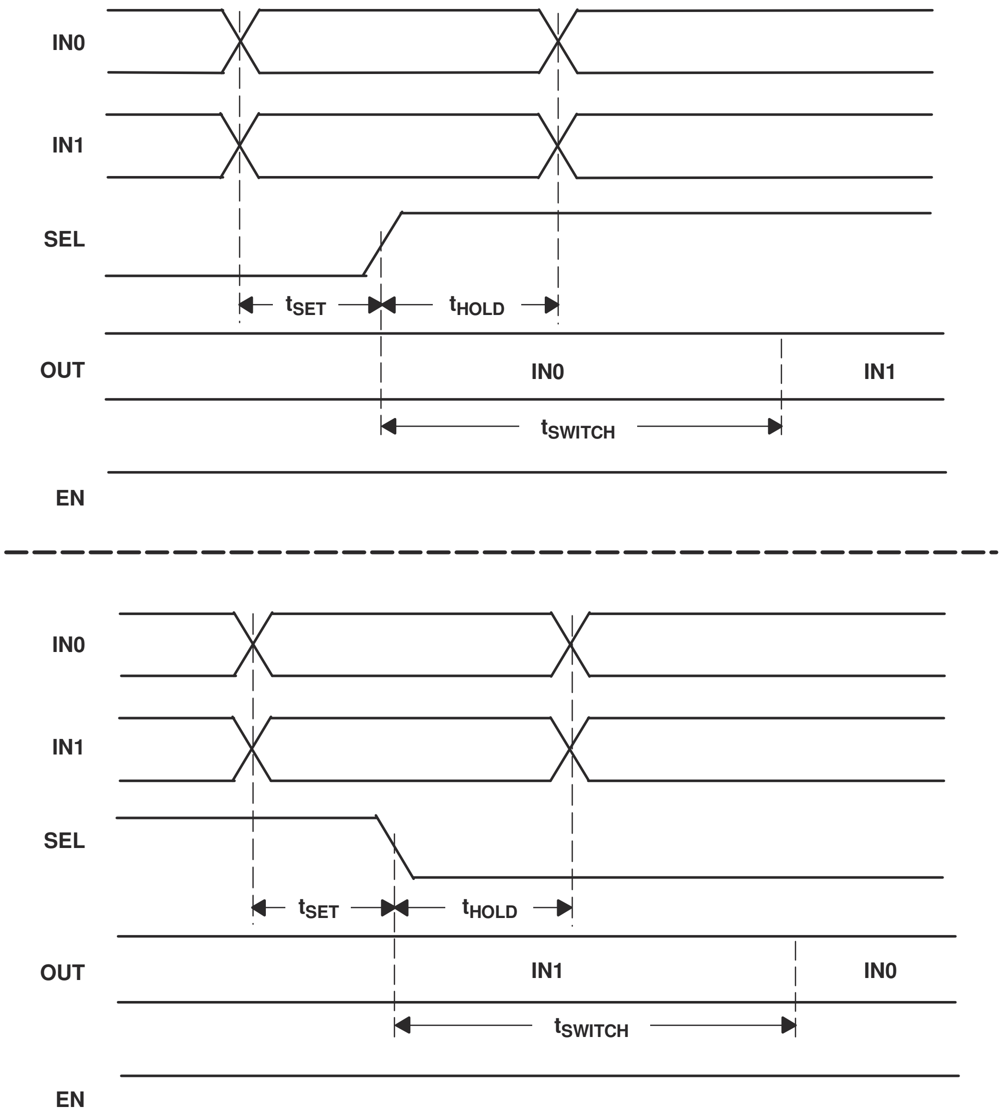
All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

図 7-6. Enable And Disable Time Circuit And Definitions

表 7-1. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4. 0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	–100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

(1) H = high level, L = low level



t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

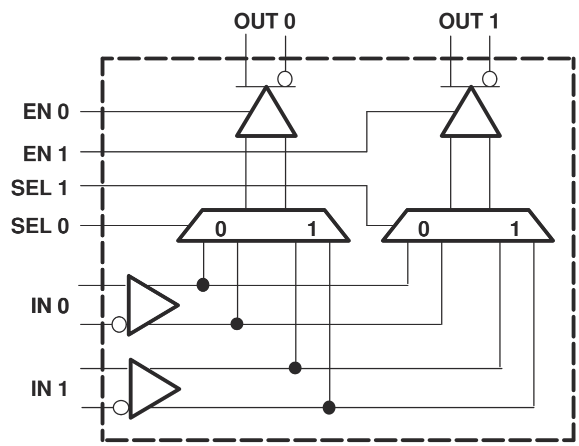
図 7-7. Input To Select For Both Rising And Falling Edge Setup And Hold Times

8 Detailed Description

8.1 Overview

The SN55LVCP22A-SP is a high-speed 1-Gbps 2x2 LVDS redriving cross-point switch that can be used in mux or demux or splitter configurations. The SN55LVCP22A-SP provides multiple signal switching options that allow system implementation flexibility as described in 表 8-1. The SN55LVCP22A-SP incorporates wide common-mode (0 V to 4 V) receivers, allowing for the receipt of LVDS, LVPECL, and CML signals and low-power LVDS drivers to provide high-speed operations. The SN55LVCP22A-SP uses a fully differential data path to ensure low-noise generation, fast switching times, low pulse width distortion, and low jitter.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Select Pins

SEL0 pin selects which differential input lane will be routed to Lane 0 driver differential output OUT0 and SEL1 pin selects which differential input lane will be routed to Lane 1 driver differential output OUT1

8.3.2 Output Enable Pins

EN0 pin is an active high enable for OUT0 driver differential output and EN1 pin is an active high enable for OUT1 driver differential output.

8.4 Device Functional Modes

表 8-1. Function Table

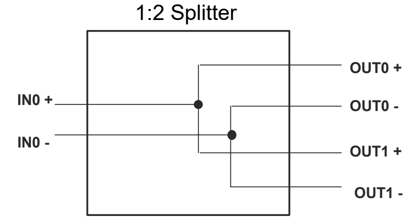
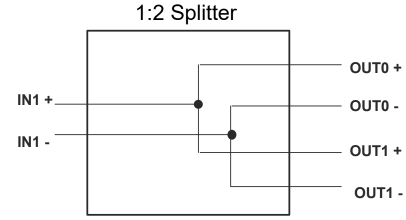
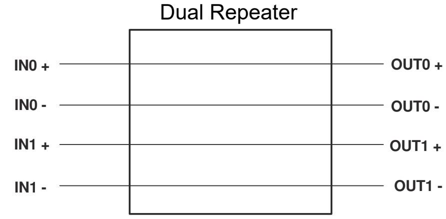
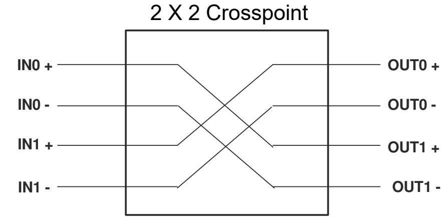
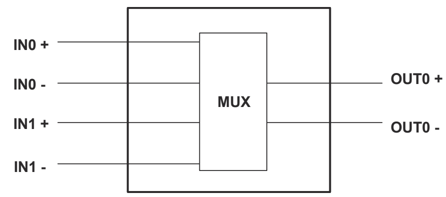
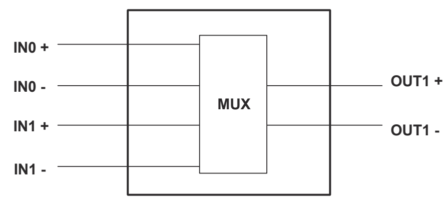
SEL0	SEL1	EN0	EN1	OUT0	OUT1	FUNCTION	SIGNAL FLOW
0	0	1	1	IN0	IN0	1:2 Splitter Input IN0	1:2 Splitter 
1	1	1	1	IN1	IN1	1:2 Splitter Input IN1	1:2 Splitter 

表 8-1. Function Table (continued)

<table>
<tr><th>SEL0</th><th>SEL1</th><th>EN0</th><th>EN1</th><th>OUT0</th><th>OUT1</th><th>FUNCTION</th><th>SIGNAL FLOW</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>IN0</td><td>IN1</td><td>2-lane Repeater</td><td>Dual Repeater
</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>IN1</td><td>IN0</td><td>Cross-switch</td><td>2 X 2 Crosspoint
</td></tr>
<tr><td>0</td><td rowspan="2">X</td><td rowspan="2">1</td><td rowspan="2">0</td><td>IN0</td><td rowspan="2">High-Z</td><td rowspan="2">2:1 Mux Output OUT0</td><td rowspan="2">2:1 Mux
</td></tr>
<tr><td>1</td><td>IN1</td></tr>
<tr><td rowspan="2">X</td><td>0</td><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">High-Z</td><td>IN0</td><td rowspan="2">2:1 Mux Output OUT1</td><td rowspan="2">2:1 Mux
</td></tr>
<tr><td>1</td><td>IN1</td></tr>
</table>

9 Application and Implementation

注

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9.1 Application Information

The SN55LVCP22A-SP can support different kind of signaling at the receiver with proper termination network. The output drivers will output LVDS differential signals.

9.2 Typical Application

9.2.1 Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

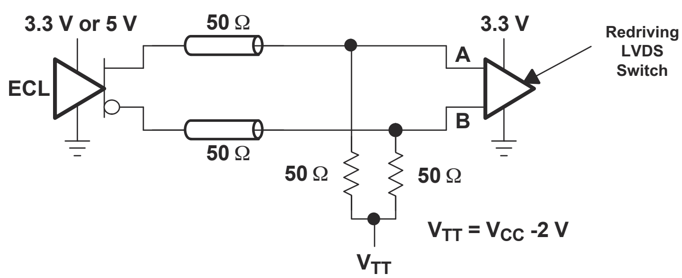

図 9-1. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

9.2.1.1 Design Requirements

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Single-ended termination	50 Ω
V_{TT} termination voltage	V_{CC} -2 V

9.2.1.2 Detailed Design Procedure

Use two 50 Ω termination resistors (as close to the input pins as possible) with termination voltage of V_{TT} as described in 図 9-1 to receive LVPECL input signals.

9.2.2 Current-Mode Logic (CML)

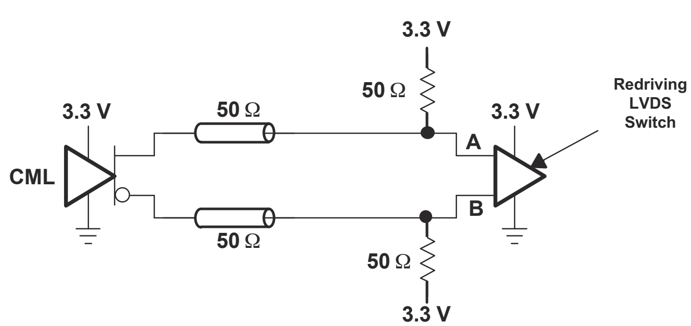

図 9-2. Current-Mode Logic (CML)

9.2.2.1 Design Requirements

表 9-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Single-ended termination	50 Ω
Termination Voltage	V_{CC} = 3.3V

9.2.2.2 Detailed Design Procedure

Use two 50 Ω termination resistors (as close to the input pin as possible) with termination voltage of V_{CC} as described in 図 9-2 to receive CML input signals.

9.2.3 Single-Ended (LVPECL)

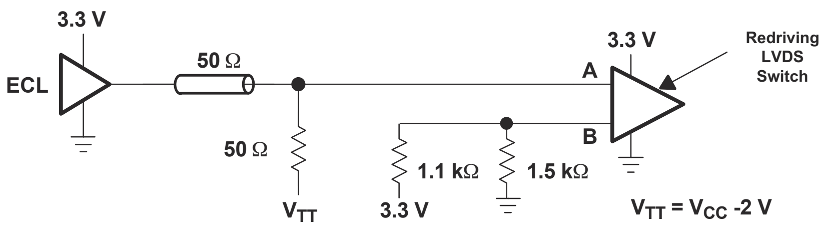

図 9-3. Single-Ended (LVPECL)

9.2.3.1 Design Requirements

表 9-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Single-ended termination for input used	50 Ω
V_{TT} termination voltage	V_{CC} - 2 V
Unused input pull-up termination to V_{CC}	1.1 kΩ
Unused input pull-down termination to Gound	1.5 kΩ

9.2.3.2 Detailed Design Procedure

Use a 50 Ω termination resistor (as close to the input pin as possible) with termination voltage of V_{TT} as described in 図 9-3 to receive Single-ended LVPECL input signals. Terminate Unused input pin with 1.1 kΩ pull-up to V_{CC} and 1.5 kΩ pull-down to ground.

9.2.4 Low-Voltage Differential Signaling (LVDS)

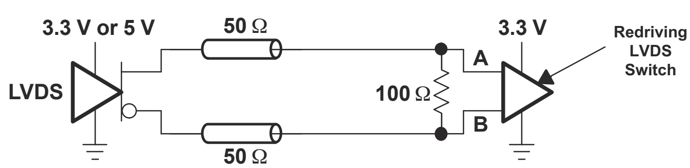

図 9-4. Low-Voltage Differential Signaling (LVDS)

9.2.4.1 Design Requirements

表 9-4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Differential Termination	100 Ω

9.2.4.2 Detailed Design Procedure

Use a 100 Ω differential termination resistor (as close to the input pins as possible) as described in 図 9-4 to receive LVDS input signals.

9.2.5 Cold Sparing

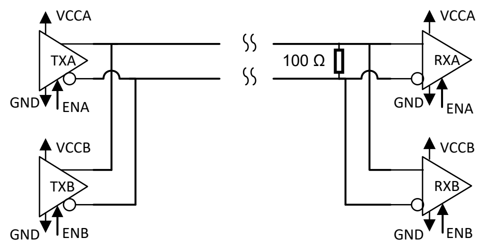

図 9-5. LVDS Cold sparing example

SN55LVCP22A-SP can be used in cold sparing application where a redundant device is on the data bus without drawing additional power. One of the devices TXA or TXB form transmitter redundant pair can be powered down in cold spare mode. Similarly, one for the devices RXA or RXB from receiver redundant pair can be powered down in cold spare mode.

SN55LVCP22A-SP remains in a high impedance power-off state, when VCC is grounded at 0V (within 250mV of GND).

表 9-5. Cold sparing TX configuration example

Transmitter redundant pair	Operating state	VCCA	VCCB
TXA	Active	3.3 V	0 V
TXB	Cold spare		
TXA	Cold spare	0 V	3.3 V
TXB	Active		

表 9-6. Cold sparing RX configuration example

Receiver redundant pair	Operating state	VCCA	VCCB
RXA	Active	3.3 V	0 V
RXB	Cold spare		
RXA	Cold spare	0 V	3.3 V
RXB	Active		

9.2.6 Application Curves

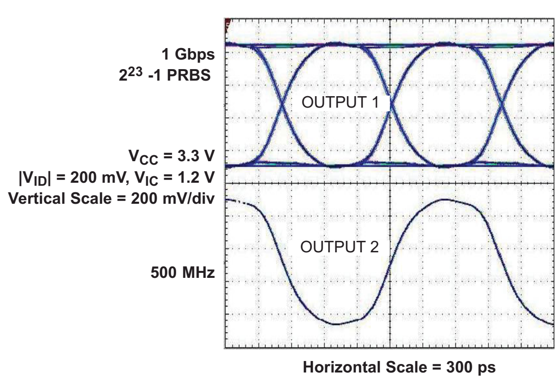

図 9-6. LVDS Output

10 Power Supply Recommendations

There is no power supply sequence required for SN55LVCP22A-SP. It is recommended that at least a 0.1uF decoupling capacitor is placed at the device VCC near the pin.

11 Layout

11.1 Layout Guidelines

High performance layout practices are paramount for board layout for high speed signals to ensure good signal integrity. Even minor imperfection can cause impedance mismatch resulting reflection. Special care is warranted for traces, connections to device, and connectors.

11.2 Layout Example

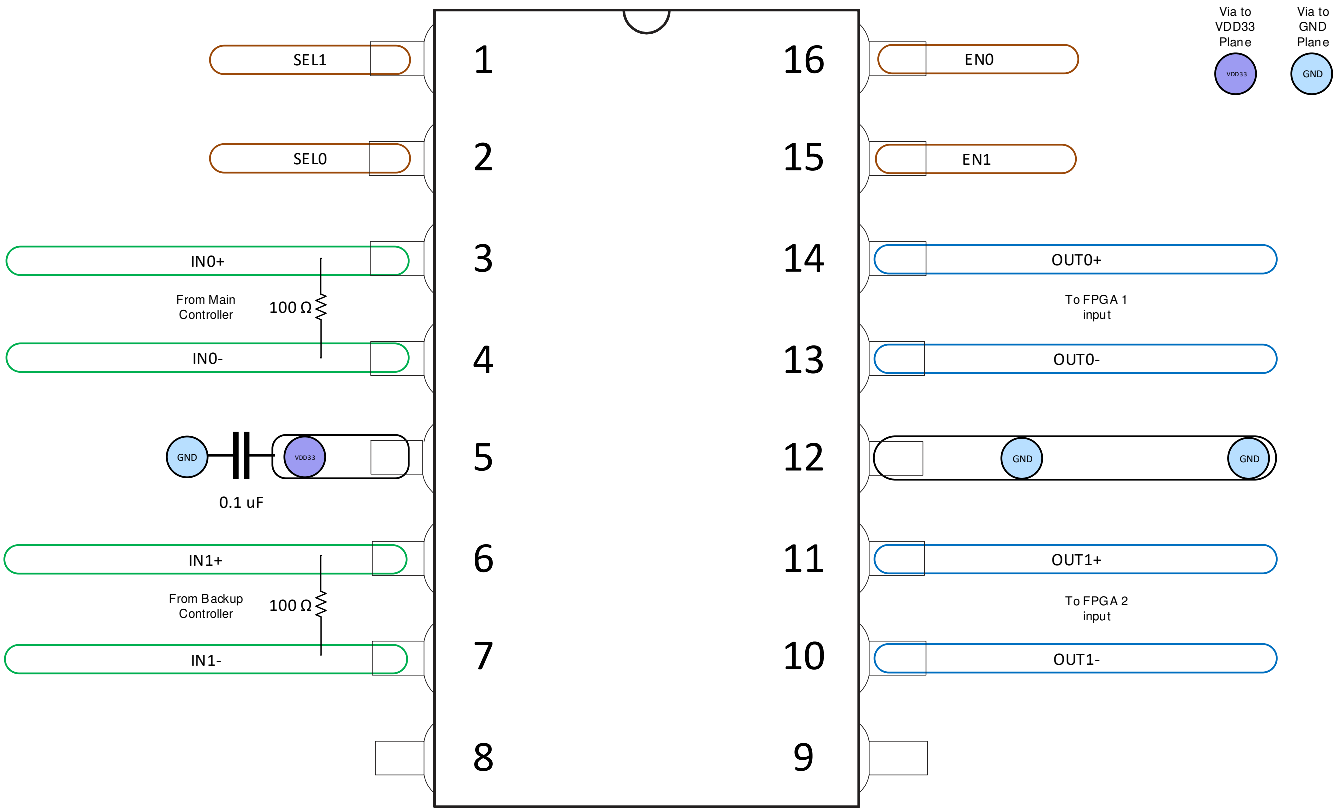

図 11-1. Layout Example with LVDS input signals

12 Device and Documentation Support

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R1124201VFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962R1124201VF A LVCP22W-SP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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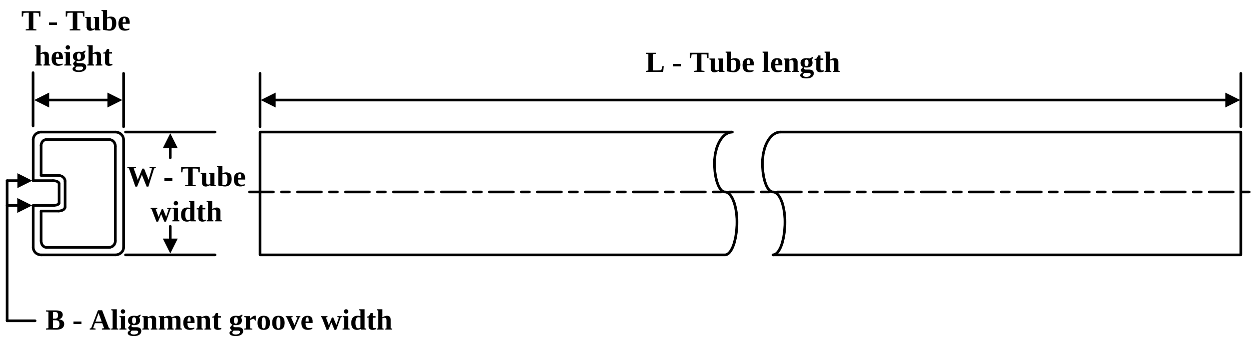
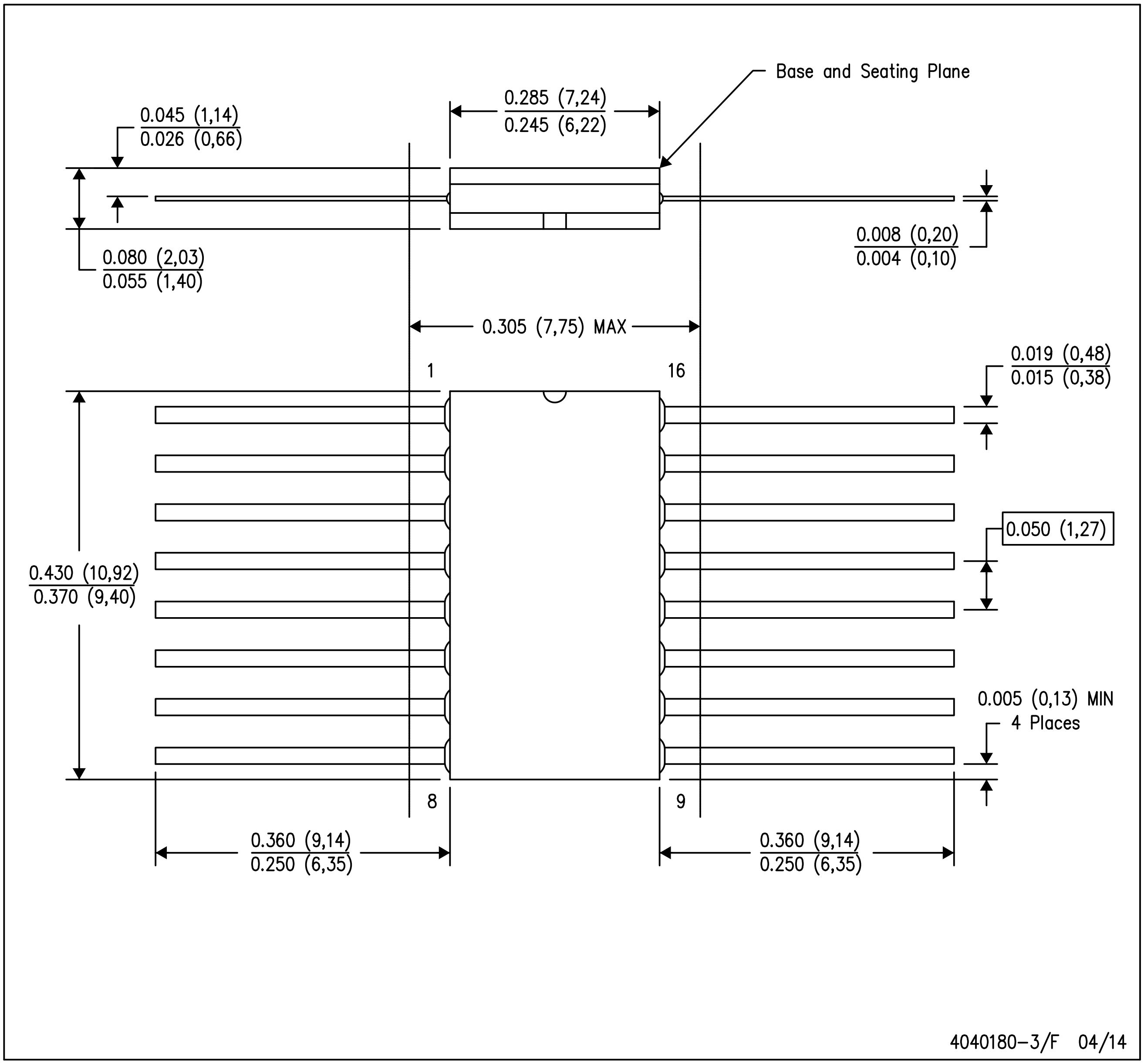
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R1124201VFA	W	CFP	16	25	506.98	26.16	6220	NA

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2–F16

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