SN55HVD233-SEP 宇宙用強化プラスチックに搭載された 3.3V 耐放射線特性 CAN トランシーバ

1 特長

- VID V62/18617
- 放射線耐性を強化
  - 単一イベント・ラッチアップ(SEL)耐性：125°C で43MeV-cm^2/mgまで
  - 30krad(Si)までELDRSフリー
  - 20krad(Si)まで、すべてのウェハー・ロットについて吸収線量(TID) RLAT
- 宇宙向けに強化されたプラスチック
  - 管理されたベースライン
  - 金線
  - NiPdAuリード仕上げ
  - 単一のアセンブリ/テスト施設
  - 単一の製造施設
  - 軍用温度範囲(-55℃～125℃)で利用可能
  - 長期にわたる製品ライフ・サイクル
  - 長期にわたる製品変更通知
  - 製品のトレーサビリティ
  - モールド・コンパウンドの改良による低いガス放出
- ISO 11898-2準拠
- バス・ピンのフォルト保護: ±16V超
- バス・ピンの ESD 保護：±14kV 超、HBM
- データレート: 最大1Mbps
- 広い同相電圧範囲: －7V～12V
- 高い入力インピーダンスにより120ノードが可能
- LVTTL I/Oは5V許容
- ドライバ出力電圧の遷移時間制御による信号品質の向上
- 電力オフのノードはバスに不干渉
- 低電流のスタンバイ・モード： 200µA (標準値)
- 診断用ループバック機能
- サーマル・シャットダウン保護機能
- グリッチ・フリーのバス入力および出力による電源オンおよびオフ
  - 高い入力インピーダンスと低いV_{CC}
  - 電源サイクル中のモノリシック出力

2 アプリケーション

- 低軌道衛星用途のサポート
- 宇宙でのデータバス通信および制御
- オンボード・データ処理用の衛星テレメトリおよびテレコマンド
- CANopen、DeviceNet、CAN Kingdom、ISO 11783、NMEA 2000、SAE J1939 などの CAN バス規格

3 概要

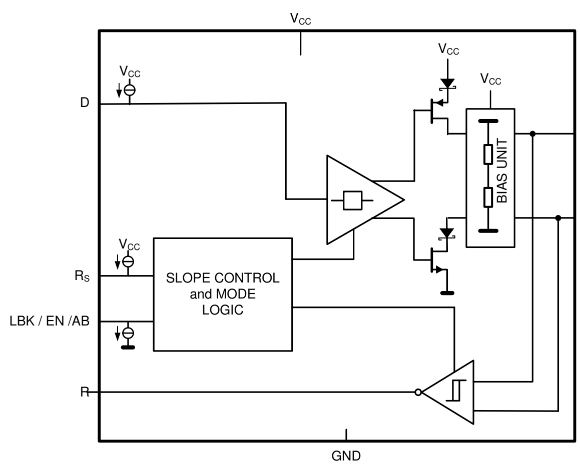
SN55HVD233-SEP は、ISO 11898 規格に準拠したコントローラ・エリア・ネットワーク (CAN) シリアル通信物理層を採用しているアプリケーションで使用されます。この CAN トランシーバは、最大 1Mbps の信号速度で、差動 CAN バスと CAN コントローラの間の送受信を実行する機能を備えています。

製品情報[(1)]

型番	グレード	パッケージ
SN55HVD233MDPSEP	20 krad(Si) RLAT	8 リード SOIC [D] 6.48mm×6.48 mm
SN55HVD233MDTPSEP		

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2018年12月	*	初版

5 概要（続き）

SN55HVD233-SEP は、特に厳しい放射線環境向けに設計されているため、±16V までのクロスワイヤ保護、過電圧保護、および接地損失保護といった機能のほか、過熱 (サーマル・シャットダウン) 保護機能も搭載しています。また、−7V～12Vの広い同相電圧範囲で動作します。このトランシーバは、マイクロプロセッサ、FPGA、またはASIC上のホストCANコントローラと、衛星アプリケーションで使用される差動CANバスとの間のインターフェイスになります。

モード: SN55HVD233-SEP の R_S (ピン 8) を使用して、高速、勾配制御、および低消費電力スタンバイ・モードの 3 つの動作モードを選択できます。ピン8を直接グランドに接続して高速モードの動作を選択すると、立ち上がり/立ち下がり勾配の制限なしに、ドライバ出力トランジスタが可能な限り高速にオン/オフのスイッチングを実行できます。立ち上がり/立ち下がり勾配はピンの出力電流に比例するため、この勾配はピン8とグランドの間に抵抗を接続することにより調整できます。抵抗値 0Ω で勾配制御を実装した場合、シングルエンド・スルーレートは約 38V/μs となり、50kΩ までの抵抗値では約 4V/μs のスルーレートが得られます。勾配制御の詳細については、*アプリケーションと実装*セクションを参照してください。

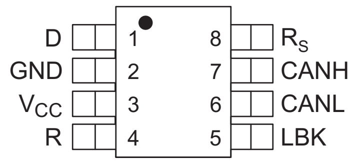
SN55HVD233-SEP は、ピン 8 に HIGH ロジック・レベルが印加されると、低電流のスタンバイ (リッスンのみ) モードへ移行し、このモードでは、ドライバのスイッチがオフになり、レシーバはアクティブのまま保持されます。ローカル・プロトコル・コントローラがバスへメッセージを送信する必要がある場合は、この低電流スタンバイ・モードを元に戻す必要があります。ループバック・モードの詳細については、*アプリケーション情報*セクションを参照してください。

ループバック: SN55HVD233-SEP のループバック LBK ピン 5 がロジック HIGH になると、バス出力とバス入力が高インピーダンス状態になります。残りの回路はアクティブに維持され、ドライバからレシーバへのループバックに利用可能なため、バスに干渉することなく自己診断ノード機能に使用できます。

CANバスの状態: デバイスの通電動作中、CANバスにはドミナントとリセッシブという2つの状態があります。ドミナント・バス状態とは、バスが差動で駆動される場合をいい、DおよびRピンがLOWになります。リセッシブ・バス状態とは、バスがV_{CC}/2に、レシーバの高抵抗の内部入力抵抗R_{IN}によりバイアスされる場合をいい、DおよびRピンがHIGHになります(バスの状態(物理的ビット表現)およびリセッシブ同相バイアスとレシーバの概略図を参照)。

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input.
GND	2	GND	Ground connection.
V_{CC}	3	Supply	Transceiver 3.3-V supply voltage.
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output.
LBK	5	I	Loopback mode input pin.
CANL	6	I/O	Low-level CAN bus line.
CANH	7	I/O	High-level CAN bus line.
RS	8	I	Mode select pin: Tie to GND = high-speed mode, Strong pullup to V_{CC} = low power mode, 0-Ω to 50-kΩ pulldown to GND = slope control mode.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature unless otherwise noted[(1)(2)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	7	V
	Voltage at any bus pin (CANH or CANL)	–16	16	V
	Voltage input, transient pulse, CANH and CANL, through 100 Ω (see Figure 18)	–100	100	V
V_I	Input voltage, (D, RS, LBK)	–0.5	7	V
V_O	Output voltage, (R)	–0.5	7	V
I_O	Receiver output current	–10	10	mA
T_J	Operating junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground pin.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	CANH, CANL, and GND	±14000	V
			Other pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]		±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
	Voltage at any bus pin (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage	D, LBK	2		5.5	V
V_{IL}	Low-level input voltage	D, LBK	0		0.8	V
V_{ID}	Differential input voltage		–6		6	V
	Resistance from RS to ground for slope control		0		50	kΩ
$V_{I(RS)}$	Input voltage at RS for standby		0.75 V_{CC}		5.5	V
I_{OH}	High-level output current	Driver	–50			mA
		Receiver	–10			
I_{OL}	Low-level output current	Driver			50	mA
		Receiver			10	
T_J	Operating junction temperature[(1)]		–55		125	°C

(1) Maximum junction temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

7.4 Thermal Information

THERMAL METRIC (1)(2)		SN55HVD233-SEP D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.2	°C/W

(1) All values except $R_{\theta JC}$ were taken on a JEDEC-51 standard High-K PCB using a nominal lead form. Differences in lead form, component density, or PCB design can affect these values.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Driver Electrical Characteristics

At T_A = –55°C to 125°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (dominant)	CANH	$V_{(D)}$ = 0 V, $V_{(RS)}$ = 0 V, see Figure 12 and Figure 13	2.4		V_{CC}	V
		CANL		0.5		1.25	
V_O	Bus output voltage (recessive)	CANH	$V_{(D)}$ = 3 V, $V_{(RS)}$ = 0 V, see Figure 12 and Figure 13		2.3		V
		CANL			2.3		
$V_{OD(D)}$	Differential output voltage (dominant)		$V_{(D)}$ = 0 V, $V_{(RS)}$ = 0 V, see Figure 12 and Figure 13	1.5	2	3	V
			$V_{(D)}$ = 0 V, $V_{(RS)}$ = 0 V, see Figure 13 and Figure 14	1.2	2	3	
V_{OD}	Differential output voltage (recessive)		$V_{(D)}$ = 3 V, $V_{(RS)}$ = 0 V, see Figure 12 and Figure 13	–120		12	mV
			$V_{(D)}$ = 3 V, $V_{(RS)}$ = 0 V, no load	–0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 20		1		V
I_{IH}	High-level input current	D, LBK	$V_{(D)}$ = 2 V	–30		30	μA
I_{IL}	Low-level input current	D, LBK	$V_{(D)}$ = 0.8 V	–30		30	μA
I_{OS}	Short-circuit output current		$V_{(CANH)}$ = –7 V, CANL open, see Figure 23	–250			mA
			$V_{(CANH)}$ = 12 V, CANL open, see Figure 23			1	
			$V_{(CANL)}$ = –7 V, CANH open, see Figure 23	–1			
			$V_{(CANL)}$ = 12 V, CANH open, see Figure 23			250	
C_O	Output capacitance		See receiver input capacitance				
$I_{IRS(s)}$	RS input current for standby		$V_{(RS)}$ = 0.75 V_{CC}	–10			μA
I_{CC}	Supply current	Standby	$V_{(RS)}$ = V_{CC}, $V_{(D)}$ = V_{CC}, $V_{(LBK)}$ = 0 V		200	700	μA
		Dominant	$V_{(D)}$ = 0 V, no load, $V_{(LBK)}$ = 0 V, RS = 0 V			6	mA
		Recessive	$V_{(D)}$ = V_{CC}, no load, $V_{(LBK)}$ = 0 V, $V_{(RS)}$ = 0 V			6	

(1) All typical values are at 25°C and with a 3.3-V supply.

7.6 Receiver Electrical Characteristics

At T_A = –55°C to 125°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		$V_{(LBK)}$ = 0 V, see Table 1			750	900	mV
V_{IT-}	Negative-going input threshold voltage				500	650		mV
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})					100		mV
V_{OH}	High-level output voltage		I_O = –4 mA, see Figure 17		2.4			V
V_{OL}	Low-level output voltage		I_O = 4 mA, see Figure 17				0.4	V
I_I	Bus input current		$V_{(CANH)}$ or $V_{(CANL)}$ = 12 V	Other bus pin = 0 V, $V_{(D)}$ = 3 V, $V_{(LBK)}$ = 0 V, $V_{(RS)}$ = 0 V	150		500	μA
			$V_{(CANH)}$ or $V_{(CANL)}$ = 12 V, V_{CC} = 0 V		150		600	
			CANH or CANL = –7 V		–610		–100	
			CANH or CANL = –7 V, V_{CC} = 0 V		–450		–100	
C_I	Input capacitance (CANH or CANL)		Pin-to-ground, V_I = 0.4 sin(4E6πt) + 0.5 V, $V_{(D)}$ = 3 V, $V_{(LBK)}$ = 0 V			40		pF
C_{ID}	Differential input capacitance		Pin-to-pin, V_I = 0.4 sin(4E6πt) + 0.5 V, $V_{(D)}$ = 3 V, $V_{(LBK)}$ = 0 V			20		pF
R_{ID}	Differential input resistance		$V_{(D)}$ = 3 V, $V_{(LBK)}$ = 0 V		40		105	kΩ
R_{IN}	Input resistance (CANH or CANL)				20		55	kΩ
I_{CC}	Supply current	Standby	$V_{(RS)}$ = V_{CC}, $V_{(D)}$ = V_{CC}, $V_{(LBK)}$ = 0 V			200	700	μA
		Dominant	$V_{(D)}$ = 0 V, no load, $V_{(RS)}$ = 0 V, $V_{(LBK)}$ = 0 V				6	mA
		Recessive	$V_{(D)}$ = V_{CC}, no load, $V_{(RS)}$ = 0 V, $V_{(LBK)}$ = 0 V				6	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

7.7 Driver Switching Characteristics

At T_A = –55°C to 125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$V_{(RS)}$ = 0 V, see Figure 15		35	85	ns
		RS with 10 kΩ to ground, see Figure 15		70	125	
		RS with 50 kΩ to ground, see Figure 15		500	870	
t_{PHL}	Propagation delay time, high-to-low-level output	$V_{(RS)}$ = 0 V, see Figure 15		70	120	ns
		RS with 10 kΩ to ground, see Figure 15		130	180	
		RS with 50 kΩ to ground, see Figure 15		870	1200	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	$V_{(RS)}$ = 0 V, see Figure 15		35		ns
		RS with 10 kΩ to ground, see Figure 15		60		
		RS with 50 kΩ to ground, see Figure 15		370		
t_r	Differential output signal rise time	$V_{(RS)}$ = 0 V, see Figure 15	20		70	ns
t_f	Differential output signal fall time		20		70	ns
t_r	Differential output signal rise time	RS with 10 kΩ to ground, see Figure 15	30		135	ns
t_f	Differential output signal fall time		30		135	ns
t_r	Differential output signal rise time	RS with 50 kΩ to ground, see Figure 15	350		1400	ns
t_f	Differential output signal fall time		350		1400	ns
$t_{en(s)}$	Enable time from standby to dominant	See Figure 19		0.6	1.5	µs

(1) All typical values are at 25°C and with a 3.3-V supply.

7.8 Receiver Switching Characteristics

At T_A = –55°C to 125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 17		35	105	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	105	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)			7		ns
t_r	Output signal rise time			2		ns
t_f	Output signal fall time			2		ns

(1) All typical values are at 25°C and with a 3.3-V supply.

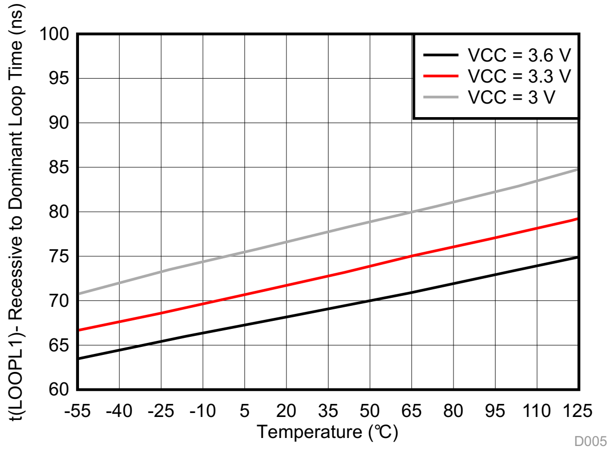
7.9 Device Switching Characteristics

At T_A = –55°C to 125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	See Figure 22		7.5		ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant	$V_{(RS)}$ at 0 V, see Figure 21		70	215	ns
		$V_{(RS)}$ with 10 kΩ to ground, see Figure 21		105	225	
		$V_{(RS)}$ with 50 kΩ to ground, see Figure 21		500	800	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive	$V_{(RS)}$ at 0 V, see Figure 21		70	215	ns
		$V_{(RS)}$ with 10 kΩ to ground, see Figure 21		105	225	
		$V_{(RS)}$ with 50 kΩ to ground, see Figure 21		500	800	

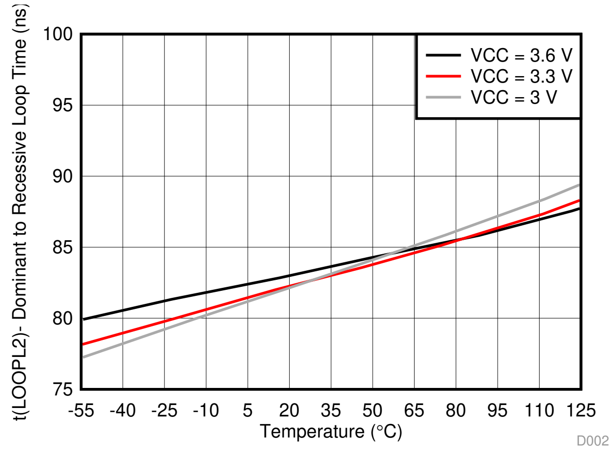
(1) All typical values are at 25°C and with a 3.3-V supply.

7.10 Typical Characteristics



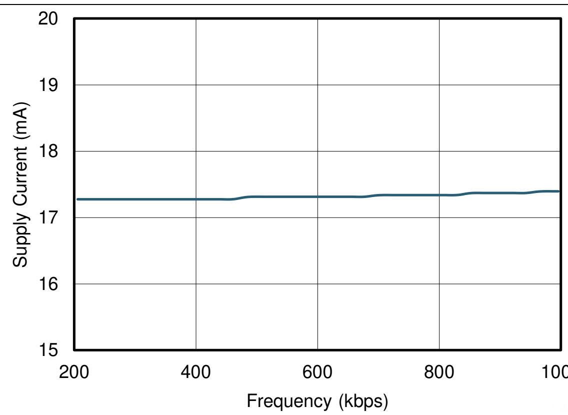
$V_{(RS)}$, $V_{(LBK)}$ = 0 V

Figure 1. Recessive-To-Dominant Loop Time vs Temperature



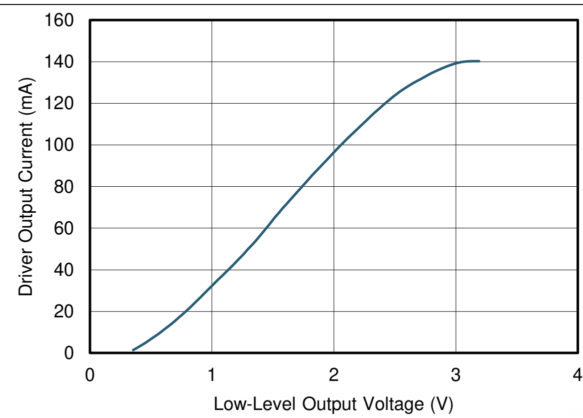
$V_{(RS)}$, $V_{(LBK)}$ = 0 V

Figure 2. Dominant-To-Recessive Loop Time vs Temperature



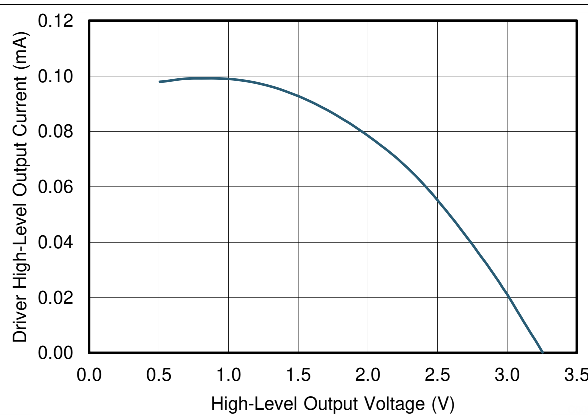
V_{CC} = 3.3 V
60-Ω load
$V_{(RS)}$, $V_{(LBK)}$ = 0 V
T_A = 25°C

Figure 3. Supply Current vs Frequency



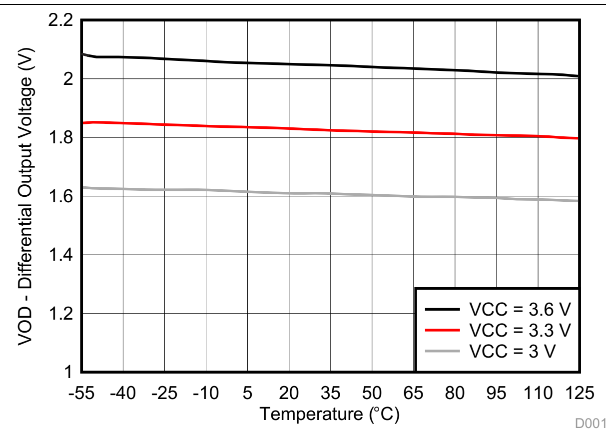
V_{CC} = 3.3 V
$V_{(RS)}$, $V_{(LBK)}$ = 0 V
T_A = 25°C

Figure 4. Driver Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 3.3 V
$V_{(RS)}$, $V_{(LBK)}$ = 0 V
T_A = 25°C

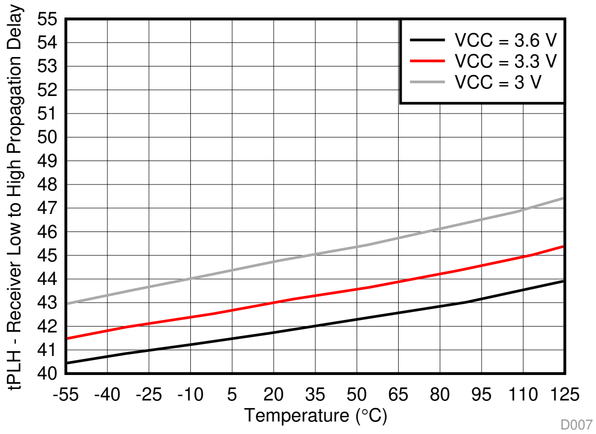
Figure 5. Driver High-Level Output Current vs High-Level Output Voltage



R_L = 60 Ω
$V_{(RS)}$, $V_{(LBK)}$ = 0 V

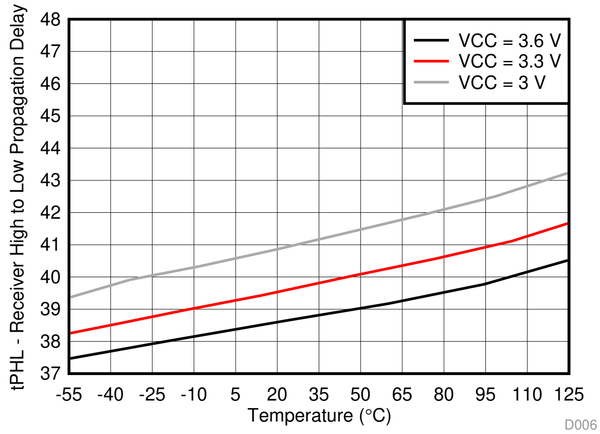
Figure 6. Differential Output Voltage vs Temperature

Typical Characteristics (continued)



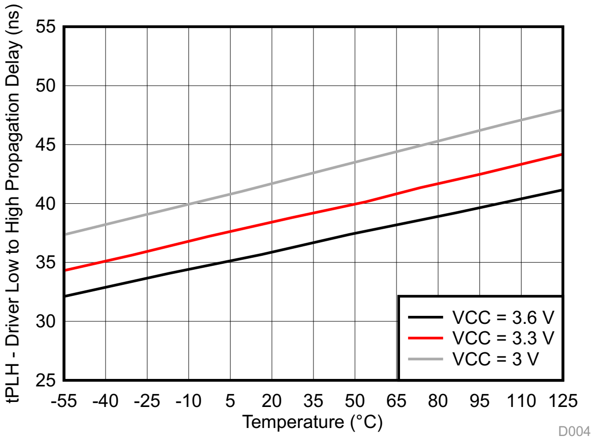
$V_{(RS)}$, $V_{(LBK)}$ = 0 V See Figure 17

Figure 7. Receiver Low-To-High Propagation Delay vs Temperature



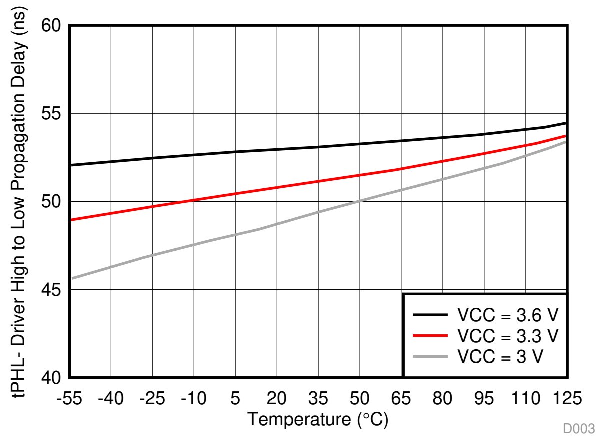
$V_{(RS)}$, $V_{(LBK)}$ = 0 V See Figure 17

Figure 8. Receiver High-To-Low Propagation Delay vs Temperature



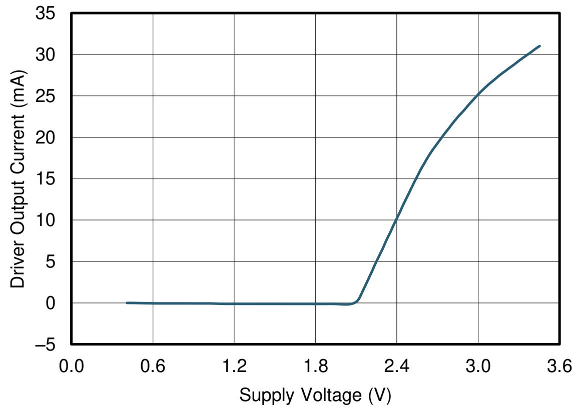
$V_{(RS)}$, $V_{(LBK)}$ = 0 V See Figure 15

Figure 9. Driver Low-To-High Propagation Delay vs Temperature



$V_{(RS)}$, $V_{(LBK)}$ = 0 V See Figure 15

Figure 10. Driver High-To-Low Propagation Delay vs Temperature



$V_{(RS)}$, $V_{(LBK)}$ = 0 V T_A = 25°C R_L = 60 Ω

Figure 11. Driver Output Current vs Supply Voltage

8 Parameter Measurement Information

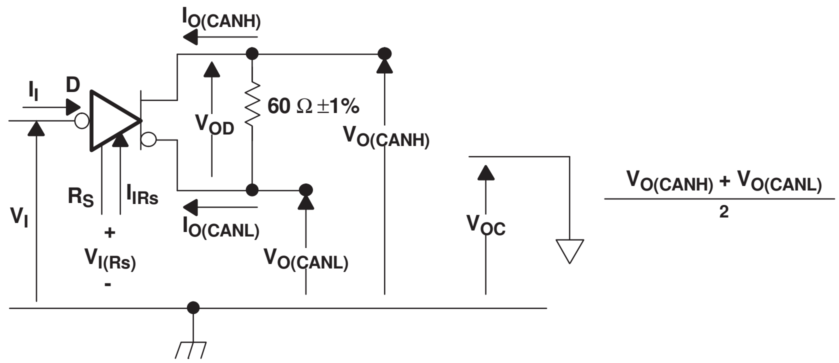


Figure 12. Driver Voltage, Current, and Test Definition

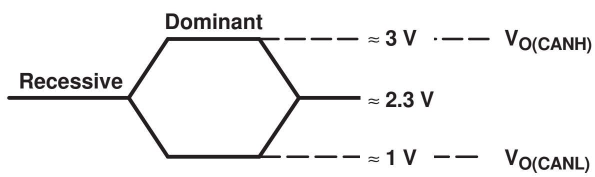


Figure 13. Bus Logic State Voltage Definitions

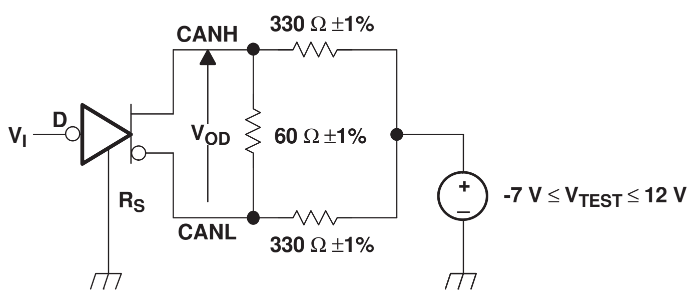
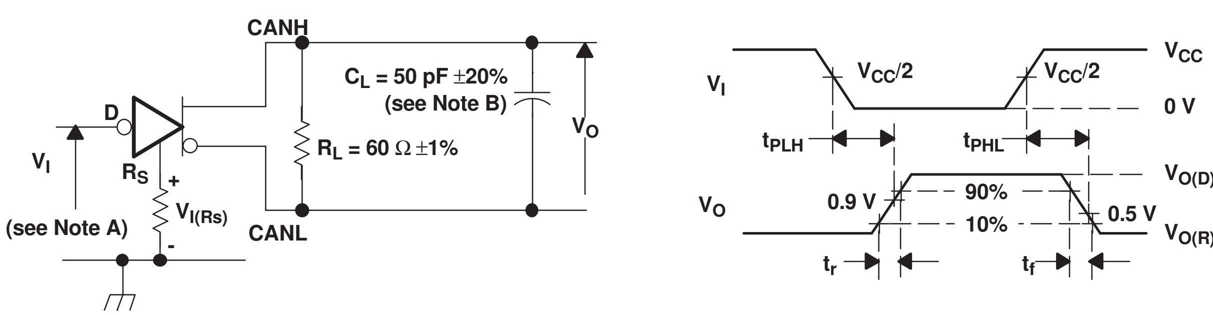


Figure 14. Driver V_{OD}



A. The input pulse is supplied by a generator having the following characteristics:
   - Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle
   - t_r ≤ 6 ns
   - t_f ≤ 6 ns
   - Z_O = 50 Ω

B. C_L includes fixture and instrumentation capacitance.

Figure 15. Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

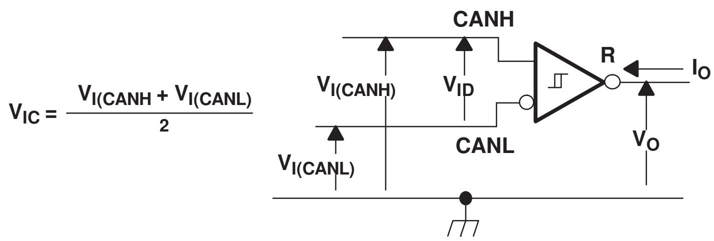
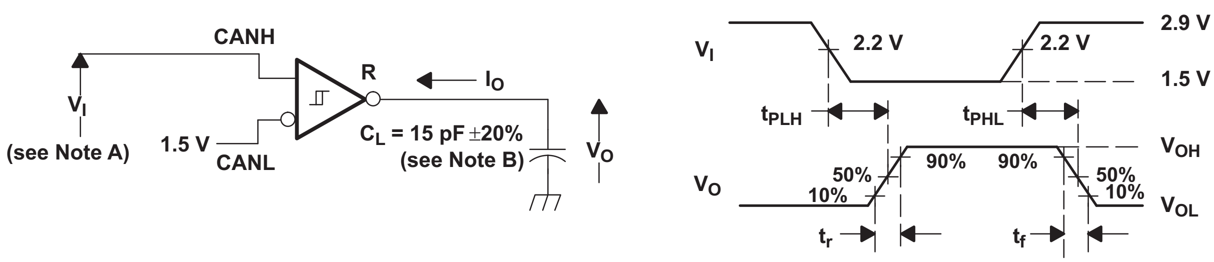


Figure 16. Receiver Voltage and Current Definitions



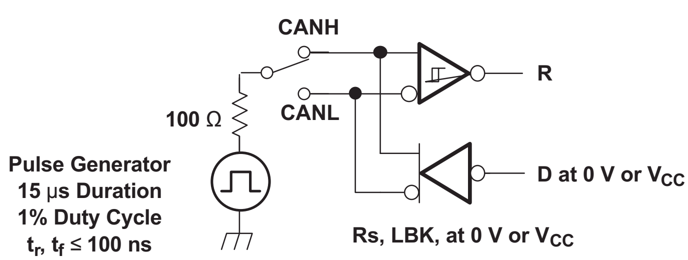
A. The input pulse is supplied by a generator having the following characteristics:
   - PRR ≤ 125 kHz, 50% duty cycle
   - t_r ≤ 6 ns
   - t_f ≤ 6 ns
   - Z_O = 50 Ω

B. C_L includes fixture and instrumentation capacitance.

Figure 17. Receiver Test Circuit and Voltage Waveforms

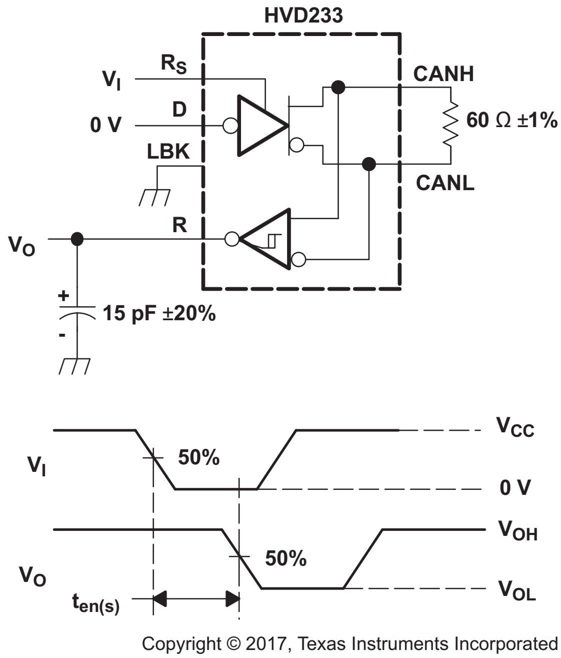
Table 1. Differential Input Voltage Threshold Test

INPUT		OUTPUT		MEASURED
V_{CANH}	V_{CANL}	R		$\|V_{ID}\|$
–6.1 V	–7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
–1 V	–7 V	L		6 V
12 V	6 V	L		6 V
–6.5 V	–7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
–7 V	–1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X



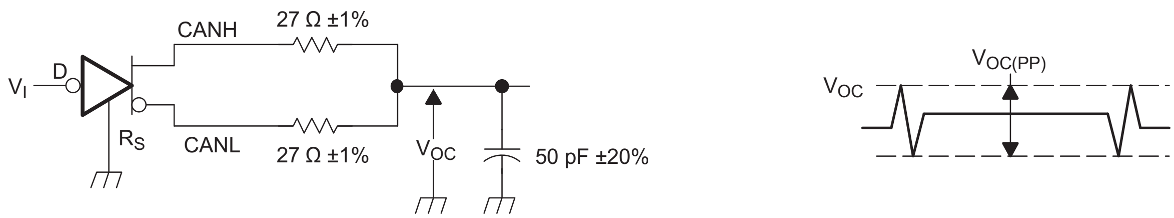
NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 18. Test Circuit, Transient Overvoltage Test



NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
- t_r or t_f ≤ 6 ns
- PRR = 125 kHz, 50% duty cycle

Figure 19. $T_{en(s)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
- t_r or t_f ≤ 6 ns
- PRR = 125 kHz, 50% duty cycle

Figure 20. $V_{OC(pp)}$ Test Circuit and Voltage Waveforms

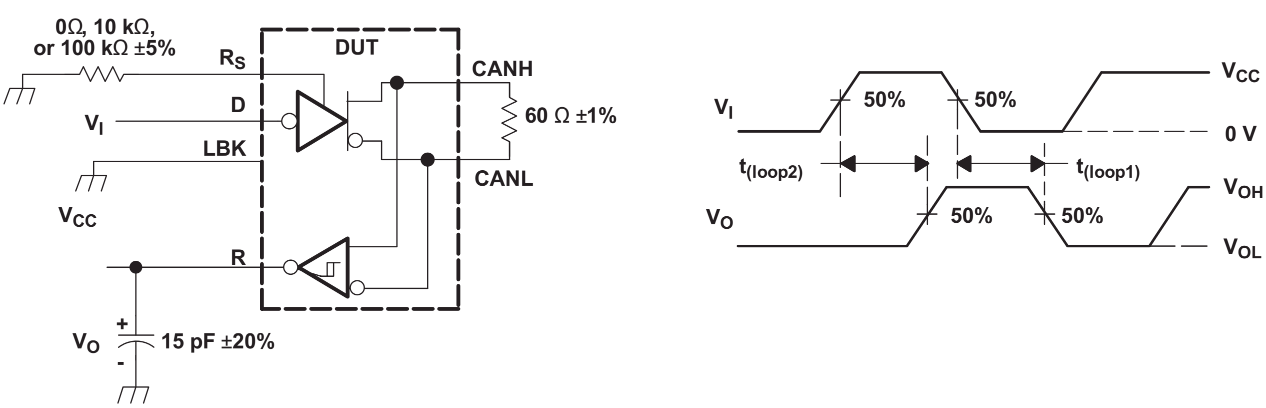


Figure 21. $T_{(loop)}$ Test Circuit and Voltage Waveforms

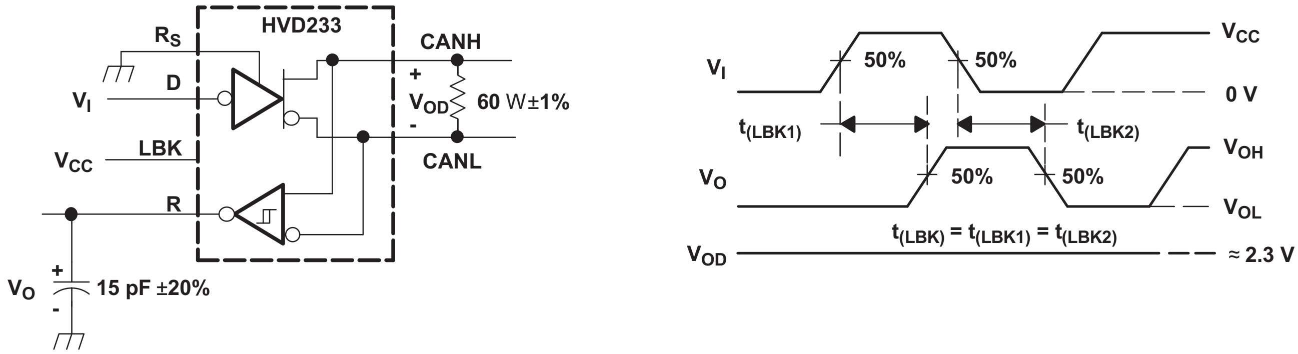


Figure 22. $T_{(LBK)}$ Test Circuit and Voltage Waveforms

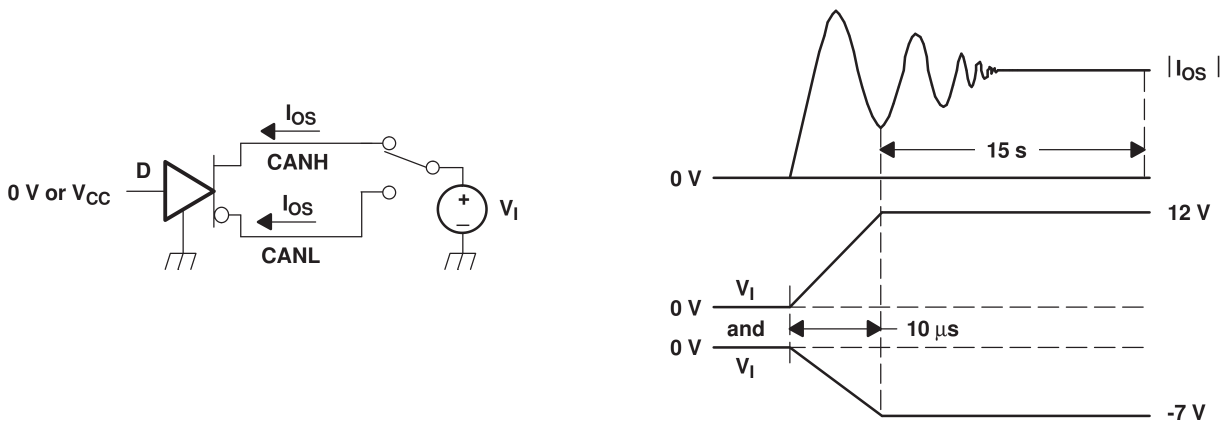
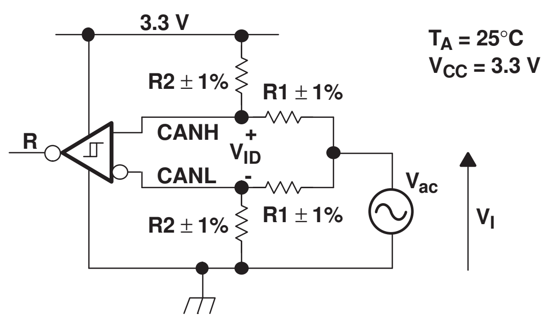
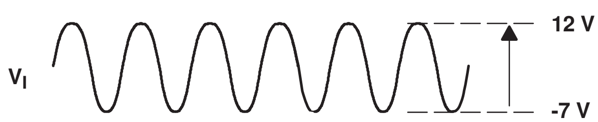


Figure 23. I_{OS} Test Circuit and Waveforms



The R Output State Does Not Change During Application of the Input Waveform.

V_{ID}	R1	R2
500 mV	50 Ω	280 Ω
900 mV	50 Ω	130 Ω



NOTE: All input pulses are supplied by a generator with $f \leq 1.5$ MHz.

Figure 24. Common-Mode Voltage Rejection

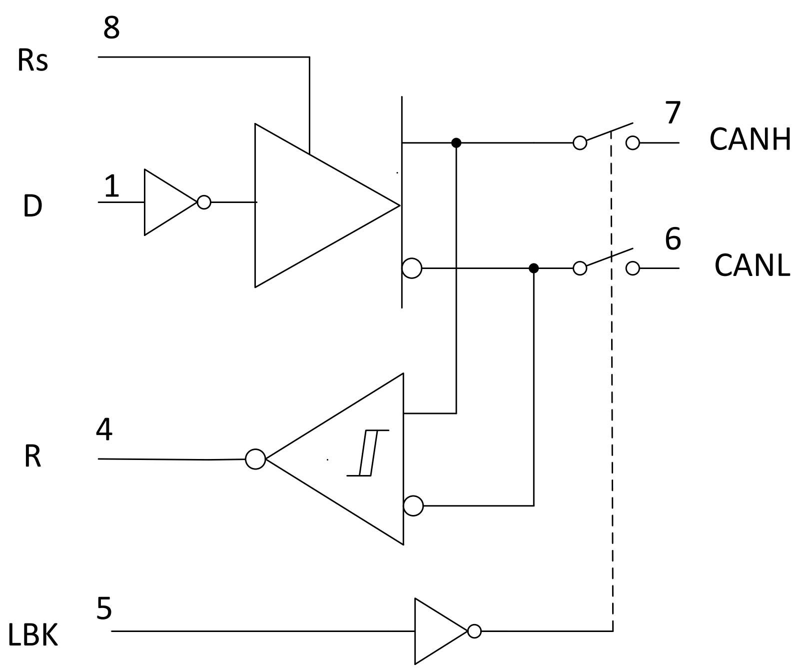
9 Detailed Description

9.1 Overview

The SN55HVD233-SEP is used in applications employing the CAN serial communication physical layer in accordance with the ISO 11898 standard. As a CAN transceiver, the device provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

Designed for operation in especially harsh environments, the SN55HVD233-SEP features cross-wire, overvoltage, and loss of ground protection to ±16 V, overtemperature (thermal shutdown) protection, and common-mode transient protection of ±100 V. This device operates over a wide –7-V to 12-V common mode range. This transceiver is the interface between the host CAN controller on the microprocessor, FPGA, or ASIC; and the differential CAN bus used in satellite applications.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Modes

The R_S, pin 8 of the SN55HVD233-SEP, provides for three modes of operation: high-speed, slope control, or low-power standby mode. The user selects the high-speed mode of operation by connecting pin 8 directly to ground, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The user can adjust the rise and fall slope by connecting a resistor to ground at pin 8, because the slope is proportional to the pin's output current. Slope control is implemented with a resistor value of 0 Ω to achieve a single ended slew rate of approximately 38-V/µs, and up to a value of 50 kΩ to achieve approximately 4-V/µs slew rate. For more information about slope control, refer to *Application and Implementation* section.

The SN55HVD233-SEP enters a low-current standby (listen-only) mode during which the driver is switched off and the receiver remains active if a high logic level is applied to pin 8. The local protocol controller reverses this low-current standby mode when it needs to transmit to the bus.

Feature Description (continued)

9.3.2 Loopback

A logic high on the loopback LBK pin 5 of the SN55HVD233-SEP places the bus output and bus input in a high-impedance state. The remaining circuit remains active and available for driver-to-receiver loopback, self-diagnostic node functions without disturbing the bus. For more information on the loopback mode, refer to the *Application Information* section.

9.3.3 CAN Bus States

The CAN bus has two states during powered operation of the device: dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to V_{CC} / 2 through the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the D and R pins (see Figure 25 and Figure 26).

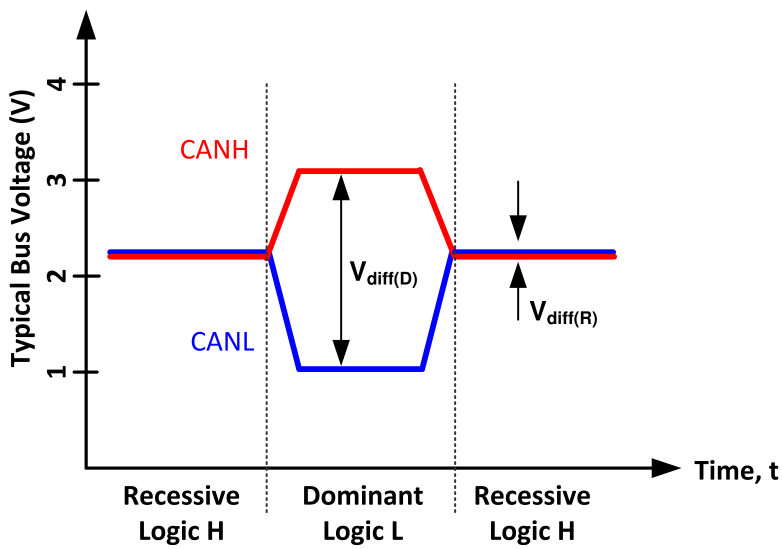


Figure 25. Bus States (Physical Bit Representation)

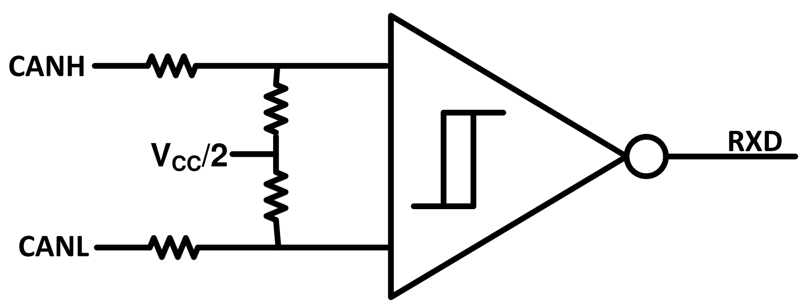


Figure 26. Simplified Recessive Common Mode Bias and Receiver

9.3.4 ISO 11898 Compliance of SN55HVD233-SEP

9.3.4.1 Introduction

Many users value the low-power consumption of operating their CAN transceivers from a 3.3-V supply. However, some users are concerned about the interoperability with 5-V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

Feature Description (continued)

9.3.4.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single-ended output signal.

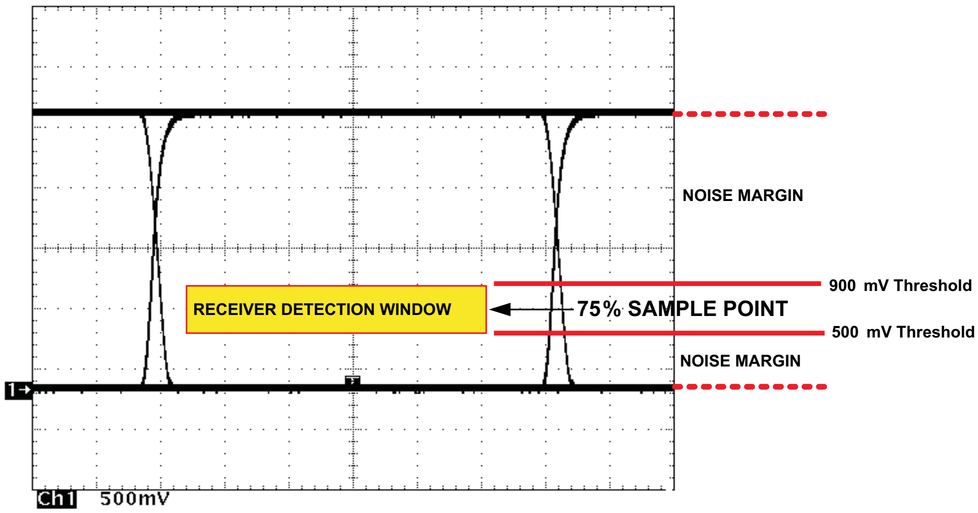


Figure 27. Typical SN55HVD233-SEP Differential Output Voltage Waveform

The CAN driver creates the difference in voltage between CANH and CANL in the dominant state. The dominant differential output of the SN55HVD233-SEP is greater than 1.5 V and less than 3 V across a 60-Ω load. The minimum required by ISO 11898 is 1.5 V and maximum is 3 V. These are the same limiting values for 5-V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state with less than 500 mV and a dominant state with more than 900-mV difference voltage on its bus inputs. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V. The SN55HVD233-SEP receiver meets these same input specifications as 5-V supplied receivers.

9.3.4.2.1 Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. The supply voltage of the CAN transceiver has nothing to do with noise. The SN55HVD233-SEP driver lowers the common-mode output in a dominant bit by a couple hundred millivolts from that of most 5-V drivers. While this does not fully comply with ISO 11898, this small variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins, or error rates.

9.3.4.3 Interoperability of 3.3-V CAN in 5-V CAN Systems

The 3.3-V supplied CAN transceivers are electrically interchangeable with 5-V CAN transceivers. The differential output is the same. The recessive common mode output is the same. The dominant common mode output voltage is a couple hundred millivolts lower than 5-V supplied drivers, while the receivers exhibit identical specifications as 5-V devices.

To help ensure the widest interoperability possible, the SN55HVD233-SEP successfully passed the internationally recognized GIFT ICT conformance and interoperability testing for CAN transceivers. Electrical interoperability does not always assure interchangeability, however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure full interchangeability. Interchangeability is ensured with thorough equipment testing.

Feature Description (continued)

9.3.5 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold, the device turns off the CAN driver circuits thus blocking the D pin to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device. The CAN bus pins are high-impedance biased to recessive level during a thermal shutdown, and the receiver-to-R pin path remains operational.

9.4 Device Functional Modes

Table 2. Driver I/O

DRIVER[1]					
INPUTS			OUTPUTS		
D	LBK	RS	CANH	CANL	BUS STATE
X	X	> 0.75 V_{CC}	Z	Z	Recessive
L	L or open	≤ 0.33 V_{CC}	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	≤ 0.33 V_{CC}	Z	Z	Recessive

(1) H = High level; L = Low level; Z = High impedance; X = Irrelevant

Table 3. Receiver I/O

RECEIVER[1]			
INPUTS			OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	D	R
Dominant	$V_{ID} \geq 0.9$ V	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	H or open	H
?	0.5 V < V_{ID} < 0.9 V	H or open	?
Dominant	$V_{ID} \geq 0.9$ V	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	H	H
Recessive	$V_{ID} \leq 0.5$ V or open	L	L
?	0.5 V < V_{ID} < 0.9 V	L	L

(1) H = High level; L = Low level; Z = High impedance; X = Irrelevant; ? = Indeterminate

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Diagnostic Loopback

The diagnostic loopback or internal loopback function of the SN55HVD233-SEP is enabled with a high-level input on pin 7, LBK. This mode disables the driver output while keeping the bus pins biased to the recessive state. This mode also redirects the D data input (transmit data) through logic to the received data output (R), thus creating an internal loopback of the transmit-to-receive data path. This mimics the loopback that occurs normally with a CAN transceiver because the receiver loops back the driven output to the R (receive data) pin. This mode allows the host microprocessor to input and read back a bit sequence or CAN messages to perform diagnostic routines without disturbing the CAN bus. Figure 33 shows a typical CAN bus application.

If the LBK pin is not used, it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

Application Information (continued)

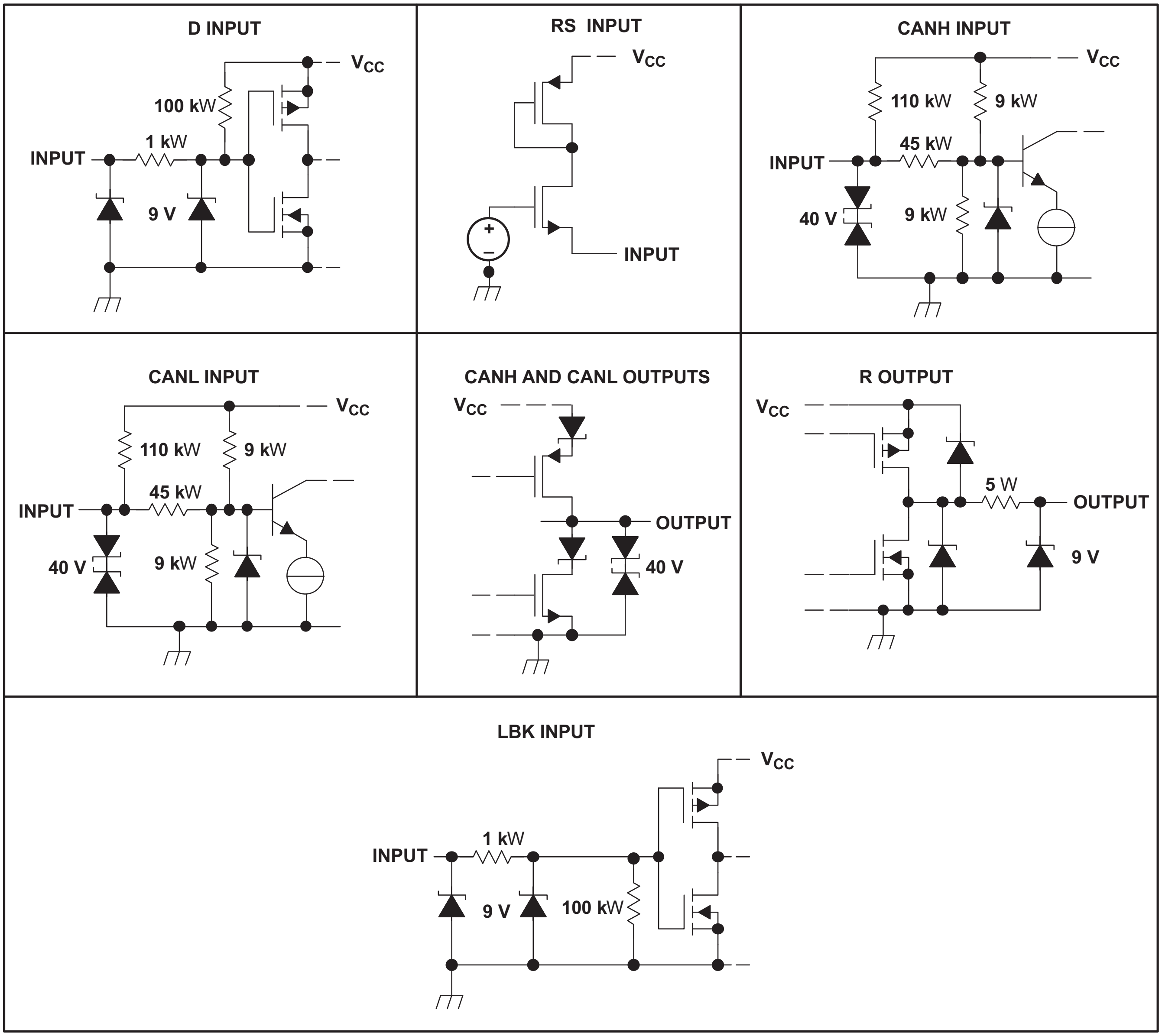


Figure 28. Equivalent Input and Output Schematic Diagrams

10.2 Typical Application

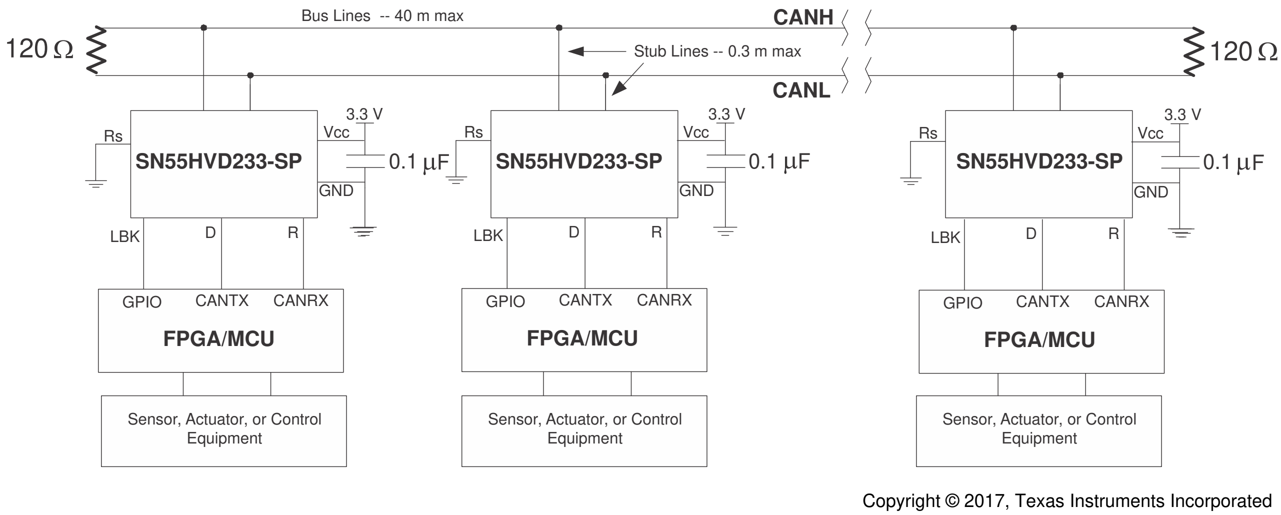


Figure 29. Typical Application Schematic

10.2.1 Design Requirements

The High-Speed ISO 11898 Standard specifications are given for a maximum signaling rate of 1 Mbps with a bus length of 40 m and a maximum of 30 nodes. It also recommends a maximum unterminated stub length of 0.3 m. The cable is specified to be a shielded or unshielded twisted-pair with a 120-Ω characteristic impedance (ZO). The standard defines a single line of twisted-pair cable with the network topology as shown in Figure 29. It is terminated at both ends with 120-Ω resistors, which match the characteristic impedance of the line to prevent signal reflections. According to ISO 11898, placing RL on a node should be avoided because the bus lines lose termination if the node is disconnected from the bus.

10.2.2 Detailed Design Procedure

Table 4. Suggested Cable Length vs Signaling Rate

BUS LENGTH (m)	SIGNALING RATE (Mbps)
40	1
100	0.5
200	0.25
500	0.1
1000	0.05

Basically, the maximum bus length is determined by, or rather is a trade-off with the selected signaling rate as listed in Table 4.

A signaling rate decreases as transmission distance increases. While steady-state losses may become a factor at the longest transmission distances, the major factors limiting signaling rate as distance is increased are time varying. Cable bandwidth limitations, which degrade the signal transition time and introduce inter-symbol interference (ISI), are primary factors reducing the achievable signaling rate when transmission distance is increased.

For a CAN bus, the signaling rate is also determined from the total system delay – down and back between the two most distant nodes of a system and the sum of the delays into and out of the nodes on a bus with the typical 5-ns/m prop delay of a twisted-pair cable. Also, consideration must be given the signal amplitude loss due to resistance of the cable and the input resistance of the transceivers. Under strict analysis, skin effects, proximity to other circuitry, dielectric loss, and radiation loss effects all act to influence the primary line parameters and degrade the signal.

A conservative rule of thumb for bus lengths over 100 m is derived from the product of the signaling rate in Mbps and the bus length in m, which should be less than or equal to 50.

Signaling Rate (Mbps) × Bus Length (m) ≤ 50. Operation at extreme temperatures should employ additional conservatism.

10.2.2.1 Slope Control

Adjust the rise and fall slope of the SN55HVD233-SEP driver output by connecting a resistor from the RS (pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 30.

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value ranging from 0 Ω to achieve a ≈38-V/µs single ended slew rate, and up to 50 kΩ to achieve a ≈4-V/µs slew rate as displayed in Figure 31. Figure 32 shows typical driver output waveforms with slope control.

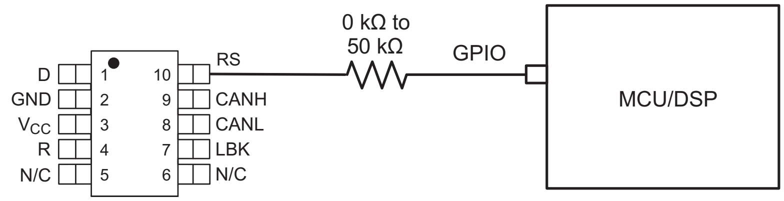


Figure 30. Slope Control/Standby Connection to a DSP

10.2.2.2 Standby

If a high-level input (> 0.75 V_{CC}) is applied to RS (pin 8), the circuit enters a low-current, listen-only standby mode during which the driver is switched off and the receiver remains active. The local controller can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage > 900-mV typical) occurs on the bus.

10.2.3 Application Curves

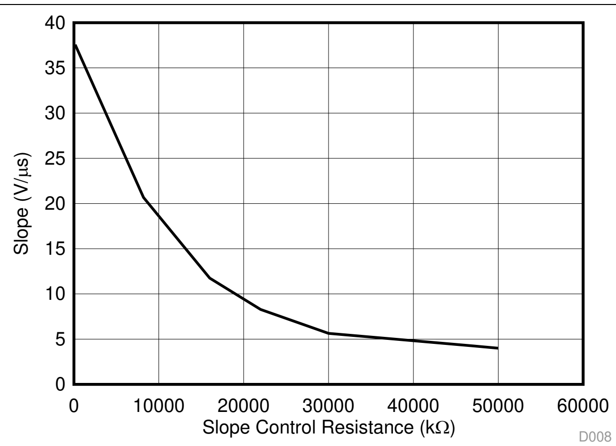


Figure 31. HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

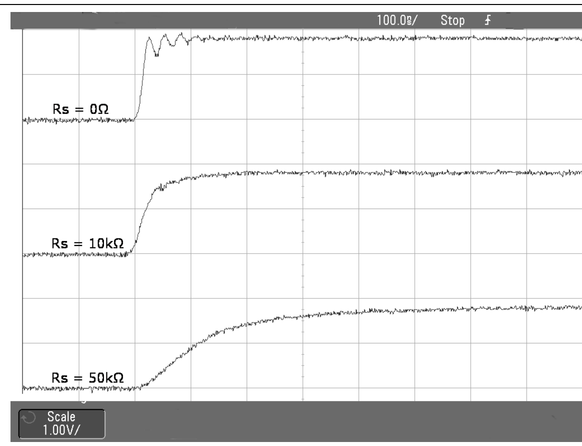


Figure 32. Typical SN55HVD233-SEP 250-Kbps Output Pulse Waveforms With Slope Control

11 Power Supply Recommendations

TI recommends to have localized capacitive decoupling near device VCC pin to GND. Values of 4.7 µF at VCC pin and 10 µF, 1 µF, and 0.1 µF at supply have tested well on evaluation modules.

12 Layout

12.1 Layout Guidelines

Minimize stub length from node insertion to bus.

12.1.1 Bus Loading, Length, and Number of Nodes

The ISO11898 standard specifies up to 1-Mbps data rate, maximum bus length of 40 m, maximum drop line (stub) length of 0.3 m, and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet, and NMEA200.

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the SN55HVD233-SEP CAN. ISO11898-2 specifies the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel), and the differential output must be greater than 1.5 V. The SN55HVD233-SEP is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common mode range of –2 V to 7 V through a 330-Ω coupling network. This network represents the bus loading of 120 SN55HVD233-SEP transceivers based on their minimum differential input resistance of 40 kΩ. Therefore, the SN55HVD233-SEP supports up to 120 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets, and signal integrity; thus, a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes, and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO11898 CAN standard. Using this flexibility requires good network design.

12.1.2 CAN Termination

The ISO11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Use resistors equal to the characteristic impedance of the line to terminate both ends of the cable to prevent signal reflections. Keep unterminated drop lines (stubs) connecting nodes to the bus as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

Layout Guidelines (continued)

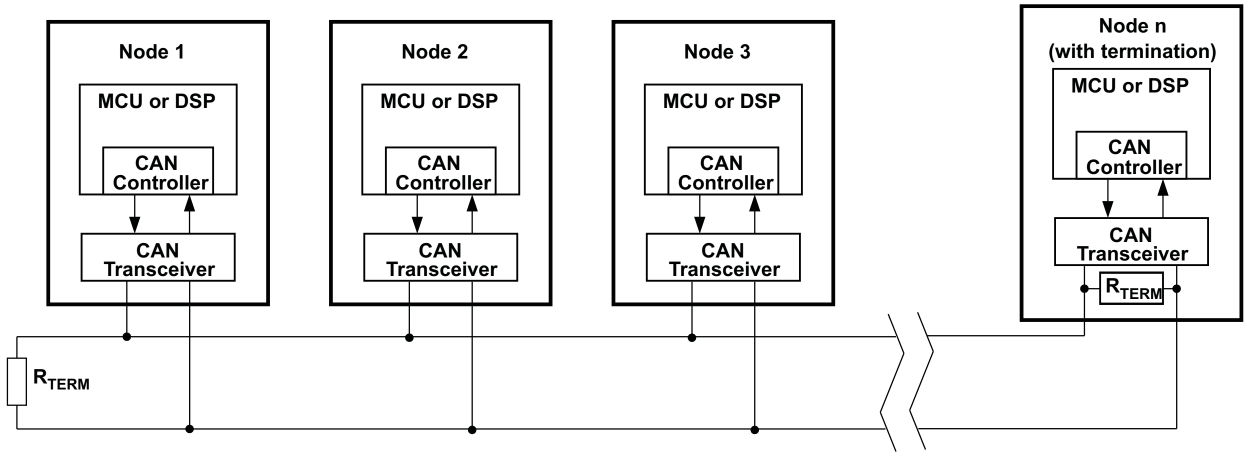


Figure 33. Typical CAN Bus

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then the user may use split termination (see Figure 34). Split termination uses two 60-Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Take care with the power ratings of the termination resistors used, especially for the worst-case condition (if a system power supply is shorted across the termination resistance to ground). In most cases, under the worst-case condition, much higher current passes through the termination resistance than the CAN transceiver's current limit.

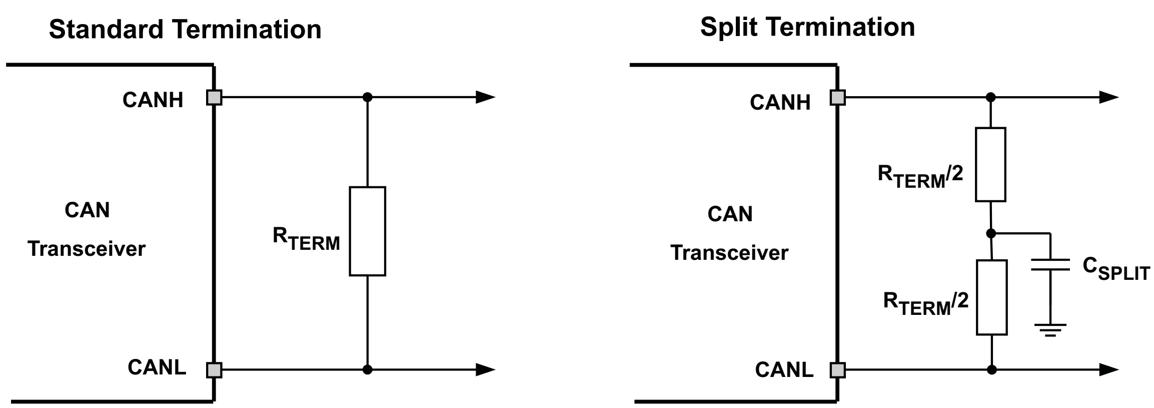


Figure 34. CAN Bus Termination Concepts

12.2 Layout Example

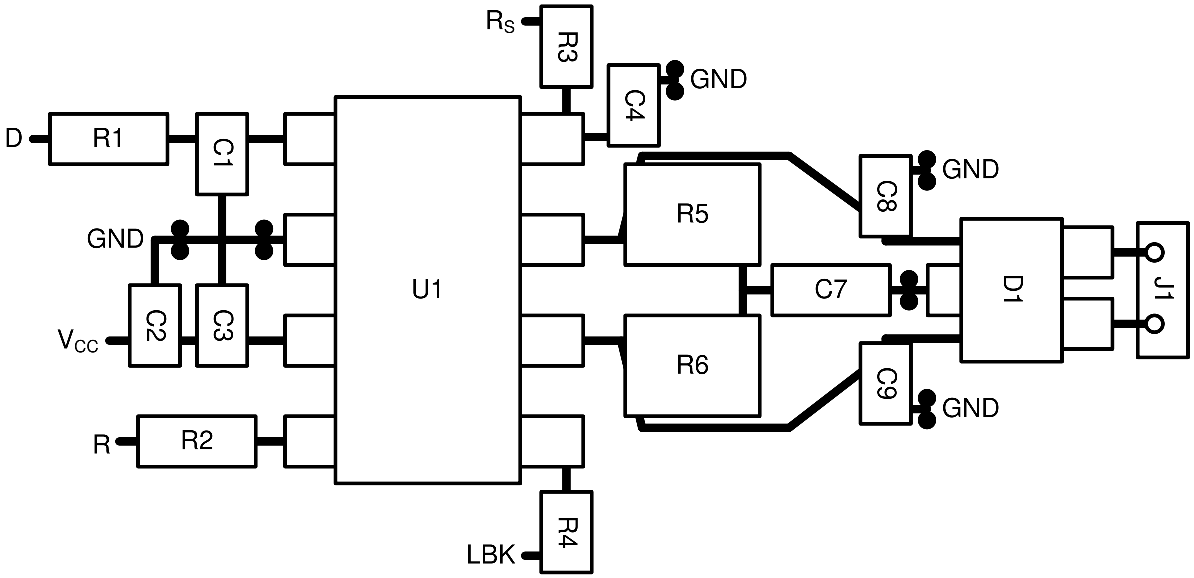


Figure 35. Board Layout Example

13 デバイスおよびドキュメントのサポート

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN55HVD233MDPSEP	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	33PSEP
SN55HVD233MDPSEP.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	33PSEP
SN55HVD233MDTPSEP	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	33PSEP
SN55HVD233MDTPSEP.A	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	33PSEP
V62/18617-01XE	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	33PSEP
V62/18617-01XE-T	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	33PSEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

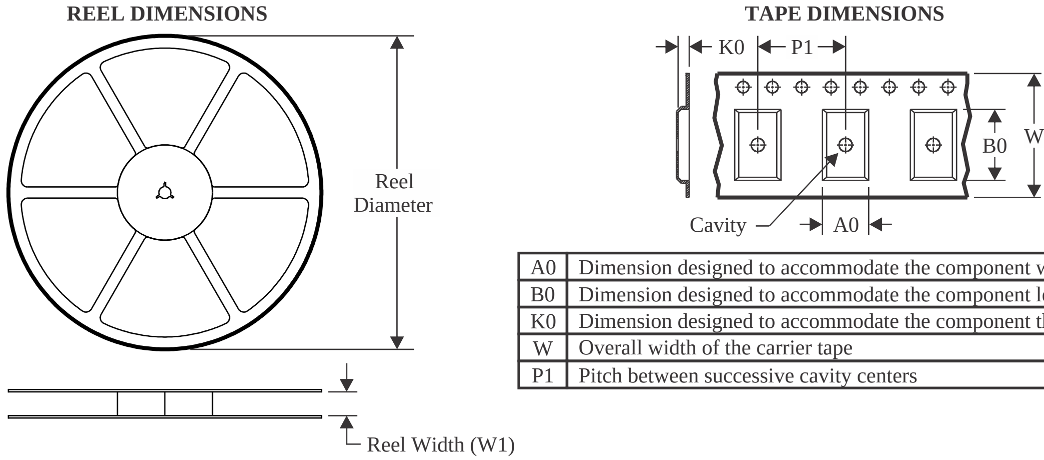
OTHER QUALIFIED VERSIONS OF SN55HVD233-SEP :

- Space : SN55HVD233-SP

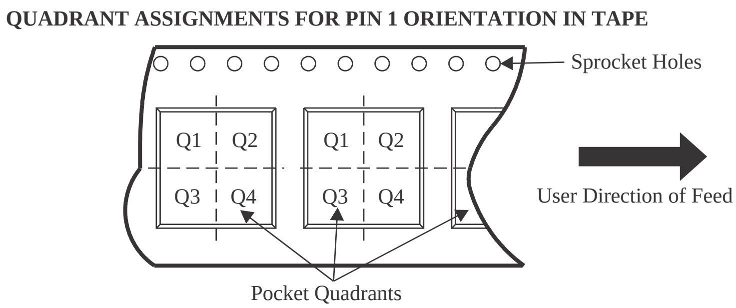
NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



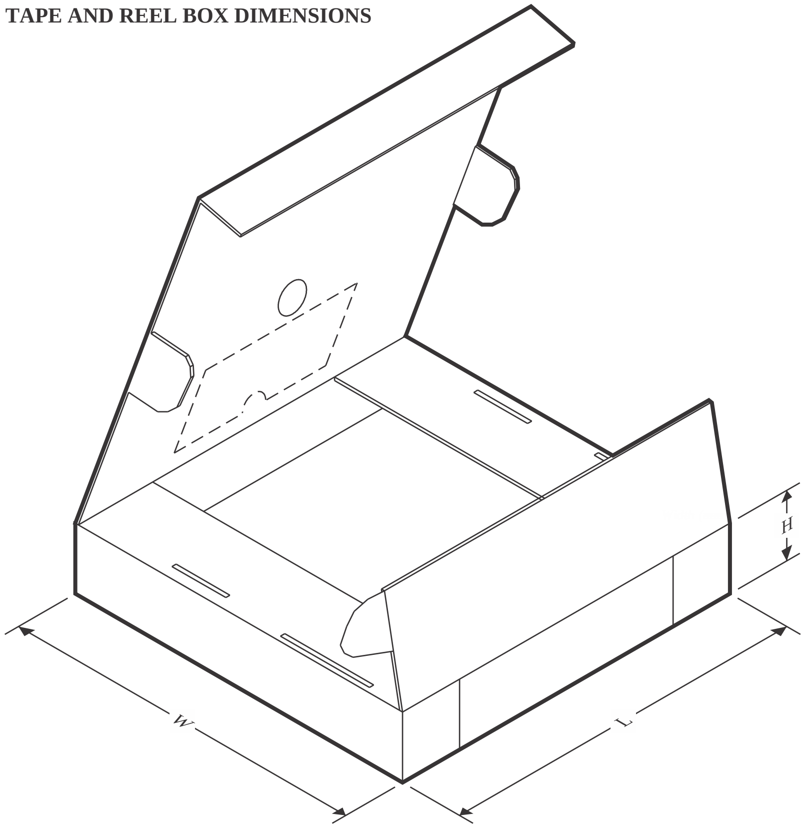
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN55HVD233MDTPSEP	SOIC	D	8	250	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

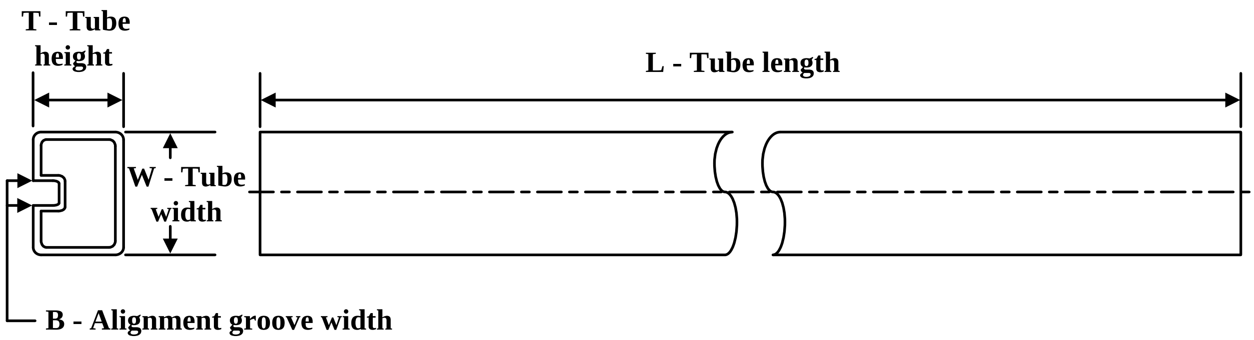
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

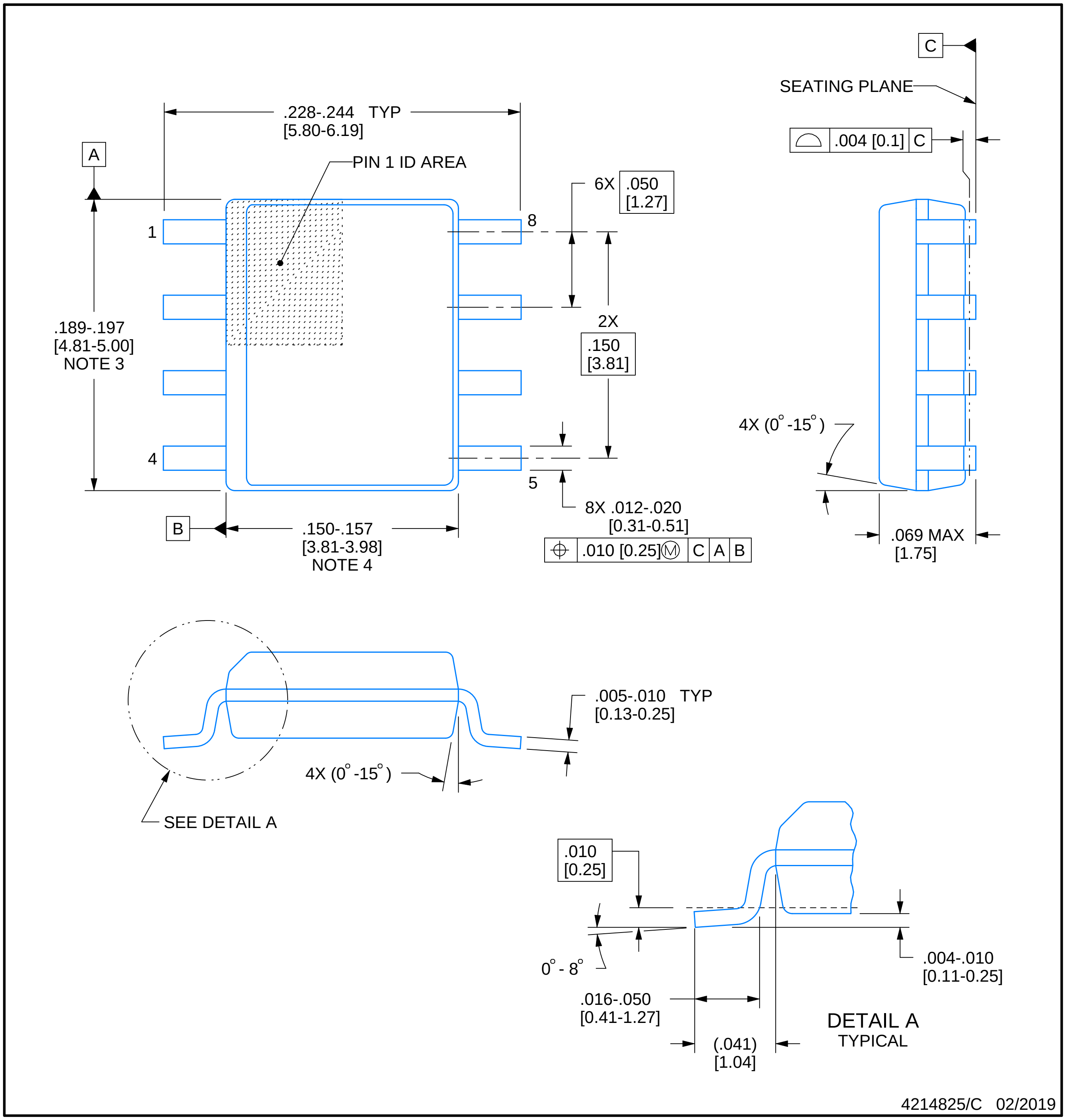
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN55HVD233MDTPSEP	SOIC	D	8	250	340.5	336.1	25.0

TUBE



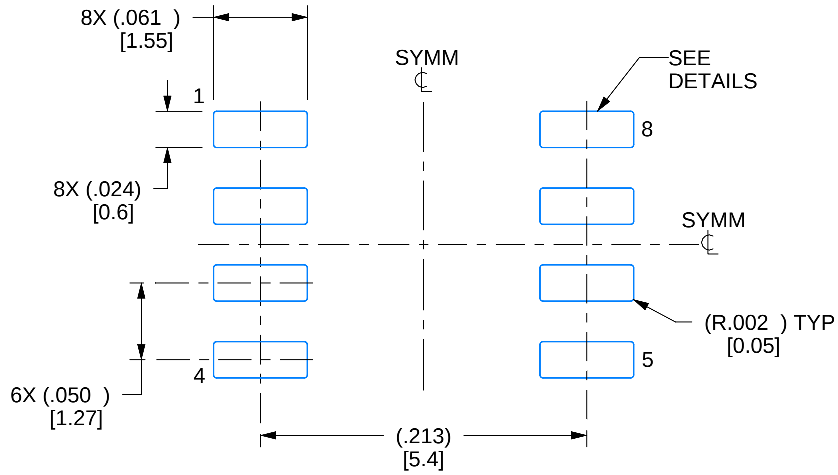
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN55HVD233MDPSEP	D	SOIC	8	75	507	8	3940	4.32
SN55HVD233MDPSEP.A	D	SOIC	8	75	507	8	3940	4.32
V62/18617-01XE-T	D	SOIC	8	75	507	8	3940	4.32

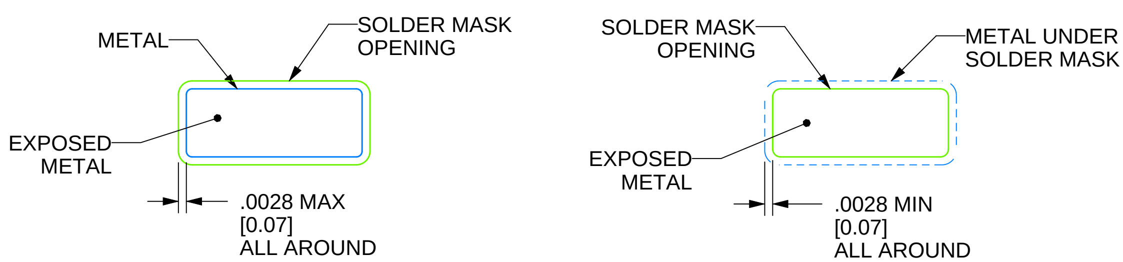


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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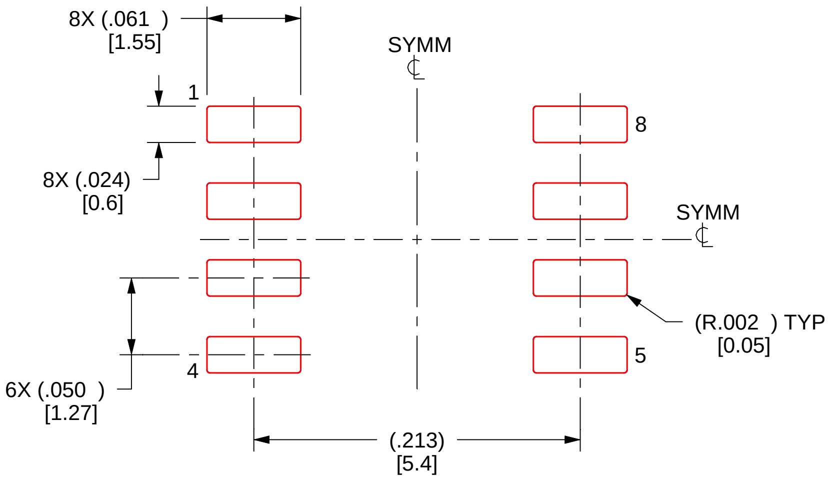
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項