SN54SC4T125-SEP 耐放射線特性、単電源 4 バッファ トランスレータ ゲート、3 ステート出力 CMOS ロジック レベル シフタ付き

1 特長

- VID V62/23631-01XE
- 放射線耐性
  - 125℃において 43MeV-cm^2/mg のシングル イベント ラッチアップ (SEL) 耐性
  - すべてのウェハー ロットについての 30krad(Si) までの吸収線量耐性放射線ロット受け入れテスト (TID RLAT)
  - シングル イベント過渡 (SET) 特性:LET = 43MeV-cm^2/mg (最大値)
- 広い動作範囲:1.2V～5.5V
- 単一電源電圧レベル シフタ:
  - 昇圧変換:
    - 1.2V から 1.8V
    - 1.5V から 2.5V
    - 1.8V から 3.3V
    - 3.3V から 5.0V
  - 降圧変換:
    - 5.0V、3.3V、2.5V から 1.8V
    - 5.0V、3.3V から 2.5V
    - 5.0V から 3.3V
- 5.5V 許容入力ピン
- 標準ピン配置をサポート
- 5V または 3.3V の V_{CC} で最大 150Mbps
- JESD 17 準拠で 250mA 超のラッチアップ性能
- 宇宙向けに強化されたプラスチック
  - 管理されたベースライン
  - Au ボンド・ワイヤと NiPdAu リード仕上げ
  - NASA ASTM E595 アウトガス仕様に適合
  - 単一の製造、アセンブリ、テスト施設
  - 長い製品ライフ・サイクル
  - 製品のトレーサビリティ

2 アプリケーション

- デジタル信号のイネーブルまたはディセーブル
- インジケータ LED の制御
- 通信モジュールとシステム・コントローラの間のレベル変換

3 概要

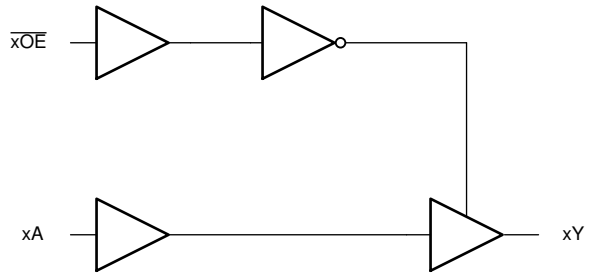
SN54SC4T125-SEP は、4 つの独立した 3 ステート出力付きバッファを内蔵し、広い電圧範囲で動作してレベル変換を実現します。各バッファはブール関数 Y = A を正論理で実行します。$\overline{OE}$ ピンに HIGH を印加することで、出力をハイ・インピーダンス (Hi-Z) 状態にできます。出力レベルは電源電圧 (V_{CC}) を基準としており、1.8V、2.5V、3.3V、5V の CMOS レベルをサポートしています。

入力は低スレッショルド回路を使用して設計され、低電圧 CMOS 入力の昇圧変換 (例:1.2V 入力から 1.8V 出力、1.8V 入力から 3.3V 出力) をサポートします。また、5V 許容入力ピンにより、降圧変換 (例:3.3V から 2.5V 出力) が可能です。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ (2)	本体サイズ (公称)(3)
SN54SC4T125-SEP	PW (TSSOP、14)	5mm × 6.4mm	5mm × 4.4mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



概略論理図 (正論理)

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4 Pin Configuration and Functions

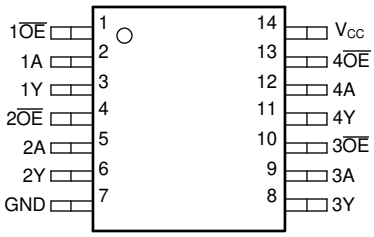


図 4-1. PW Package, 14-Pin TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1$\overline{OE}$	1	I	Channel 1, output enable, active low
1A	2	I	Channel 1, input A
1Y	3	O	Channel 1, output Y
2$\overline{OE}$	4	I	Channel 2, output enable, active low
2A	5	I	Channel 2, input A
2Y	6	O	Channel 2, output Y
GND	7	G	Ground
3Y	8	O	Channel 3, output Y
3A	9	I	Channel 3, input A
3$\overline{OE}$	10	I	Channel 3, output enable, active low
4Y	11	O	Channel 4, output Y
4A	12	I	Channel 4, input A
4$\overline{OE}$	13	I	Channel 4, output enable, active low
V_{CC}	14	P	Positive supply

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5 V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.2	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
V_{IH}	High-level input voltage	V_{CC} = 1.2 V to 1.3 V	0.78		V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 2 V	1.1		V
		V_{CC} = 2.25 V to 2.75 V	1.28		
		V_{CC} = 3 V to 3.6 V	1.45		
		V_{CC} = 4.5 V to 5.5 V	2		
V_{IL}	Low-Level input voltage	V_{CC} = 1.2 V to 1.3 V		0.18	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.65 V to 2 V		0.5	V
		V_{CC} = 2.25 V to 2.75 V		0.65	
		V_{CC} = 3 V to 3.6 V		0.75	
		V_{CC} = 4.5 V to 5.5 V		0.85	
I_O	Output current	V_{CC} = 1.6 V to 2 V		±3	mA
		V_{CC} = 2.25 V to 2.75 V		±7	
		V_{CC} = 3.3 V to 5.0 V		±15	
I_O	Output Current	V_{CC} = 4.5 V to 5.5 V		±25	mA

5.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.6 V to 5.0 V		20	ns/V
T_A	Operating free-air temperature		-55	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		SN54SC4T125-SEP PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	90.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = -50 µA	1.2 V to 5.5 V	V_{CC}-0.2			V
	I_{OH}= -50 µA	1.65 V to 5.5 V	V_{CC}-0.1			
	I_{OH} = -1 mA	1.2 V	0.8			
	I_{OH} = -2 mA	1.65 V to 2 V	1.21	1.7(1)		
	I_{OH} = -3 mA	2.25 V to 2.75 V	1.93	2.4(1)		
	I_{OH} = -5.5 mA	3 V to 3.6 V	2.49	3.08(1)		
	I_{OH} = -8 mA	4.5 V to 5.5 V	3.95	4.65(1)		
	I_{OH}= –24 mA	4.5 V to 5.5 V	3.15			
V_{OL}	I_{OL}= 50 µA	1.2 V to 5.5 V			0.1	V
	I_{OL}= 50 µA	1.65 V to 5.5 V			0.1	
	I_{OL} = 1 mA	1.2 V			0.2	
	I_{OL} = 2 mA	1.65 V to 2 V		0.1(1)	0.25	
	I_{OL} = 3 mA	2.25 V to 2.75 V		0.1(1)	0.2	
	I_{OL} = 5.5 mA	3 V to 3.6 V		0.2(1)	0.25	
	I_{OL}= 8 mA	4.5 V to 5.5 V		0.3(1)	0.35	
	I_{OL}= 24 mA	4.5 V to 5.5 V			0.75	
I_I	V_I = 0 V or V_{CC}	0 V to 5.5 V		±0.1	±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	1.2 V to 5.5 V		2	93	µA
ΔI_{CC}	One input at 0.3 V or 3.4 V, other inputs at 0 or V_{CC}, I_O = 0	5.5 V		1.35	1.5	mA
	One input at 0.3 V or 1.1 V, other inputs at 0 or V_{CC}, I_O = 0	1.8 V			68	µA
C_I	V_I = V_{CC} or GND	5 V		3	5	pF
C_O	V_O = V_{CC} or GND	5 V		5	8	pF

5.5 Electrical Characteristics (続き)

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{OZ}	V_O = V_{CC} or GND and V_{CC} = 5.5 V	5.5 V			±2.5	μA
C_{PD} (2) (3)	C_L = 50 pF, F = 10 MHz	1.2 V to 5.5 V		11	25	pF

(1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)
(2) C_{PD} is used to determine the dynamic power consumption, per channel.
(3) P_D= V_{CC} ^{2}xF_Ix(C_{PD}+ C_L) where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage.

5.6 Switching Characteristics

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	MIN	TYP	MAX	UNIT
t_{PHL}	A	Y	C_L = 15 pF	1.2 V		41.8	178.9	ns
t_{PLH}	A	Y	C_L = 15 pF	1.2 V		27.8	163.6	ns
t_{PHZ}	OE	Y	C_L = 15 pF	1.2 V		29.8	66.2	ns
t_{PLZ}	OE	Y	C_L = 15 pF	1.2 V		26.7	59.2	ns
t_{PZH}	OE	Y	C_L = 15 pF	1.2 V		41.6	101.4	ns
t_{PZL}	OE	Y	C_L = 15 pF	1.2 V		40.4	100.7	ns
t_{PHL}	A	Y	C_L = 50 pF	1.2 V		46.4	200.2	ns
t_{PLH}	A	Y	C_L = 50 pF	1.2 V		42.6	176.2	ns
t_{PHZ}	OE	Y	C_L = 50 pF	1.2 V		40.8	78.2	ns
t_{PLZ}	OE	Y	C_L = 50 pF	1.2 V		37.8	71.7	ns
t_{PZH}	OE	Y	C_L = 50 pF	1.2 V		47.5	113.6	ns
t_{PZL}	OE	Y	C_L = 50 pF	1.2 V		46.3	113.8	ns
t_{PHL}	A	Y	C_L = 15 pF	1.8 V		15.6	40.1	ns
t_{PLH}	A	Y	C_L = 15 pF	1.8 V		11.8	40.1	ns
t_{PHZ}	OE	Y	C_L = 15 pF	1.8 V		13.0	20.9	ns
t_{PLZ}	OE	Y	C_L = 15 pF	1.8 V		11.7	18.5	ns
t_{PZH}	OE	Y	C_L = 15 pF	1.8 V		17.4	33.3	ns
t_{PZL}	OE	Y	C_L = 15 pF	1.8 V		16.8	32.3	ns
t_{PHL}	A	Y	C_L = 50 pF	1.8 V		21.0	46.7	ns
t_{PLH}	A	Y	C_L = 50 pF	1.8 V		16.1	46.7	ns
t_{PHZ}	OE	Y	C_L = 50 pF	1.8 V		19.7	28.2	ns
t_{PLZ}	OE	Y	C_L = 50 pF	1.8 V		18.6	25.9	ns
t_{PZH}	OE	Y	C_L = 50 pF	1.8 V		19.9	37.1	ns
t_{PZL}	OE	Y	C_L = 50 pF	1.8 V		19.1	35.8	ns
t_{PHL}	A	Y	C_L = 15 pF	2.5 V		10.6	24.0	ns
t_{PLH}	A	Y	C_L = 15 pF	2.5 V		7.1	24.0	ns
t_{PHZ}	OE	Y	C_L = 15 pF	2.5 V		8.2	12.6	ns
t_{PLZ}	OE	Y	C_L = 15 pF	2.5 V		7.4	11.1	ns
t_{PZH}	OE	Y	C_L = 15 pF	2.5 V		10.4	19.8	ns
t_{PZL}	OE	Y	C_L = 15 pF	2.5 V		9.9	19.0	ns
t_{PHL}	A	Y	C_L = 50 pF	2.5 V		13.5	25.4	ns
t_{PLH}	A	Y	C_L = 50 pF	2.5 V		10.1	25.4	ns
t_{PHZ}	OE	Y	C_L = 50 pF	2.5 V		13.1	18.5	ns

5.6 Switching Characteristics (続き)

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	MIN	TYP	MAX	UNIT
t_{PLZ}	OE	Y	C_L = 50 pF	2.5 V		12.0	16.4	ns
t_{PZH}	OE	Y	C_L = 50 pF	2.5 V		12.0	22.5	ns
t_{PZL}	OE	Y	C_L = 50 pF	2.5 V		11.1	21.5	ns
t_{PHL}	A	Y	C_L = 15 pF	3.3 V		7.9	15.2	ns
t_{PLH}	A	Y	C_L = 15 pF	3.3 V		5.4	13.8	ns
t_{PHZ}	OE	Y	C_L = 15 pF	3.3 V		6.0	9.9	ns
t_{PLZ}	OE	Y	C_L = 15 pF	3.3 V		5.3	8.2	ns
t_{PZH}	OE	Y	C_L = 15 pF	3.3 V		7.9	14.1	ns
t_{PZL}	OE	Y	C_L = 15 pF	3.3 V		7.4	13.5	ns
t_{PHL}	A	Y	C_L = 50 pF	3.3 V		10.2	18.3	ns
t_{PLH}	A	Y	C_L = 50 pF	3.3 V		7.8	16.0	ns
t_{PHZ}	OE	Y	C_L = 50 pF	3.3 V		9.7	15.1	ns
t_{PLZ}	OE	Y	C_L = 50 pF	3.3 V		9.2	12.9	ns
t_{PZH}	OE	Y	C_L = 50 pF	3.3 V		9.1	16.4	ns
t_{PZL}	OE	Y	C_L = 50 pF	3.3 V		8.3	15.3	ns
t_{PHL}	A	Y	C_L = 15 pF	5 V		5.3	10.2	ns
t_{PLH}	A	Y	C_L = 15 pF	5 V		4.2	9.9	ns
t_{PHZ}	OE	Y	C_L = 15 pF	5 V		4.6	7.5	ns
t_{PLZ}	OE	Y	C_L = 15 pF	5 V		4.2	6.1	ns
t_{PZH}	OE	Y	C_L = 15 pF	5 V		5.6	9.6	ns
t_{PZL}	OE	Y	C_L = 15 pF	5 V		5.1	8.9	ns
t_{PHL}	A	Y	C_L = 50 pF	5 V		7.1	12.5	ns
t_{PLH}	A	Y	C_L = 50 pF	5 V		5.8	11.5	ns
t_{PHZ}	OE	Y	C_L = 50 pF	5 V		6.9	10.9	ns
t_{PLZ}	OE	Y	C_L = 50 pF	5 V		6.8	9.1	ns
t_{PZH}	OE	Y	C_L = 50 pF	5 V		6.6	11.0	ns
t_{PZL}	OE	Y	C_L = 50 pF	5 V		5.7	10.0	ns

5.7 Noise Characteristics

VCC = 5 V, CL = 50 pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4	5		V
$V_{IH(D)}$	High-level dynamic input voltage	2.1			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.5	V

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

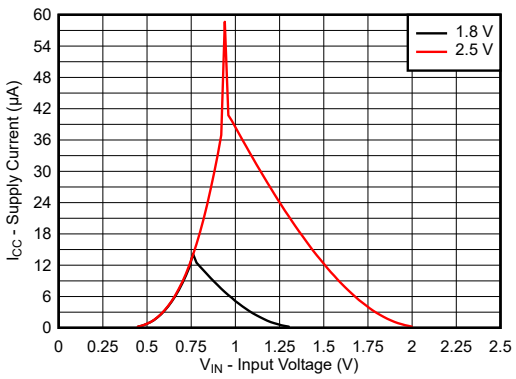


図 5-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

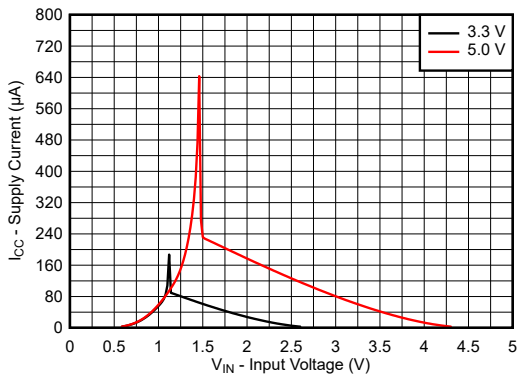


図 5-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply

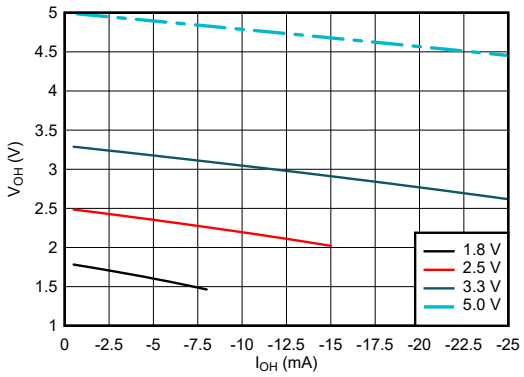


図 5-3. Output Voltage vs Current in HIGH State

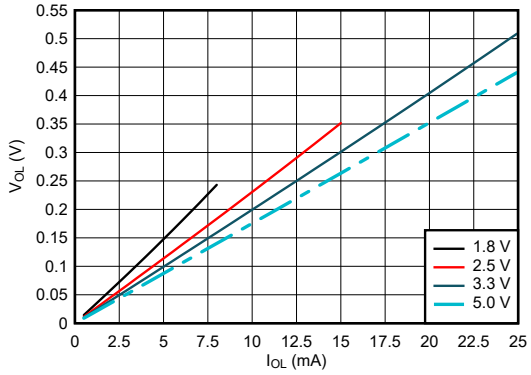


図 5-4. Output Voltage vs Current in LOW State

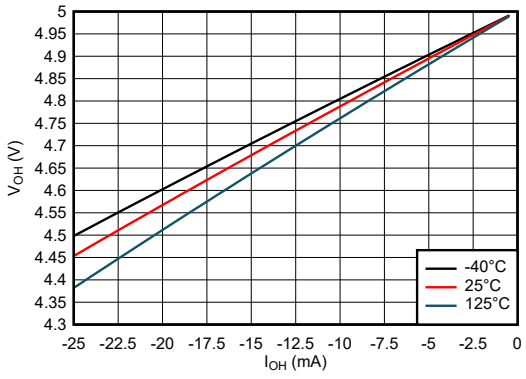


図 5-5. Output Voltage vs Current in HIGH State; 5-V Supply

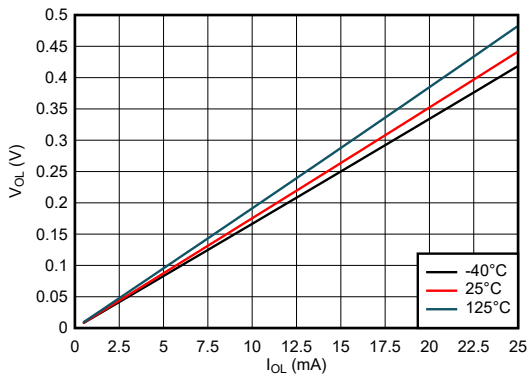


図 5-6. Output Voltage vs Current in LOW State; 5-V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

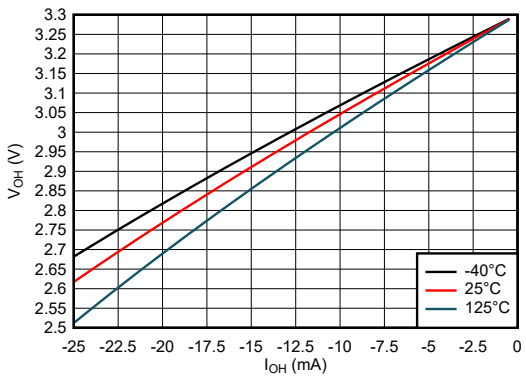


図 5-7. Output Voltage vs Current in HIGH State; 3.3-V Supply

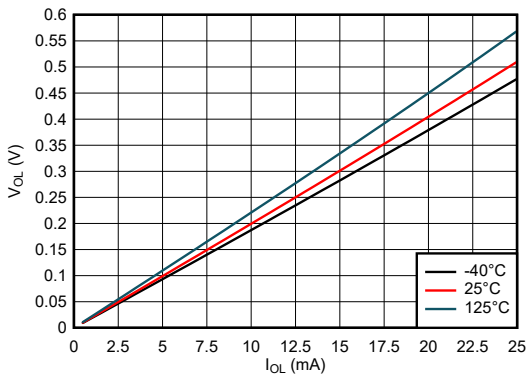


図 5-8. Output Voltage vs Current in LOW State; 3.3-V Supply

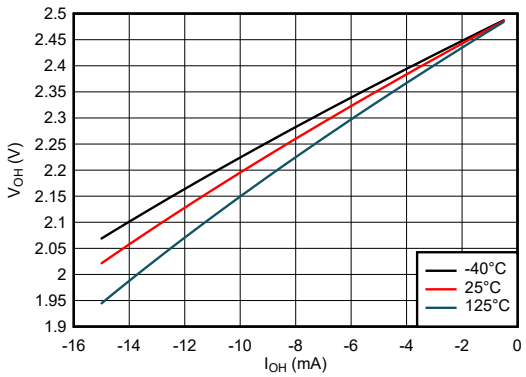


図 5-9. Output Voltage vs Current in HIGH State; 2.5-V Supply

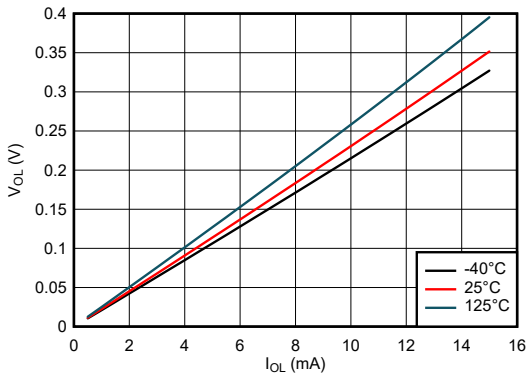


図 5-10. Output Voltage vs Current in LOW State; 2.5-V Supply

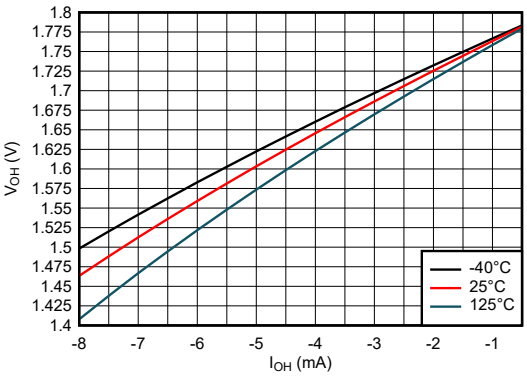


図 5-11. Output Voltage vs Current in HIGH State; 1.8-V Supply

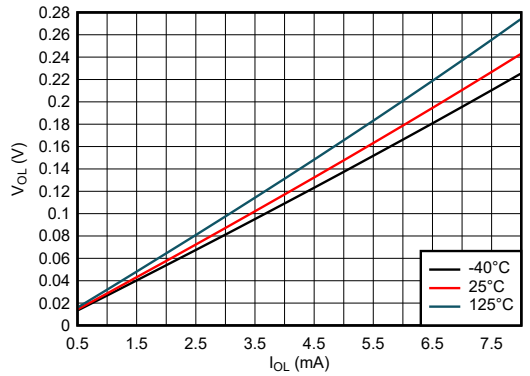


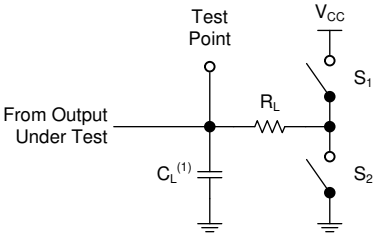
図 5-12. Output Voltage vs Current in LOW State; 1.8-V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω.

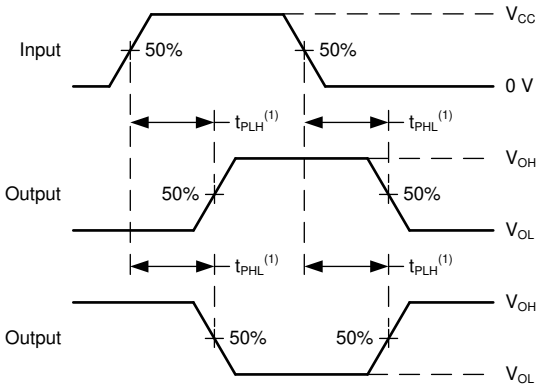
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



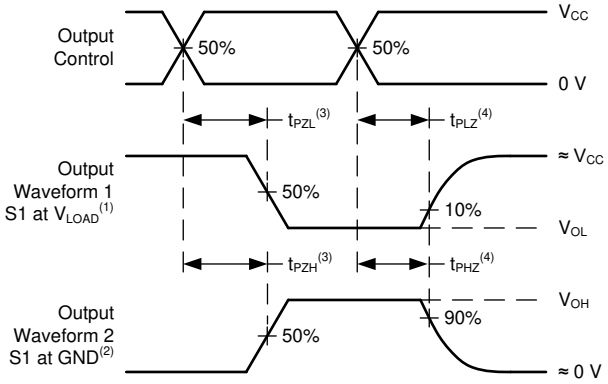
(1) C_L includes probe and test-fixture capacitance.

図 6-1. Load Circuit for 3-State Outputs



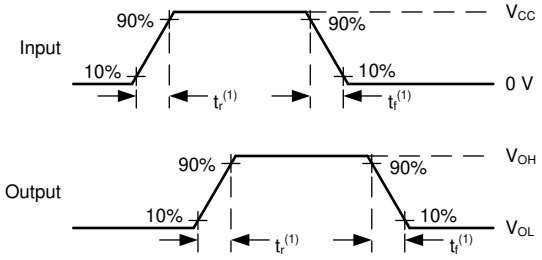
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 6-2. Voltage Waveforms Propagation Delays



(1) S1 = CLOSED, S2 = OPEN.
(2) S1 = OPEN, S2 = CLOSED.
(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.
(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

図 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

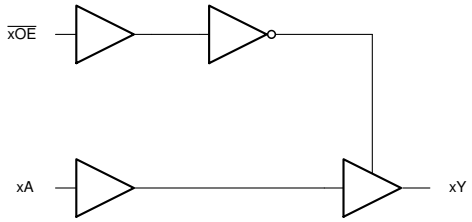
図 6-4. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74LV4T125-Q1 contains four independent buffers with 3-state outputs and extended voltage operation to allow for level translation. Each buffer performs the Boolean function Y = A in positive logic. The outputs can be put into a Hi-Z state by applying a High on the $\overline{OE}$ pin. The output level is referenced to the supply voltage (V_{CC}) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as depicted in 図 7-1.

> **注意**
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

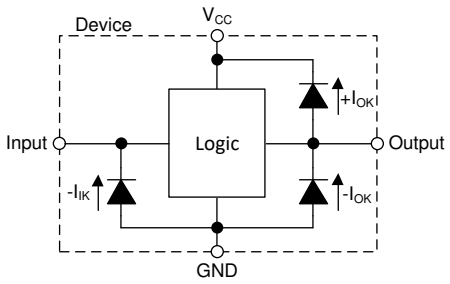


図 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.3 LVxT Enhanced Input Voltage

The SN54SC4T125-SEP belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage (V_{CC}), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. 図 7-2 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

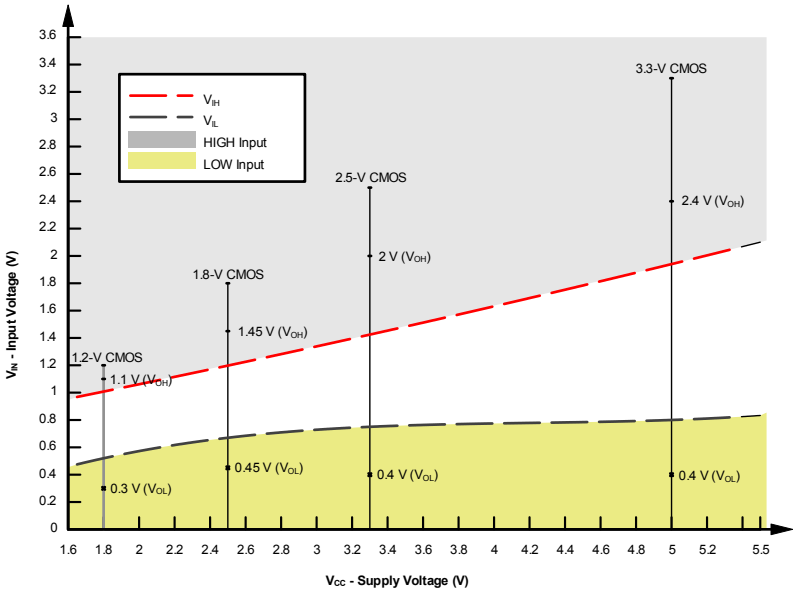


図 7-2. LVxT Input Voltage Levels

7.3.3.1 Down Translation

Signals can be translated down using the SN54SC4T125-SEP. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state. Ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in 図 7-2.

For example, standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V V_{CC}. See 図 7-3.

Down Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V V_{CC} – Inputs from 3.3 V and 5.0 V
- 3.3-V V_{CC} – Inputs from 5.0 V

7.3.3.2 Up Translation

Input signals can be up translated using the SN54SC4T125-SEP. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN54SC4T125-SEP, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in 図 7-3, ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

Up Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 1.2 V
- 2.5-V V_{CC} – Inputs from 1.8 V
- 3.3-V V_{CC} – Inputs from 1.8 V and 2.5 V
- 5.0-V V_{CC} – Inputs from 2.5 V and 3.3 V

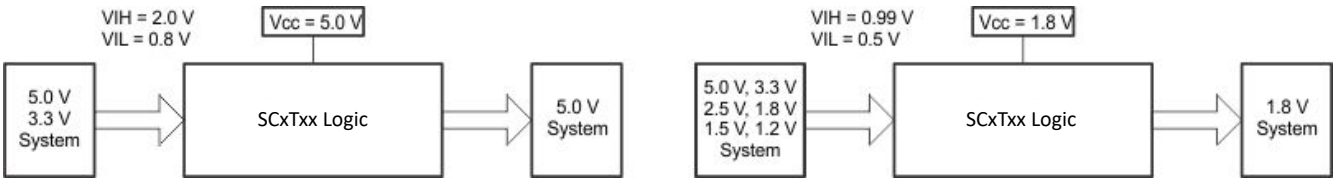


図 7-3. SCxT Up and Down Translation Example

7.4 Device Functional Modes

Function Table lists the functional modes of the SN74LV4T125-Q1.

表 7-1. Function Table

INPUTS(1)		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, a buffer with a 3-state output is used to disable a data signal as shown in 図 8-1. The remaining three buffers can be used for signal conditioning in other places in the system, or the inputs can be grounded and the channels left unused.

8.2 Typical Application

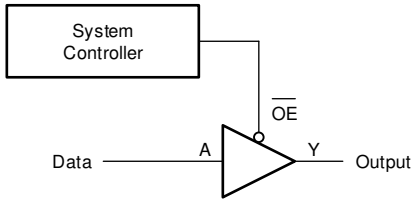


図 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN54SC4T125-SEP plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN54SC4T125-SEP plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN54SC4T125-SEP can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN54SC4T125-SEP can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

注意
The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN54SC4T125-SEP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN54SC4T125-SEP to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. Doing this will not violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves

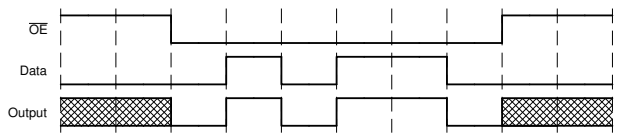


図 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

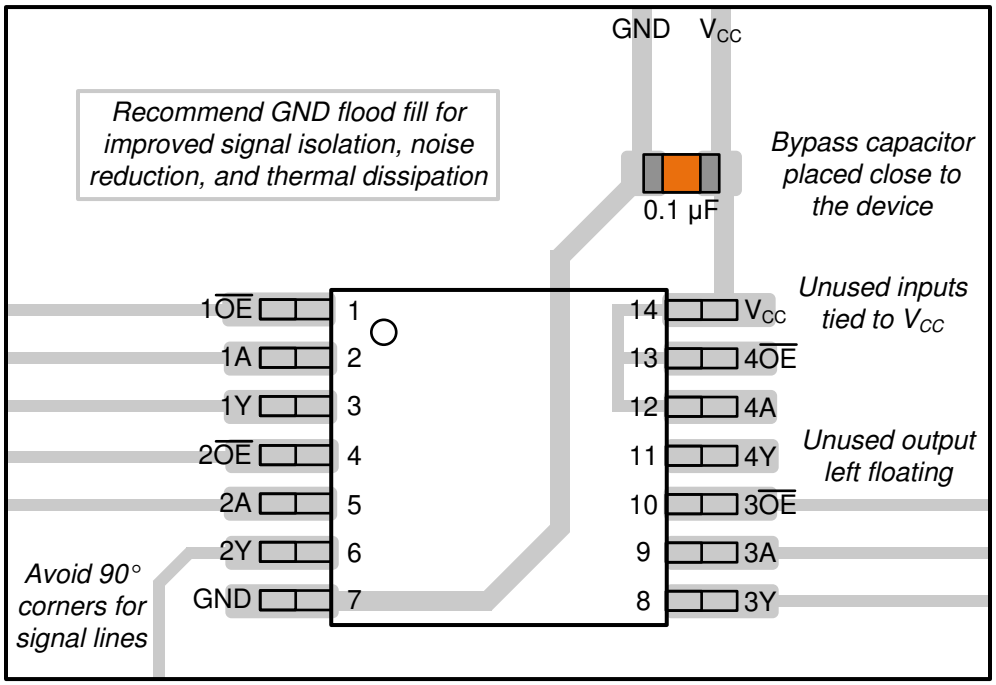


図 8-3. Example Layout for the SN74LV4T125-Q1

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *HCMOS Design Considerations* data sheet

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

DATE	REVISION	NOTES
November 2023	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN54SC4T125MPWTSEP	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S125SEP
SN54SC4T125MPWTSEP.A	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S125SEP
V62/23631-01XE	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See SN54SC4T125MPWTSE	S125SEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

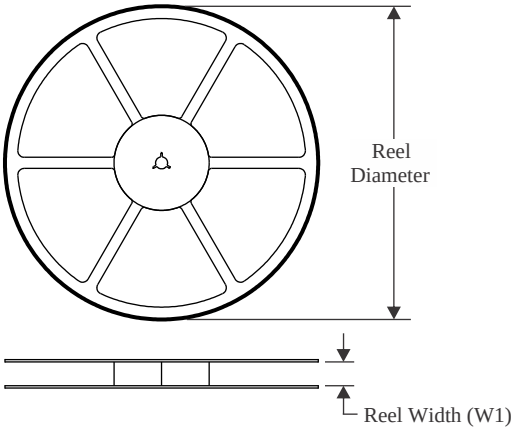
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

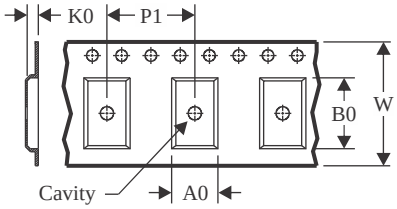
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

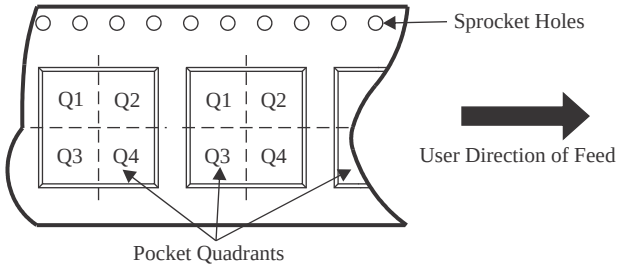


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

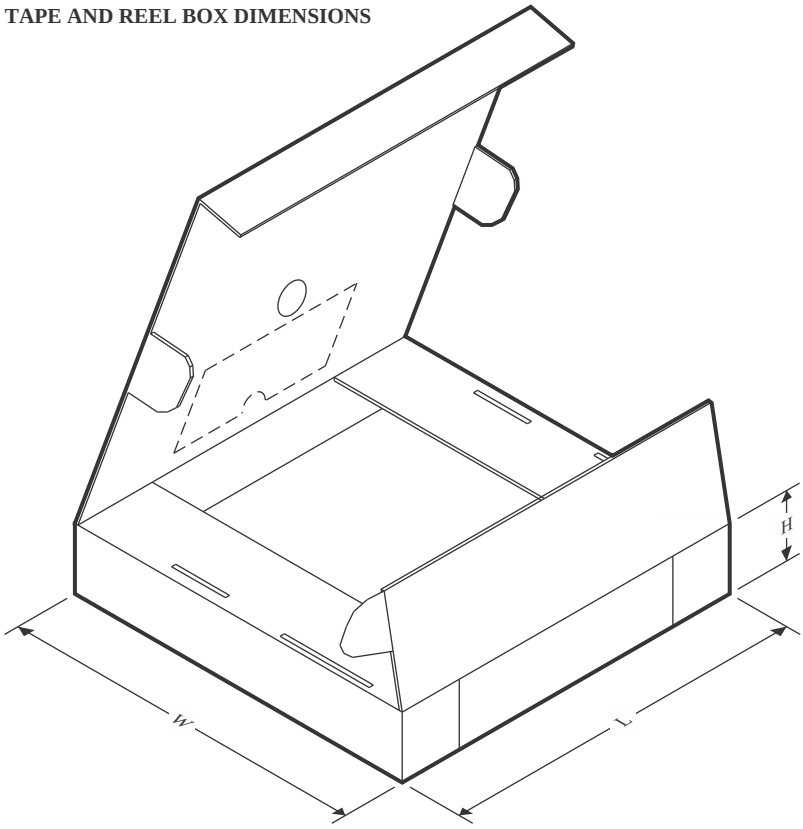
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN54SC4T125MPWTSEP	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

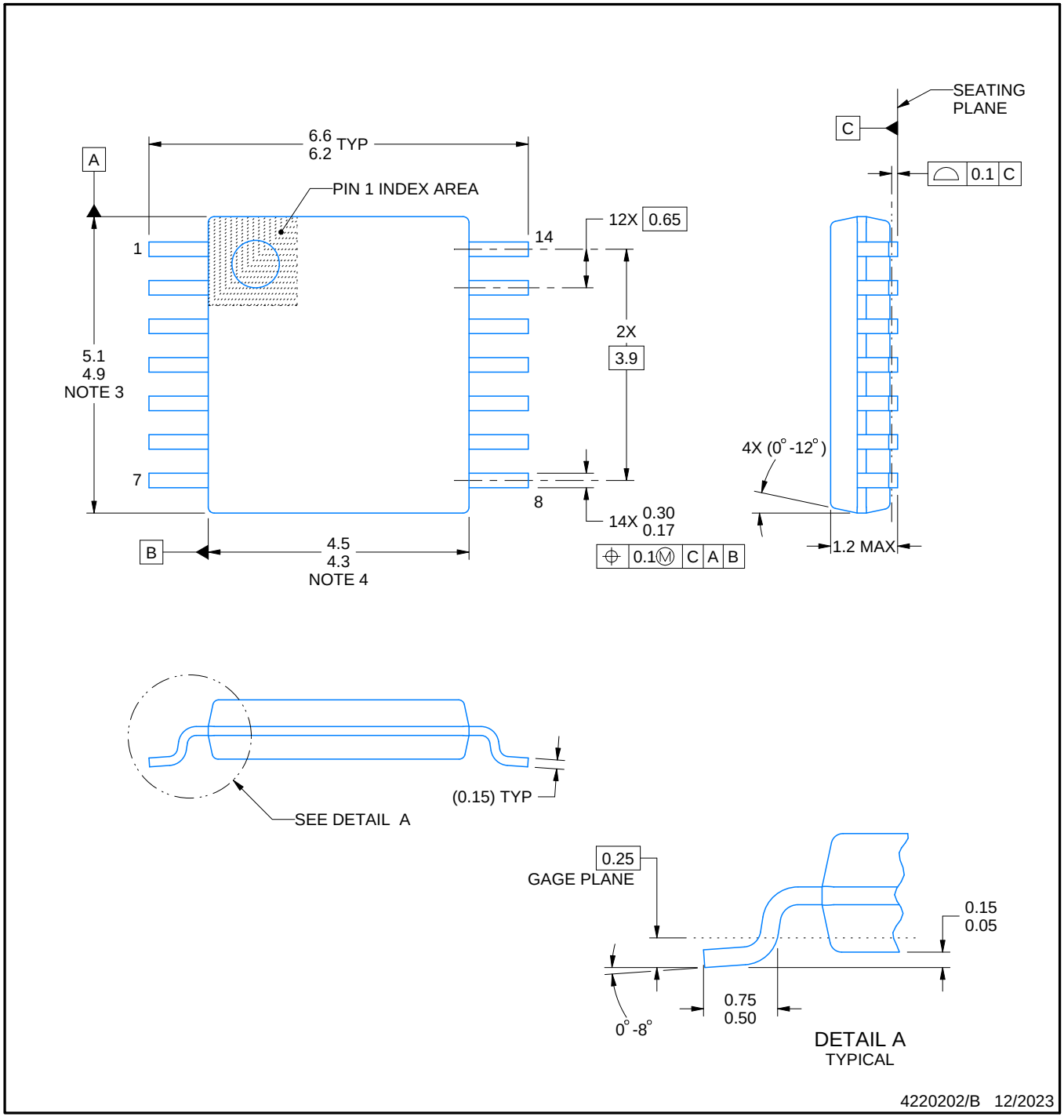
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN54SC4T125MPWTSEP	TSSOP	PW	14	250	353.0	353.0	32.0

PACKAGE OUTLINE

PW0014A

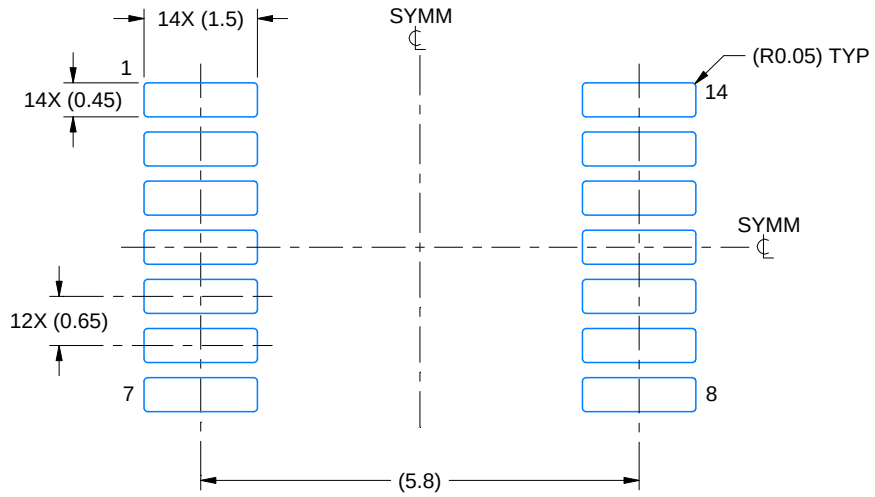
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

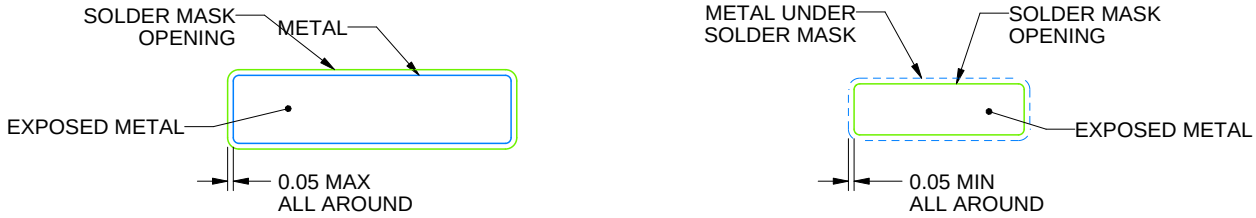


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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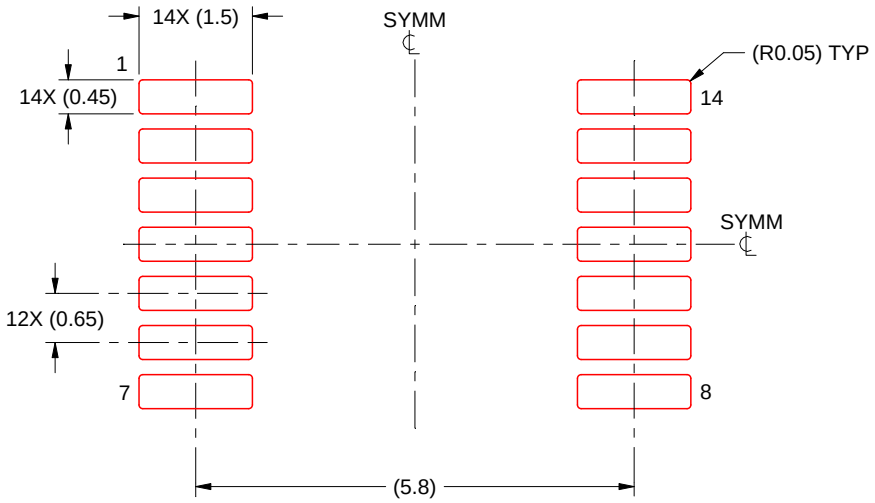
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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