

SNx4LVC157A クワッド、2 ライン入力 1 ライン出力、データ セレクタ / マルチプレクサ

1 特長

- 1.65V ~ 3.6V で動作
- 40°C ~ 85°C、-40°C ~ 125°C、
-55°C ~ 125°C で動作が規定
- 5.5V までの入力電圧に対応
- 最大 t_{pd} 5.2ns (3.3V 時)
- V_{OLP} 標準値 (出力グランド バウンス)
<0.8V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$)
- V_{OHV} 標準値 (出力 V_{OH} アンダーシュート)
>2V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$)
- JESD 17 準拠
250mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
 - 2000V、人体モデル (A114-A)
 - 1000V、デバイス帯電モデル (C101)

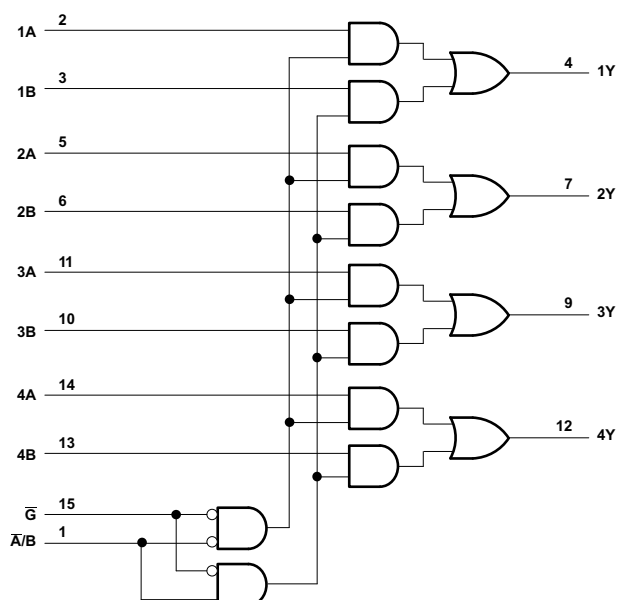
2 概要

この クワッド 2 ライン入力 1 ライン出力、データ セレクタ / マルチプレクサは、1.65V ~ 3.6V の V_{CC} で動作するように設計されています。

製品情報

部品番号	パッケージ (1)	パッケージサイズ (2)	本体サイズ (3)
SNx4LVC157A	BQB (WQFN、16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	D (SOIC、16)	9.90mm × 6mm	9.90mm × 3.90mm
	DB (SSOP、16)	6.20mm × 7.8mm	6.20mm × 5.30mm
	NS (SOP、16)	5mm × 6.4mm	5mm × 4.4mm
	PW (TSSOP、16)	5.00mm × 6.4mm	5.00mm × 4.40mm
	RGY (VQFN、16)	4mm × 3.5mm	4mm × 3.5mm

- (1) 詳細については、「[メカニカル、パッケージ、および注文情報](#)」を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



論理図 (正論理)



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3 Pin Configuration and Functions

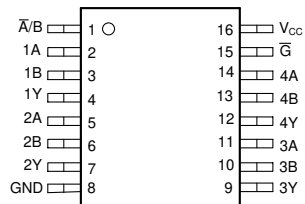


図 3-1. SN54LVC157A J or W Package, 16-Pin CDIP or CFP; SN74LVC157A D, DB, NS, or, PW Package, 16-Pin SOIC, SSOP, SOP, or TSSOP (Top View)

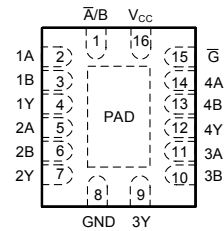


図 3-2. SN74LVC157A BQB or RGY Package, 16-Pin WQFN or VQFN (Top View)

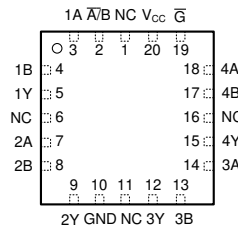


図 3-3. SN54LVC157A FK Package, 16-Pin LCCC (Top View)

表 3-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
A/B	1	I	Address select
1A	2	I	Channel 1, data input A
1B	3	I	Channel 1, data input B
1Y	4	O	Channel 1, data output
2A	5	I	Channel 2, data input A
2B	6	I	Channel 2, data input B
2Y	7	O	Channel 2, data output
GND	8	G	Ground
3Y	9	O	Channel 3, data output
3B	10	I	Channel 3, data input B
3A	11	I	Channel 3, data input A
4Y	12	O	Channel 4, data output
4B	13	I	Channel 4, data input B
4A	14	I	Channel 4, data input A
G-bar	15	I	Output strobe, active low
V _{CC}	16	P	Positive supply
Thermal pad ⁽²⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.

(2) WBQB package only.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	6.5	V
V_I	Input voltage range ⁽¹⁾	–0.5	6.5	V
V_O	Output voltage range ^{(1) (2)}	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–50 mA
I_{OK}	Output clamp current	$V_O < 0$		–50 mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	mA
T_{stg}	Storage temperature range	–65	150	°C
P_{tot}	Power dissipation ^{(3) (4)}	$T_A = -40^{\circ}\text{C to } 125^{\circ}\text{C}$		500 mW

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) The value of V_{CC} is provided in the recommended operating conditions table.

(3) For the D package, above 70°C the value of P_{tot} derates linearly with 8 mW/K.

(4) For the DB, NS, and PW packages, above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions, SN54LVC157A

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54LVC157A		UNIT
			−55 TO 125°C		
			MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 2.7V to 3.6V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7V to 3.6V		0.8	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7V		−12	mA
		V _{CC} = 3V		−24	
I _{OL}	Low-level output current	V _{CC} = 2.7V		12	mA
		V _{CC} = 3V		24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

4.4 Recommended Operating Conditions, SN74LVC157A

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN74LVC157A						UNIT
			T _A = 25°C		–40 TO 85°C		–40 TO 125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65V to 1.95V	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	1.7		1.7		1.7		
		V _{CC} = 2.7V to 3.6V	2		2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65V to 1.95V	0.35 × V _{CC}		0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	0.7		0.7		0.7		
		V _{CC} = 2.7V to 3.6V	0.8		0.8		0.8		
V _I	Input voltage		0	5.5	0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65V	–4		–4		–4		mA
		V _{CC} = 2.3V	–8		–8		–8		
		V _{CC} = 2.7V	–12		–12		–12		
		V _{CC} = 3V	–24		–24		–24		
I _{OL}	Low-level output current	V _{CC} = 1.65V	4		4		4		mA
		V _{CC} = 2.3V	8		8		8		
		V _{CC} = 2.7V	12		12		12		
		V _{CC} = 3V	24		24		24		
Δt/Δv	Input transition rise and fall rate		10		10		10		ns/V

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

4.5 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC157A						UNIT
		BQB (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		16 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	98.8	118.1	82	64	141.8	87.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

4.6 Electrical Characteristics, SN54LVC157A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC157A		UNIT
			–55 TO 125°C		
			MIN	MAX	
V _{OH}	I _{OH} = –100μA	2.7V to 3.6V	V _{CC} – 0.2		V
	I _{OH} = –12mA	2.7V	2.2		
		3V	2.4		
		I _{OH} = –24mA	3V	2.2	

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LVC157A		UNIT	
				–55 TO 125°C			
				MIN	MAX		
V _{OL}		I _{OL} = 100μA	2.7V to 3.6V	0.2		V	
		I _{OL} = 12mA	2.7V	0.4			
		I _{OL} = 24mA	3V	0.55			
I _I	All inputs	V _I = 5.5V or GND	3.6V	±5		μA	
I _{CC}		V _I = V _{CC} or GND	I _O = 0	3.6V	10		μA
ΔI _{CC}		One input at V _{CC} – 0.6V, Other inputs at V _{CC} or GND		2.7V to 3.6V	500		μA

4.7 Electrical Characteristics, SN74LVC157A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN74LVC157A						UNIT		
				T _A = 25°C			−40 TO 85°C		−40 TO 125°C			
				MIN	TYP	MAX	MIN	MAX	MIN		MAX	
V _{OH}	I _{OH} = −100μA		1.65V to 3.6V	V _{CC} − 0.2			V _{CC} − 0.2		V _{CC} − 0.3		V	
	I _{OH} = −4mA		1.65V	1.29			1.2		1.05			
	I _{OH} = −8mA		2.3V	1.9			1.7		1.55			
	I _{OH} = −12mA		2.7V	2.2			2.2		2.05			
			3V	2.4			2.4		2.25			
I _{OH} = −24mA		3V	2.3			2.2		2				
V _{OL}	I _{OL} = 100μA		1.65V to 3.6V	0.1			0.2		0.3		V	
	I _{OL} = 4mA		1.65V	0.24			0.45		0.6			
	I _{OL} = 8mA		2.3V	0.3			0.7		0.75			
	I _{OL} = 12mA		2.7V	0.4			0.4		0.6			
	I _{OL} = 24mA		3V	0.55			0.55		0.8			
I _I	All inputs	V _I = 5.5V or GND		3.6V	±1			±5		±20		μA
I _{CC}		V _I = V _{CC} or GND	I _O = 0	3.6V	1			10		40		μA
ΔI _{CC}		One input at V _{CC} − 0.6V, Other inputs at V _{CC} or GND		2.7V to 3.6V	500			500		5000		μA
C _i		V _I = V _{CC} or GND		3.3V	5							pF

4.8 Switching Characteristics, SN54LVC157A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54LVC157A		UNIT
				–55 TO 125°C		
				MIN	MAX	
t _{pd}	A or B	Y	2.7V		6.2	ns
			3.3V ± 0.3V	0.8	5.4	
	A̅/B		2.7V		8.2	
			3.3V ± 0.3V	0.8	7	
	G̅		2.7V		7.8	
			3.3V ± 0.3V	0.8	6.5	

4.9 Switching Characteristics, SN74LVC157A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74LVC157A							UNIT
				T _A = 25°C			−40 TO 85°C		−40 TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1.8V ± 0.15V	1	5.5	13.5	1	14	1	15.5	ns
			2.5V ± 0.2V	1	3.2	7.4	1	7.9	1	10	
			2.7V	1	3.6	5.7	1	5.9	1	7.4	
			3.3V ± 0.3V	1	3	5	1	5.2	1	6.4	
	A̅/B		1.8V ± 0.15V	1	6	15.5	1	16	1	17.5	
			2.5V ± 0.2V	1	3.7	9.6	1	10.1	1	12.2	
			2.7V	1	4.1	7.9	1	8.1	1	10	
			3.3V ± 0.3V	1	3.4	6.6	1	6.8	1	8.4	
	G̅		1.8V ± 0.15V	1	5.9	13.5	1	14	1	15.5	
			2.5V ± 0.2V	1	3.5	9.3	1	9.8	1	11.9	
			2.7V	1	3.9	7.6	1	7.8	1	9.3	
			3.3V ± 0.3V	1	3.3	6.3	1	6.5	1	7.9	
t _{sk(o)}			1.8V ± 0.15V				2		2.5		ns
			3.3V ± 0.3V				1		1.5		

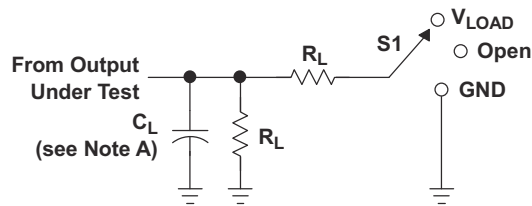
4.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	1.8V	14 ⁽¹⁾	pF
			2.5V	15 ⁽¹⁾	
			3.3V	16	

(1) On products compliant to MIL-PRF-38535, this parameter does not apply.

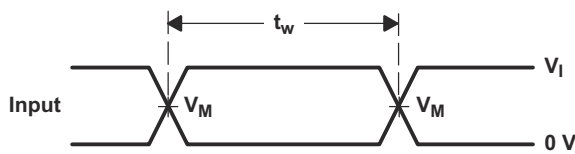
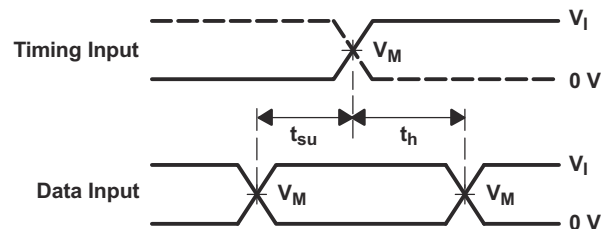
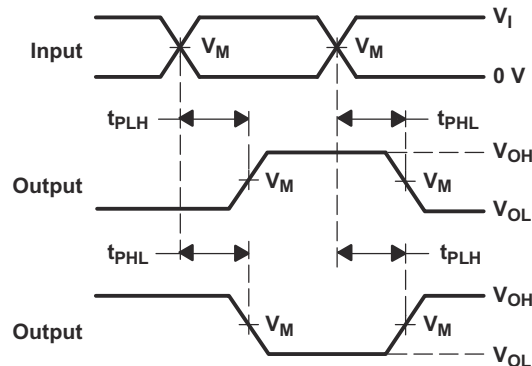
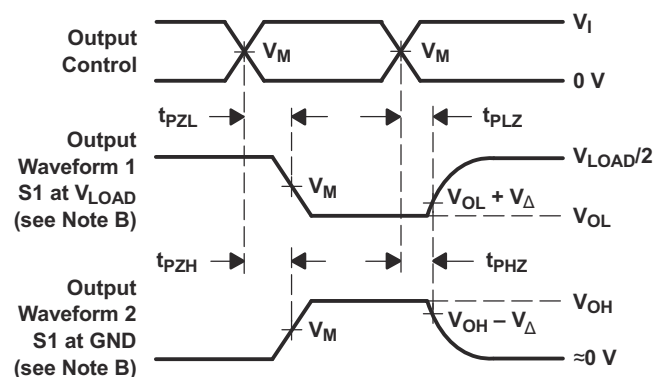
5 Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kW	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 W	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 W	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 W	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATIONVOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTSVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

图 5-1. Load Circuit and Voltage Waveforms

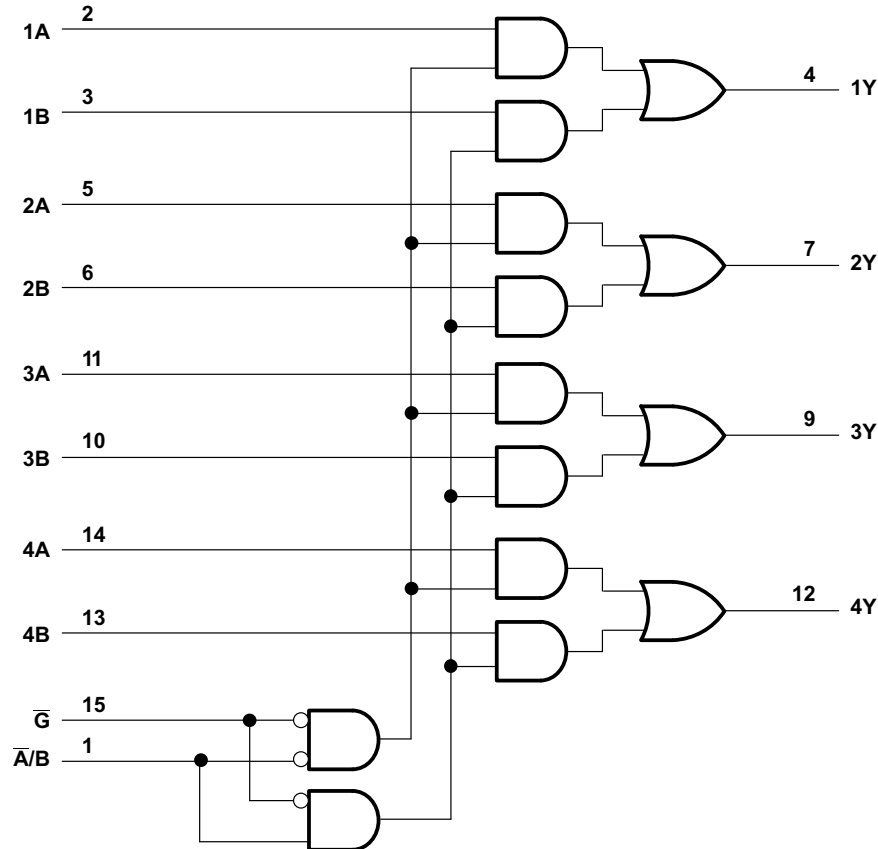
6 Detailed Description

6.1 Overview

The 'LVC157A devices feature a common strobe ($\overline{G}$) input. When $\overline{G}$ is high, all outputs are low. When $\overline{G}$ is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The 'LVC157A devices provide true data.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

6.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

図 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Function Table

INPUTS				OUTPUT Y
$\overline{G}$	A/B	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

7 Application and Implementation

注

以下のアプリケーションに関するセクションの情報は、TI の部品仕様の一部ではなく、TI はこれらの情報の正確性や完全性を保証しません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [セクション 4.4](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Layout Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.2 Layout Example

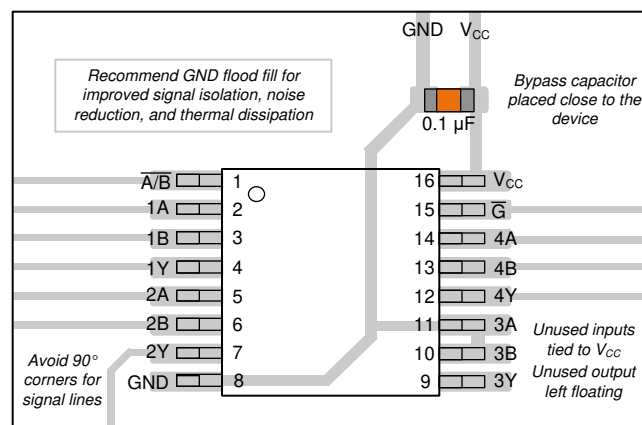


図 7-1. Example Layout for the SN74LVC157A

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC157A	Click here	Click here	Click here	Click here	Click here
SN74LVC157A	Click here	Click here	Click here	Click here	Click here

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。
[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision R (May 2024) to Revision S (December 2024)	Page
Updated RθJA values: D = 73 to 118.1, PW = 108 to 141.8, RGY = 39 to 87.1; Updated D, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W.....	5
Changes from Revision Q (December 2010) to Revision R (May 2024)	Page
「パッケージ情報」表、「ピン構成および機能」セクション、および「熱に関する情報」表に BQA パッケージを追加	1

- 「製品情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加 1
- 「特長」からマシン モデルを削除 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-0050601QEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0050601QE A SNJ54LVC157AJ
5962-0050601QFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0050601QF A SNJ54LVC157AW
SN74LVC157ABQBR	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157ABQBR.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157AD	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157AD.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157ADBR.B	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157ADG4	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADRE4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADRG3	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADRG3.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADRG4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADRG4.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADT	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ADT.B	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ANSR.B	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157ANSRE4	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A
SN74LVC157APW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APW.B	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWE4	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC157APWG4	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWRE4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWRG4.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWT	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157APWT.B	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A
SN74LVC157ARGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC157A
SN74LVC157ARGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC157A
SN74LVC157ARGYR.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC157A
SNJ54LVC157AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0050601QE A SNJ54LVC157AJ
SNJ54LVC157AW	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0050601QF A SNJ54LVC157AW

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC157A, SN74LVC157A :

- Catalog : [SN74LVC157A](#)
- Automotive : [SN74LVC157A-Q1](#), [SN74LVC157A-Q1](#)
- Enhanced Product : [SN74LVC157A-EP](#), [SN74LVC157A-EP](#)
- Military : [SN54LVC157A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC157ABQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74LVC157ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC157ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC157ADRG3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC157ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC157ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC157APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC157APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC157APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC157ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC157ABQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74LVC157ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LVC157ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LVC157ADRG3	SOIC	D	16	2500	364.0	364.0	27.0
SN74LVC157ADRG4	SOIC	D	16	2500	340.5	336.1	32.0
SN74LVC157ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LVC157APWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC157APWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC157APWT	TSSOP	PW	16	250	353.0	353.0	32.0
SN74LVC157ARGYR	VQFN	RGY	16	3000	353.0	353.0	32.0

TUBE

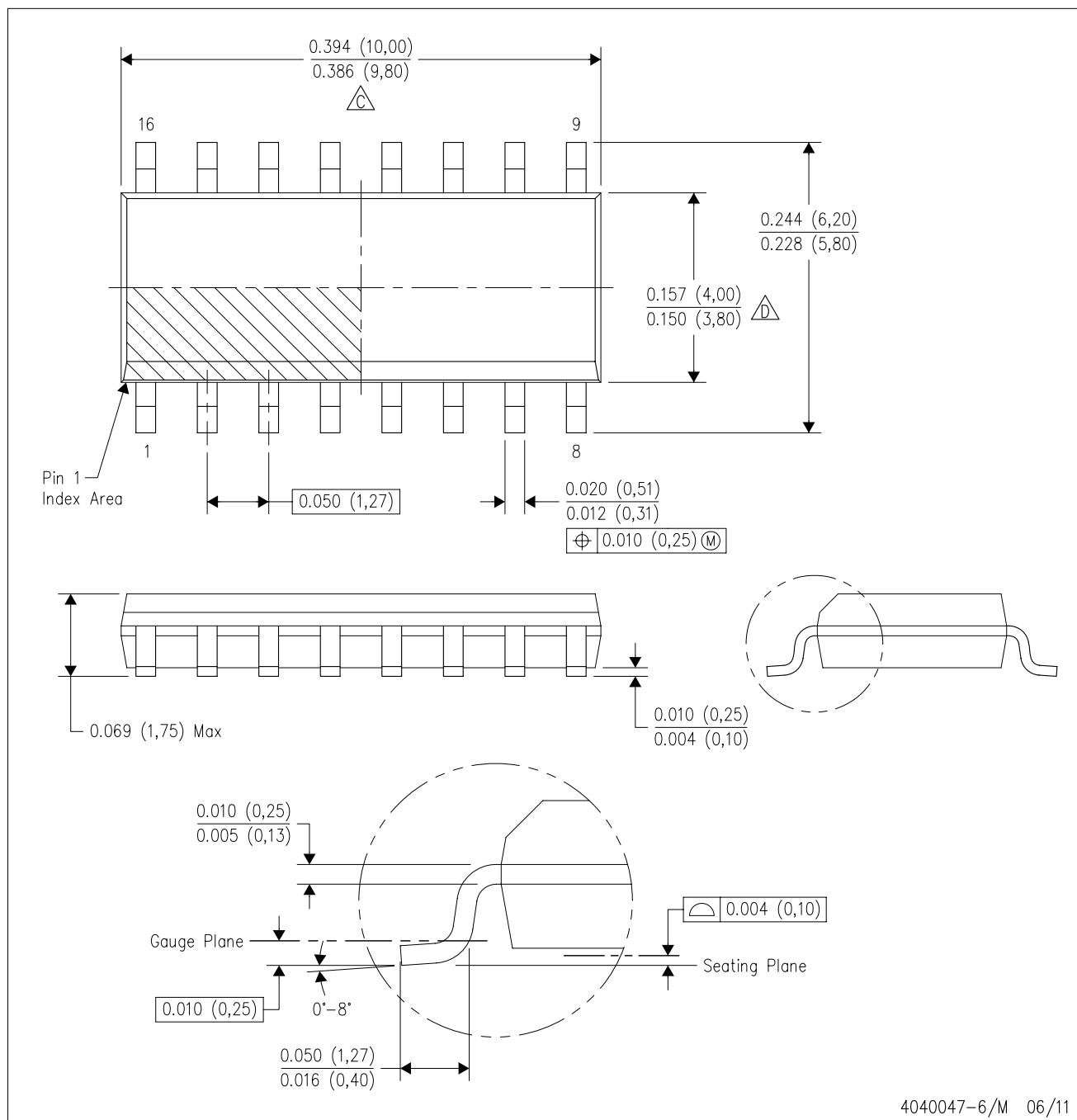


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-0050601QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LVC157AD	D	SOIC	16	40	507	8	3940	4.32
SN74LVC157AD.B	D	SOIC	16	40	507	8	3940	4.32
SN74LVC157ADG4	D	SOIC	16	40	507	8	3940	4.32
SN74LVC157APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC157APW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC157APWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC157APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54LVC157AW	W	CFP	16	25	506.98	26.16	6220	NA

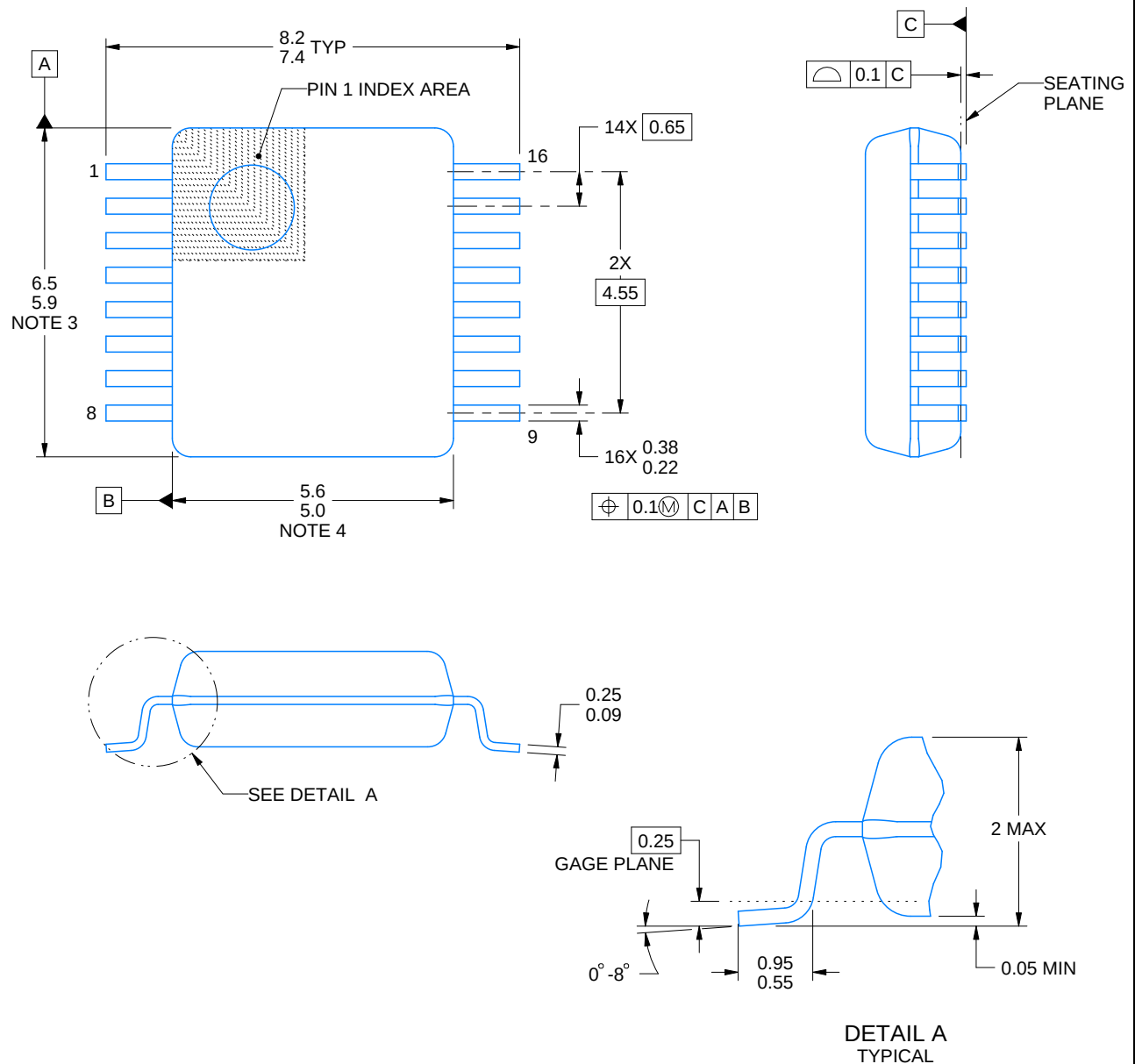
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220763/A 05/2022

NOTES:

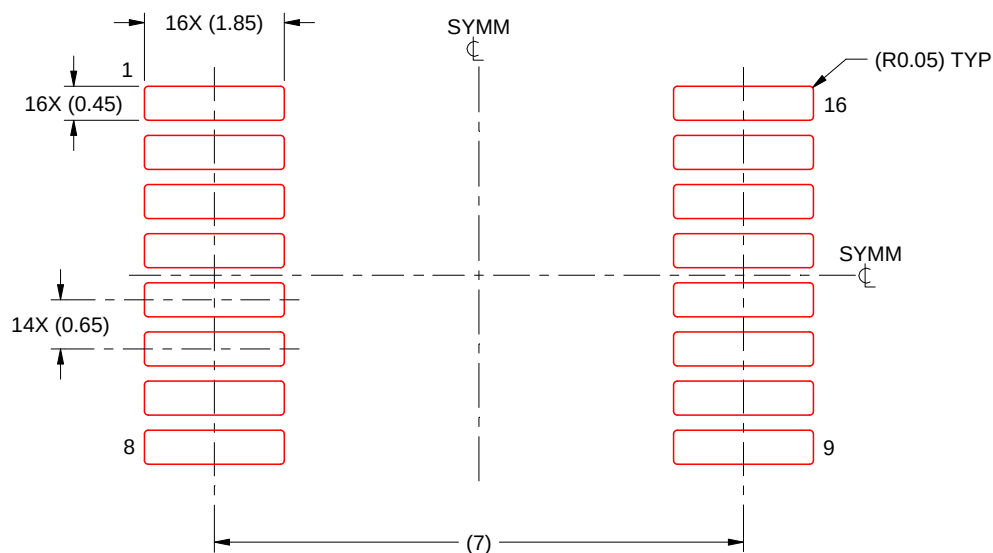
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

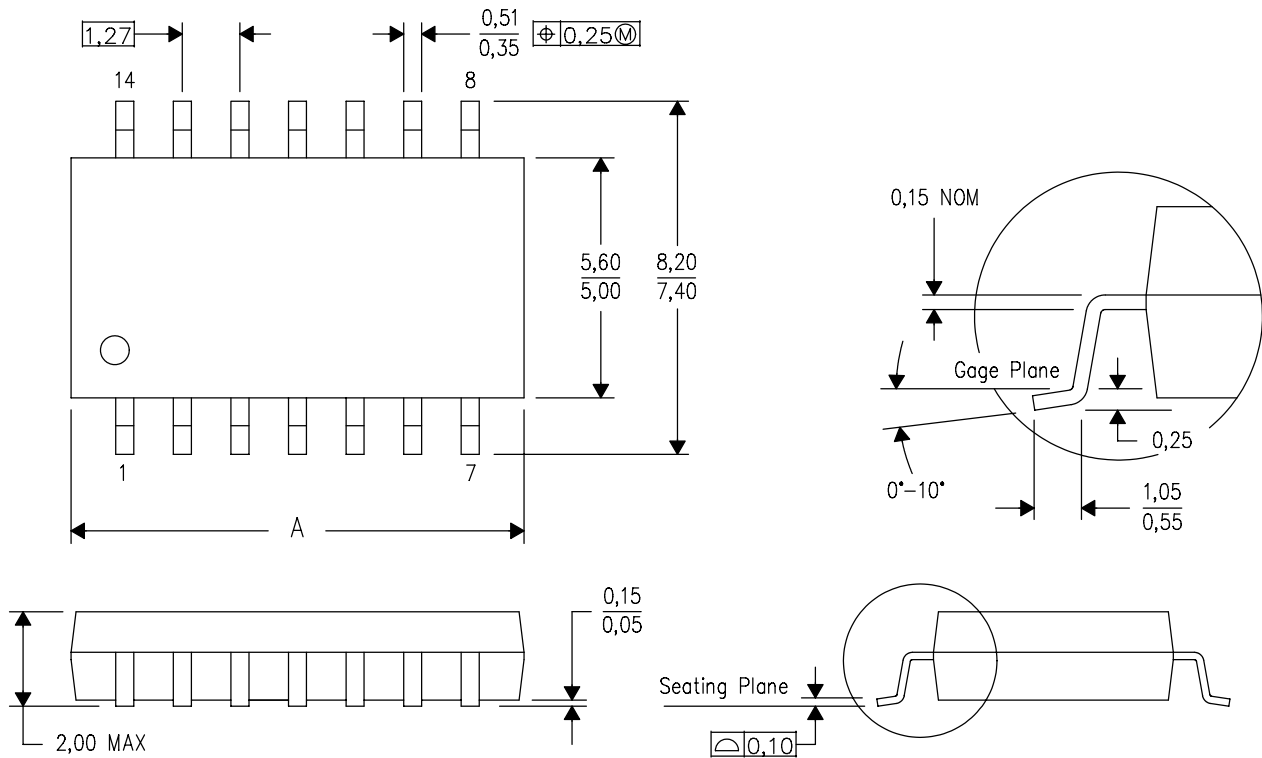
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

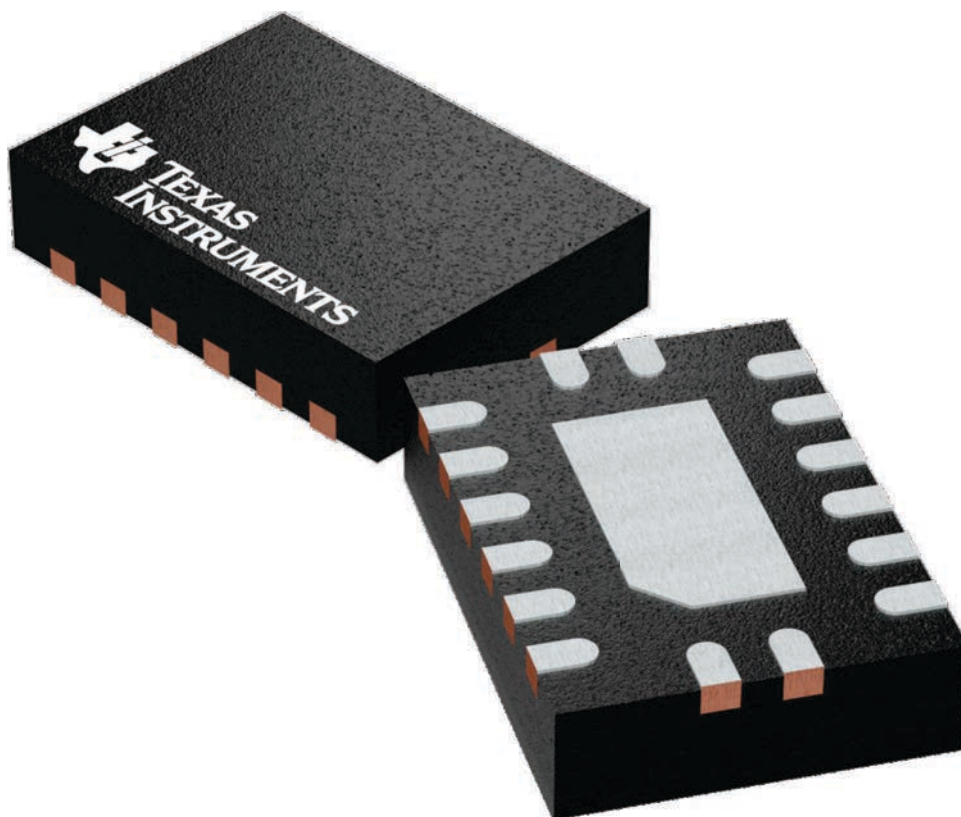
BQB 16

WQFN - 0.8 mm max height

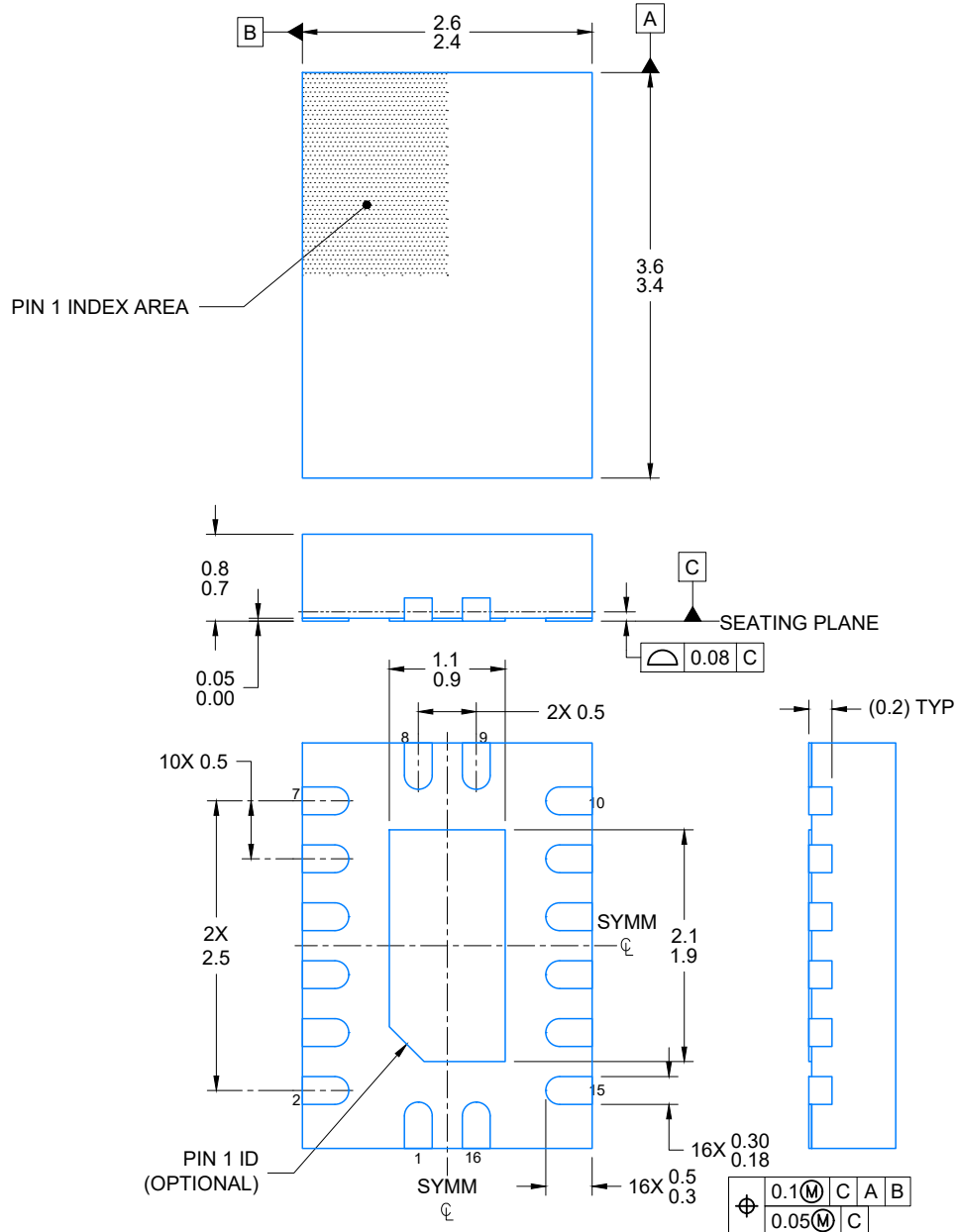
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



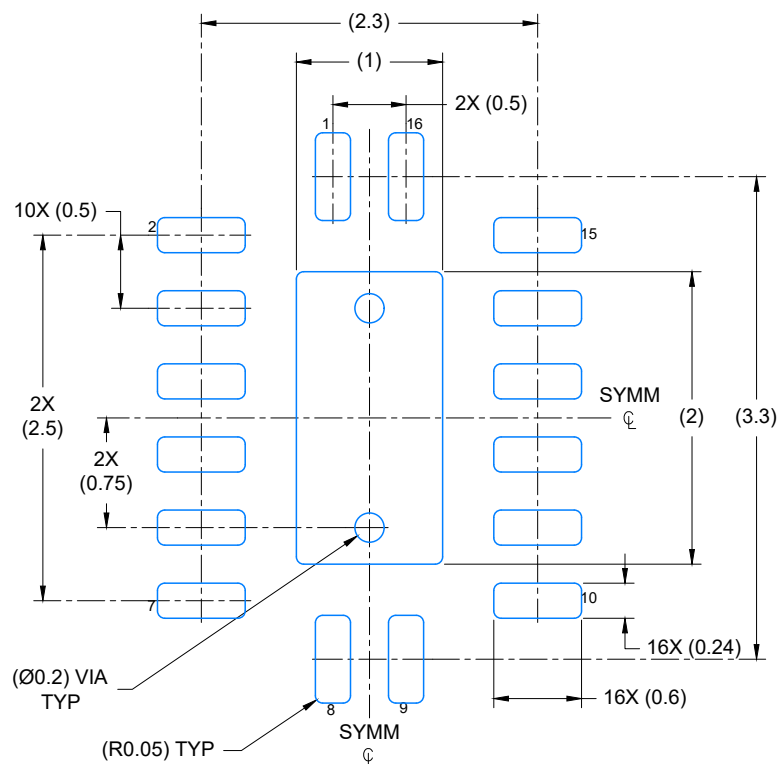
4226161/A



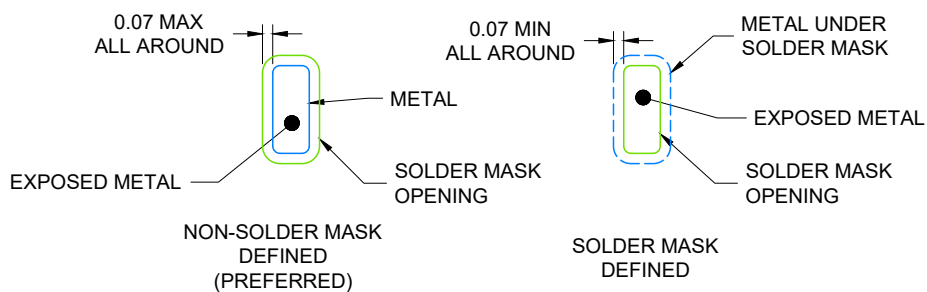
4224640/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

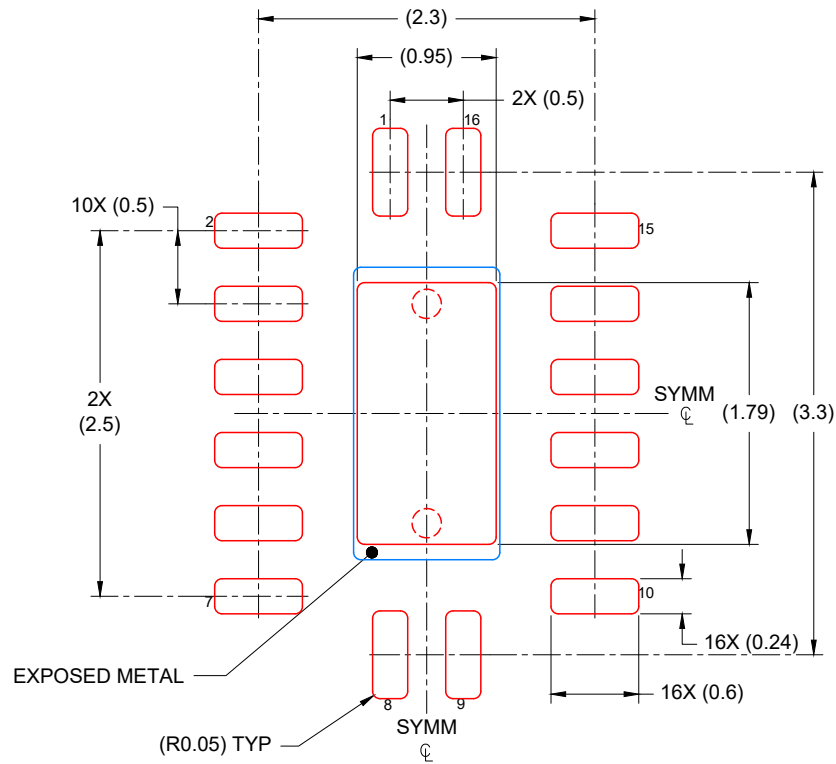
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQB0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

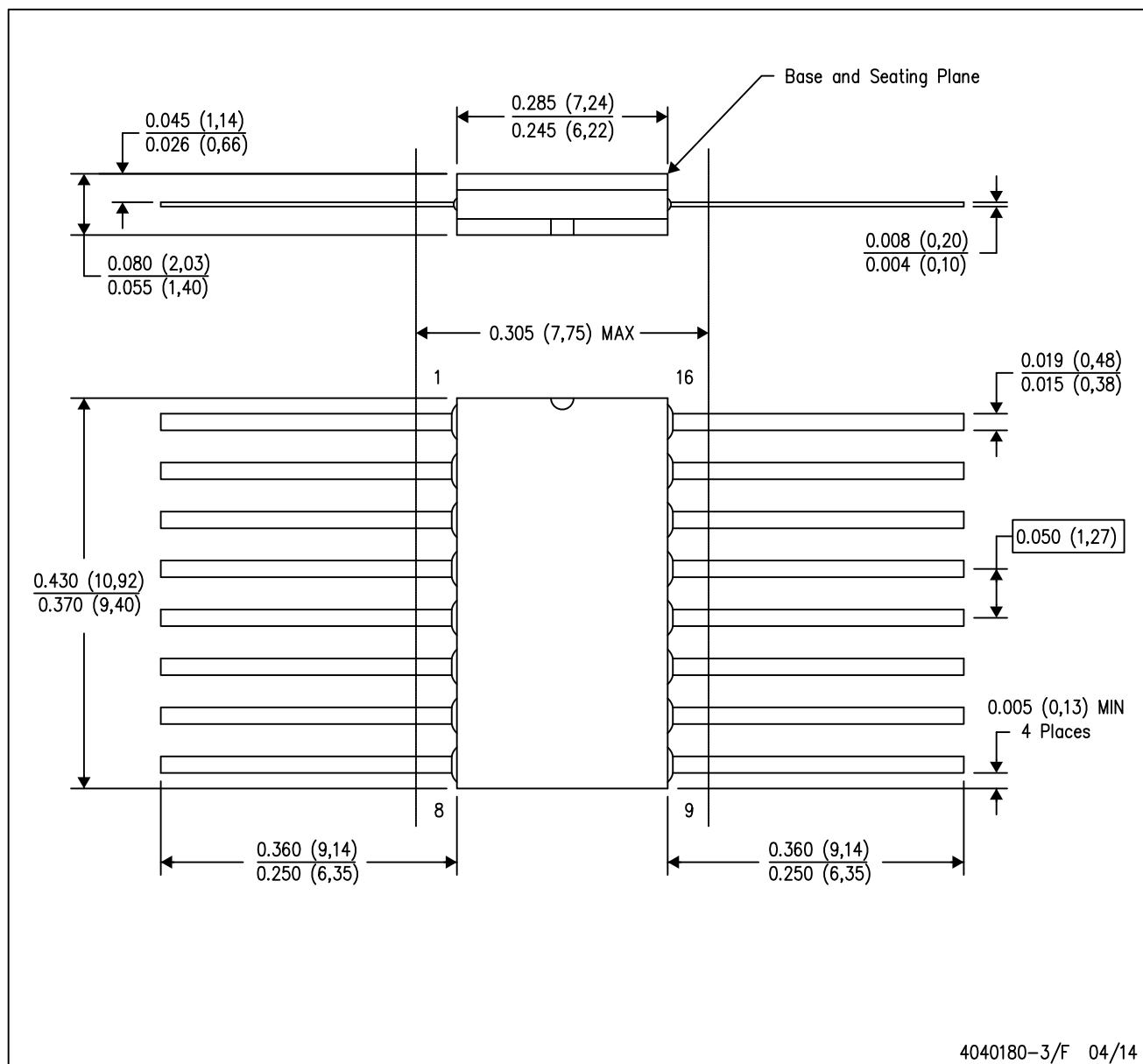
4224640/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

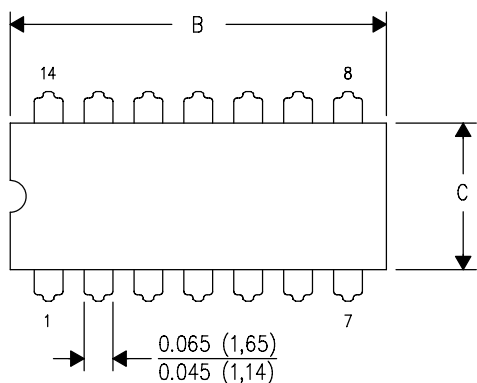


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

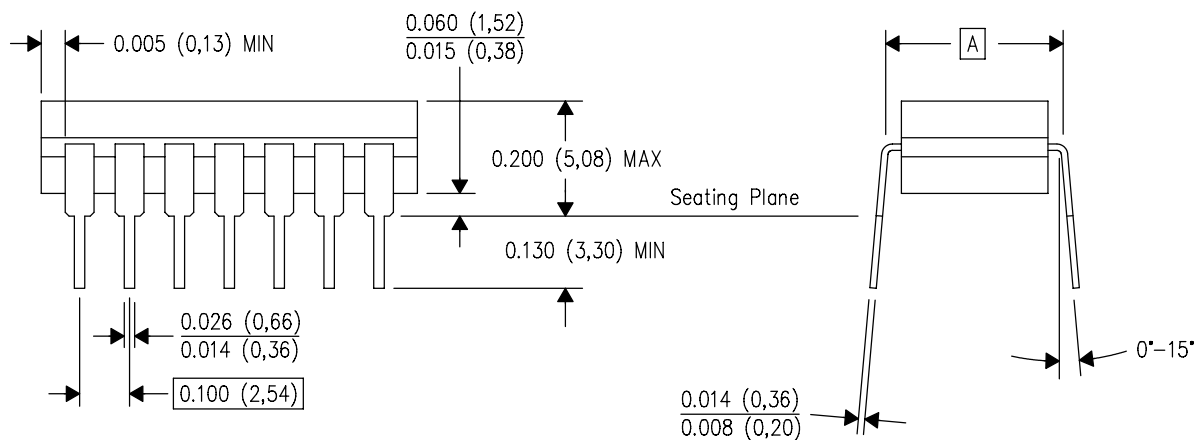
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

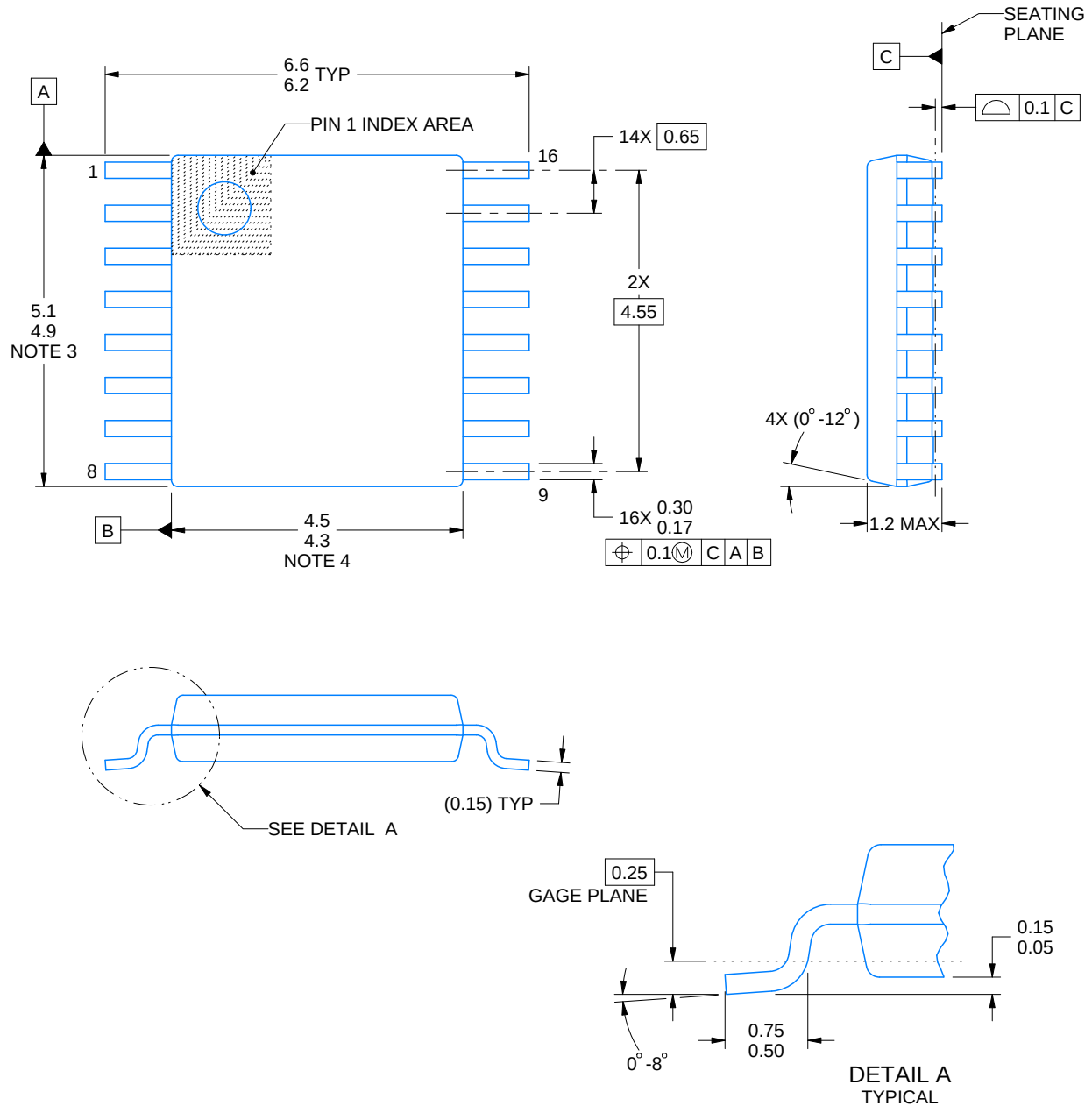
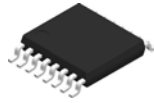


PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

NOTES:

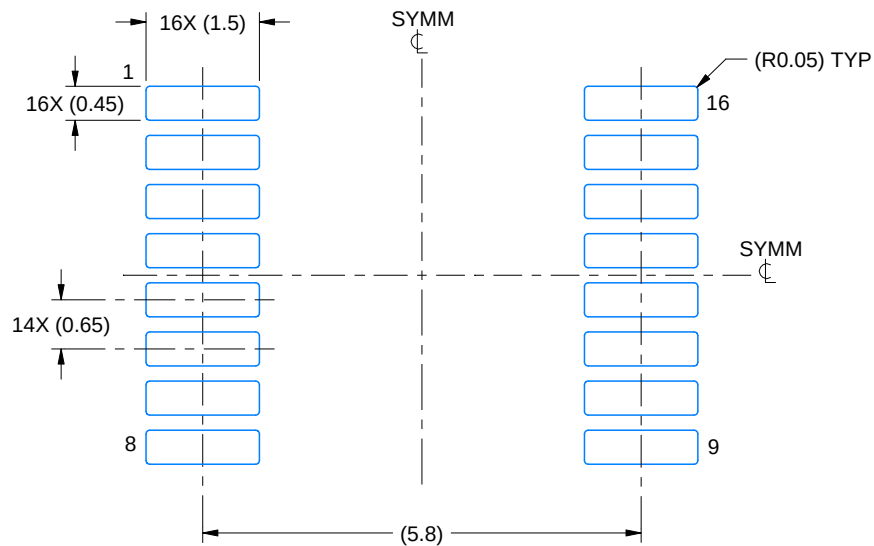
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

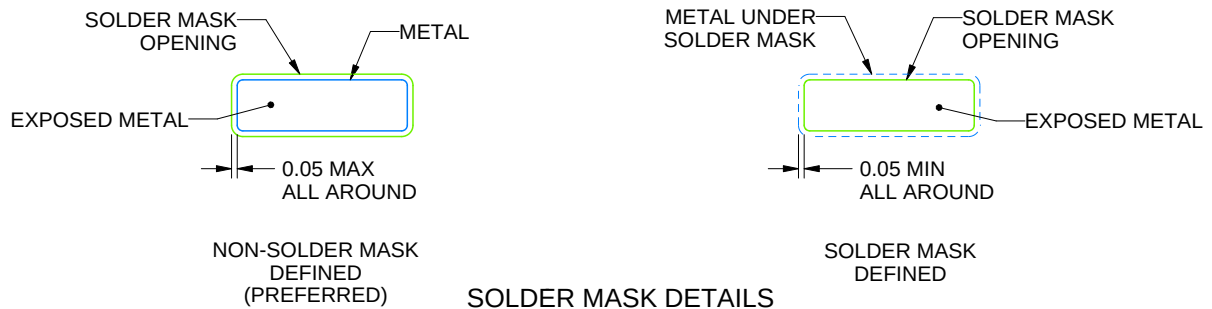
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

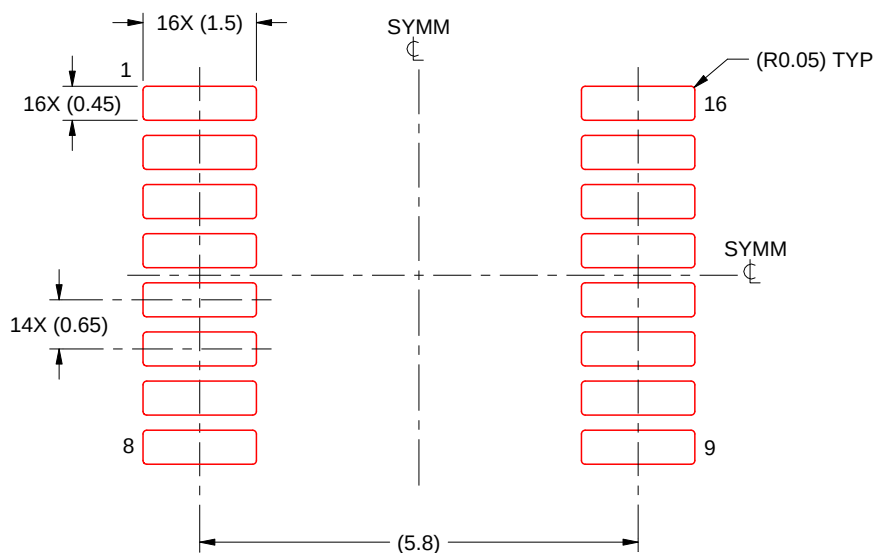
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

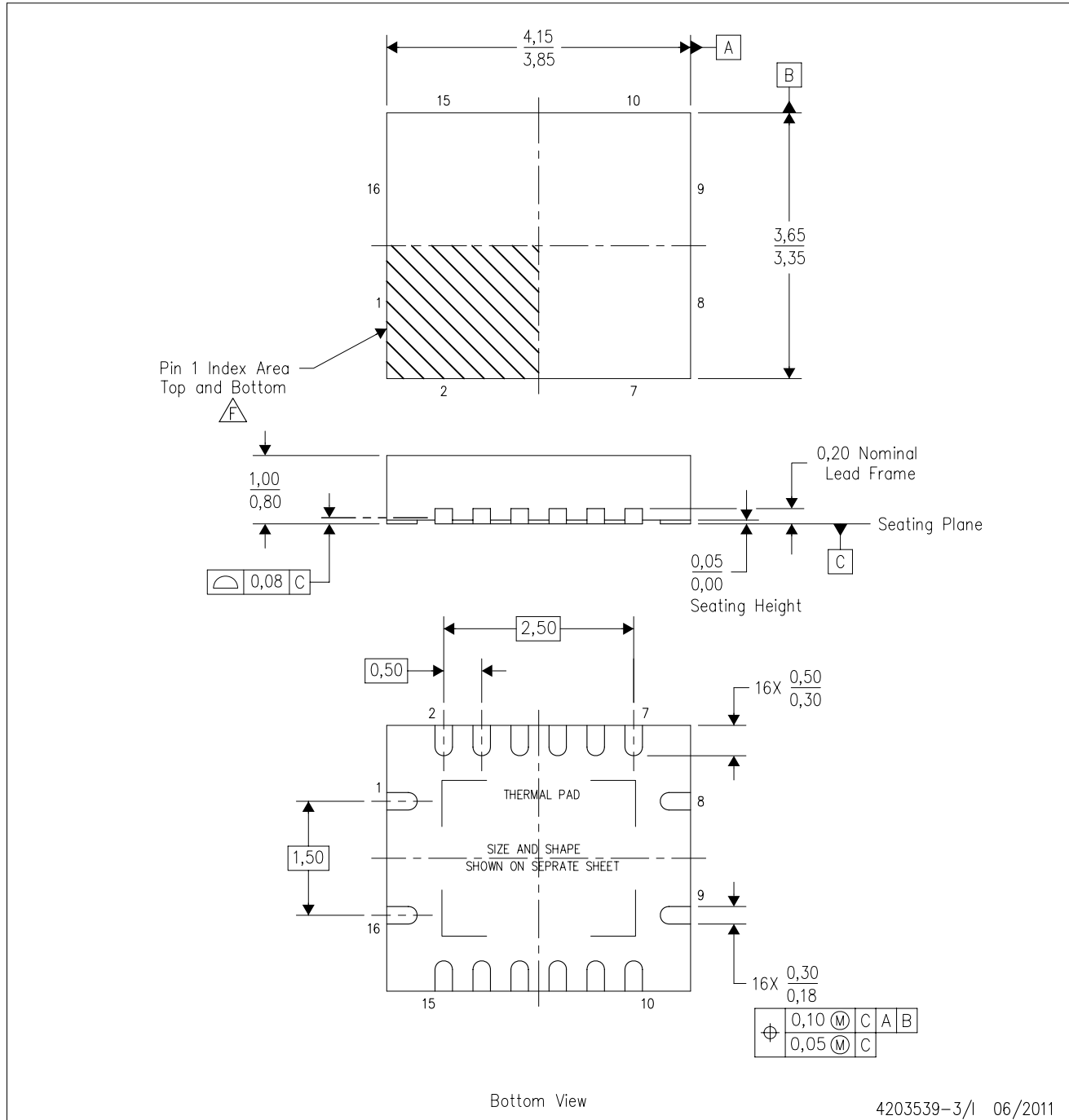
4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

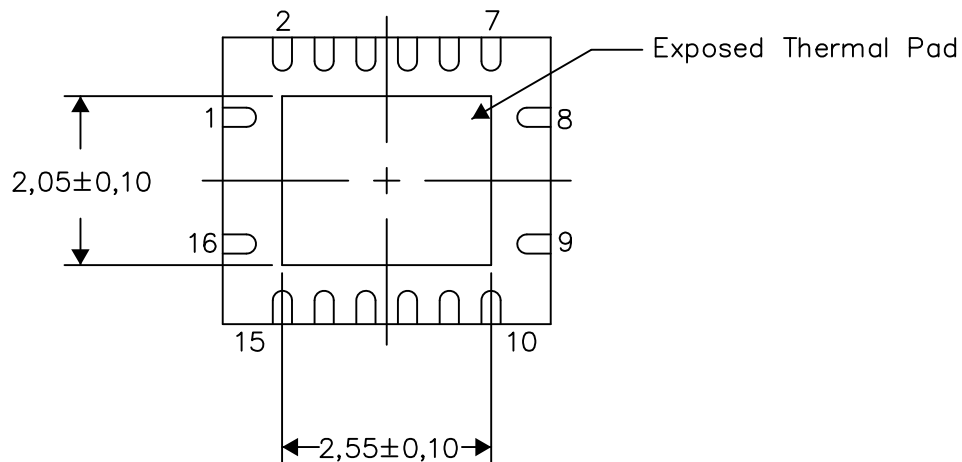
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

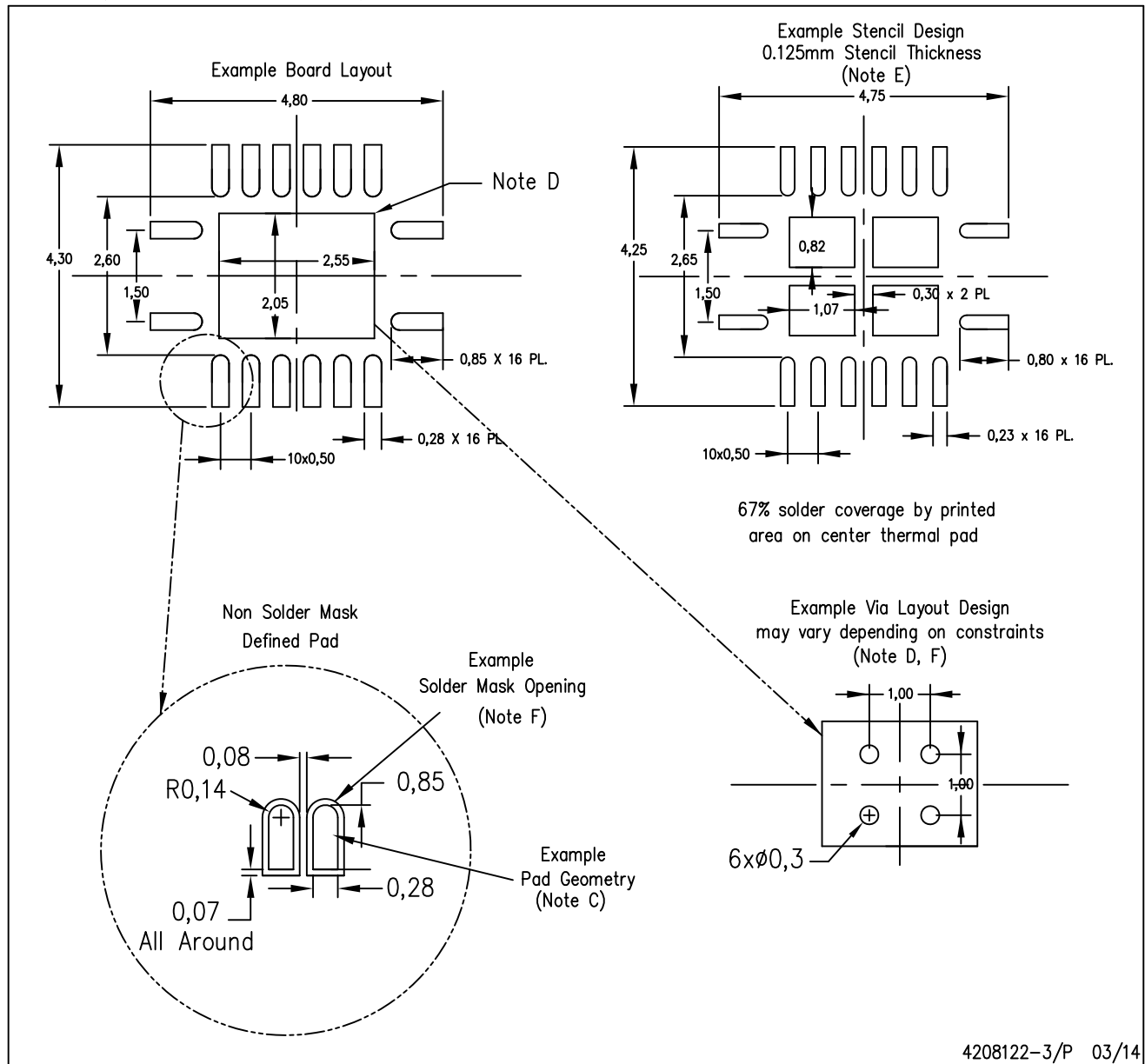
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

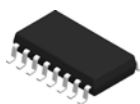
NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

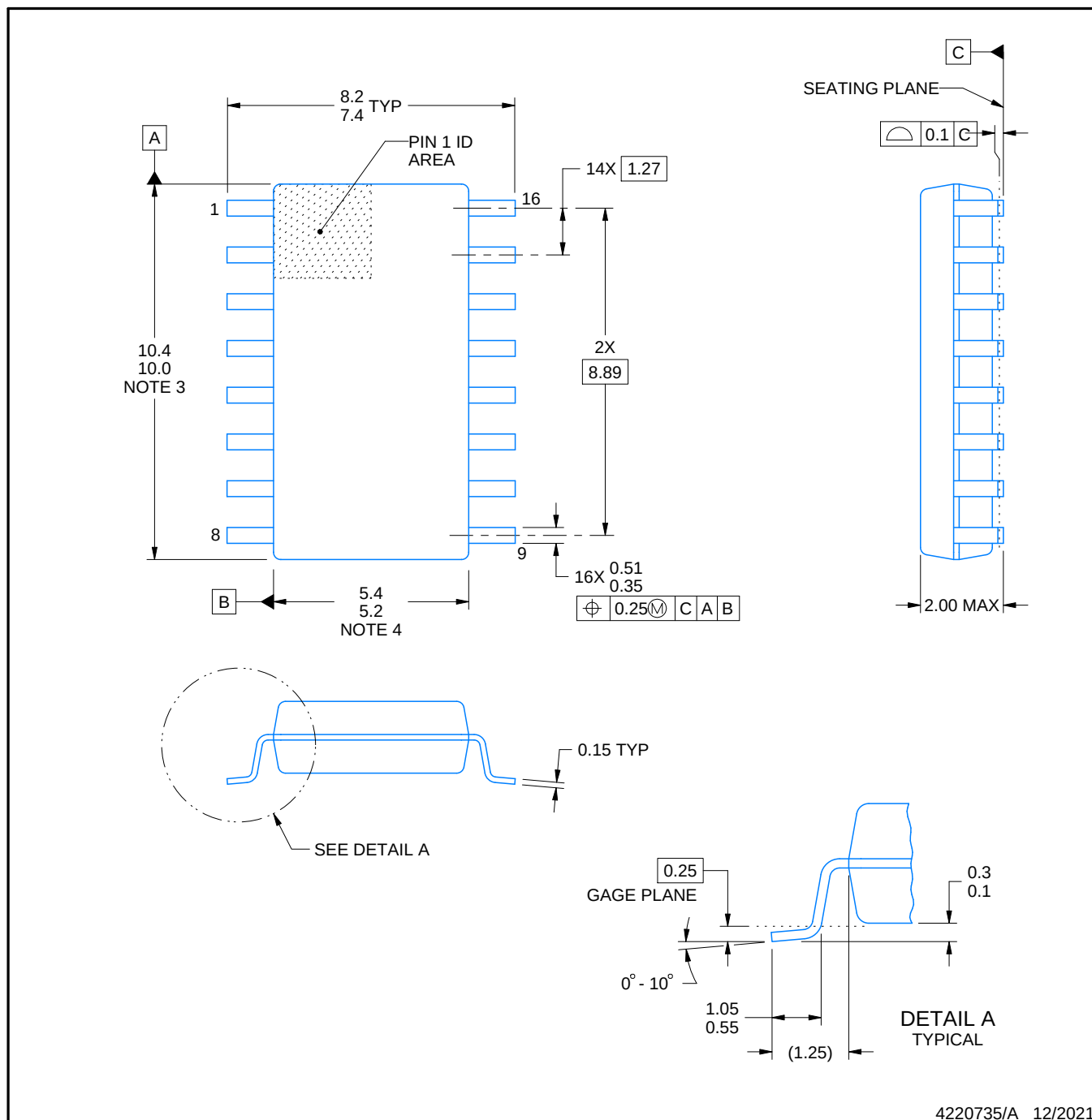


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

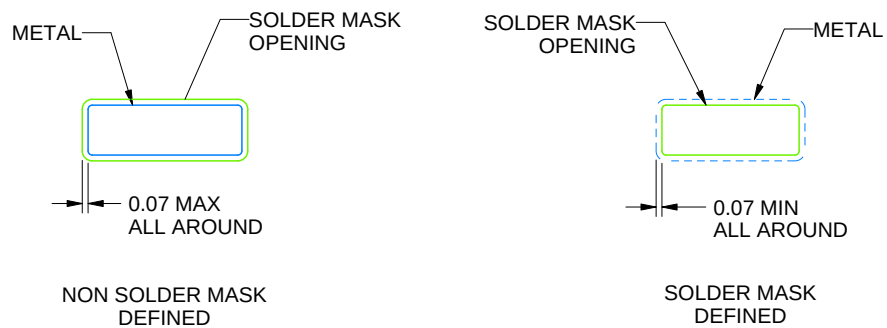
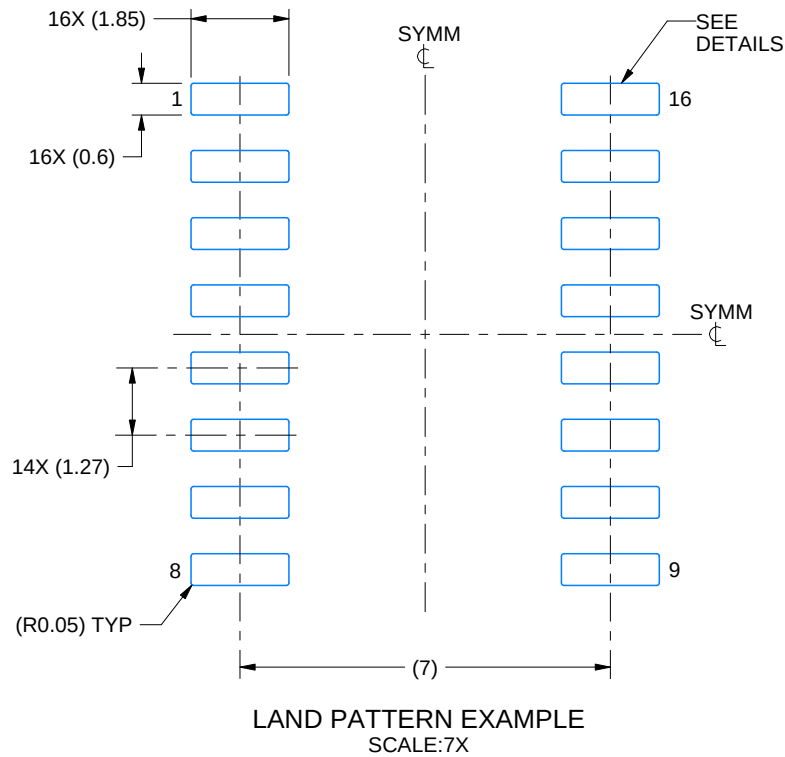
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP

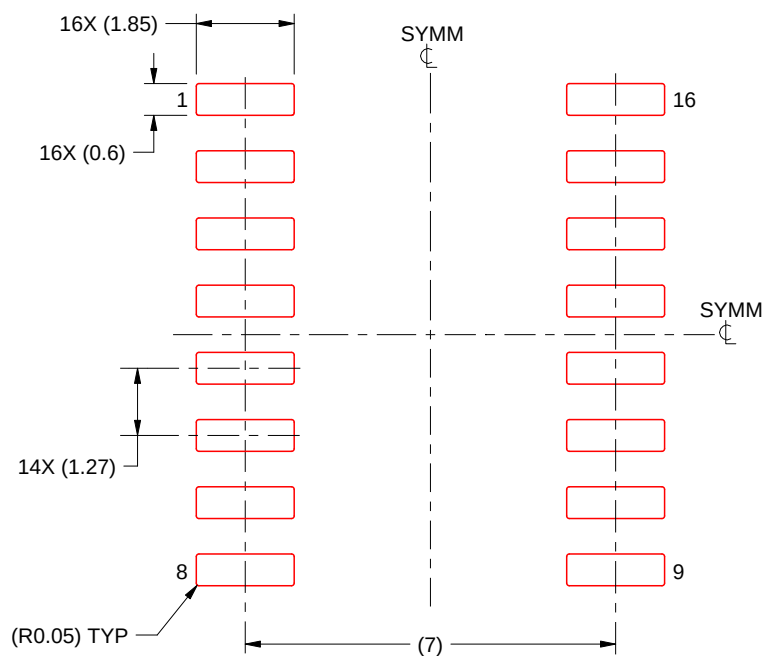


4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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