

SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

SDLS195 – MARCH 1985 – REVISED MARCH 1988

'LS673

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

'LS674

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

description

SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-level ($\overline{CS}$) input disables both the shift-register clock and the storage register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

SN54LS674, SN74LS674

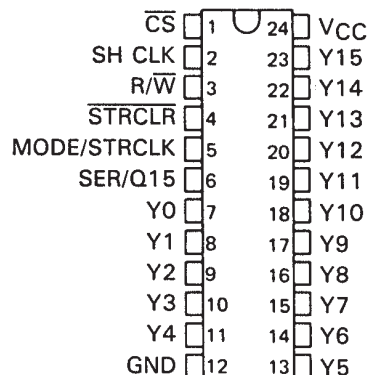
The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering a serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

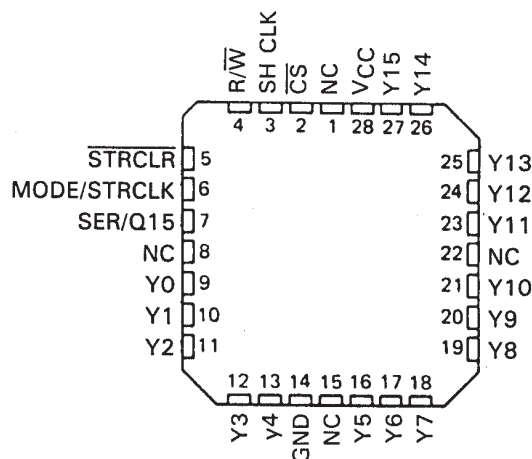
- 1) Hold (do nothing)
- 2) Write (serially via input/output)
- 3) Read (serially)
- 4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

SN54LS673 . . . J OR W PACKAGE SN74LS673 . . . DW OR N PACKAGE (TOP VIEW)



SN54LS673 . . . FK PACKAGE (TOP VIEW)

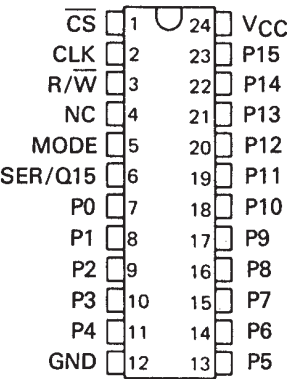


NC—No internal connection

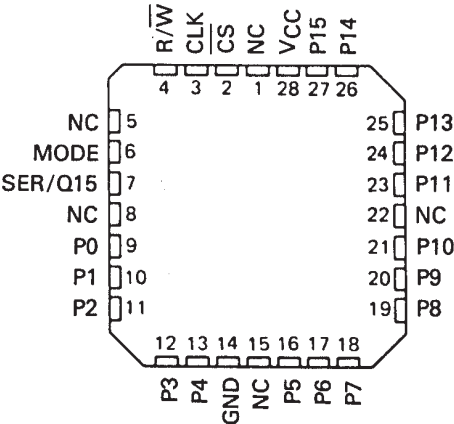
SN54LS673, SN54LS674, SN74LS673, SN74LS674
16-BIT SHIFT REGISTERS

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SN54LS674 . . . J OR W PACKAGE
SN74LS674 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS674 . . . FK PACKAGE
(TOP VIEW)



'LS673
FUNCTION TABLE

INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
CS	R/W	SH CLK	STRCLR	MODE/ STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES		YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO		NO	NO	YES

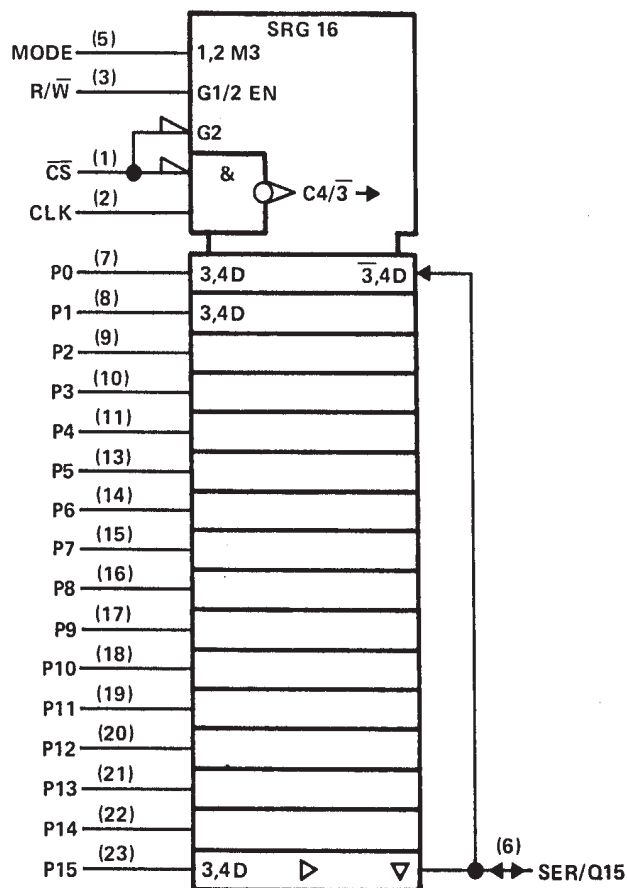
'LS674 FUNCTION TABLE

INPUTS				SER/ Q15	OPERATION
CS	R/W	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input including transitions)
Z = high impedance, input mode
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.
Q15 = present content of 15th bit of the shift register
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.
P15 = level of input P15

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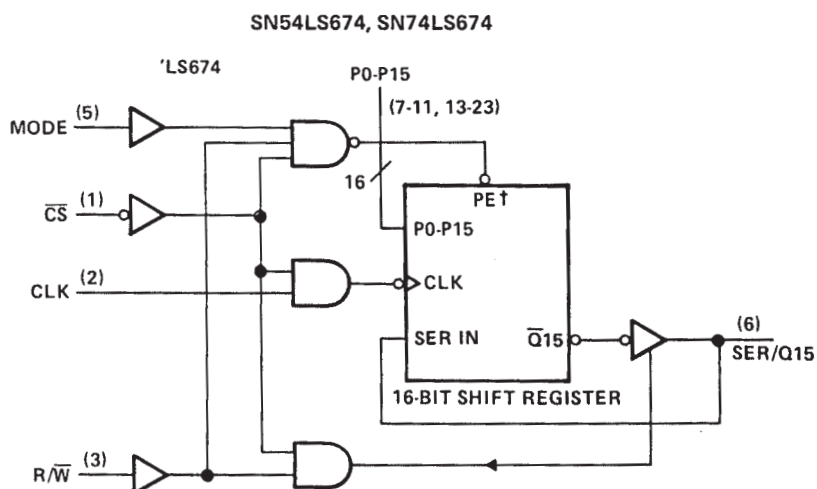
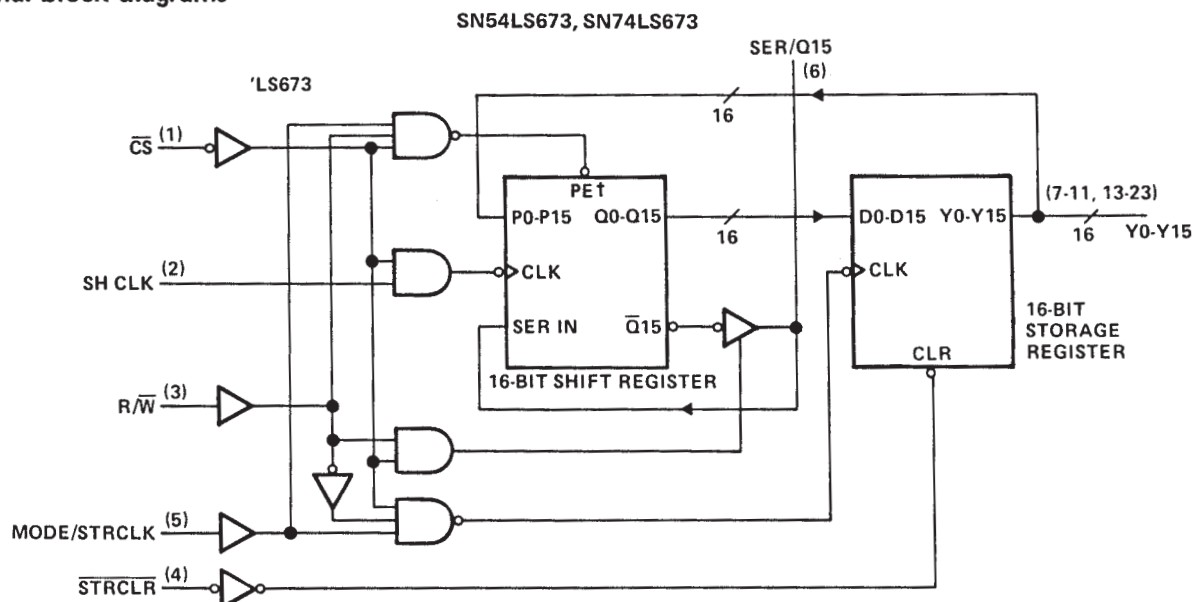
'LS673



SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

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functional block diagrams



†When PE is active, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place. Pin numbers shown are for DW, J, N, and W packages.

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EQUIVALENT OF SER/Q15 AND PARALLEL INPUTS	EQUIVALENT OF OTHER INPUTS	SER/Q15 OUTPUT	TYPICAL OF Y0 THRU Y15 OUTPUTS ('LS673 ONLY)
SER/Q15: $R_{eq} = 20\text{ k}\Omega\text{ NOM}$ PARALLEL INPUTS: $R_{eq} = 30\text{ k}\Omega\text{ NOM}$			

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: SER/Q15	5.5 V
All others	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS673, SN54LS674	−55°C to 125°C
SN74LS673, SN74LS674	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

			SN54LS'			SN74LS'			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V	
I _{OH}	High-level output current	SER/Q15	−1			−2.6			mA	
		Y0 thru Y15	−0.4			−0.4				
I _{OL}	Low-level output current	SER/Q15	12			24			mA	
		Y0 thru Y15	4			8				
f _{clock}	Clock frequency		0	20		0	20		MHz	
t _{w(clock)}	Width of clock input pulse		20			20			ns	
t _{w(clear)}	Width of clear input pulse		20			20			ns	
t _{su}	Setup time	SER/Q15	20			20			ns	
		P0 thru P15	20			20				
		Mode	35			35				
		R/ $\overline{W}$, $\overline{CS}$	35			35				
		SH CLK ↓ to Mode/STR CLK ↑ See Note 2	25			25				
t _h	Hold time	SER/Q15	0			0			ns	
		P0 thru P15	'LS673	0			0			
			'LS674	5.0			5.0			
		Mode	0			0				
T _A	Operating free-air temperature		−55	125		0	70		°C	

NOTE 2: This setup time ensures the storage register will see stable data from the shift register.

SN54LS673, SN54LS674, SN74LS673, SN74LS674

16-BIT SHIFT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage		0.7			0.8			V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V	
V _{OH}	High-level output voltage	SER/Q15	V _{CC} = MIN, V _{IH} = 2 V,			2.4	3.2	2.4	3.1	V
		Y0 thru Y15¶	V _{IL} = V _{ILmax} , I _{OH} = MAX			2.5	3.4	2.7	3.4	
V _{OL}	Low-level output voltage	SER/Q15	V _{CC} = MIN, V _{IH} = 2 V,	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
				I _{OL} = 24 mA			0.35	0.5		
		Y0 thru Y15¶	V _{IL} = V _{ILmax}	I _{OL} = 4 mA	0.25	0.4	0.25	0.4		
				I _{OL} = 8 mA			0.35	0.5		
I _{OZH}	Off-state output current, high-level voltage applied	SER/Q15	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 2.7 V			40			μA	
I _{OZL}	Off-state output current, low-level voltage applied	SER/Q15	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 0.4 V			- 0.4			mA	
I _I	Input current at maximum input voltage	SER/Q15	V _{CC} = MAX	V _I = 5.5 V	0.1			0.1	mA	
		Others		V _I = 7 V	0.1			0.1		
I _{IH}	High-level input current	SER/Q15	V _{CC} = MAX, V _I = 2.7 V	40			40			μA
		Others		20			20			
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.4 V			-0.4			mA	
I _{OS}	Short-circuit output current§	SER/Q15	V _{CC} = MAX			-30	-130	-30	-130	mA
		Y0 thru Y15¶				-20	-100	-20	-100	
I _{CC}	Supply current	'LS673	V _{CC} = MAX			50	80	52	80	mA
		'LS674				25	40	25	40	

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

¶ 'LS673 only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	'LS673		'LS674		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	FROM	TO	FROM	TO					
f _{max}	SH CLK	SER/Q15	CLK	SER/Q15	R _L = 667 Ω, C _L = 45 pF	20	28		MHz
t _{PHL}	STRCLR	Y0 thru Y15			R _L = 2 kΩ, C _L = 15 pF		25	40	ns
t _{PLH}	MODE/	Y0 thru Y15					28	45	
t _{PHL}	STRCLK						30	45	
t _{PLH}	SH CLK	SER/Q15	CLK	SER/Q15	R _L = 667 Ω, C _L = 45 pF		21	33	ns
t _{PHL}							26	40	
t _{PZH}	CS, R/W	SER/Q15	CS, R/W	SER/Q15	R _L = 667 Ω, C _L = 45 pF		30	45	ns
t _{PZL}							30	45	
t _{PHZ}	CS, R/W	SER/Q15	CS, R/W	SER/Q15	R _L = 667 Ω, C _L = 5 pF		25	40	ns
t _{PLZ}							25	40	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-88602013A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88602013A SNJ54LS 673FK
5962-8860201JA	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860201JA SNJ54LS673J
5962-8860201JA	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860201JA SNJ54LS673J
5962-8860201LA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8860201LA SNJ54LS673JT
5962-8860201LA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8860201LA SNJ54LS673JT
5962-88607013A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88607013A SNJ54LS 674FK
5962-88607013A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88607013A SNJ54LS 674FK
5962-8860701JA	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860701JA SNJ54LS674J
5962-8860701JA	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860701JA SNJ54LS674J
SN54LS673J	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS673J
SN54LS673J	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS673J
SN54LS673J.A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS673J
SN54LS673J.A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS673J
SN54LS674J	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS674J
SN54LS674J	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS674J
SN54LS674J.A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS674J
SN54LS674J.A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS674J
SN74LS673DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS673

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS673DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS673
SN74LS673DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS673
SN74LS673DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS673
SN74LS674DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS674
SN74LS674DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS674
SN74LS674DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS674
SN74LS674DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS674
SNJ54LS673FK	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88602013A SNJ54LS 673FK
SNJ54LS673FK	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88602013A SNJ54LS 673FK
SNJ54LS673FK.A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88602013A SNJ54LS 673FK
SNJ54LS673FK.A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88602013A SNJ54LS 673FK
SNJ54LS673J	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860201JA SNJ54LS673J
SNJ54LS673J	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860201JA SNJ54LS673J
SNJ54LS673J.A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860201JA SNJ54LS673J
SNJ54LS673J.A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860201JA SNJ54LS673J
SNJ54LS673JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8860201LA SNJ54LS673JT
SNJ54LS673JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8860201LA SNJ54LS673JT

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS673JT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8860201LA SNJ54LS673JT
SNJ54LS673JT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8860201LA SNJ54LS673JT
SNJ54LS674FK	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88607013A SNJ54LS 674FK
SNJ54LS674FK	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88607013A SNJ54LS 674FK
SNJ54LS674FK.A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88607013A SNJ54LS 674FK
SNJ54LS674FK.A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88607013A SNJ54LS 674FK
SNJ54LS674J	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860701JA SNJ54LS674J
SNJ54LS674J	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860701JA SNJ54LS674J
SNJ54LS674J.A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860701JA SNJ54LS674J
SNJ54LS674J.A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860701JA SNJ54LS674J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54LS673, SN54LS674, SN74LS673, SN74LS674 :

- Catalog : [SN74LS673](#), [SN74LS674](#)
- Military : [SN54LS673](#), [SN54LS674](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE

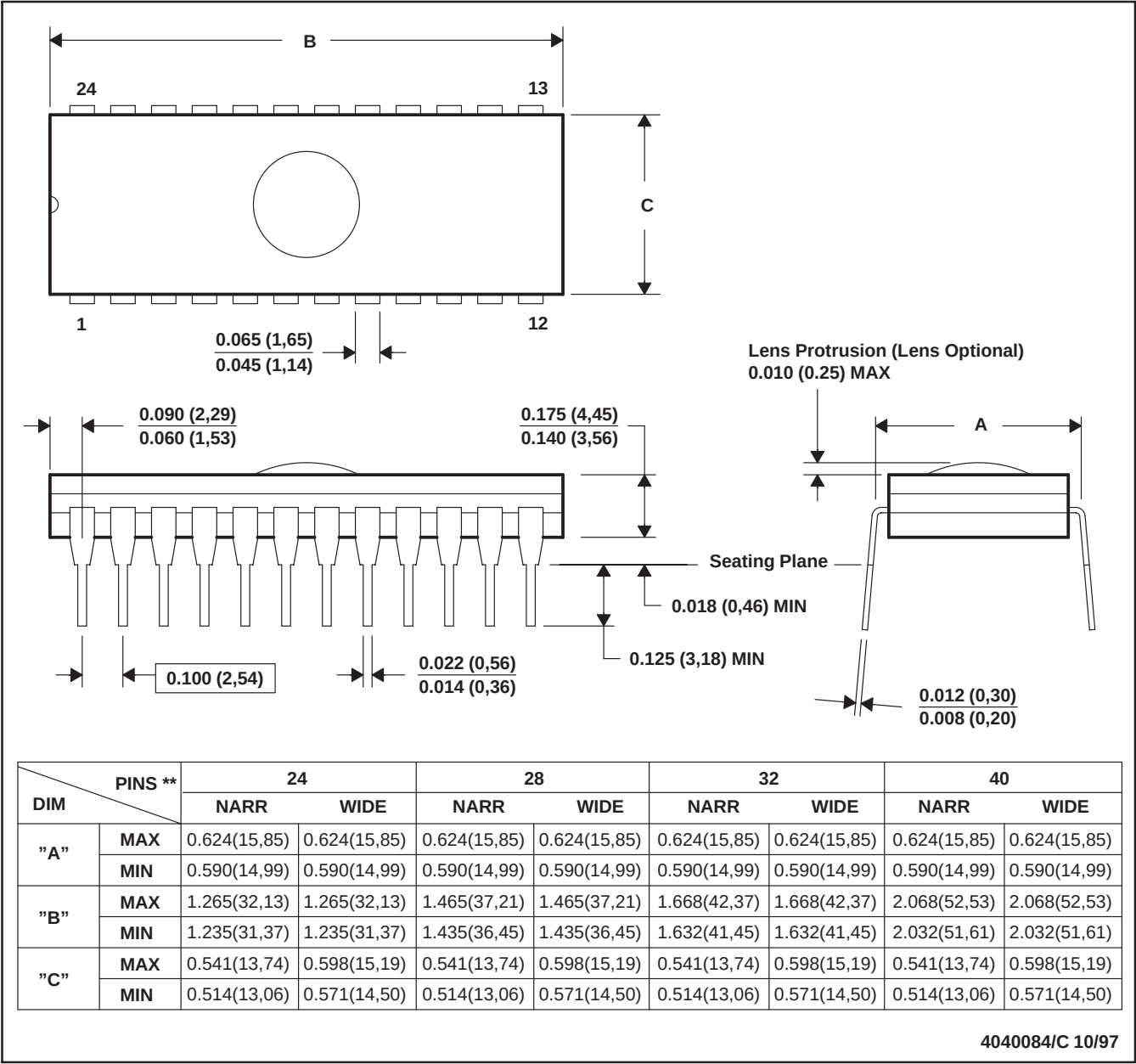


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS673DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LS673DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LS674DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LS674DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

J (R-GDIP-T**)
24 PINS SHOWN

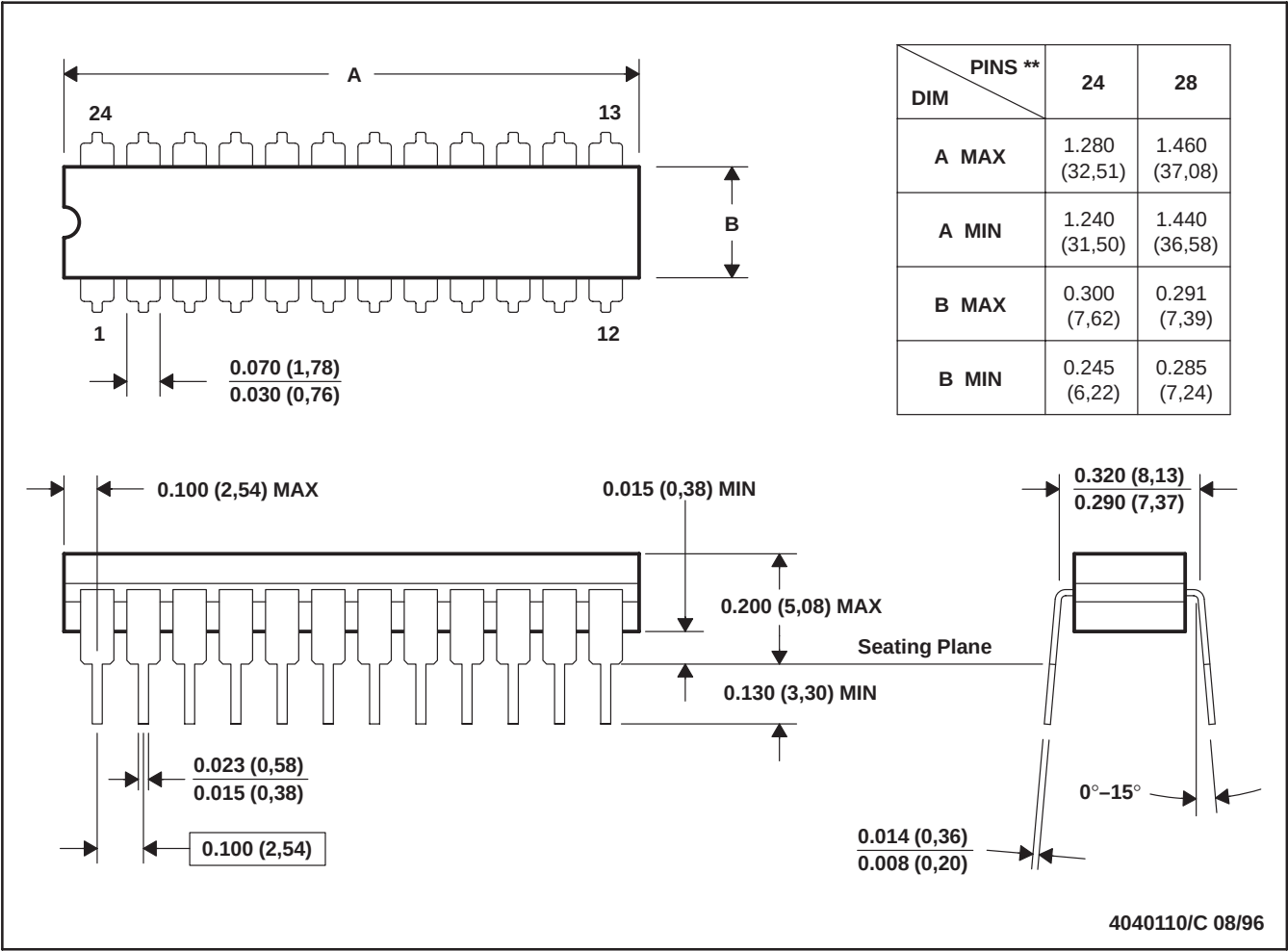
CERAMIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
- D. This package can be hermetically sealed with a ceramic lid using glass frit.
- E. Index point is provided on cap for terminal identification.

JT (R-GDIP-T**) 24 LEADS SHOWN

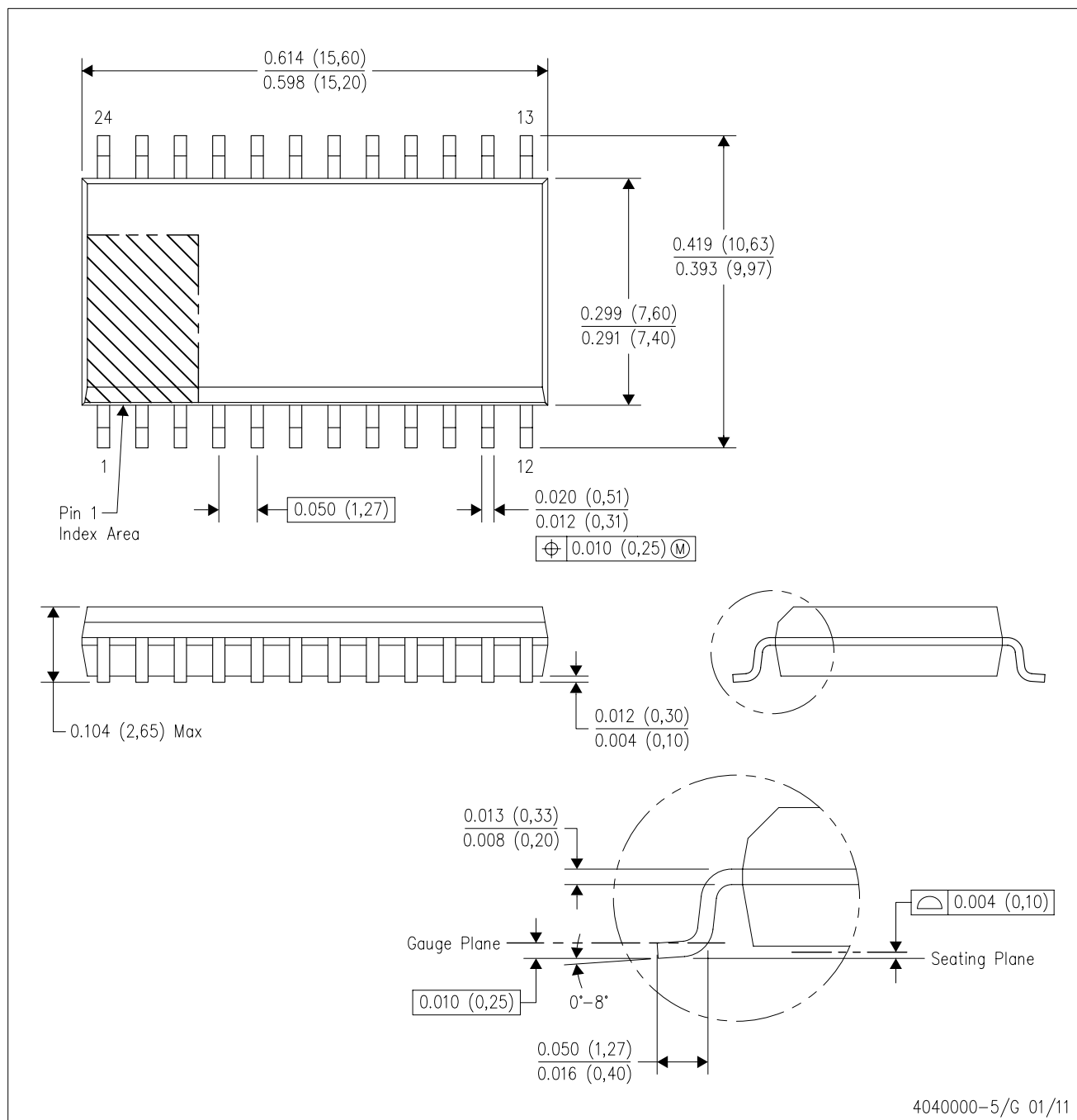
CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



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