

SN54F74, SN74F74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDFS046A – MARCH 1987 – REVISED OCTOBER 1993

- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

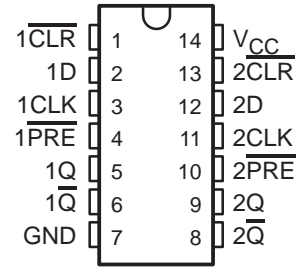
The SN54F74 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F74 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

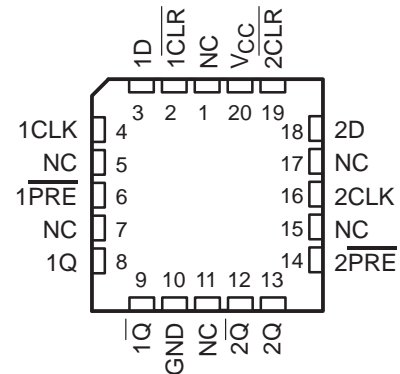
INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H^{\dagger}	H^{\dagger}
H	H	\uparrow	H	H	L
H	H	\uparrow	L	L	H
H	H	L	X	Q_0	$\overline{\text{Q}}_0$

\dagger The output levels are not guaranteed to meet the minimum levels for V_{OH} . Furthermore, this configuration is nonstable; that is, it will not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

SN54F74 ... J PACKAGE
SN74F74 ... D OR N PACKAGE
(TOP VIEW)



SN54F74 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

SDFS046A – MARCH 1987 – REVISED OCTOBER 1993

Timing diagram for the 74VHC163 4-bit binary counter. The diagram shows two clock inputs, 1CLK and 2CLK, and two data outputs, 1Q and 2Q. The 1Q output is shown in two states: 1Q and 1Q-bar. The 2Q output is shown in two states: 2Q and 2Q-bar. The diagram illustrates the timing relationship between the clock inputs and the data outputs, showing that the outputs change state on the rising edge of the clock inputs.

The logic diagram shows a 2-bit counter implemented with three T flip-flops (labeled 'TG') and various combinational logic gates. The inputs are PRE (active-low), CLK, D, and CLR (active-low). The outputs are q and q-bar. The circuit uses clock (C) and complemented clock (C-bar) signals. The logic involves AND, OR, and XOR gates to generate the next state based on the current state and inputs.

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−1.2 V to 7 V
Input current range	−30 mA to 5 mA
Voltage range applied to any output in the high state	−0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F74	−55°C to 125°C
SN74F74	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

SN54F74, SN74F74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDFS046A – MARCH 1987 – REVISED OCTOBER 1993

recommended operating conditions

		SN54F74			SN74F74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–1			–1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F74		SN74F74		UNIT
				MIN	TYP†	MAX	MIN	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				–1.2	–1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -1\text{ mA}$		2.5	3.4	2.5	3.4	V
		$V_{CC} = 4.75\text{ V}$, $I_{OH} = -1\text{ mA}$				2.7		
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 20\text{ mA}$		0.3	0.5	0.3	0.5	V
I_I		$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1		0.1	mA
I_{IH}		$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20		20	μA
I_{IL}	Data, CLK	$V_{CC} = 5.5\text{ V}$, $V_I = 0.5\text{ V}$			–0.6		–0.6	mA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$				–1.8		–1.8	
I_{OS}^\ddagger		$V_{CC} = 5.5\text{ V}$, $V_O = 0$		–60	–150	–60	–150	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, See Note 2		10.5	16	10.5	16	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with D, CLK, and $\overline{\text{PRE}}$ grounded then with D, CLK, and $\overline{\text{CLR}}$ grounded.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 5 V, T _A = 25°C		SN54F74		SN74F74		UNIT
			'F74						
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	100	0	80	0	100	MHz
t _w	Pulse duration		CLK high, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4	4	4		ns	
			CLK low	5	6	5			
t _{su}	Setup time, data before CLK↑	High	2	3	2		ns		
		Low	3	4	3				
	Setup time, inactive-state before CLK↑§	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ to CLK	2	3	2				
t _h	Hold time, data after CLK↑	High	1	2	1		ns		
		Low	1	2	1				

§ Inactive-state setup time is also referred to as recovery time.



SN54F74, SN74F74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDFS046A – MARCH 1987 – REVISED OCTOBER 1993

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			'F74			SN54F74		SN74F74		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			100	145		80		100		MHz
t _{PLH}	CLK	Q or \overline{Q}	3	4.9	6.8	3.8	8.5	3	7.8	ns
t _{PHL}			3.6	5.8	8	4.4	10.5	3.6	9.2	
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or \overline{Q}	2.4	4.2	6.1	3.2	8	2.4	7.1	ns
t _{PHL}			2.7	6.6	9	3.5	11.5	2.7	10.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9759201Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9759201Q2A SNJ54F 74FK
5962-9759201QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759201QC A SNJ54F74J
5962-9759201QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759201QD A SNJ54F74W
JM38510/34101B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34101B2A
JM38510/34101B2A.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34101B2A
JM38510/34101BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34101BCA
JM38510/34101BCA.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34101BCA
JM38510/34101BDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34101BDA
JM38510/34101BDA.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34101BDA
M38510/34101B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34101B2A
M38510/34101BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34101BCA
M38510/34101BDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34101BDA
SN54F74J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54F74J
SN54F74J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54F74J
SN74F74D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	F74
SN74F74DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F74
SN74F74DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F74

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74F74DRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F74
SN74F74N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F74N
SN74F74N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F74N
SN74F74NE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F74N
SN74F74NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F74
SN74F74NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F74
SNJ54F74FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759201Q2A SNJ54F74FK
SNJ54F74FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759201Q2A SNJ54F74FK
SNJ54F74J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759201QC A SNJ54F74J
SNJ54F74J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759201QC A SNJ54F74J
SNJ54F74W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759201QD A SNJ54F74W
SNJ54F74W.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759201QD A SNJ54F74W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54F74, SN74F74 :

- Catalog : [SN74F74](#)
- Military : [SN54F74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74F74NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F74DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74F74NSR	SOP	NS	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9759201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9759201QDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/34101B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/34101B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/34101BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/34101BDA.A	W	CFP	14	25	506.98	26.16	6220	NA
M38510/34101B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/34101BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74F74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F74N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74F74N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74F74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74F74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54F74FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54F74FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54F74W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54F74W.A	W	CFP	14	25	506.98	26.16	6220	NA

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated