



REF60xx 高精度電圧リファレンス、内蔵ADCドライブ・バッファ付

1 特長

- 優れた温度ドリフト係数性能
 - 40°C~+125°Cの範囲で5ppm/°C (最大値)
- 非常に低ノイズ
 - 総ノイズ: 47μFコンデンサで5μV_{RMS}
 - 1/fノイズ(0.1Hz~10Hz): 3μV_{pp}/V
- ADCドライブ・バッファ内蔵
 - 低い出力インピーダンス: 50mΩ未満(0~200kHz)
 - ADS8881との組み合わせで最初のサンプルでも18ビットの精度
 - バースト・モードのDAQシステムに対応
- 低い消費電流: 820μA
- 低いシャットダウン時電流: 1μA
- 高い初期精度: ±0.05%
- 非常に低いノイズと歪み
 - SNR: 100.5dB, THD: -125dB (ADS8881)
 - SNR: 106dB, THD: -120dB (ADS127L01)
- 出力電流ドライブ: ±4mA
- 短絡電流をプログラム可能
- ADS88xxファミリのSAR ADCおよびADS127xxファミリの広帯域ΔΣ ADCのREFピンを駆動できることを確認済み

2 アプリケーション

- ATEテスターおよびオシロスコープ
- テストおよび計測機器
- PLC用のアナログ入力モジュール
- 医療用機器
- 高精度データ・アキュイジション・システム

3 概要

REF6000ファミリの電圧リファレンスには、低出力インピーダンスのバッファが搭載されているため、ユーザーは高精度データ・コンバータのREFピンを直接駆動しながら、直線性、歪み、ノイズ性能を維持できます。ほとんどの高精度SARおよびデルタ・シグマADCでは、変換プロセス中に、バイナリ重み付けされたコンデンサをREFピン上に切り替えます。この動的な負荷をサポートするため、電圧リファレンスの出力は、低い出力インピーダンス(高い帯域幅)のバッファを経由する必要があります。REF6000ファミリのデバイスは、ADS88xxファミリのSAR ADC、ADS127xxファミリのデルタ・シグマADC、および他のD/Aコンバータ(DAC)のREFピンを駆動するのに最適ですが、他の用途にも使用できます。

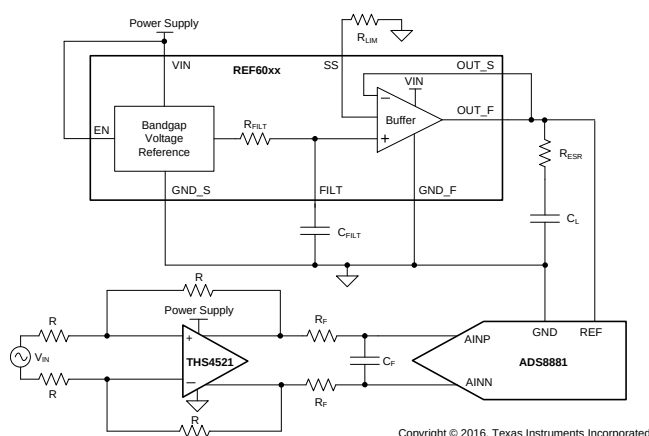
REF6000ファミリの電圧リファレンスは、ADS8881のREFピンを駆動中の最初の変換時でも出力電圧が1 LSB (18ビット)以上低下しません。この機能は、バースト・モード、イベント・トリガ、等価時間サンプリング、可変サンプリング・レートのデータ・アキュイジション・システムに非常に便利です。REF6000ファミリのREF60xxバリエーションは、最大温度ドリフト係数の定格がわずか5 ppm/°Cで、電圧リファレンスと低インピーダンスの出力バッファの両方の組み合わせについて、初期精度が0.05%です。REF6000ファミリの各種の温度ドリフト係数オプションについては、デバイス比較表を参照してください。

製品情報⁽¹⁾

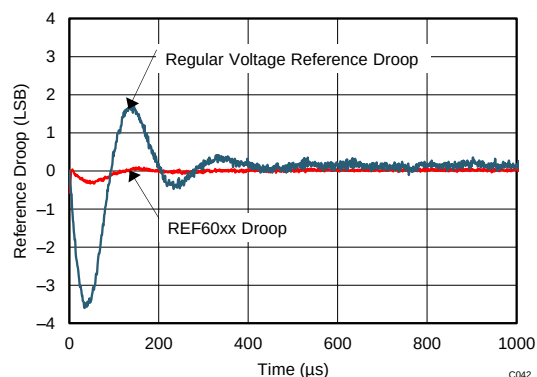
型番	パッケージ	本体サイズ(公称)
REF60xx	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション



リファレンス電圧低下の比較 (1 LSB = 19.07μV、ADS8881で1 MSPSの場合)



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4 改訂履歴

Revision A (June 2016) から Revision B に変更

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• 「概要」を変更	1
• Changed the <i>Device Comparison Table</i>	3
• Changed list of devices for output current in Recommended Operating Conditions	4
• Changed load regulation max value for REF6050 at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ from 30 to 50	5
• Changed "second pass" to "final pass" in last paragraph of <i>Solder Heat Shift</i> section	14
• Added link to SLYY097 in <i>Overview</i> section	19

2016年5月発行のものから更新

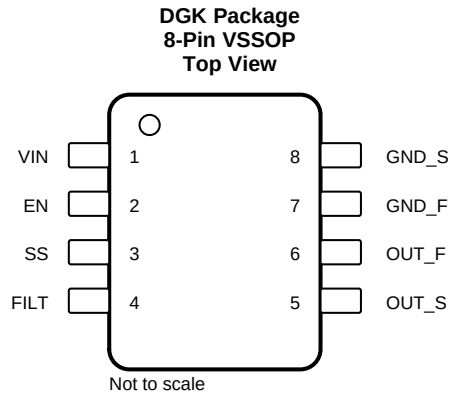
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• 製品プレビューから生産データへ変更	1
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5 Device Comparison Table

DEVICE FAMILY	TEMPERATURE DRIFT
REF60xx	5 ppm/°C from –40 to 125°C
REF61xx	8 ppm/°C from –40 to 125°C
REF62xx	3 ppm/°C from 0 to 70°C

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	2	Input	Enable pin
FILT	4	—	Filter capacitor pin. A capacitor ($C_{FILT} \geq 1 \mu F$) must be connected between the FILT pin and ground for stability.
GND_F	7	Ground	Ground force pin
GND_S	8	Ground	Ground sense pin
OUT_F	6	Output	Output voltage force pin
OUT_S	5	Input	Output voltage sense pin
SS	3	—	Short circuit current limit pin. Connect a resistor to this pin to set the output short-circuit current limit. Connect to VIN pin for highest current limit
VIN	1	Power	Input supply voltage pin

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	V_{IN}	−0.3	6	V
	V_{EN}	−0.3	$V_{IN} + 0.3$	V
Operating temperature, T_A		−55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN} Supply input voltage ($I_{OUT} = 0$ mA)	REF6025	3		5.5	V
	REF6030, REF6033, REF6041, REF6045	$V_{OUT} + 0.25$		5.5	
	REF6050	5.3		5.5	
V_{EN} Enable voltage		0		V_{IN}	V
I_L Output current	REF6025, REF6030, REF6033, REF6041	−4		4	mA
	REF6045	−3.5		3.5	
	REF6050	−3		3	
T_A Operating temperature		−40	25	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REF60xx	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{ V}$ for all devices except REF6050, $V_{IN} = 5.4\text{ V}$ for REF6050, $I_L = 0\text{ mA}$, $C_L = 22\text{ }\mu\text{F}$, $C_{FILT} = 1\text{ }\mu\text{F}$, and $V_{EN} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
Output voltage accuracy				-0.05%	0.05%		
Output voltage temperature coefficient ⁽¹⁾					5		ppm/°C
LINE AND LOAD REGULATION							
$\Delta V_{O(\Delta V)}$ Line regulation	REF6025	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$T_A = 25^\circ\text{C}$	4	20	ppm/V	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		30		
	REF6030, REF6033, REF6041, REF6045	$V_{OUT} + 0.25\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$T_A = 25^\circ\text{C}$	4	20		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		30		
	REF6050	$V_{OUT} + 0.3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$T_A = 25^\circ\text{C}$	7	60		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		120		
$\Delta V_{O(\Delta I_L)}$ Load regulation, sourcing and sinking	REF6025, REF6030, REF6033, REF6041	$I_L = 0\text{ mA}$ to 4 mA , $V_{IN} = V_{OUT} + 600\text{ mV}$	$T_A = 25^\circ\text{C}$	2	20	ppm/mA	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		30		
	REF6045	$I_L = 0\text{ mA}$ to 3.5 mA , $V_{IN} = V_{OUT} + 600\text{ mV}$	$T_A = 25^\circ\text{C}$	2	20		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		30		
	REF6050	$I_L = 0\text{ mA}$ to 3 mA , $V_{IN} = V_{OUT} + 400\text{ mV}$	$T_A = 25^\circ\text{C}$	2	20		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		50		
I_{SC} Short-circuit current	SS = open			10.5		mA	
NOISE							
Total integrated noise	$C_L = 22\text{ }\mu\text{F}$				5		μV_{RMS}
	$C_L = 47\text{ }\mu\text{F}$				5		
Low frequency noise	0.1 Hz $\leq f \leq$ 10 Hz				3		$\mu\text{V}_{PP}/\text{V}$
OUTPUT IMPEDANCE							
Output impedance	f = DC to 200 kHz, $C_L = 47\text{ }\mu\text{F}$				50		m Ω
TURN-ON TIME							
t_{on} Turn-on time	0.1% settling, $C_L = 47\text{ }\mu\text{F}$, SS = open, REF6025				100		ms
HYSTERESIS AND LONG TERM DRIFT							
Long term stability	0 to 1000h at 25°C				80		ppm
	1000h to 2000h at 25°C				20		
Output voltage hysteresis ⁽²⁾	25°C , -40°C , 125°C , 25°C (cycle 1)				33		ppm
	25°C , -40°C , 125°C , 25°C (cycle 2)				8		
CAPACITIVE LOAD							
C_L Stable output capacitor value					10	47	μF

(1) Temperature drift is specified according to the box method. See the [Feature Description](#) section for more details.

(2) See the [Thermal Hysteresis](#) section.

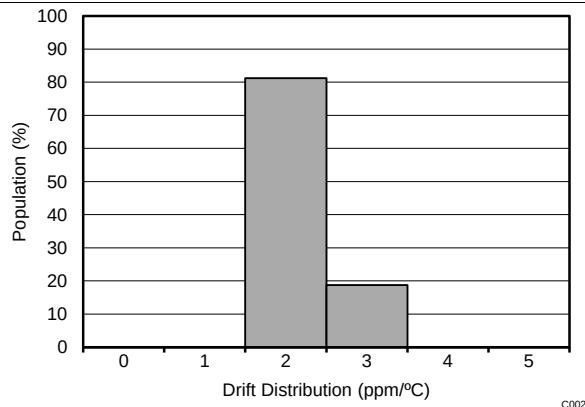
Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{ V}$ for all devices except REF6050, $V_{IN} = 5.4\text{ V}$ for REF6050, $I_L = 0\text{ mA}$, $C_L = 22\text{ }\mu\text{F}$, $C_{FILT} = 1\text{ }\mu\text{F}$, and $V_{EN} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE								
V _{OUT}	Output voltage	REF6025			2.5		V	
		REF6030			3			
		REF6033			3.3			
		REF6041			4.096			
		REF6045			4.5			
		REF6050			5			
POWER SUPPLY								
I _{CC}	Supply current	REF6025, REF6030, REF6033, REF6041	Active mode, V _{EN} = 5 V	T _A = 25°C	0.82	0.90	mA	
				T _A = −40°C to +125°C		1.1		
		REF6045, REF6050	Active mode, V _{EN} = 5 V	T _A = 25°C	0.83	0.95		
				T _A = −40°C to +125°C		1.15		
		Shutdown mode, V _{EN} = 0 V			T _A = 25°C	1	3	μA
					T _A = −40°C to +125°C		15	
Enable pin voltage		Voltage reference in active mode (EN = 1)			1.6		V	
		Voltage reference in shutdown mode (EN = 0)			0.6			
Enable pin current		V _{EN} = 5 V			100	150	nA	
Dropout voltage		REF6025		I _L = 0 mA	500	500	mV	
				I _L = 4 mA		600		
		REF6030, REF6033, REF6041		I _L = 0 mA	50	250		
				I _L = 4 mA		600		
		REF6045		I _L = 0 mA	50	250		
				I _L = 3.5 mA		600		
		REF6050		I _L = 0 mA	100	300		
				I _L = 3 mA		400		

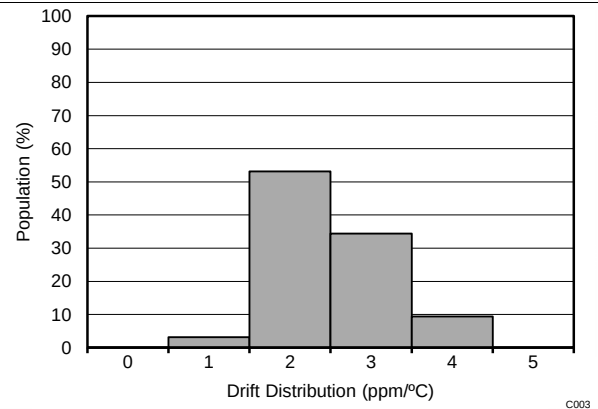
7.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6025 (unless otherwise noted)



$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$

Figure 1. Drift Distribution



$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Figure 2. Drift Distribution

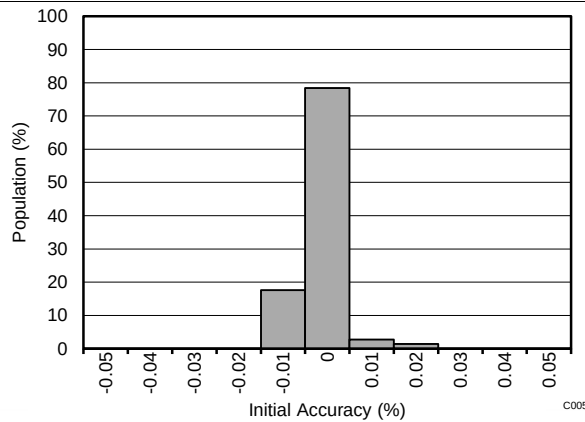


Figure 3. Initial Accuracy Distribution

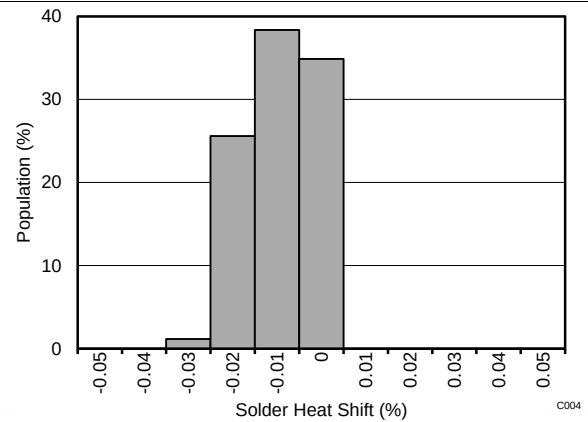


Figure 4. Solder-Heat Shift Distribution

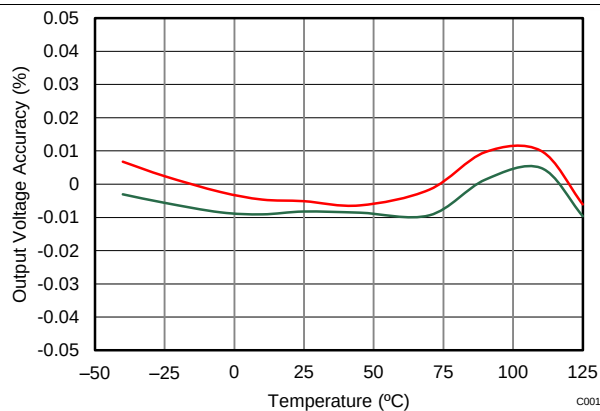


Figure 5. Output Voltage Accuracy vs Temperature

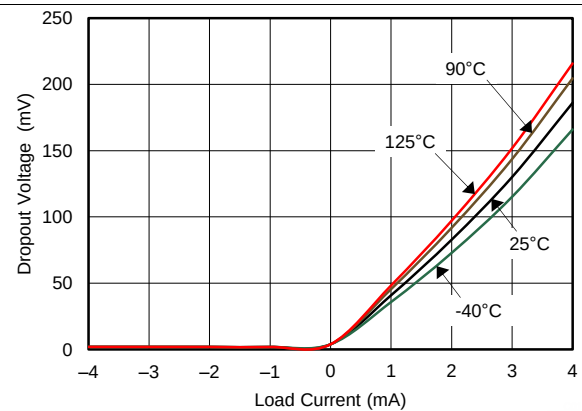
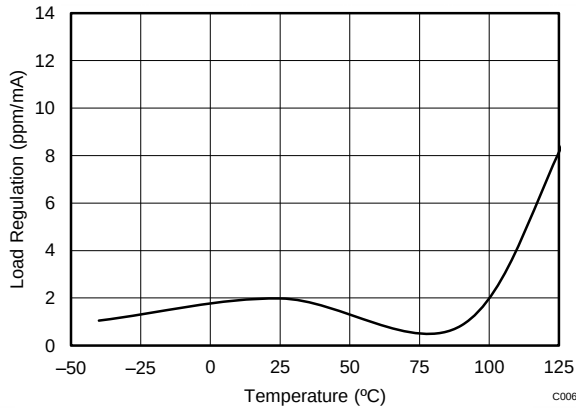


Figure 6. Dropout Voltage vs Load Current

Typical Characteristics (continued)

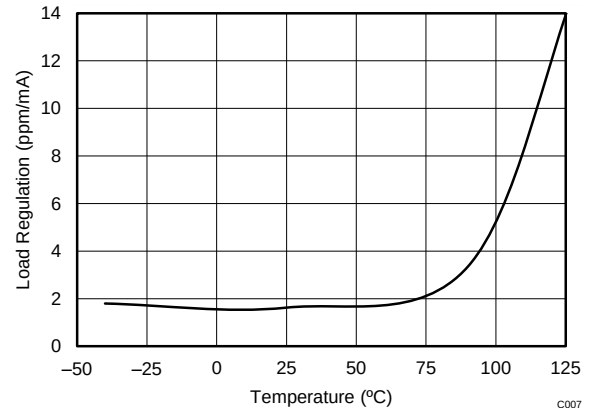
at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6025 (unless otherwise noted)



$$V_{IN} = V_{OUT} + 600\text{ mV},$$

$$I_L = 0\text{ mA to }4\text{ mA}$$

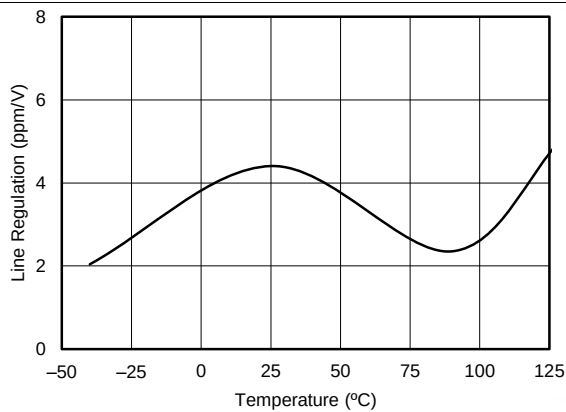
Figure 7. Load Regulation Sourcing vs Temperature



$$V_{IN} = V_{OUT} + 600\text{ mV},$$

$$I_L = 0\text{ mA to }4\text{ mA}$$

Figure 8. Load Regulation Sinking vs Temperature



$$V_{OUT} + 0.25\text{ V} \leq V_{IN} \leq 5.5\text{ V}$$

Figure 9. Line Regulation vs Temperature

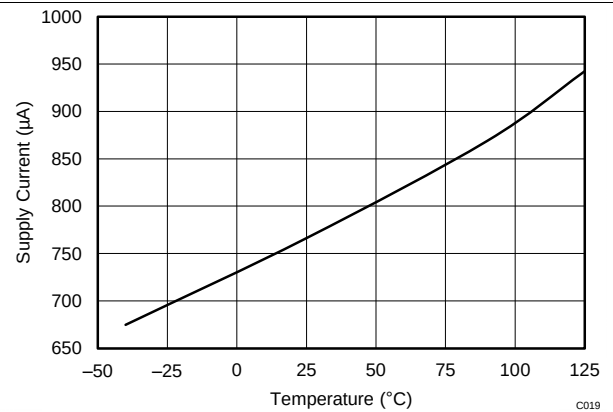


Figure 10. Supply Current vs Temperature

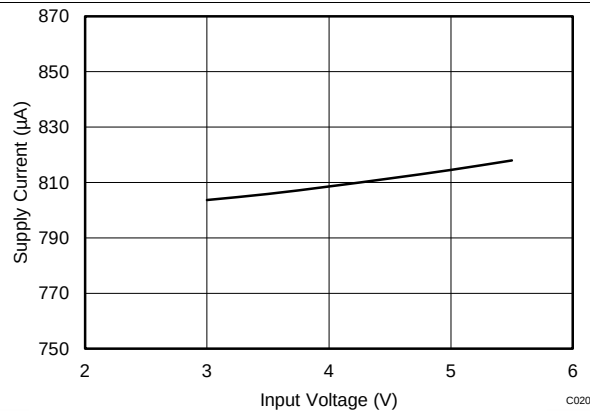


Figure 11. Supply Current vs Input Voltage

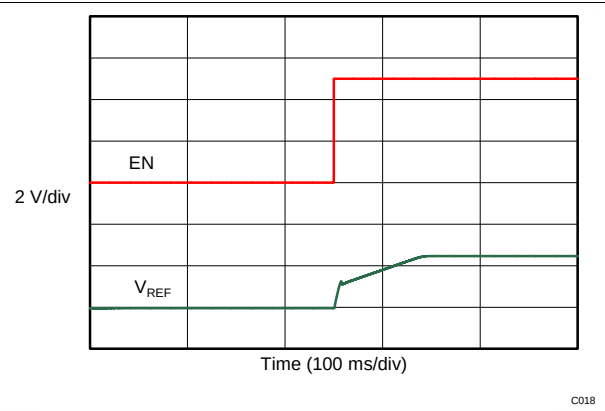
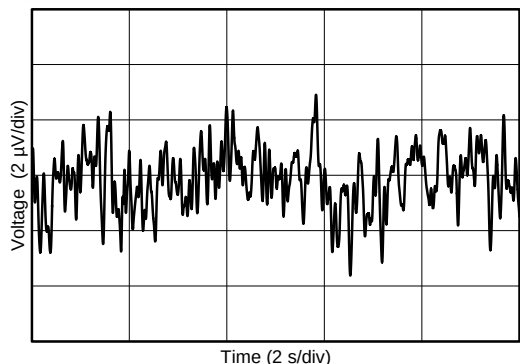


Figure 12. Turn-On Settling Time

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6025 (unless otherwise noted)



C021

Figure 13. 0.1-Hz to 10-Hz Noise

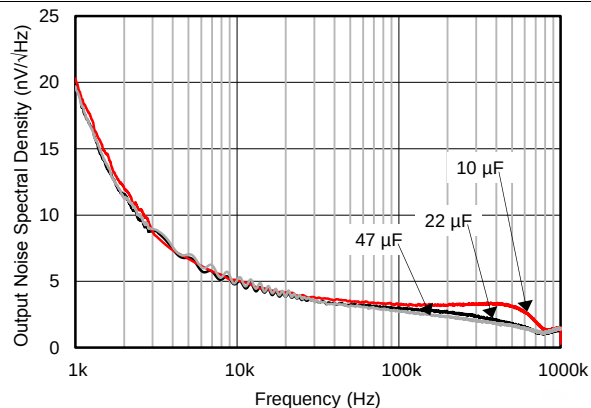


Figure 14. Output-Voltage Noise Spectrum

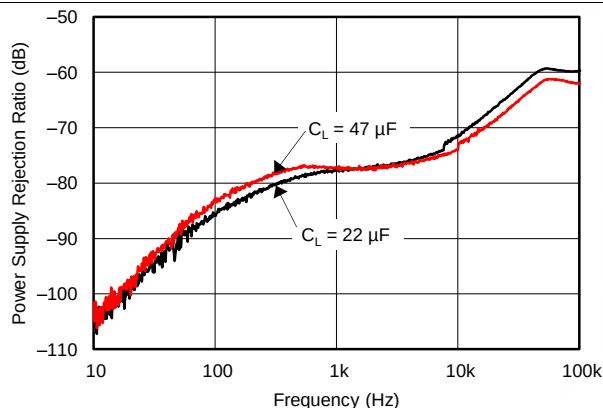
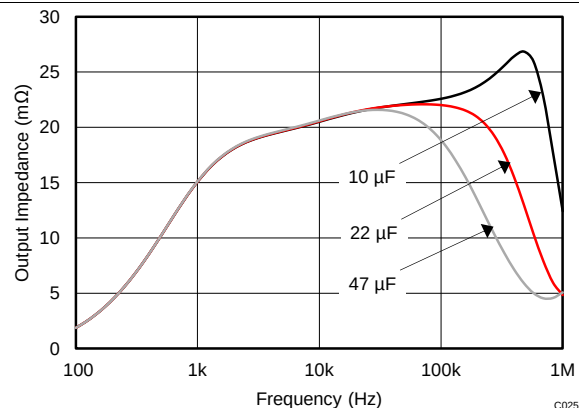


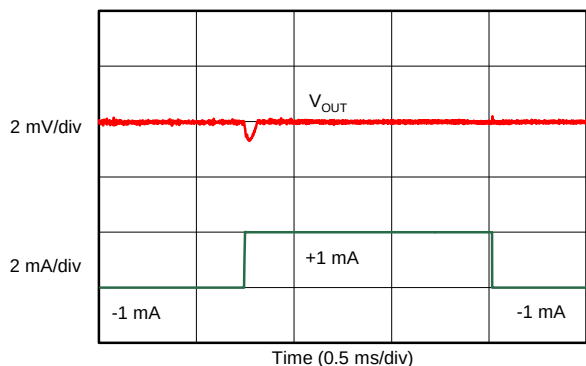
Figure 15. PSRR vs Frequency



C025

Graph obtained by design simulation

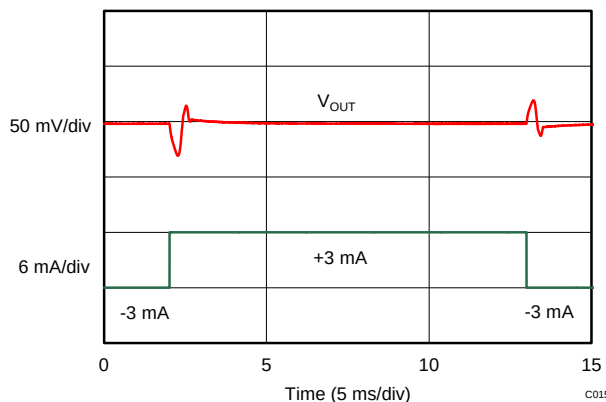
Figure 16. Output Impedance vs Frequency



C014

Load current = $\pm 1\text{ mA}$

Figure 17. Load Transient Response



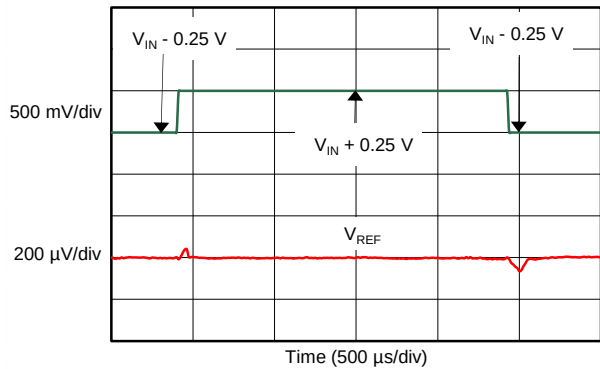
C015

Load current = $\pm 3\text{ mA}$

Figure 18. Load Transient Response

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6025 (unless otherwise noted)



C013

Figure 19. Line Transient Response

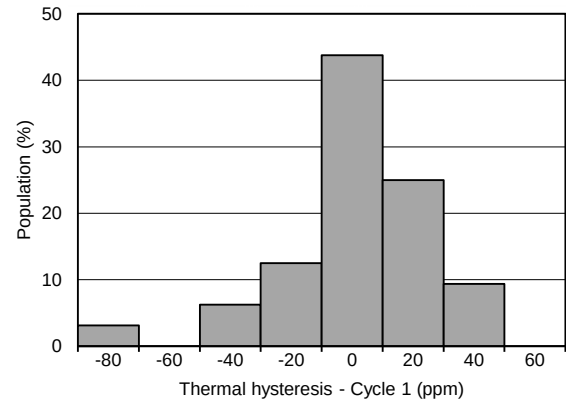


Figure 20. Thermal Hysteresis Distribution (Cycle 1)

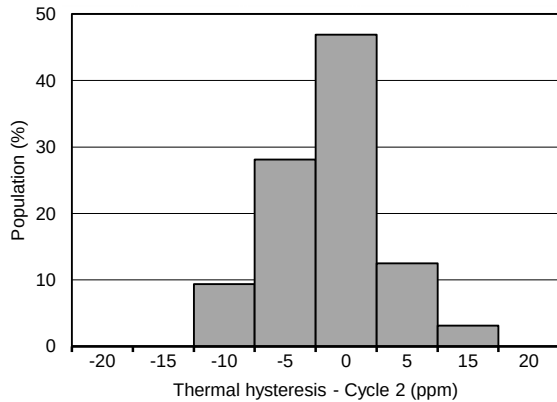
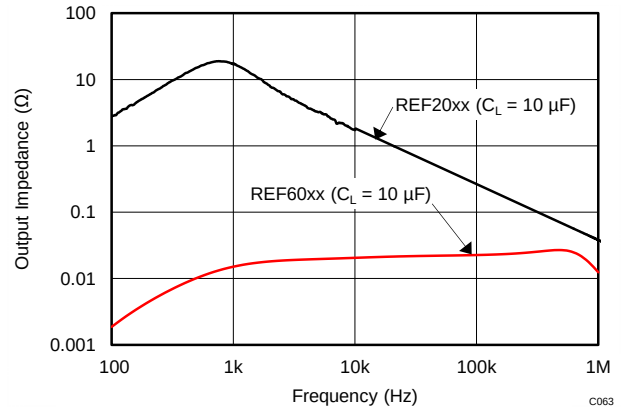
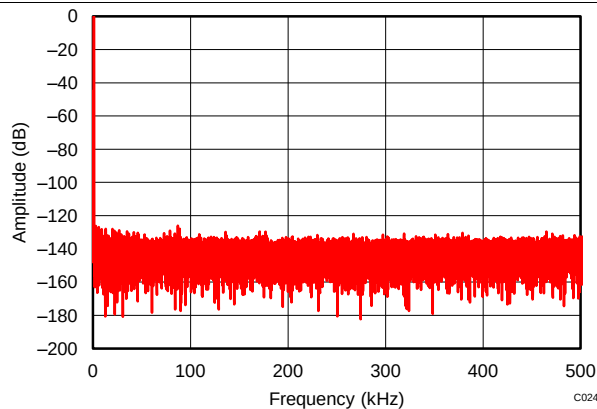


Figure 21. Thermal Hysteresis Distribution (Cycle 2)



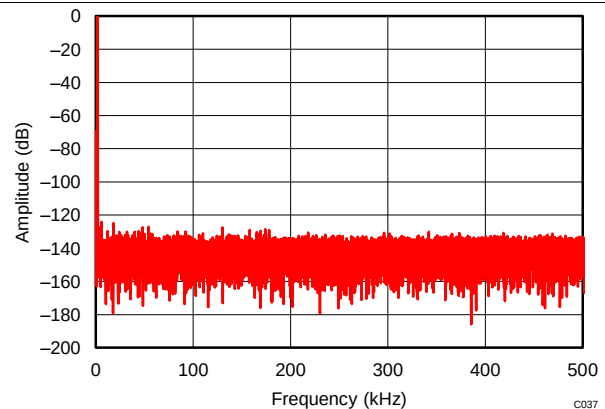
C063

Figure 22. Output Impedance Comparison



C024

Figure 23. Typical FFT Plot



C037

Figure 24. Typical FFT Plot

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6025 (unless otherwise noted)

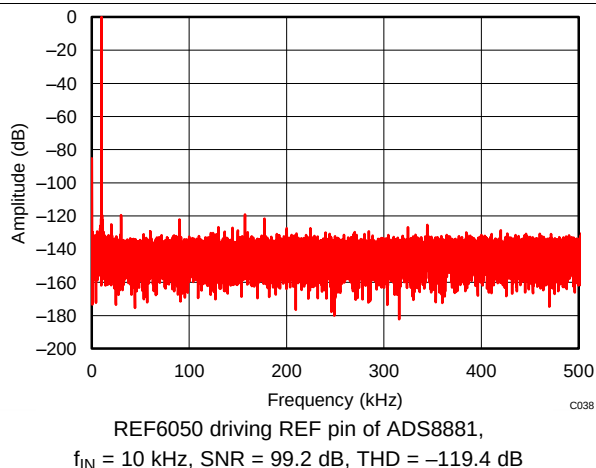


Figure 25. Typical FFT Plot

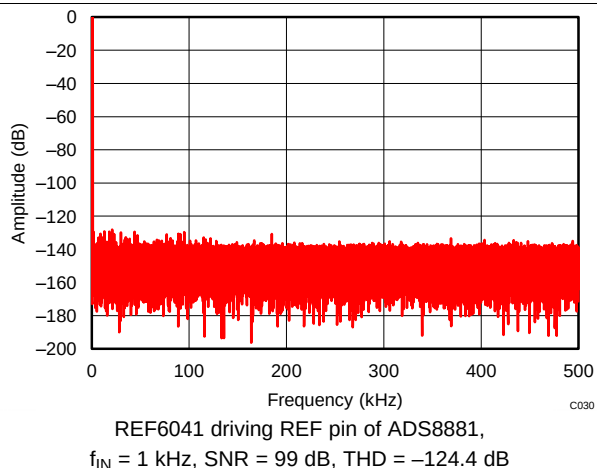


Figure 26. Typical FFT Plot

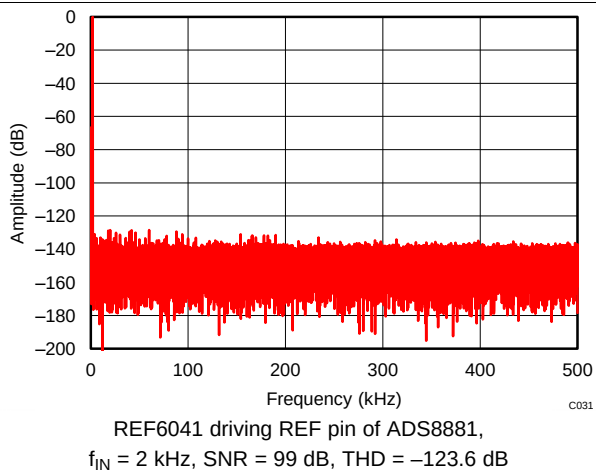


Figure 27. Typical FFT Plot

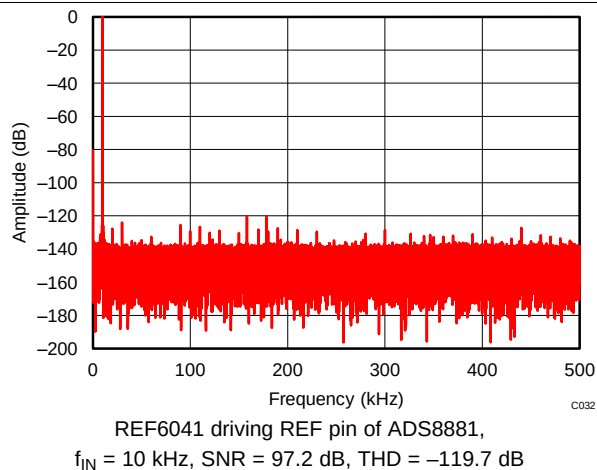


Figure 28. Typical FFT Plot

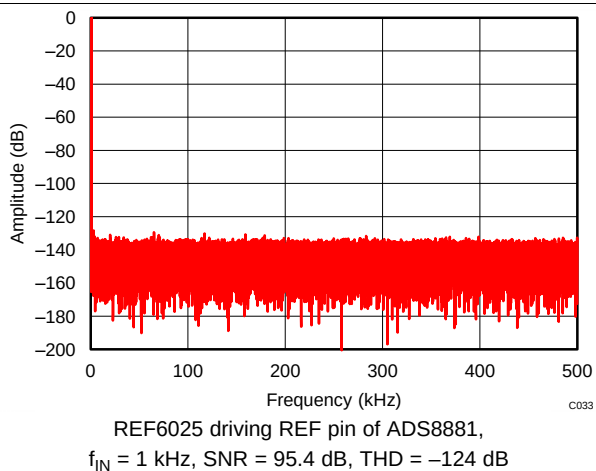


Figure 29. Typical FFT Plot

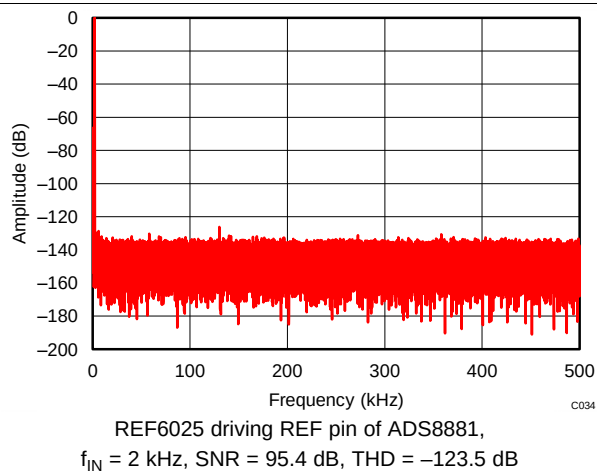


Figure 30. Typical FFT Plot

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6025 (unless otherwise noted)

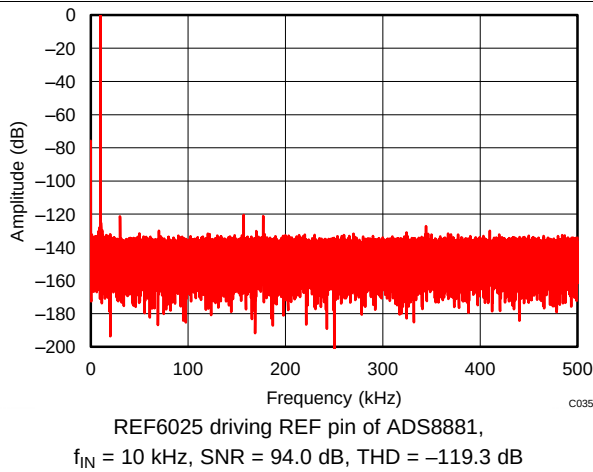


Figure 31. Typical FFT Plot

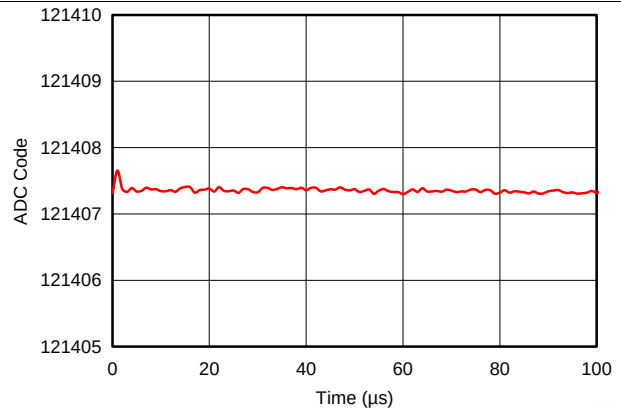


Figure 32. Reference Droop

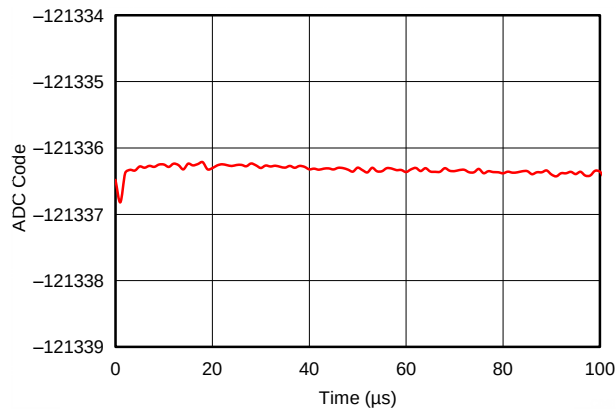


Figure 33. Reference Droop

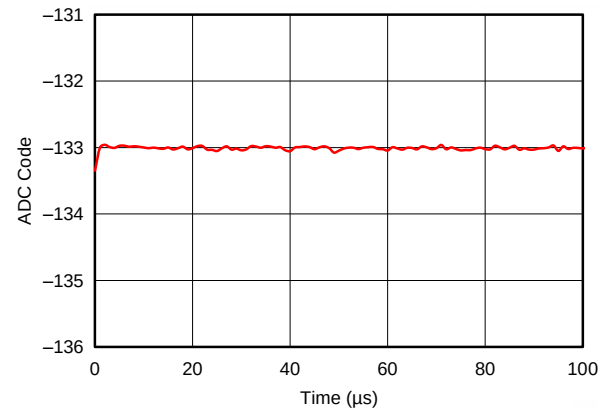


Figure 34. Reference Droop

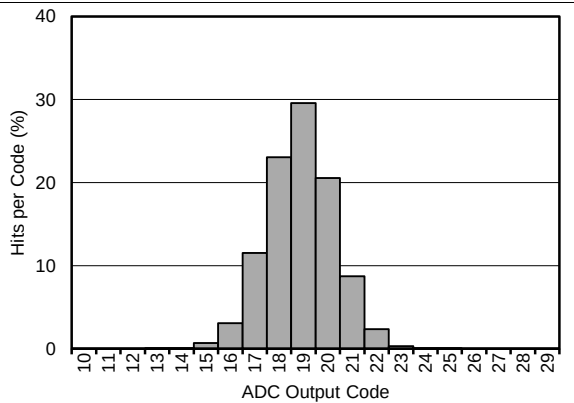


Figure 35. DC Input Histogram

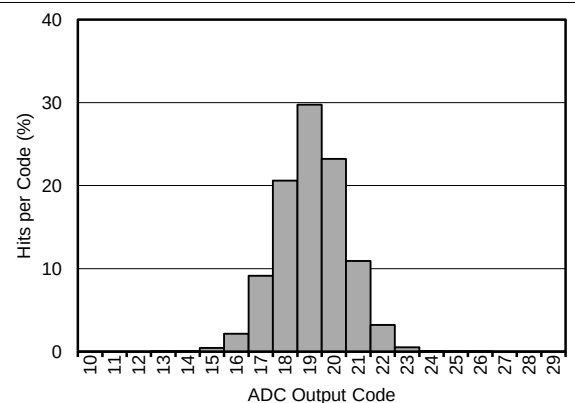
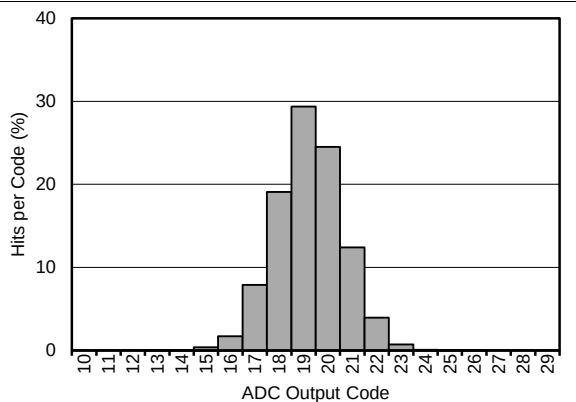


Figure 36. DC Input Histogram

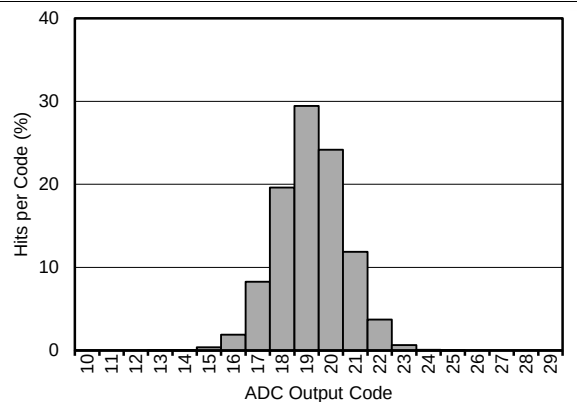
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6025 (unless otherwise noted)



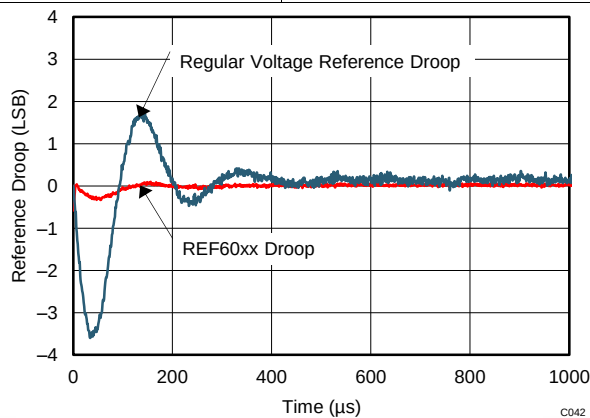
AINP = AINN = $V_{REF} / 2$ for ADS8881,
sampling rate = 100 kSPS

Figure 37. DC Input Histogram



AINP = AINN = $V_{REF} / 2$ for ADS8881,
sampling rate = 20 kSPS

Figure 38. DC Input Histogram



1 LSB = $19.07\text{ }\mu\text{V}$, with ADS8881 at 1 MSPS

Figure 39. Reference Droop Comparison

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF60xx have differing coefficients of thermal expansion, and result in stress on the device die when the part is heated. Mechanical and thermal stress on the device die sometimes causes the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 128 devices were soldered on eight printed circuit boards (PCBs), with 16 devices on each PCB, using lead-free solder paste, and the manufacturer-suggested reflow profile. The reflow profile is as shown in [Figure 40](#). The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 101.6 mm × 127 mm.

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in [Figure 41](#). Although all tested units exhibit very low shifts (< 0.03%), higher shifts are also possible depending on the size, thickness, and material of the PCB.

The histogram displays the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, solder the device in the final pass to minimize exposure to thermal stress.

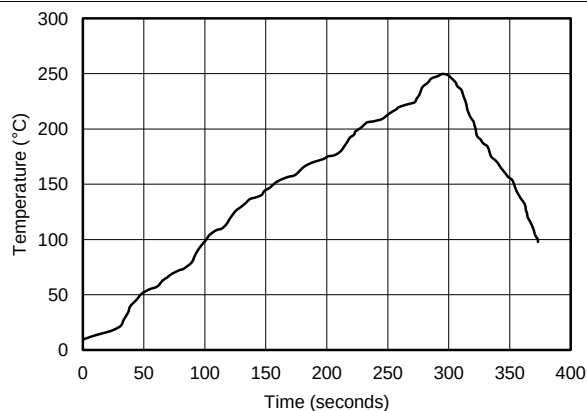


Figure 40. Reflow Profile

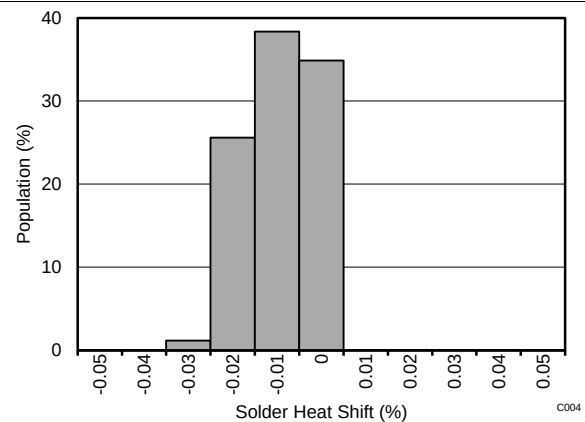


Figure 41. Solder Heat Shift Distribution

8.2 Thermal Hysteresis

Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Thermal hysteresis was measured with the REF60xx soldered to a PCB, similar to a real-world application. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Thermal hysteresis is expressed as:

$$V_{\text{HYST}} = \left(\frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \cdot 10^6 \text{ (ppm)}$$

where

- V_{HYST} = thermal hysteresis (in units of ppm).
 - V_{NOM} = the specified output voltage.
 - V_{PRE} = output voltage measured at 25°C pretemperature cycling.
 - V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C.
- (1)

Typical thermal hysteresis distribution is shown in [Figure 42](#) and [Figure 43](#).

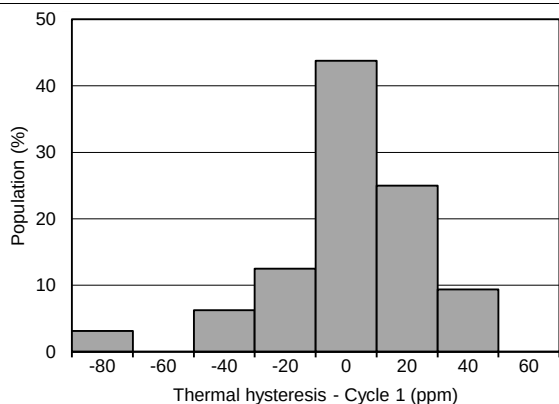


Figure 42. Thermal Hysteresis Distribution (Cycle 1)

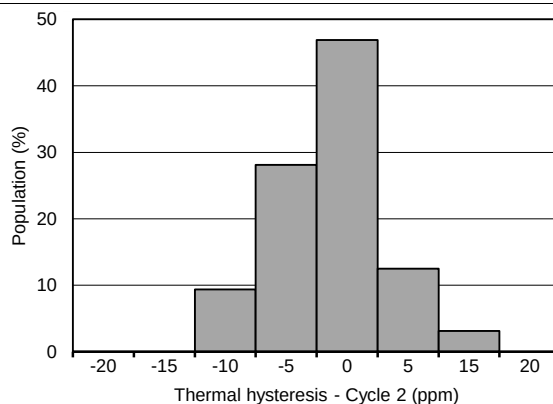


Figure 43. Thermal Hysteresis Distribution (Cycle 2)

8.3 Reference Droop Measurements

Many applications, such as event-triggered and multiplexed data-acquisition systems, require the very first conversion of the ADC to have 18-bit or greater precision. These types of data-acquisition systems capture data in bursts, and are also called burst-mode, data-acquisition systems. Achieving 18-bit precision for the first sample is a very difficult using a conventional voltage reference because the voltage reference droop limits the accuracy of the first few conversions. The REF60xx have an integrated ADC drive buffer that makes sure the reference droop is less than 1 LSB at 18-bit precision when used with the ADS8881, even at full throughput. [Figure 44](#) and [Figure 45](#) show the REF60xx output voltage droop when driving the REF pin of the ADS8881 at positive and negative full-scale inputs, respectively.

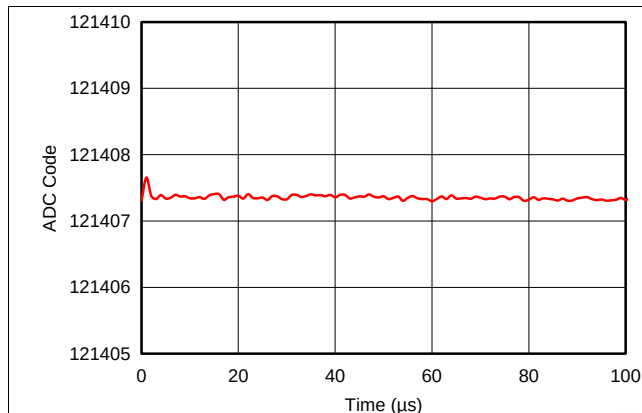


Figure 44. Output Voltage Droop

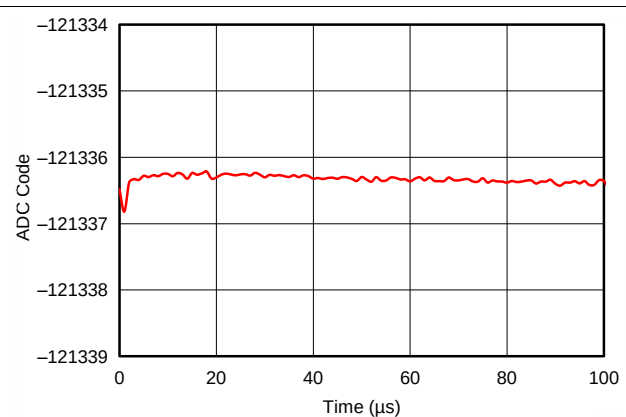


Figure 45. Output Voltage Droop

Direct measurement of the reference droop to 18-bit accuracy can be a challenging process. Therefore, the plots in [Figure 44](#) and [Figure 45](#) were obtained by processing the output code of the ADC. The ADC output code is given by:

$$C = (\text{Input Voltage} / V_{\text{REF}}) \times 2^N \quad (2)$$

If the input voltage is kept constant, V_{REF} is computed by monitoring the ADC output code C . The ADC code usually has six to seven LSBs of code spread due to the inherent noise of the ADC. In order to measure reference droop, this noise must be reduced drastically. Noise reduction is done by averaging the output code multiple times, as described in the next paragraph.

Reference Droop Measurements (continued)

Figure 46 shows the setup that was used to measure the reference droop. The output ADC code was captured using a field-programmable gate array (FPGA), and post-processing was done on a personal computer. The input to the THS4521, and hence in turn to the ADS8881, is a constant dc voltage (close to positive or negative full-scale because this condition is the worst-case for charge drawn from the REF pin). The dc source must have extremely low noise. After the REF60xx device is powered up and stable, the FPGA sends commands to the ADS8881 to capture data in bursts. The ADS8881 is initially in idle mode for 100 ms. The FPGA then sends a command to the ADS8881 to perform 100 conversions at 1 MSPS. The ADC code corresponding to these 100 conversions (one burst of data) is stored as the first row in a 1000×100 dimensional array. This operation is repeated 1000 times, and the data corresponding to each burst is stored in a new row of the 1000×100 dimensional array. Finally, each column in this array is averaged to get a final data-set of 100 elements. This final data-set now has code spread that is much less than 1 LSB because most of the noise has now been removed through averaging. This data-set was plotted on a graph with X axis = column number (each column number corresponds to $1 \mu\text{s}$ of time because the sampling rate is 1 MSPS), and Y axis = ADC output code to obtain reference-droop measurements.

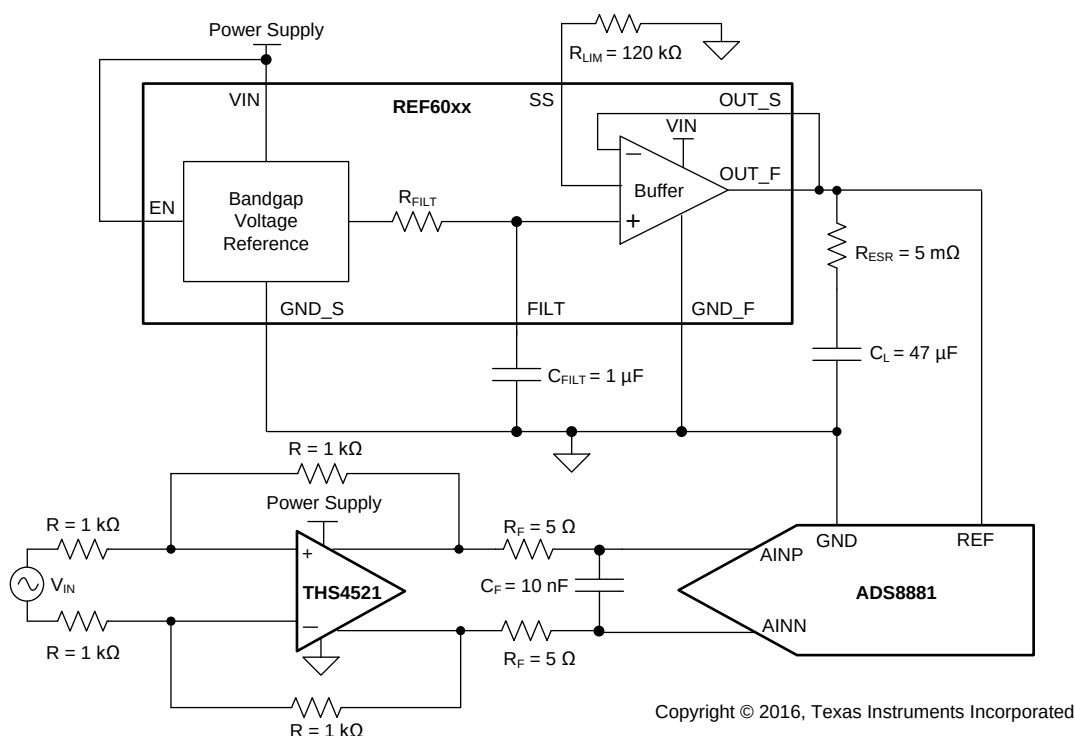
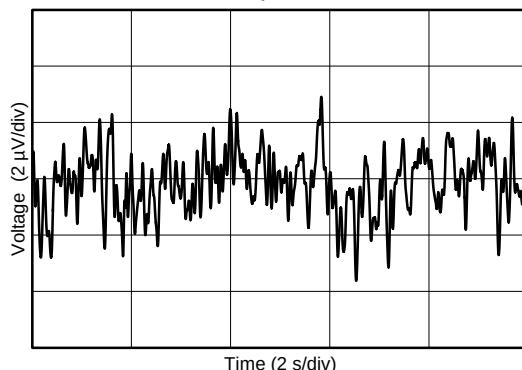


Figure 46. Burst-Mode Measurement Setup

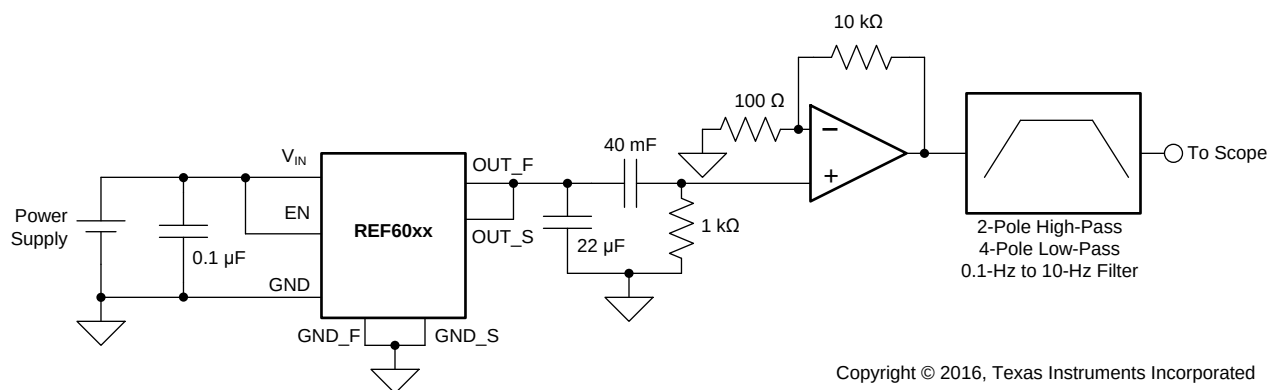
8.4 1/f Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise for the REF6025 is shown in Figure 47. The 1/f noise scales with output voltage, but remains $3\ \mu\text{V}_{\text{PP}}/\text{V}$ for all the variants. Peak-to-peak noise measurement setup is shown in Figure 48.



C021

Figure 47. 0.1-Hz to 10-Hz Noise



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Figure 48. 0.1-Hz to 10-Hz Noise Measurement Setup

9 Detailed Description

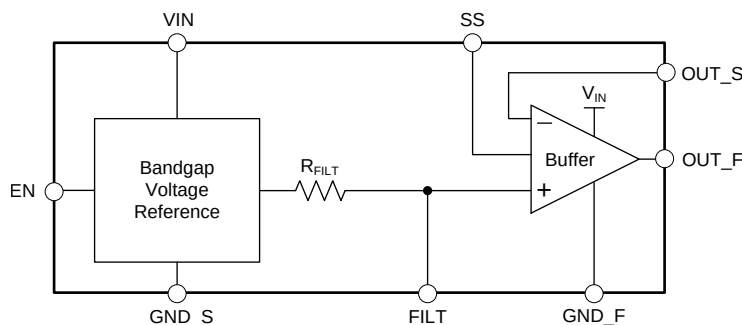
9.1 Overview

Most SAR ADCs, and a few delta-sigma ADCs, switch binary-weighted capacitors onto the REF pin during the conversion process. The magnitude of the capacitance switched onto the REF pin during each conversion depends on the input signal to the ADC. If a voltage reference is directly connected to the REF pin of these ADCs, the reference voltage droops because of the dynamic input signal dependent load of the binary-weighted capacitors. Because the reference voltage droop now has input signal dependance, significant degradation in THD and linearity for the system occurs.

In order to support this dynamic load and preserve the ADC linearity, distortion and noise performance, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF60xx family of voltage references have an integrated low output impedance buffer that enables the user to directly drive the REF pin of a SAR ADC, while preserving ADC linearity and distortion. In addition, the total noise in the full bandwidth of the REF60xx is extremely low, thus preserving the noise performance of the ADC. [Voltage-Reference Impact on Total Harmonic Distortion](#) (SLYY097) correlates the effect of reference settling to ADC distortion, and how the REF60xx achieves lowest distortion with minimal components and lowest power consumption.

The output voltage of the REF60xx does not droop below 1 LSB (18-bit), even during the first conversion while driving the REF pin of the ADS8881. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems. [Functional Block Diagram](#) shows a simplified schematic of the REF60xx.

9.2 Functional Block Diagram

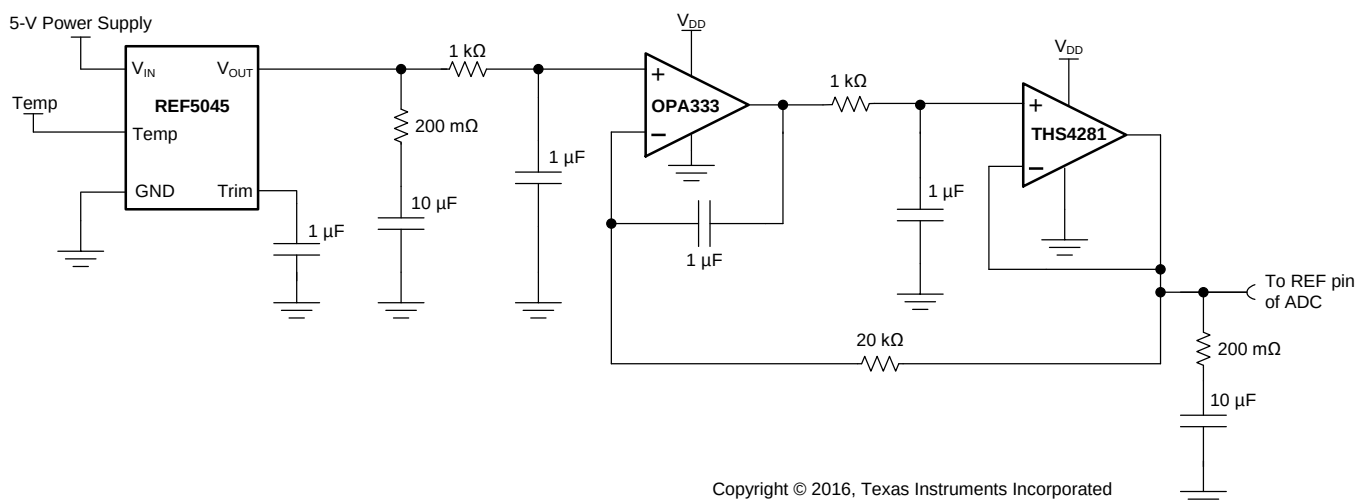


9.3 Feature Description

9.3.1 Integrated ADC Drive Buffer

Many ADC data sheets specify a few microamps of average current draw from the REF pin. Almost all voltage references provide these few microamps of average current; but not all voltage references are practical for driving a high-resolution, high-throughput SAR ADC because the peak current drawn can be very high when the capacitors are switched on the REF pin. The worst-case demand for the voltage reference is during a burst-mode conversion, when the ADC is idle for a very long time, before a conversion is initiated, and the first sample converted is expected to be precise. Usually, a large capacitor is connected between the REF pin and ground pin (or sometimes between the REFP and REFM pins) of the ADC to smoothen the current load and reduce the burden on the voltage reference. The voltage reference must then be capable of providing the average current required to completely charge the reference capacitor, but without causing the reference voltage to droop significantly. Most voltage references lack the ability to completely charge the reference capacitor, and settle when the binary-weighted capacitors are being switched onto the REF pin because of the large output impedance. Usually, voltage references have output impedances in the range of 10's of ohms at frequencies higher than 100 Hz. The output voltage of the voltage reference must be buffered with a low output impedance (usually high bandwidth) amplifier to achieve excellent linearity and distortion performance.

The key amplifier specifications to be considered when designing a reference buffer for a high-precision ADC are: low offset, low drift, wide bandwidth, and low output impedance. While it is possible to select an amplifier that sufficiently meets all these requirements, the amplifier comes at a cost of excessive power consumption. For example, the [OPA350](#) is a 38-MHz bandwidth amplifier with a maximum offset of 0.5 mV, and low offset drift of 4 $\mu\text{V}/^\circ\text{C}$, but consumes a quiescent current of 5.2mA. This is because (from an amplifier design perspective) offset and drift are dc specifications, whereas bandwidth, low output impedance, and high capacitive drive capability are high-frequency specifications. Therefore, achieving all the performance in one amplifier requires power. However, a more efficient design to meet the low power budget is to use a composite reference buffer, which uses an amplifier with superior high-frequency specifications in the feedback loop of a dc precision amplifier to get the overall performance at much lower power consumption. [Figure 49](#) shows such a composite amplifier design with the [OPA333](#) (dc precision amplifier) and [THS4281](#) (high-bandwidth amplifier). This reference buffer design requires three devices, and a large number of external components. This solution still consumes close to 2 mA of quiescent current.

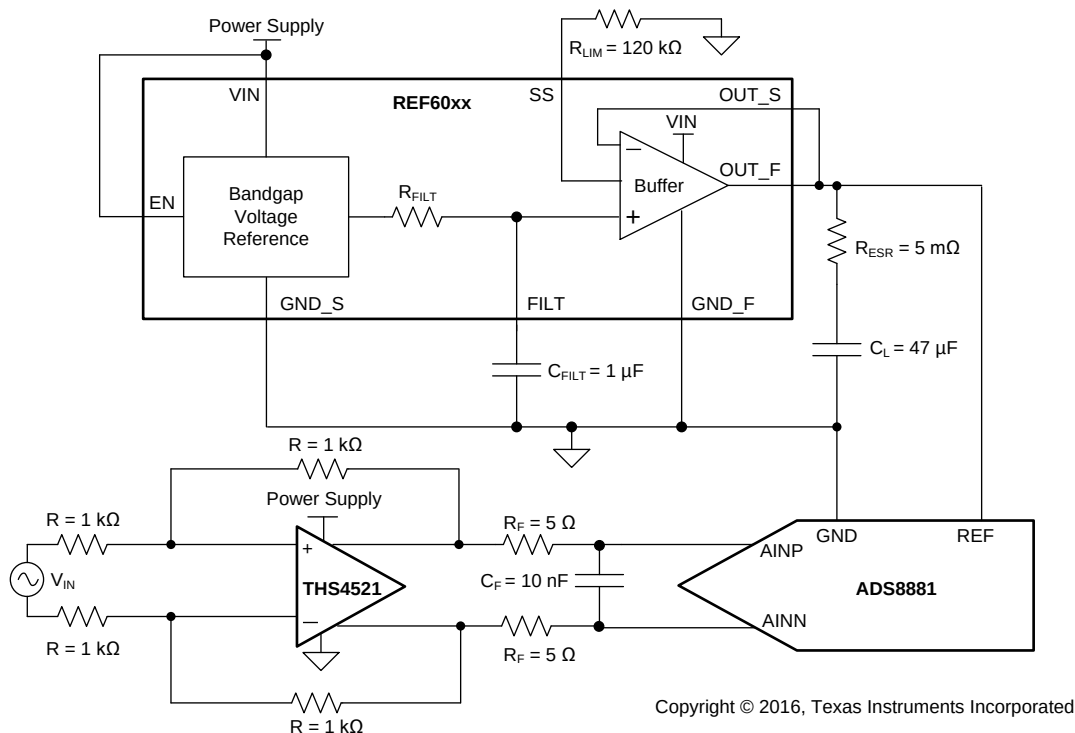


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Figure 49. Composite Amplifier Reference Buffer

Feature Description (continued)

The REF60xx family of voltage references have an integrated low output impedance buffer (ADC drive buffer); therefore, there is no need for an external buffer while driving the REF pin of high-precision, high-throughput SAR ADCs, as shown in Figure 50. The ADC drive buffer of the REF60xx is capable of replenishing a charge of 70 pC on a 47-μF capacitor in 1 μs, without allowing the voltage on the capacitor to droop more than 1 LSB at 18-bit precision. The REF60xx are trimmed at multiple temperatures in production, achieving a max drift of just 5 ppm/°C for both the voltage reference and the buffer combined, while operating at a typical quiescent current of 820 μA. Figure 51 compares the output impedance of a regular voltage reference (REF20xx) and a voltage reference with integrated ADC drive buffer (REF60xx). Figure 52 compares the burst-mode, reference-settling performance of a regular voltage reference and the REF60xx.



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Figure 50. REF60xx Driving REF Pin of ADS8881 SAR ADC

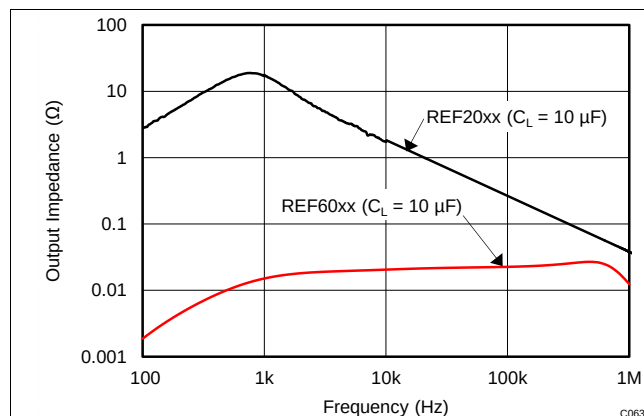
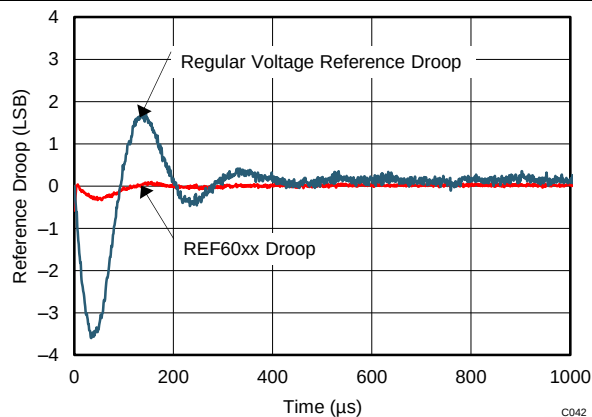


Figure 51. Output Impedance Comparison



1 LSB = 19.07 μV, with ADS8881 at 1 MSPS

Figure 52. Reference Droop Comparison

Feature Description (continued)

9.3.2 Temperature Drift

The REF60xx family is designed for minimal drift error, defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left(\frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF}} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm}) \quad (3)$$

9.3.3 Load Current

The REF6025, REF6030, REF6033 and REF6041 are specified to deliver current load of ± 4 mA. The REF6045 is specified to deliver ± 3.5 mA, and the REF6050 is specified to deliver ± 3 mA. The REF60xx are protected from short circuits at the output by limiting the output short-circuit current.

The short-circuit current limit (I_{SC}) of the REF60xx family of devices is adjusted by connecting a resistor (R_{SS}) on the SS pin. The short-circuit current limit when the REF60xx device is sourcing current can be calculated as shown in [Equation 4](#):

$$I_{\text{SC}} = (80 \cdot 10^{-9}) \cdot R_{\text{SS}} + (3 \cdot 10^{-3}) \quad (4)$$

The short circuit current limit when the REF60xx device is sinking is calculated as shown in [Equation 5](#):

$$I_{\text{SC}} = (115 \cdot 10^{-9}) \cdot R_{\text{SS}} + (4.6 \cdot 10^{-3}) \quad (5)$$

The recommended output current of the REF60xx also depends on the resistor connected to the SS pin. The recommended output current (sourcing and sinking) for the REF6025, REF6030, REF6033 and REF6041 is given by [Equation 6](#):

$$I_{\text{L}} = (31.25 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.25 \cdot 10^{-3}) \quad (6)$$

The recommended output current (sourcing and sinking) for the REF6045 is given by [Equation 7](#):

$$I_{\text{L}} = (27.08 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.25 \cdot 10^{-3}) \quad (7)$$

The recommended output current (sourcing and sinking) for the REF6050 is given by [Equation 8](#):

$$I_{\text{L}} = (23.75 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.15 \cdot 10^{-3}) \quad (8)$$

The temperature of the device increases according to [Equation 9](#):

$$T_{\text{J}} = T_{\text{A}} + P_{\text{D}} \cdot R_{\theta\text{JA}}$$

where:

- T_{J} = junction temperature ($^{\circ}\text{C}$).
 - T_{A} = ambient temperature ($^{\circ}\text{C}$).
 - P_{D} = power dissipated (W).
 - $R_{\theta\text{JA}}$ = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$).
- (9)

The REF60xx maximum junction temperature must not exceed the absolute maximum rating of 150°C .

Feature Description (continued)

9.3.4 Stability

The REF60xx family of voltage references are stable with output capacitor values ranging from 10 μF to 47 μF . At a low output-capacitor value of 10 μF , an effective series resistance (ESR) of 20 m Ω to 100 m Ω is required for stability; whereas, at a higher value of 47 μF , an ESR of 5 m Ω to 100 m Ω is required. The shaded region in [Figure 53](#) shows the stable region of operation for the REF60xx devices.

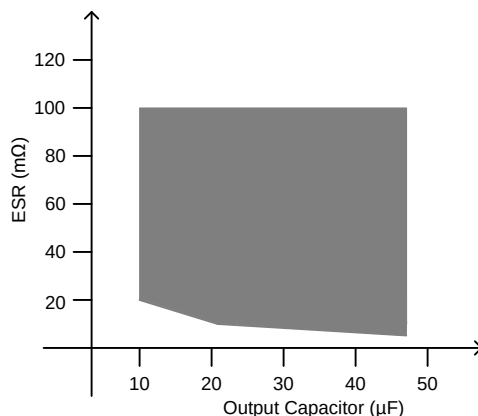


Figure 53. Stable Output Capacitor Range

A capacitor of value 1 μF is required at the FILT pin for stability and noise performance. A low ESR (5 m Ω to 20 m Ω) is easily achieved by increasing the PCB trace length, thus eliminating the need for a discrete resistor. Higher values of ESR (greater than 20 m Ω , but lesser than 100 m Ω) can be intentionally added to increase the output bandwidth of the REF60xx. This higher ESR improves the transient performance of the REF60xx, but worsens noise performance because of increased bandwidth.

9.4 Device Functional Modes

When the EN pin of the REF60xx is pulled high, the device is in active mode. The device must be in active mode for normal operation.

To place the REF60xx into a shutdown mode, pull the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 1 μA (typ). See the enable pin voltage parameter in the [Electrical Characteristics](#) table for logic high and logic low voltage levels.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Many applications, such as event-triggered and multiplexed data-acquisition systems, require the very first conversion of the ADC to have 18-bit or greater precision. These types of data acquisition systems capture data in bursts, and are also called burst-mode, data-acquisition systems. Achieving 18-bit precision for the first sample is very difficult using a conventional voltage reference because the voltage reference droop limits the accuracy of the first few conversions. Furthermore, variable-sampling-rate systems require that the gain error of the system does not vary with sampling rate. The primary objective of this design example is to demonstrate the lowest distortion and noise, burst-mode data-acquisition block with low power consumption, using an 18-bit SAR ADC operating at a throughput of 1 MSPS, for a 1-kHz, full-scale, pure sine-wave input.

10.2 Typical Application

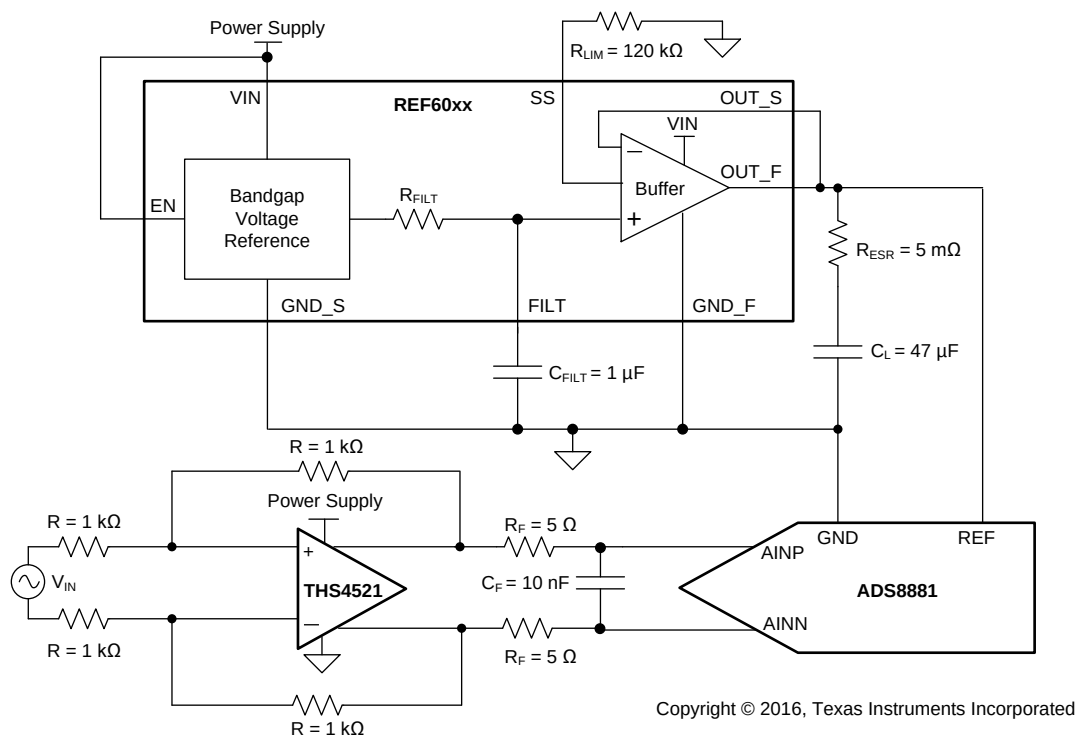


Figure 54. 18-bit, 1-MSPS, Burst-Mode Data Acquisition system

10.2.1 Design Requirements

1. Burst-mode support (see [Reference Droop Measurements](#) section for more details)
2. ENOB > 16 bits
3. THD < -120 dB
4. Power consumption < 50 mW
5. Throughput = 1 MSPS

Typical Application (continued)

10.2.2 Detailed Design Procedure

The data acquisition system shown in [Figure 54](#) has three major contributors to the noise and accuracy in the system: the input driver, the reference with driver, and the data converter. Each analog block is carefully designed so that the data converter specifications limit the system specifications. The [THS4551](#), a fully differential operational amplifier is used to drive the 18-bit ADC ([ADS8881](#)). The charge-kickback RC filter at the output of the THS4551 is used to reduce the charge kickback created by the opening and closing of the sampling switch inside the ADC. Design the RC filter so that the voltage at the sampling capacitor settles to 18-bit accuracy within the acquisition time of the ADC.

Data-acquisition systems require stable and accurate voltage references in order to perform the most accurate data conversion. The REF60xx family of voltage references have integrated an ADC drive buffer, and can therefore drive the REF pin of the ADS8881 directly, without the need for an external reference buffer. See the [Integrated ADC Drive Buffer](#) section for more details about reference-buffer requirements. Correct output capacitor selection for the REF60xx is very important in this design. The [Stability](#) section describes the ESR requirements of the output capacitor for stability and burst-mode requirements. A capacitance of 1 μ F is connected to the FILT pin to reduce broadband noise of the REF60xx.

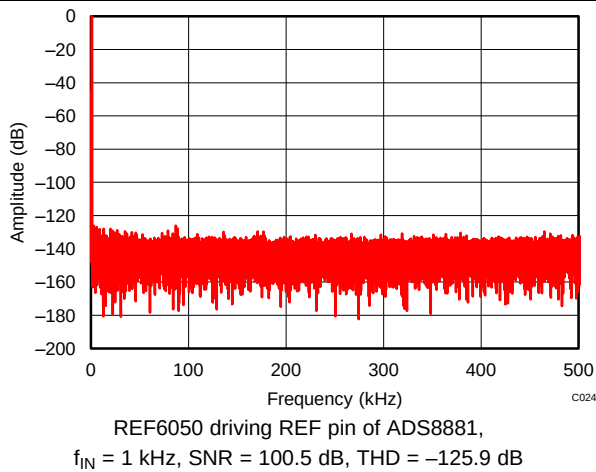
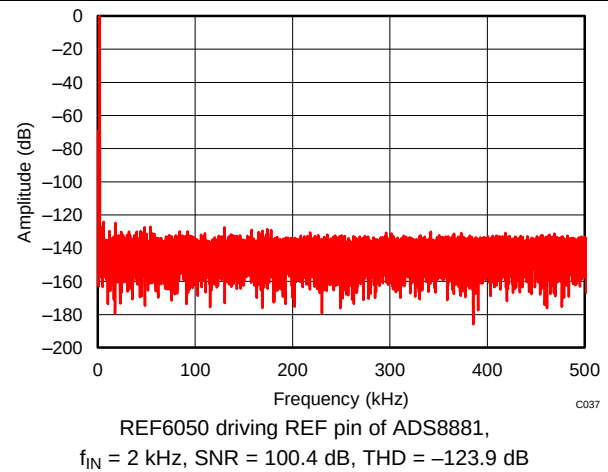
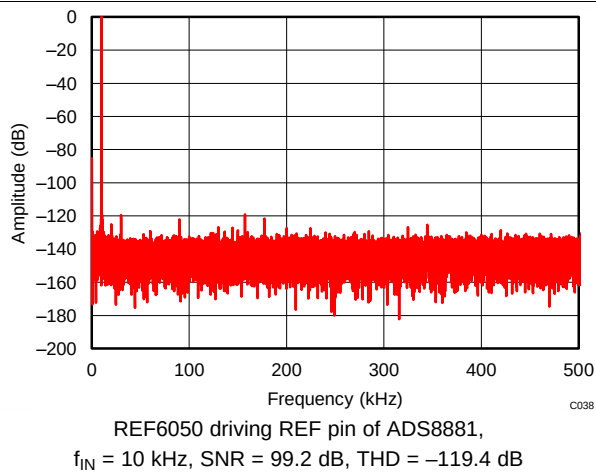
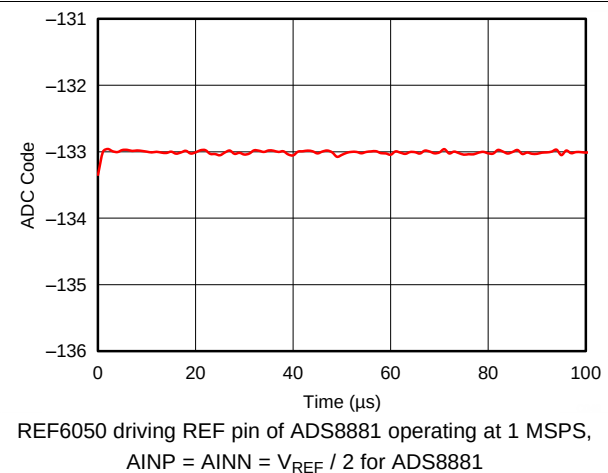
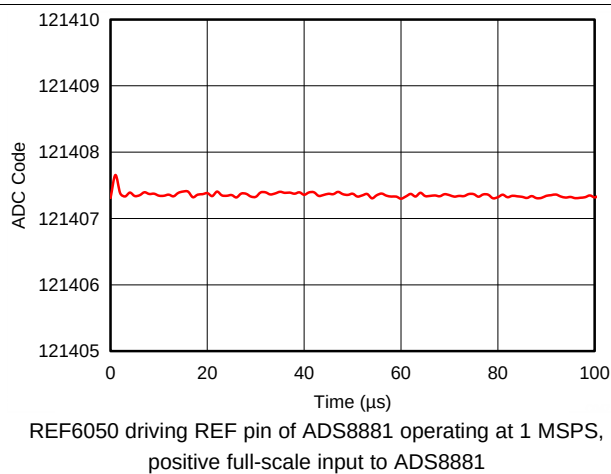
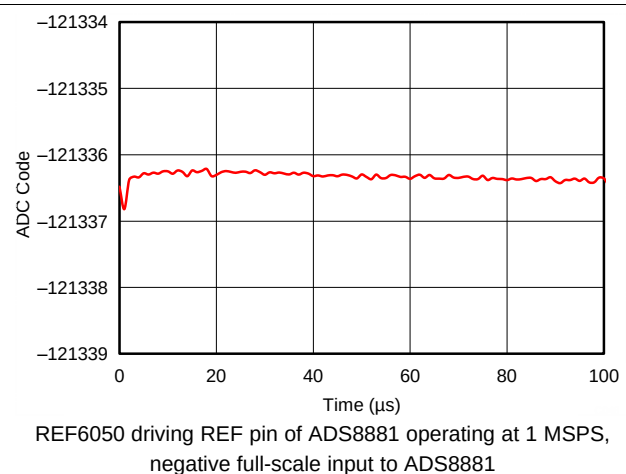
10.2.2.1 Results

[Table 1](#) summarizes the measured results.

Table 1. Measured Results

SPECIFICATION	MEASURED RESULT
SNR	100.5 dB
ENOB	16.4
THD	–125.9 dB
Throughput	1 MSPS
Burst mode	First sample > 18-bit precision
Power consumption	40 mW

10.2.3 Application Curves


Figure 55. Typical FFT Plot

Figure 56. Typical FFT Plot

Figure 57. Typical FFT Plot

Figure 58. Reference Droop

Figure 59. Reference Droop

Figure 60. Reference Droop

11 Power Supply Recommendations

The REF60xx family of references have extremely low dropout voltage. The dropout specifications can be found in the [Electrical Characteristics](#) section. A minimum 0.1 μF decoupling capacitor must be connected between the VIN and GND_F pins of the REF60xx. A typical dropout voltage versus load is shown in [Figure 61](#).

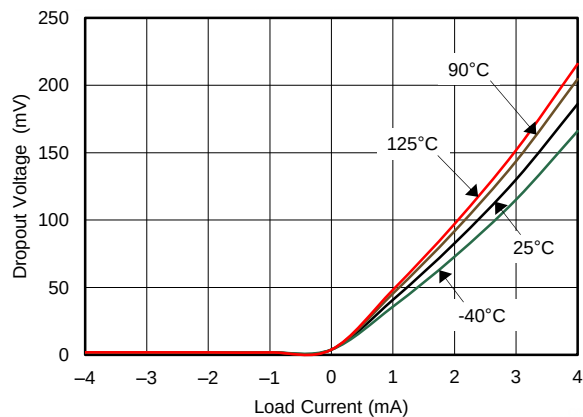


Figure 61. Dropout Voltage vs Load Current

12 Layout

12.1 Layout Guidelines

Figure 62 illustrates an example of a PCB layout for a data-acquisition system using the REF60xx. Some key considerations are:

- Connect low-ESR, 0.1- μ F ceramic bypass capacitors between the VIN pin and ground.
- Place the REF60xx output capacitor (C_L) and the ADC as close to each other as possible.
- Run two separate traces between VOUT_F, VOUT_S and the output capacitor, as shown in Figure 62.
- Short the GND_F and GND_S pins with a solid plane, and extend this plane to connect to the output capacitor C_L , as shown in Figure 62.
- Use a solid ground plane to help distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

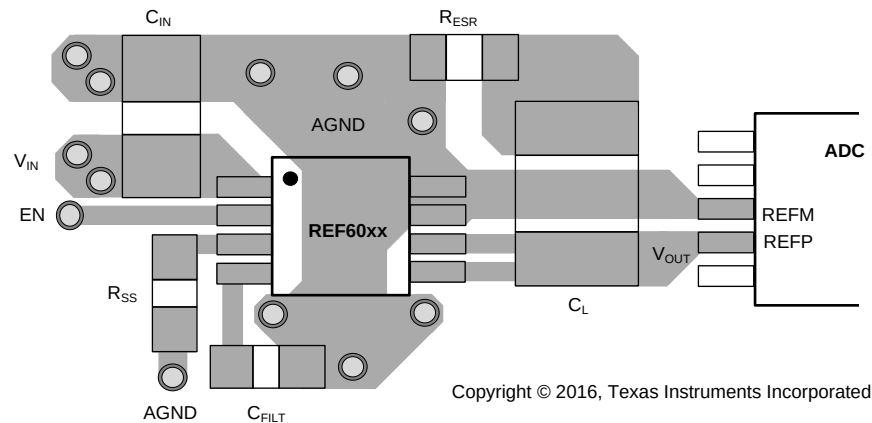


Figure 62. Layout Example

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連資料

関連資料については、以下を参照してください:

- 『[ADS8881x 18ビット、1-MSPS、シリアル・インターフェイス、マイクロパワー、小型、精密差動入力、SAR ADCデータシート](#)』(SBAS547)
- 『[ADS127L01 24ビット、高速、広帯域幅ADCデータシート](#)』(SBAS607)
- 『[REF6025EVM-PDK ユーザーズ・ガイド](#)』(SBAU258)
- 『[全高調波歪みに対する電圧リファレンスの影響](#)』(SLYY097)

13.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
REF6025	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
REF6030	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
REF6033	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
REF6041	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
REF6045	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
REF6050	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF6025IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6025IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6025IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6025IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6025IDGKTG4	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6025IDGKTG4.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6030IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV
REF6030IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV
REF6030IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV
REF6030IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV
REF6033IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV
REF6033IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV
REF6033IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV
REF6033IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV
REF6041IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6041IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6041IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6041IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6041IDGKTG4	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6041IDGKTG4.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6045IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG
REF6045IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG
REF6045IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG
REF6045IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG
REF6050IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV
REF6050IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV
REF6050IDGKRG4	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV
REF6050IDGKRG4.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV
REF6050IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF6050IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

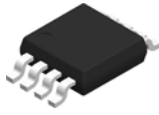
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF6025IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6025IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6025IDGKTG4	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6030IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6030IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6033IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6033IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKTG4	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6045IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6045IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

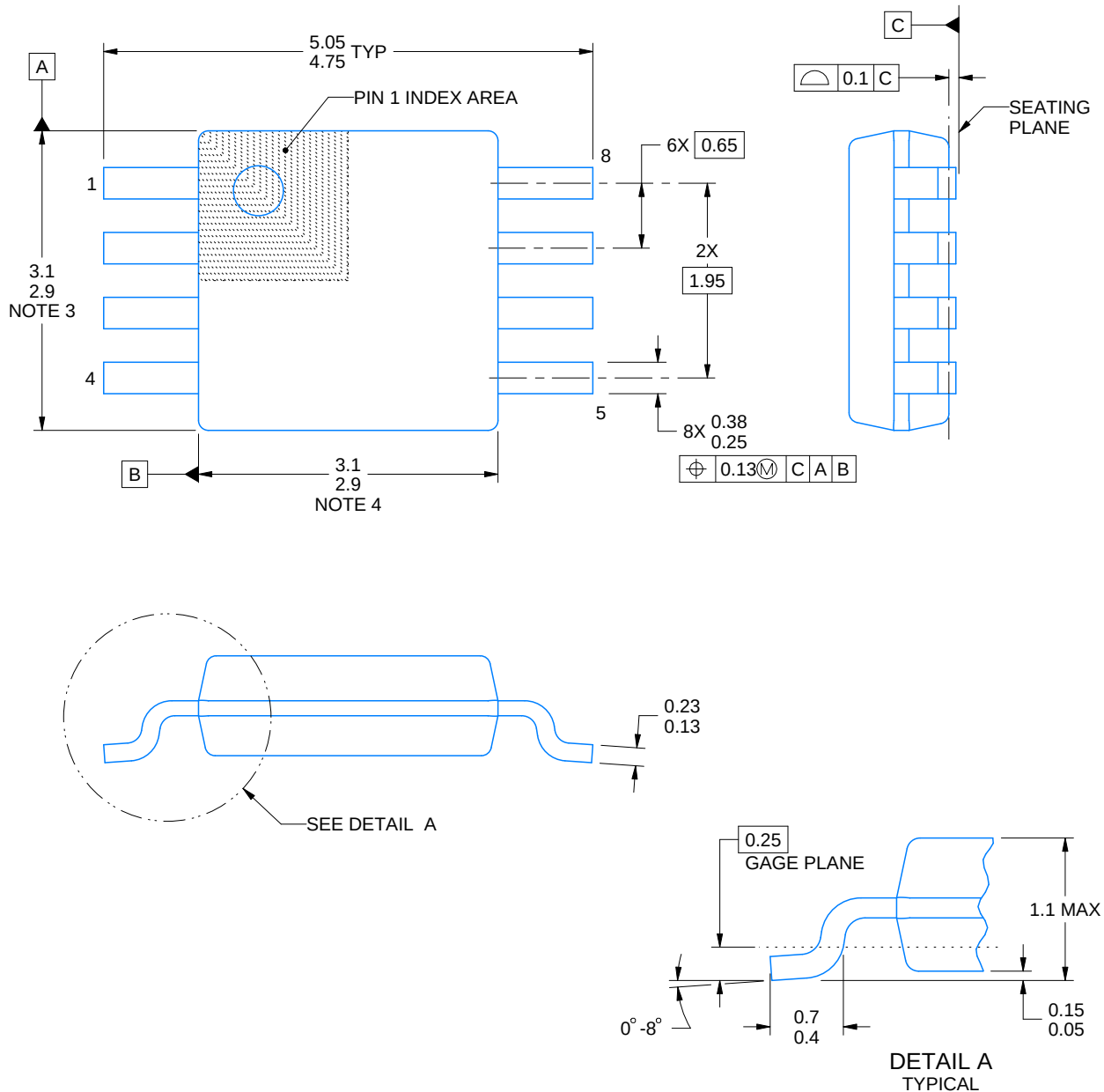


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF6025IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6025IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6025IDGKTG4	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6030IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6030IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6033IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6033IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6041IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6041IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6041IDGKTG4	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6045IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6045IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6050IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6050IDGKRG4	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6050IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

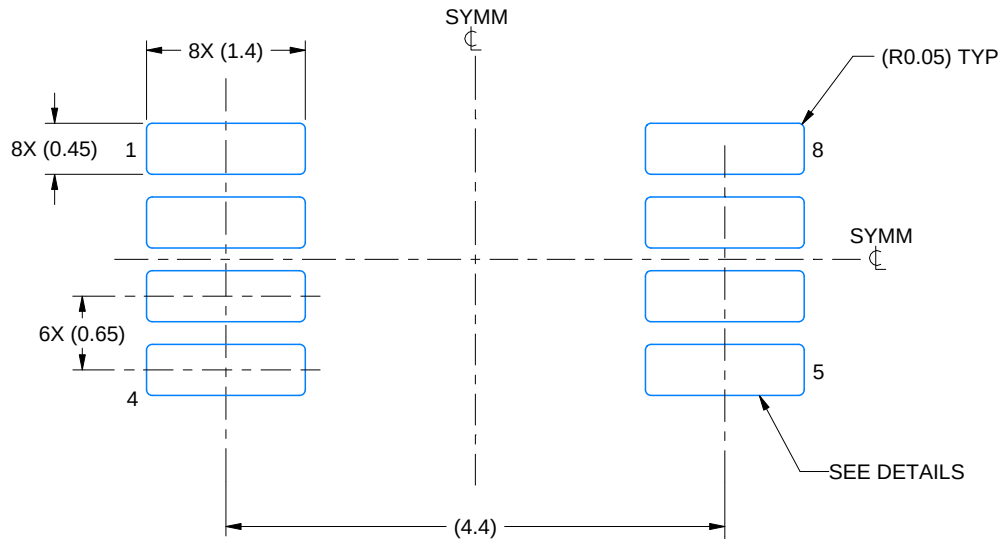
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

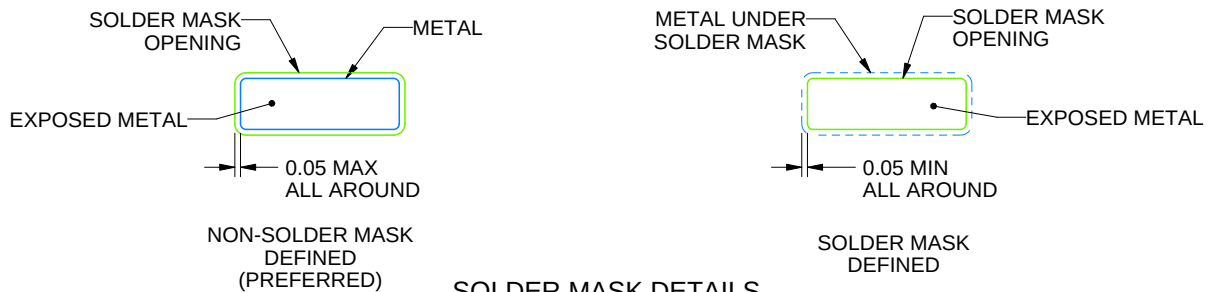
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

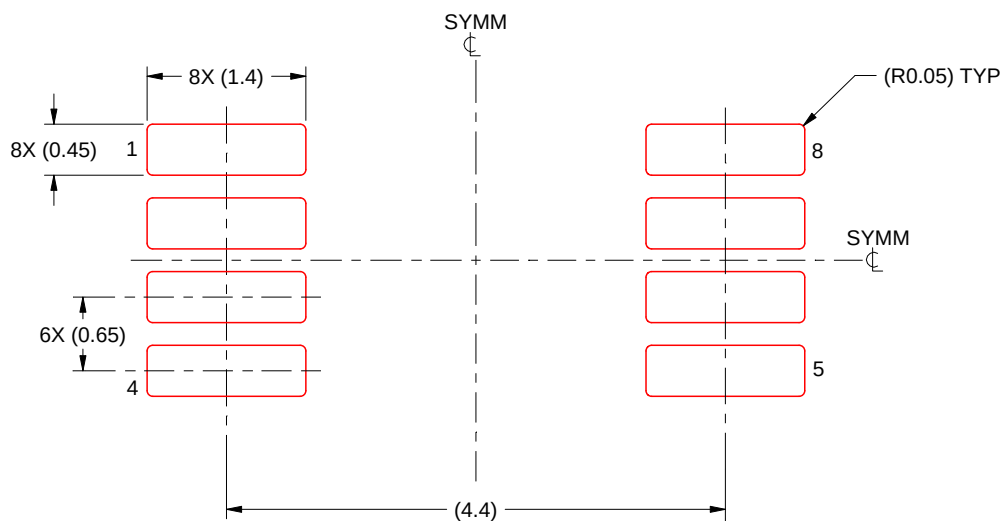
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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