REF34xx 低ドリフト、低消費電力、小フットプリントのシリーズ電圧リファレンス

1 特長

- 初期精度:±0.05% 以下
- 温度係数:6ppm/℃以下
- 動作温度範囲:−40℃~+125℃
- 出力電流:±10mA
- 低い静止電流:95µA 以下
- 極低ゼロ負荷ドロップアウト電圧:100mV (最大値)
- 広い入力電圧範囲:12V
- 出力 1/f ノイズ (0.1Hz~10Hz):3.8µV_{p-p}/V
- 優れた長期安定性:25ppm/1000 時間
- 複数の小フットプリント 6 ピン SOT-23 パッケージ・ピン配置:REF34xx、REF34xxT

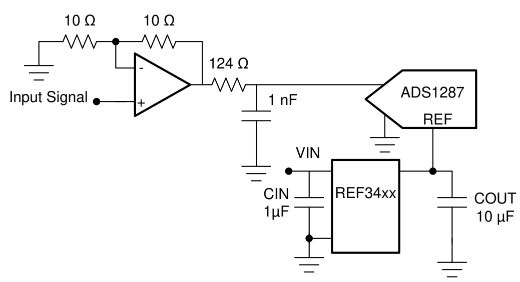
2 アプリケーション

- データ・アクイジション・システム
- アナログ I/O モジュール
- フィールド・トランスミッタ
- 計測機器:ラボ、分析、フィールド、ポータブル
- サーボ・ドライブ制御モジュール
- DC 電源、AC 電源、電子負荷

データ・コンバータ向け基準電圧設計のヒント

基準電圧	ADC の分解能 (1)	DAC の分解能 (1)
TL431LI、TLV431	10 b	8 b
LM4040、LM4050、REF30 を使用しています	12 b	10 b
REF31、REF33、REF4132	14 b to 16 b	12 b
REF34、REF50	16 b to 18 b	14 b to 16 b
REF70	18 b+	16 b+

(1) 特定の ADC/DAC 推奨事項 については、SNAA320 を参照してください



概略回路図

3 概要

REF34xx デバイスは、低温度ドリフト (6ppm/℃)、低消費電力、高精度の CMOS 電圧リファレンスで、消費電力を 95µA 未満に抑えて、±0.05% の初期精度と低動作電流を実現します。このデバイスは出力ノイズも 3.8µV_{p-p}/V と非常に低いため、ノイズの影響を受けやすいシステムにおいて、高分解能のデータ・コンバータで高いシグナル・インテグリティを維持できます。小型の SOT-23 パッケージで供給される REF34xx は仕様が拡張され、MAX607x、ADR34xx、 および LT1790 (REF34xxT、EN ピンなし) のピン互換製品です。REF34xx は、ADS1287、DAC8802、ADS1112 など、ほとんどの ADC および DAC と互換性があります。

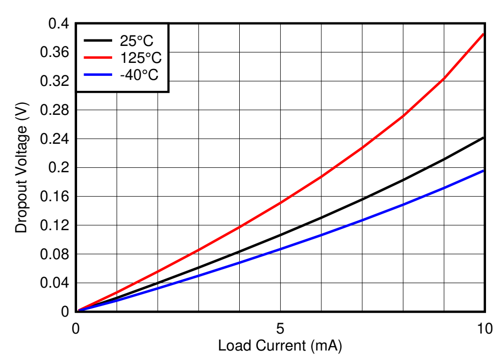
デバイスの低い出力電圧ヒステリシスと低い長期出力電圧ドリフトにより、安定性とシステム信頼性がさらに改善されています。さらに、デバイスの小さなサイズと、低い動作電流 (95µA) は、携帯型およびバッテリ駆動のアプリケーションに有用です。

REF34xx は、−40℃~+125℃の広い温度範囲で動作が規定されています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
REF34xx REF34xxT	SOT-23 (6)	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



各温度でのドロップアウトと電流負荷との関係

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (April 2021) to Revision F (June 2021)	Page
• 「特長」セクションに低ドロップアウトの項目を追加	1
• 「製品情報」表の部品番号を整理統合	1
• Changed Thermal Information parameters to correctly reflect DBV package	6
• Added second cycle thermal hysteresis plot	14
• Linked product numbers in table to datasheets	19

Changes from Revision D (February 2021) to Revision E (April 2021)	Page
• Removed the "Product Preview" note for the REF34xxT package options	4

Changes from Revision C (January 2021) to Revision D (February 2021)	Page
• 「概要」と図を更新	1
• ENABLE を EN に変更	1
• Updated values	13

Changes from Revision B (March 2018) to Revision C (February 2021)	Page
• REF34xxT を含むように「製品情報」を追加	1
• 「アプリケーション」にハイパーリンクを追加	1
• ドキュメント全体を通して「V_{REF}」を「V_{OUT}」に変更	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Added REF34xxT to "Device Comparison Table"	4
• Added REF34xxT to "Pin Configuration and Functions"	5

- Fixed pinout numbering.. 5
- Added Configuration Information to "Electrical Characteristics”.. 6
- Changed ABS MAX IN MIN to "-0.3V".. 6
- Added REF34xxT to "Layout Guidelines" and "Layout Example"..22

Changes from Revision A (December 2017) to Revision B (March 2018) **Page**

- 2 つの新しい GPNS である REF3440 と REF3450 を追加.. 1
- *セクション 1* の「優れた長期安定性：30ppm/1000 時間」を「優れた長期安定性：25ppm/1000 時間」に変更............ 1
- Changed "...typical drift value for the REF34xx is 30 ppm from 0 to 1000 hours" to "...typical drift value for the REF34xx is 25 ppm from 0 to 1000 hours" and changed 図 8-3 in *セクション 8.2* 14
- Changed "(as shown in Figure 26)" to " as shown in 図 9-1 in last paragraph of *セクション 10.2.2.2* 20

Changes from Revision * (September 2017) to Revision A (December 2017) **Page**

- 2 つの新しい出力電圧オプション・デバイスである REF3430 と REF3433 の量産リリースを追加............................ 1

5 Device Comparison Table

PRODUCT		V_{OUT}
REF3425	REF3425T	2.5 V
REF3430	REF3430T	3 V
REF3433	REF3433T	3.3 V
REF3440	REF3440T	4.096 V
REF3450	REF3450T	5 V

6 Pin Configuration and Functions

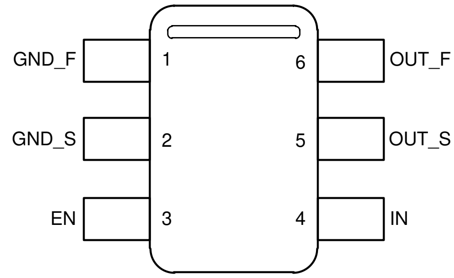


図 6-1. REF34xx DBV Package 6-Pin SOT-23 Top View

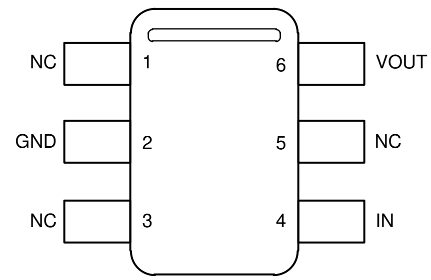


図 6-2. REF34xxT DBV Package 6-Pin SOT-23 Top View

表 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	REF34xx (DBV)	REF34xxT (DBV)		
GND_F	1		Ground	Ground force connection.
GND_S	2		Ground	Ground sense connection.
GND		2	Ground	Device ground.
EN	3		Input	Enable connection. Enables or disables the device.
IN	4	4	Power	Input supply voltage connection.
OUT_S	5		Input	Reference voltage output sense connection.
OUT_F	6		Output	Reference voltage output force connection.
VOUT		6	Output	Reference voltage output connection.
NC		1,3,5	-	Not connected. Pin can be left floating or connected to voltage within device operating range.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	IN	–0.3	13	V
	EN	–0.3	IN + 0.3	V
Output voltage	V_{OUT}	–0.3	5.5	V
Output short circuit current	I_{SC}		20	mA
Operating temperature range	T_A	–55	150	°C
Storage temperature range	T_{stg}	–65	170	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Input Voltage	V_{OUT} + V_{DO} [1]		12	V
EN	Enable Voltage	0		IN	V
I_L	Output Current	–10		10	mA
T_A	Operating Temperature	–40	25	125	°C

(1) V_{DO} = Dropout voltage

7.4 Thermal Information

THERMAL METRIC(1)		REF34T	REF34	UNIT
		DBV	DBV	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.6	122.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.2	80.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42	42	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	23.2	23.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.9	41.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

7.5 Electrical Characteristics

At $V_{IN} = V_{OUT} + V_{DO}$, C_{OUT} = 10 µF, C_{IN} = 0.1 µF, I_L = 0 mA, minimum and maximum specifications at T_A = –40℃ to 125℃; Typical specifications at T_A = 25℃ unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25℃		–0.05		0.05	%
	Output voltage temperature coefficient (1)	–40°C ≤ T_A ≤ 125°C			2.5	6	ppm/°C
LINE & LOAD REGULATION							
$\Delta V_O/\Delta V_{IN}$	Line Regulation	$V_{IN} = V_{OUT} + V_{DO}$ (2) to 12 V			2	15	ppm/V
$\Delta V_O/\Delta I_L$	Load Regulation	I_L = 0 mA to 10mA, $V_{IN} = V_{OUT} + V_{DO}$ (3)	Sourcing		20	30	ppm/mA
		I_L = 0 mA to –10mA, $V_{IN} = V_{OUT} + V_{DO}$, T_A = 25°C (3)	Sinking, REF3425		40	70	
			Sinking, REF3430		43	75	
			Sinking, REF3433		48	84	
			Sinking, REF3440		60	98	
			Sinking, REF3450		70	140	
I_{SC}	Short circuit current	V_{OUT} = 0 V at T_A = 25°C			18	22	mA
NOISE							
e_{np-p}	Low frequency noise (4)	0.1Hz ≤ f ≤ 10Hz			5		$\mu V_{p-p}/V$
		0.1Hz ≤ f ≤ 10Hz (REF3440 and REF3450)			3.8		
e_n	Integrated wide band noise	10Hz ≤ f ≤ 10kHz			24		μV_{rms}
e_n	Output voltage noise density	f = 1kHz			0.25		ppm/√Hz
		f = 1kHz (REF3440 and REF3450)			0.2		
LONG TERM STABILITY AND HYSTERESIS							
	Long-term stability (5)	DBV Package	0 to 1000h at 35°C		25		ppm
			1000h to 2000h at 35°C		10		
	Output voltage thermal hysteresis (6)	DBV Package	25°C, –40°C,125°C, 25°C Cycle 1		30		ppm
			25°C, –40°C,125°C, 25°C Cycle 2		10		
TURN-ON TIME							
t_{ON}	Turn-on time	0.1% of output voltage settling, C_L = 10 µF			2.5		ms
CAPACITIVE LOAD							
C_L	Stable output capacitor range	–40°C ≤ T_A ≤ 125°C		0.1		10	µF
OUTPUT VOLTAGE							
V_{OUT}	Output voltage	REF3425, REF3425T			2.5		V
		REF3430, REF3430T			3.0		
		REF3433, REF3433T			3.3		
		REF3440, REF3440T			4.096		
		REF3450, REF3450T			5.0		
POWER SUPPLY							
V_{IN}	Input voltage			$V_{OUT} + V_{DO}$		12	V
I_L	Output current capacity	$V_{IN} = V_{OUT} + V_{DO}$ to 12 V		–10		10	mA

7.5 Electrical Characteristics (continued)

At $V_{IN} = V_{OUT} + V_{DO}$, C_{OUT} = 10 µF, C_{IN} = 0.1 µF, I_L = 0 mA, minimum and maximum specifications at T_A = –40℃ to 125℃; Typical specifications at T_A = 25℃ unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	Active mode		72	95	µA
		Shutdown mode		2.5	3	
V_{EN}	ENABLE pin voltage	Voltage reference in active mode (EN = 1)	1.6			V
		Voltage reference in shutdown mode (EN = 0)			0.5	
V_{DO}	Dropout voltage	I_L = 0 mA		50	100	mV
		I_L = 10 mA			500	
I_{EN}	ENABLE pin leakage current	$V_{EN} = V_{IN}$ = 12V		1	2	µA

(1) Temperature drift is specified according to the box method. See Low Temperature Drift section for more details.
(2) V_{DO} for line regulation test is 50 mV.
(3) V_{DO} for load regulation test is 500 mV.
(4) The peak-to-peak noise measurement is explained in more detail in section Noise Performance.
(5) Long-term stability measurement procedure is explained in more detail in section Long–Term Stability.
(6) Thermal hysteresis measurement procedure is explained in more detail in section Thermal Hysteresis.

7.6 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

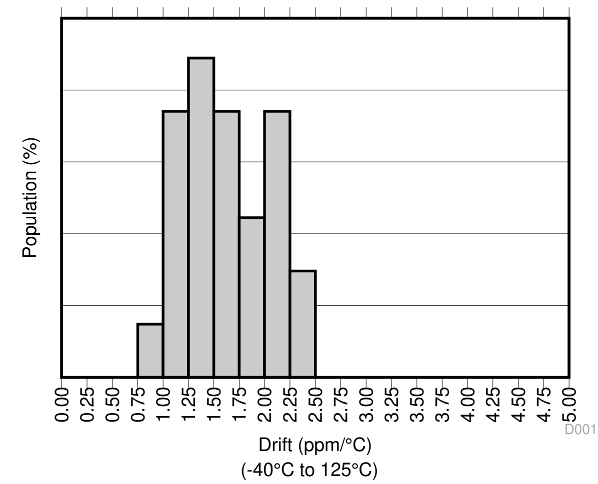


図 7-1. Temperature Drift

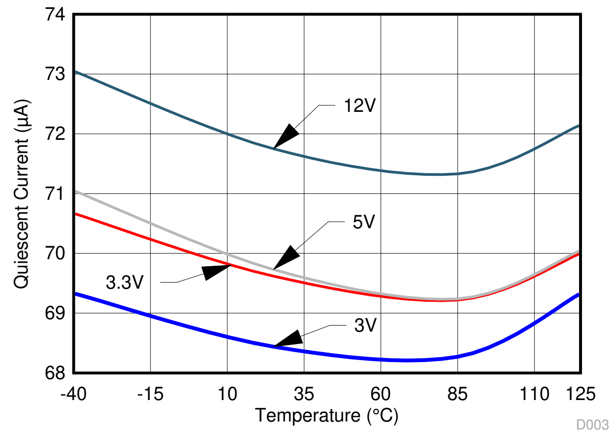


図 7-2. V_{IN} vs I_Q over Temperature

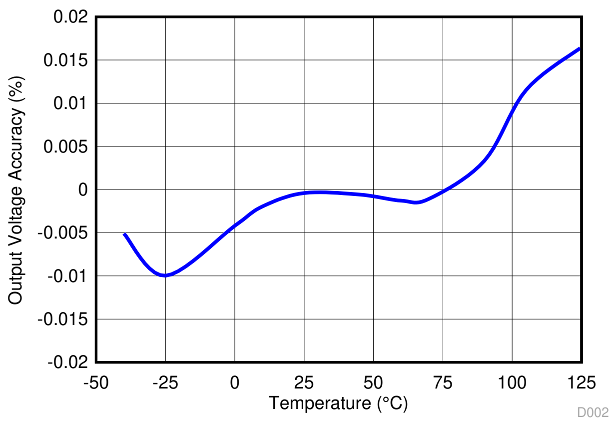


図 7-3. Output Voltage Accuracy vs Temperature

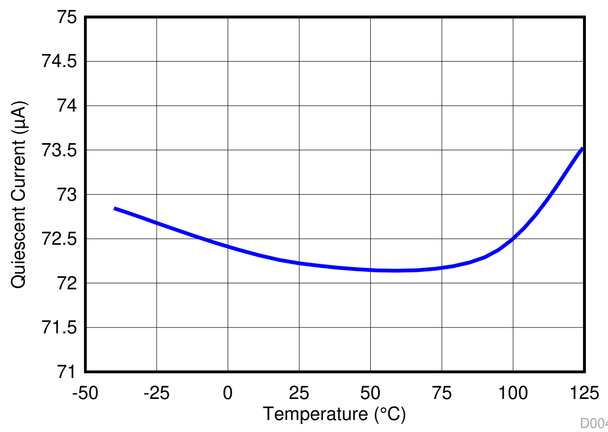


図 7-4. Quiescent Current vs Temperature

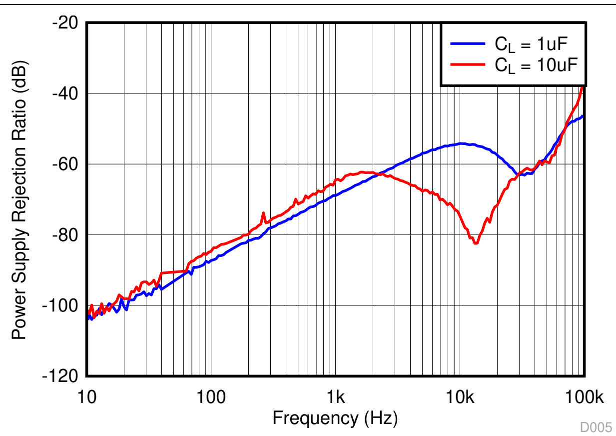


図 7-5. Power-Supply Rejection Ratio vs Frequency

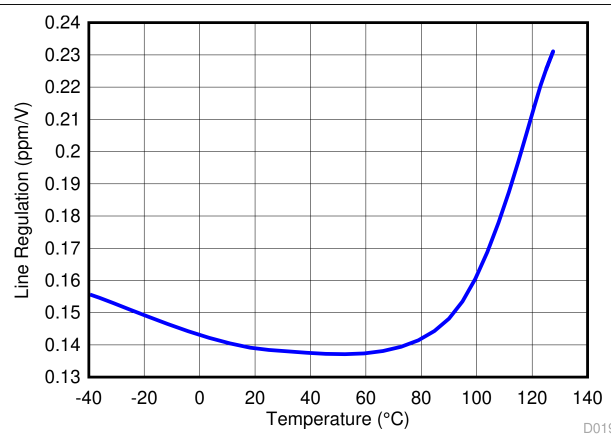


図 7-6. Line Regulation

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

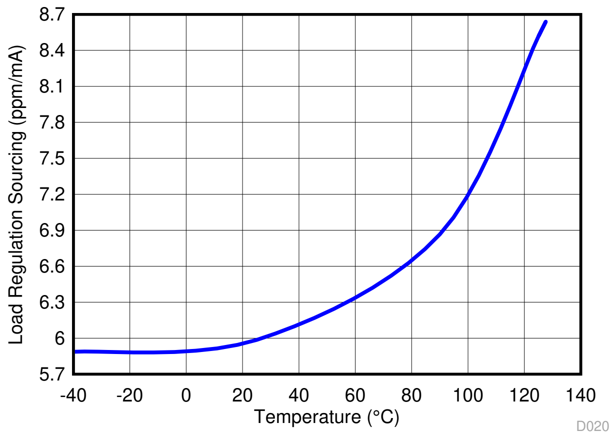


図 7-7. Load Regulation Sourcing

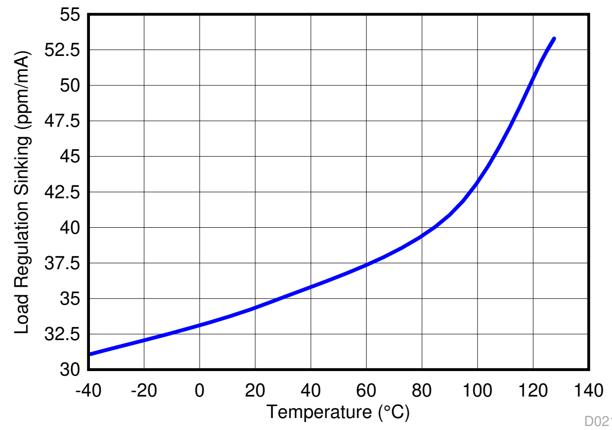


図 7-8. Load Regulation Sinking

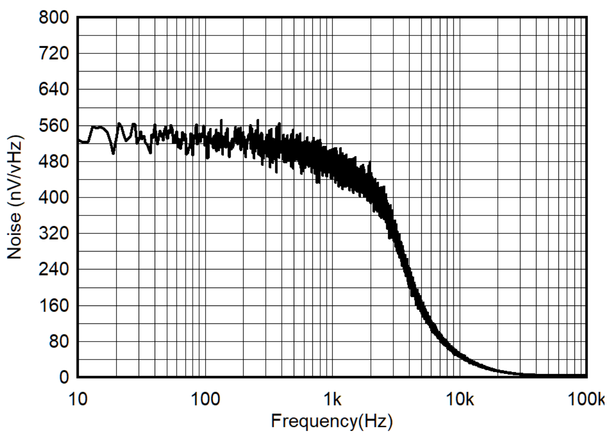


図 7-9. Noise Performance 10 Hz to 10 kHz

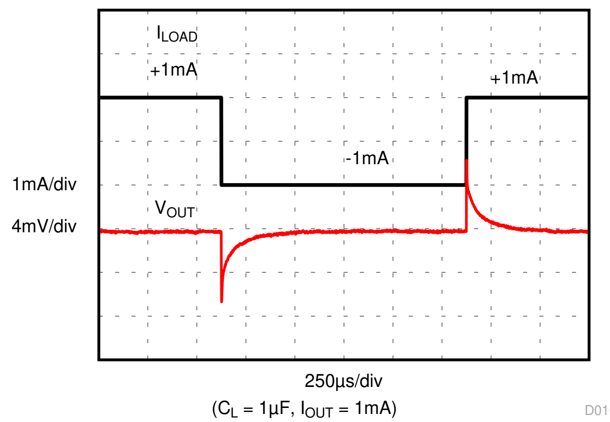


図 7-10. Load Transient

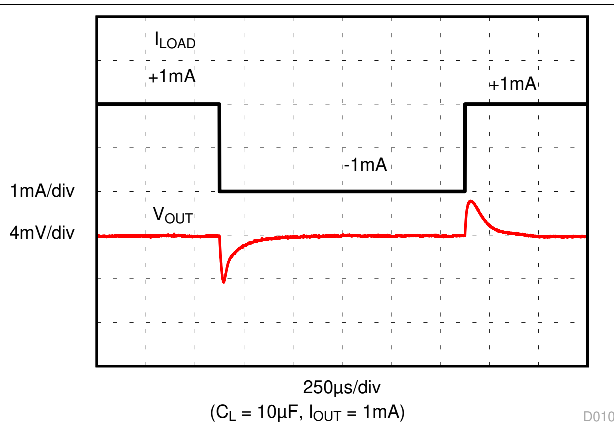


図 7-11. Load Transient

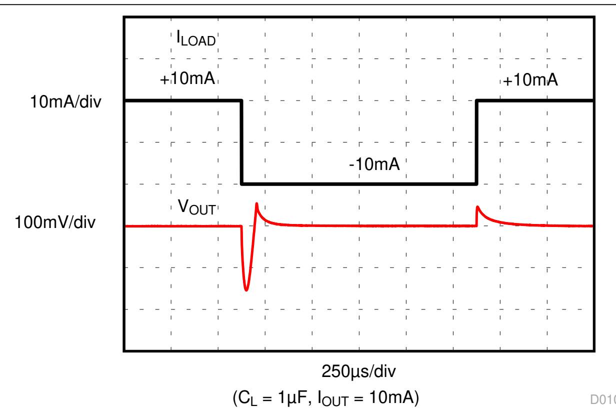


図 7-12. Load Transient

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

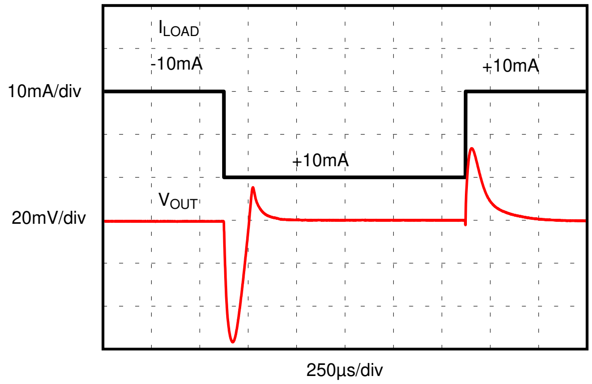


図 7-13. Load Transient

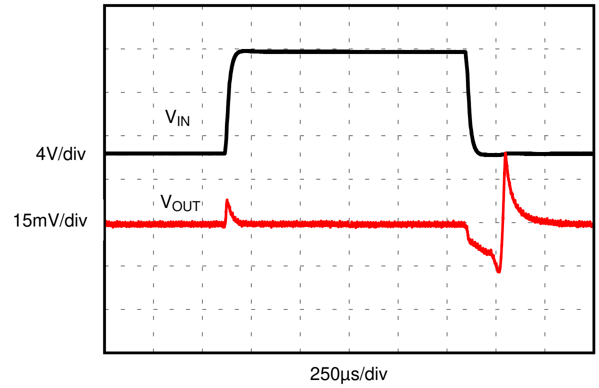


図 7-14. Line Transient

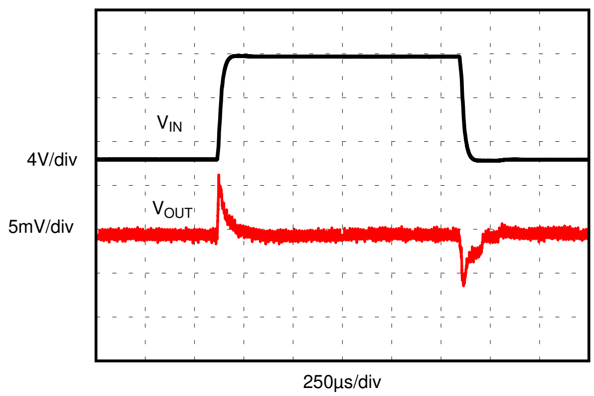


図 7-15. Line Transient

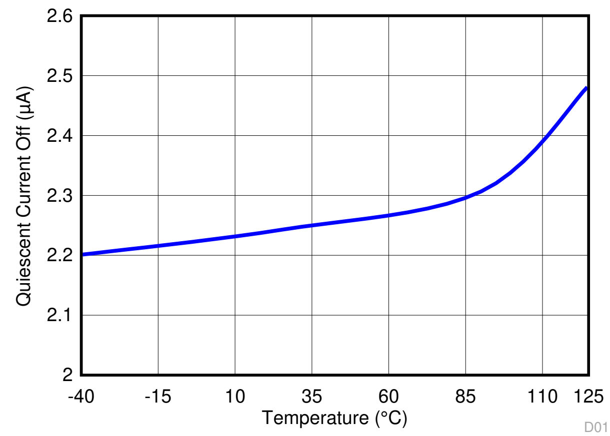


図 7-16. Quiescent Current Shutdown Mode

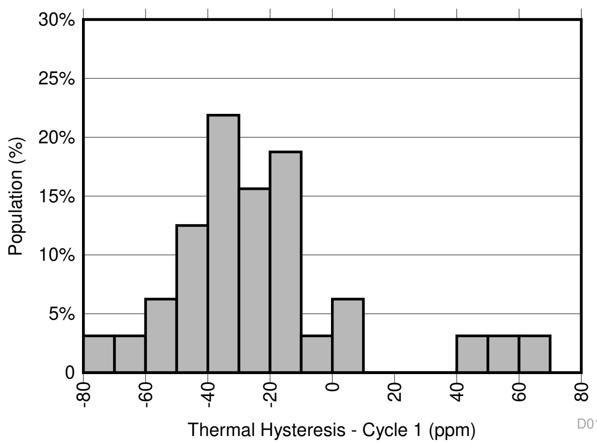


図 7-17. Thermal Hysteresis Distribution (Cycle 1)

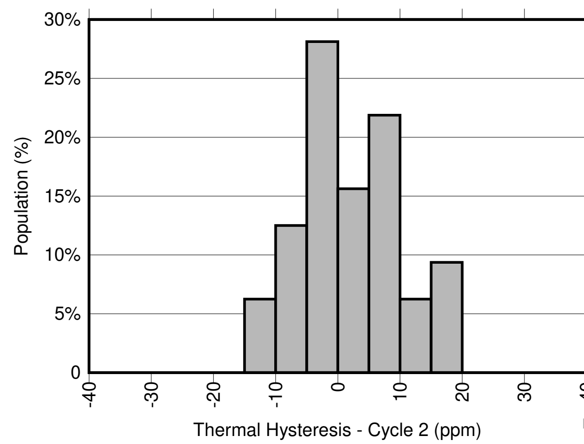
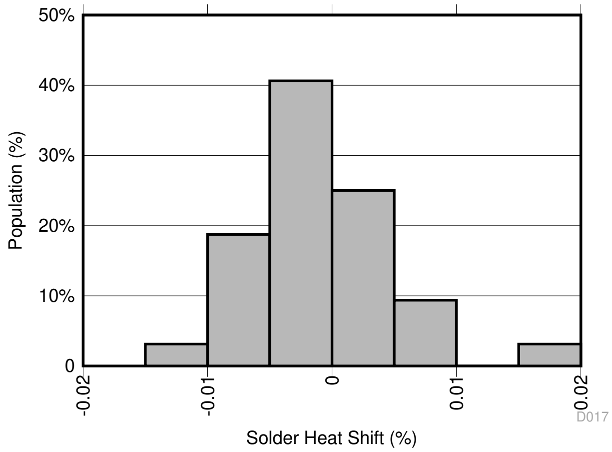


図 7-18. Thermal Hysteresis Distribution (Cycle 2)

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)



Refer to *セクション 8.1* for more information

図 7-19. Solder Heat Shift Distribution

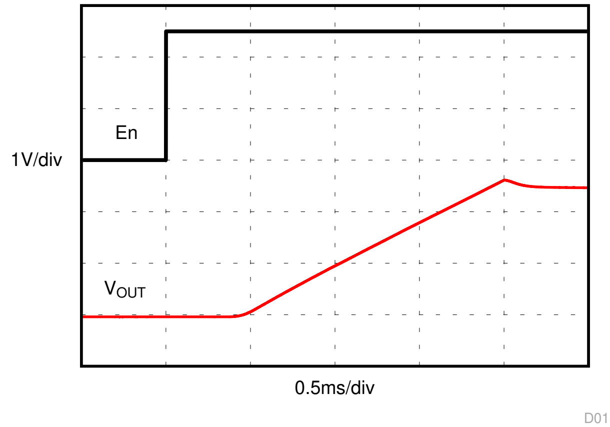


図 7-20. Turnon Time (Enable)

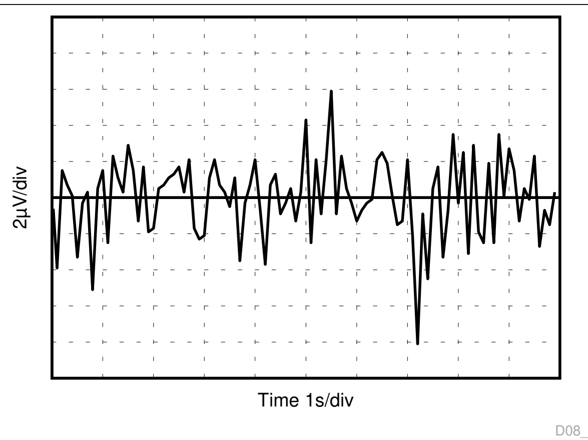


図 7-21. 0.1-Hz to 10-Hz Noise (V_{OUT})

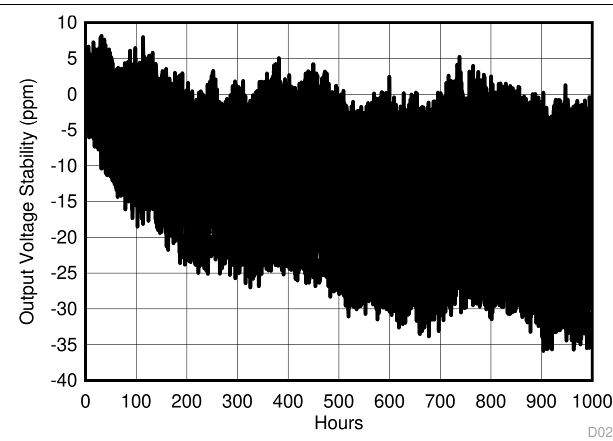


図 7-22. Long Term Stability - 1000 hours (V_{OUT})

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF34xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 32 devices were soldered on 2 printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in 図 8-1. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 114 mm × 152 mm.

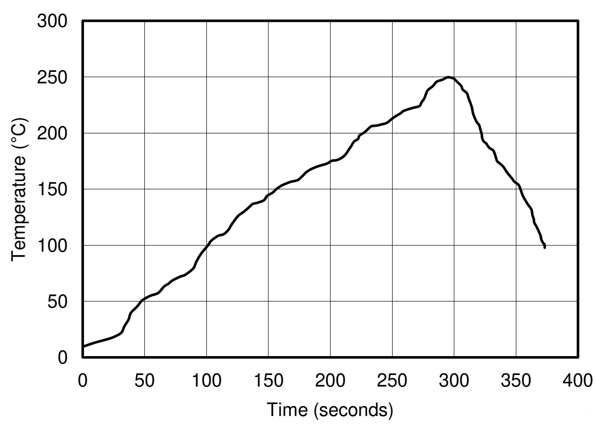


図 8-1. Reflow Profile

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in 図 8-2. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize its exposure to thermal stress.

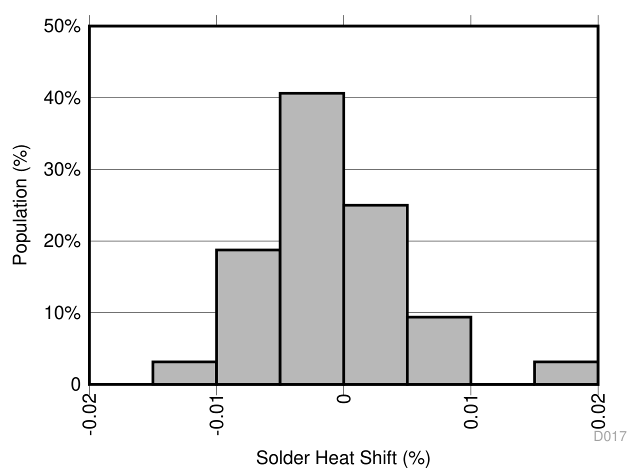


図 8-2. Solder Heat Shift Distribution, V_{OUT} (%)

8.2 Long-Term Stability

One of the key parameters of the REF34xx references is long-term stability. Typical characteristic expressed as: curves shows the typical drift value for the REF34xx is 25 ppm from 0 to 1000 hours. This parameter is characterized by measuring 32 units at regular intervals for a period of 1000 hours. It is important to understand that long-term stability is not ensured by design and that the output from the device may shift beyond the typical 25 ppm specification at any time. For systems that require highly stable output voltages over long periods of time, the designer should consider burning in the devices prior to use to minimize the amount of output drift exhibited by the reference over time.

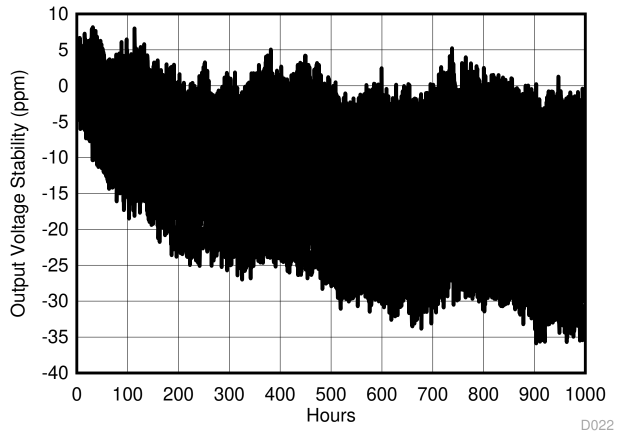


図 8-3. Long Term Stability - 1000 hours (V_{OUT})

8.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF34xx soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Hysteresis can be expressed by 式 1:

$$V_{HYST} = \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \tag{1}$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +125°C and returns to 25°C.

Typical thermal hysteresis distribution is as shown in 図 8-4 and 図 8-5.

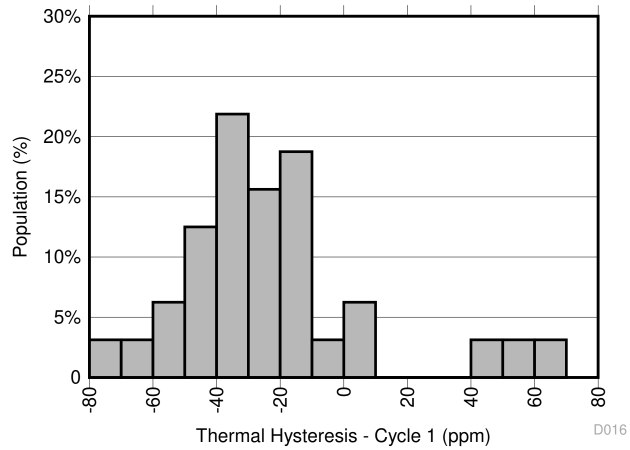


図 8-4. Thermal Hysteresis Distribution Cycle 1 (V_{OUT})

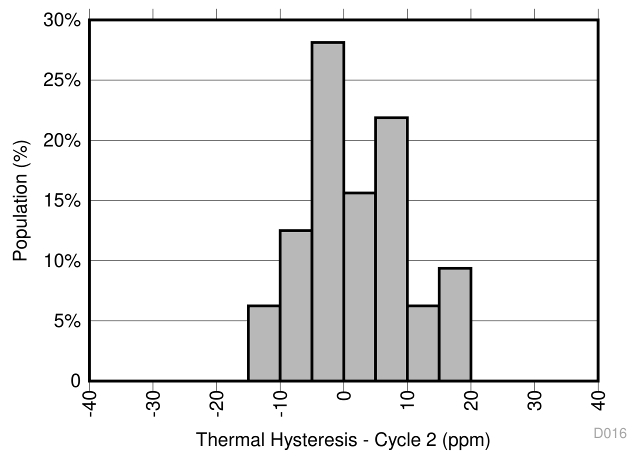


図 8-5. Thermal Hysteresis Distribution Cycle 2 (V_{OUT})

8.4 Power Dissipation

The REF34xx voltage references are capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with 式 2:

$$T_J = T_A + P_D \times R_{\theta JA} \tag{2}$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

8.5 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in 図 8-6 . Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care must be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in 図 8-6.

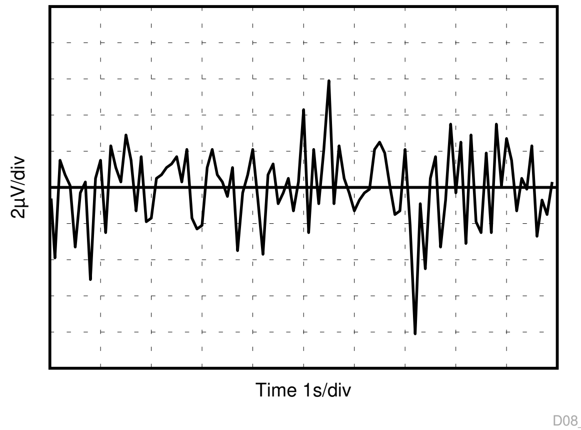


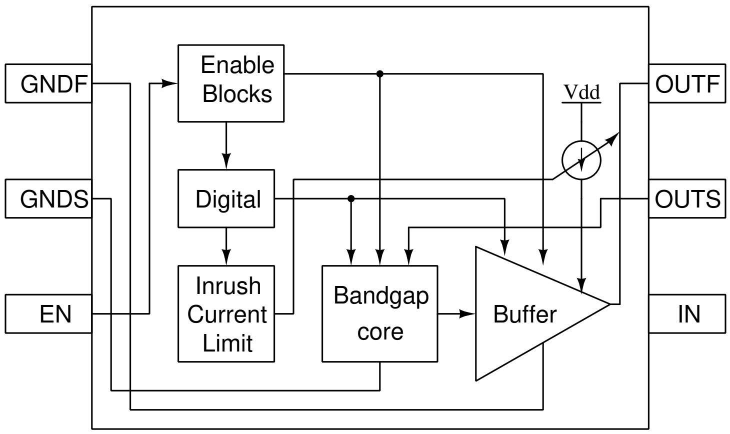
図 8-6. 0.1-Hz to 10-Hz Noise (V_{OUT})

9 Detailed Description

9.1 Overview

The REF34xx is family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The *セクション 9.2* is a simplified block diagram of the REF34xx showing basic band-gap topology.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Supply Voltage

The REF34xx family of references features an extremely low dropout voltage. For loaded conditions, a typical dropout voltage versus load is shown on the front page. The REF34xx features a low quiescent current that is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 72 µA, and the maximum quiescent current over temperature is just 95 µA. Supply voltages below the specified levels can cause the REF34xx to momentarily draw currents greater than the typical quiescent current. Use a power supply with a fast rising edge and low output impedance to easily prevent this issue.

9.3.2 Low Temperature Drift

The REF34xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by 式 3. For this equation, V_{REF} is V_{OUT} which is the output voltage seen at the junction of OUT_F and OUT_S.

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(25°C)} \times \text{Temperature Range}} \right) \times 10^6 \tag{3}$$

9.3.3 Load Current

The REF34xx family is specified to deliver a current load of ±10 mA per output. The device temperature increases according to 式 4:

$$T_J = T_A + P_D \times R_{\theta JA} \tag{4}$$

where

- T_J = junction temperature (°C),
- T_A = ambient temperature (°C),
- P_D = power dissipated (W), and
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The REF34xx maximum junction temperature must not exceed the absolute maximum rating of 150°C.

9.4 Device Functional Modes

9.4.1 EN Pin

When the EN pin of the REF34xx is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF34xx can be placed in a low-power mode by pulling the enable pin, EN, low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 2 µA in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See the セクション 7.5 for logic high and logic low voltage levels.

9.4.2 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF34xx and OPA735 can be used to provide a dual-supply reference from a 5-V supply. 図 9-1 shows the REF34xx used to provide a 2.5-V supply reference voltage. The low drift performance of the REF34xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.

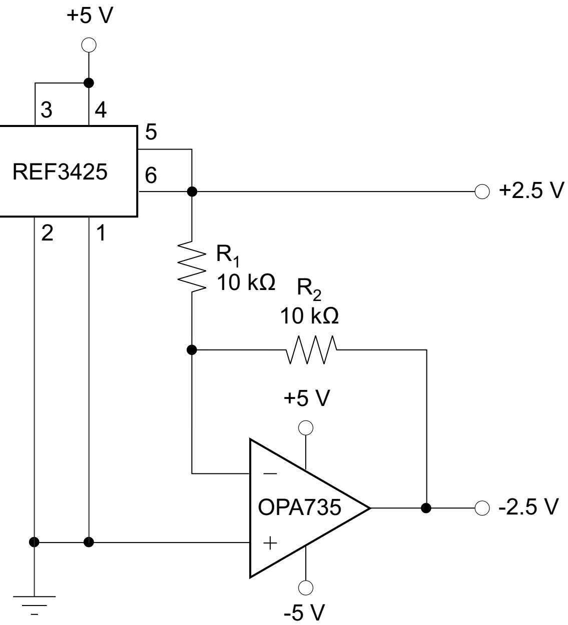


図 9-1. REF34xx and OPA735 Create Positive and Negative Reference Voltages

10 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

As this device has many applications and setups, there are many situations that this datasheet can not characterize in detail. Basic applications includes positive/negative voltage reference and data acquisition systems. The table below shows the typical application of REF34xx and its companion ADC/DAC.

表 10-1. Typical Applications and Companion ADC/DAC

Applications	ADC/DAC
PLC - DCS	DAC8881, ADS8332, ADS8568, ADS8317, ADS8588S, ADS1287
Display Test Equipment	ADS8332
Video Surveillance - Thermal Cameras	ADS7279
Medical Blood Glucose Meter	ADS1112

10.2 Typical Application: Basic Voltage Reference Connection

The circuit shown in 図 10-1 shows the basic configuration for the REF34xx references. Connect bypass capacitors according to the guidelines in *セクション 10.2.2.1*.

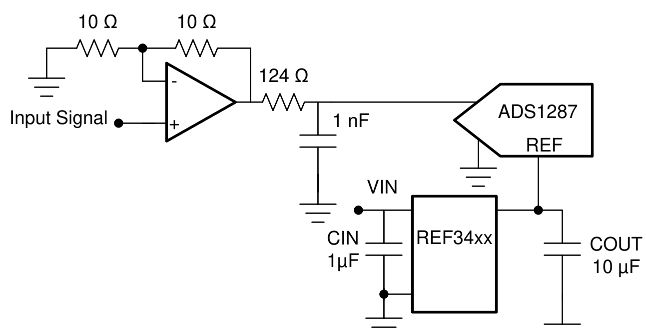


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図 10-1. Basic Reference Connection

10.2.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in 表 10-2 as the input parameters.

表 10-2. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	5 V
Output voltage V_{OUT}	2.5 V
REF34xx input capacitor	1 µF
REF34xx output capacitor	10 µF

10.2.2 Detailed Design Procedure

10.2.2.1 Input and Output Capacitors

A 1-μF to 10-μF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1-μF ceramic capacitor in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least a 0.1 μF must be connected to the output to improve stability and help filter out high frequency noise. An additional 1-μF to 10-μF electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the turnon time of the device.

Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1-μF ceramic capacitor in parallel to reduce overall ESR on the output.

10.2.2.2 4-Wire Kelvin Connections

Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this drop can reach several millivolts or more, introducing a considerable error into the output voltage of the reference. A 1-inch long, 5-millimeter wide trace of 1-ounce copper has a resistance of approximately 100 mΩ at room temperature; at a load current of 10 mA, this can introduce a full millivolt of error. In an ideal board layout, the reference must be mounted as close as possible to the load to minimize the length of the output traces, and, therefore, the error introduced by voltage drop. However, in applications where this is not possible or convenient, force and sense connections (sometimes referred to as Kelvin sensing connections) are provided as a means of minimizing the IR drop and improving accuracy.

Kelvin connections work by providing a set of high impedance voltage-sensing lines to the output and ground nodes. Because very little current flows through these connections, the IR drop across their traces is negligible, and the output and ground voltage information can be obtain with minimum IR drop error.

It is always advantageous to use Kelvin connections whenever possible. However, in applications where the IR drop is negligible or an extra set of traces cannot be routed to the load, the force and sense pins for both V_{OUT} and GND can simply be tied together, and the device can be used in the same fashion as a normal 3-terminal reference (as shown in 図 9-1).

10.2.2.3 V_{IN} Slew Rate Considerations

In applications with slow-rising input voltage signals, the reference exhibits overshoot or other transient anomalies that appear on the output. These phenomena also appear during shutdown as the internal circuitry loses power.

To avoid such conditions, ensure that the input voltage wave-form has both a rising and falling slew rate close to 6 V/ms.

10.2.2.4 Shutdown/Enable Feature

The REF34xx references can be switched to a low power shut-down mode when a voltage of 0.5 V or lower is input to the EN pin. Likewise, the reference becomes operational for EN voltages of 1.6 V or higher. During shutdown, the supply current drops to less than 2 μA, useful in applications that are sensitive to power consumption.

If using the shutdown feature, ensure that the EN pin voltage does not fall between 0.5 V and 1.6 V because this causes a large increase in the supply current of the device and may keep the reference from starting up correctly. If not using the shutdown feature, however, the EN pin can simply be tied to the IN pin, and the reference remains operational continuously.

10.2.3 Application Curves

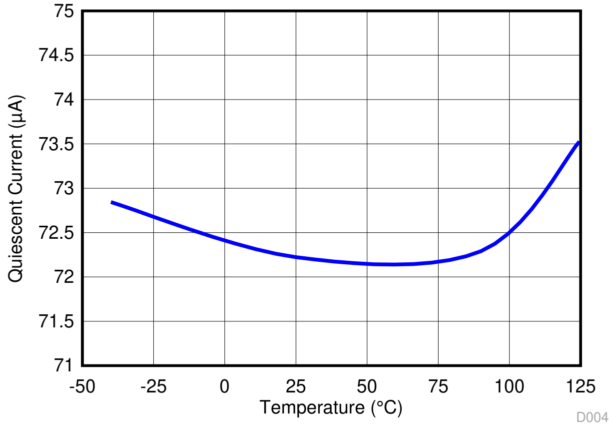

図 10-2. Quiescent Current vs Temperature

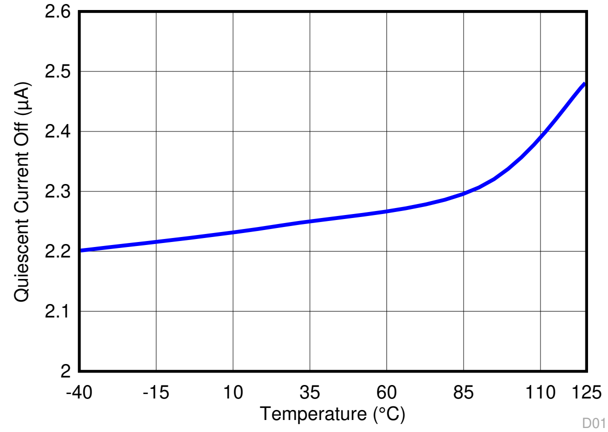

図 10-3. Quiescent Current Shutdown Mode

11 Power Supply Recommendations

The REF34xx family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage. TI recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF.

12 Layout

12.1 Layout Guidelines

図 12-1 illustrates an example of a PCB layout for a data acquisition system using the REF34xx. Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at IN, OUT_F, VOUT of the REF34xx and REF34xxT.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

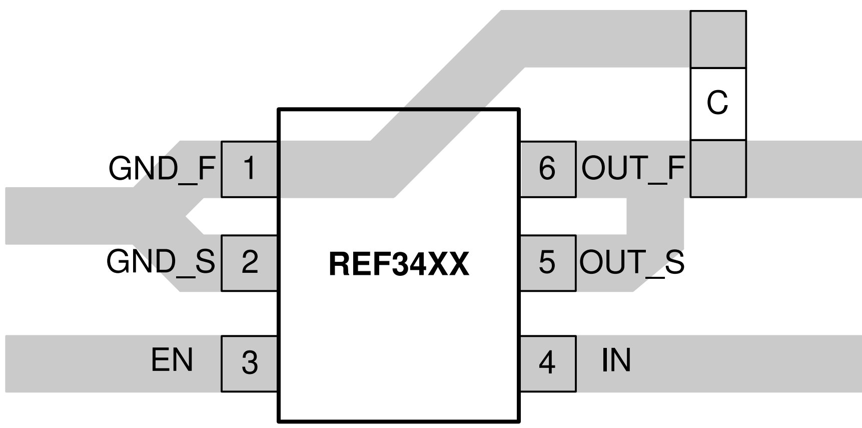

図 12-1. REF34xx Layout Example

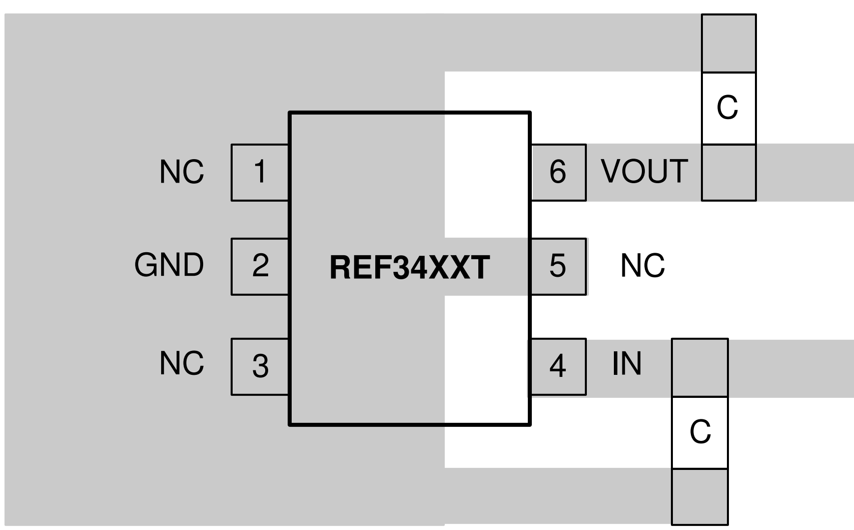

図 12-2. REF34xxT Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF3425IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-250C-1 YEAR	-40 to 125	19ED
REF3425IDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-250C-1 YEAR	-40 to 125	19ED
REF3425IDBVRG4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-250C-1 YEAR	-40 to 125	19ED
REF3425TIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2EVC
REF3425TIDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2EVC
REF3430IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1H6D
REF3430IDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1H6D
REF3430TIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2EUC
REF3430TIDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2EUC
REF3433IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1H5D
REF3433IDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1H5D
REF3433TIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2ETC
REF3433TIDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2ETC
REF3440IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MJD
REF3440IDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MJD
REF3440TIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2ESC
REF3440TIDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2ESC
REF3450IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MKD
REF3450IDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MKD
REF3450TIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2ERC
REF3450TIDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2ERC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF REF3425, REF3430, REF3433, REF3440 :

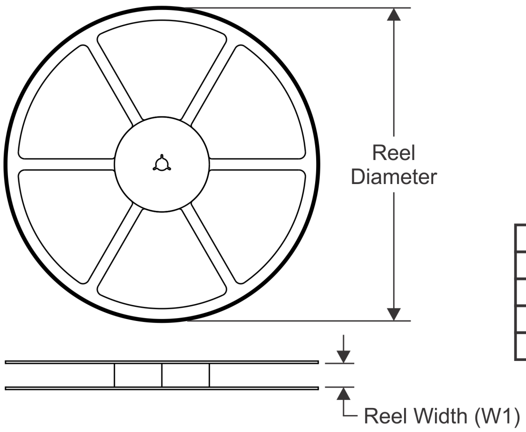
- Enhanced Product : REF3425-EP, REF3430-EP, REF3433-EP, REF3440-EP

NOTE: Qualified Version Definitions:

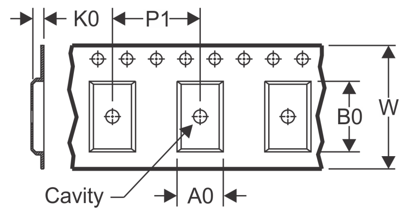
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

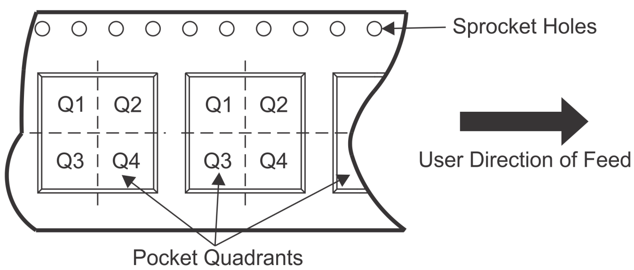


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

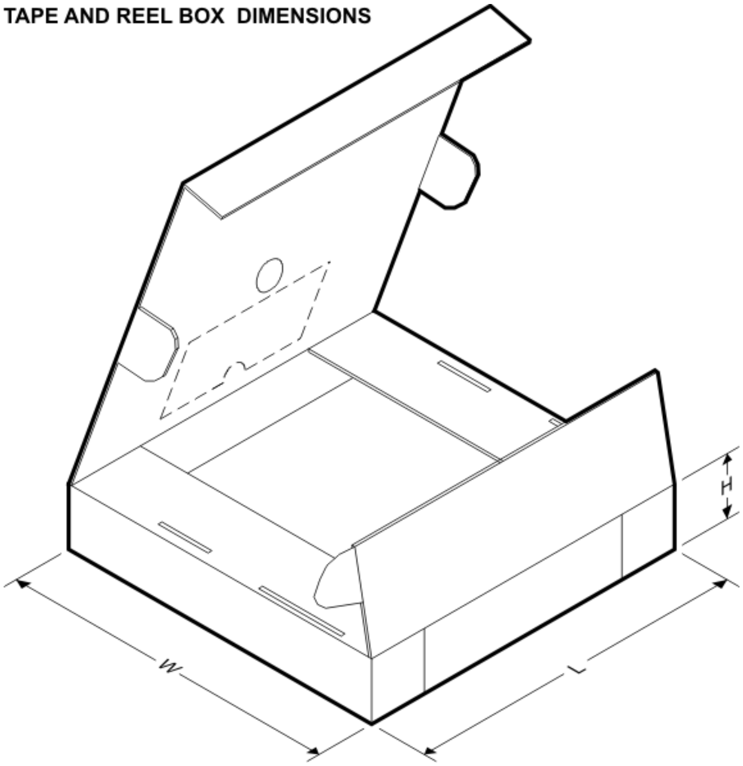
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

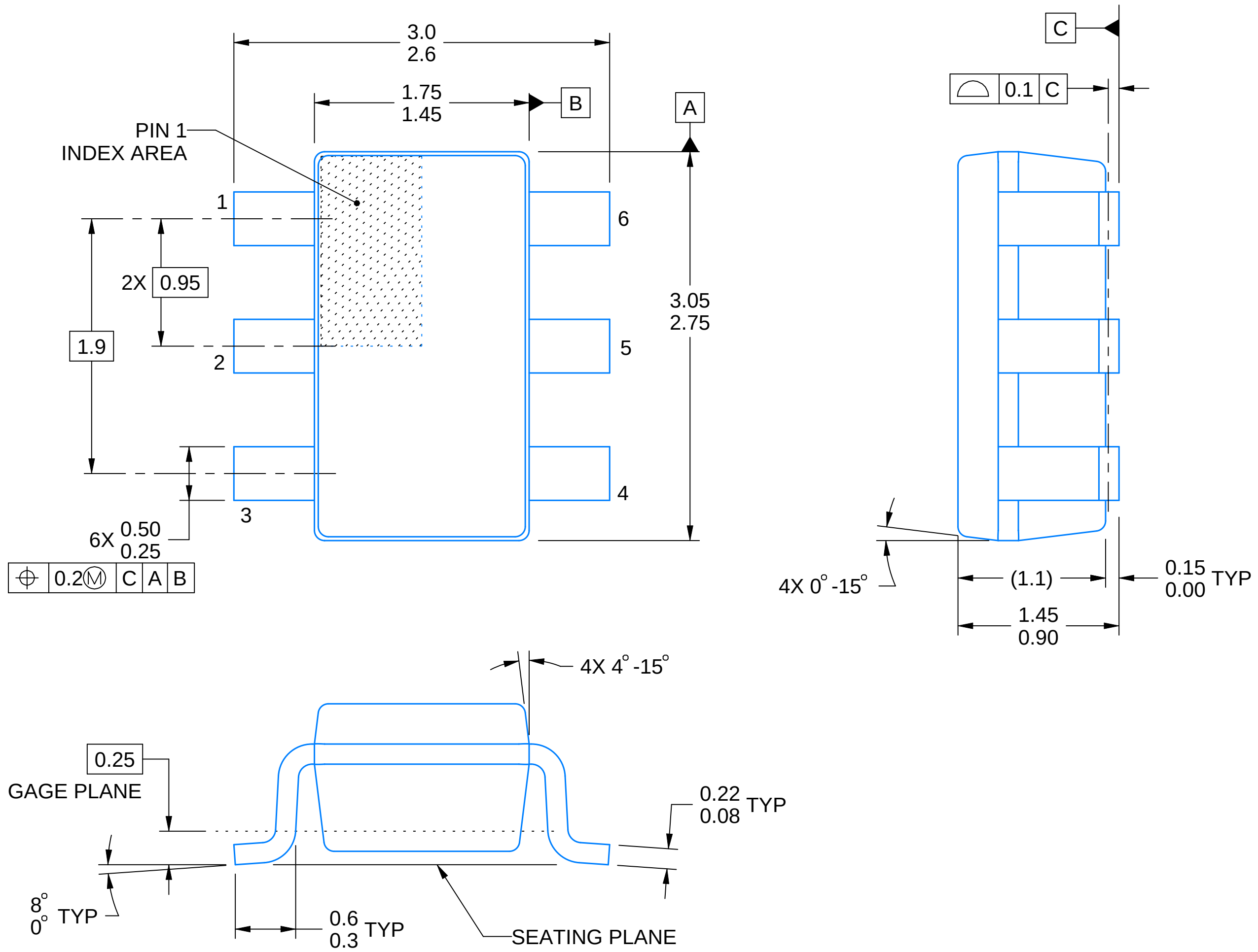
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF3425IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REF3425TIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3430IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REF3430TIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3433IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REF3433TIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3440IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REF3440TIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3450IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REF3450TIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF3425IDBVR	SOT-23	DBV	6	3000	445.0	220.0	345.0
REF3425TIDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3430IDBVR	SOT-23	DBV	6	3000	445.0	220.0	345.0
REF3430TIDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3433IDBVR	SOT-23	DBV	6	3000	445.0	220.0	345.0
REF3433TIDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3440IDBVR	SOT-23	DBV	6	3000	445.0	220.0	345.0
REF3440TIDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3450IDBVR	SOT-23	DBV	6	3000	445.0	220.0	345.0
REF3450TIDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0



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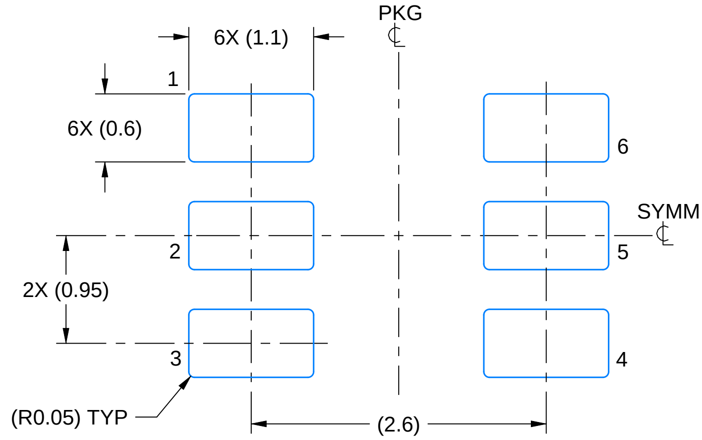
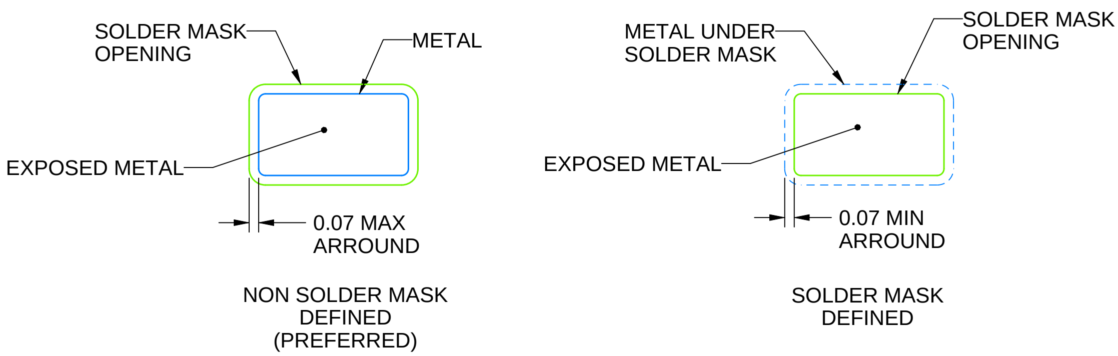
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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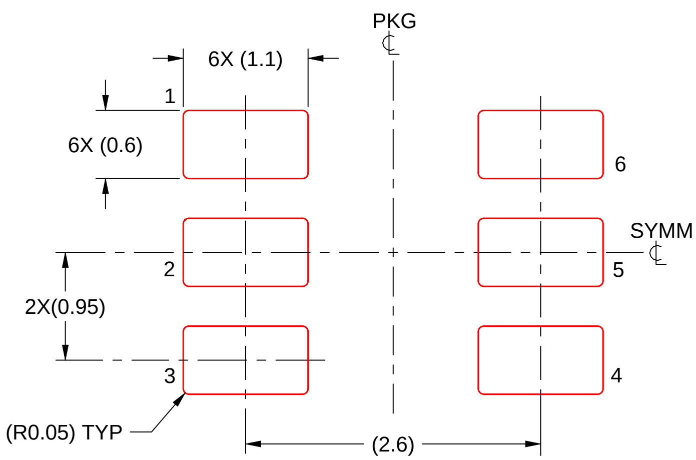
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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