TEXAS INSTRUMENTS
REF2025, REF2030, REF2033, REF2041
JAJSFP5E – JULY 2018 – REVISED FEBRUARY 2022

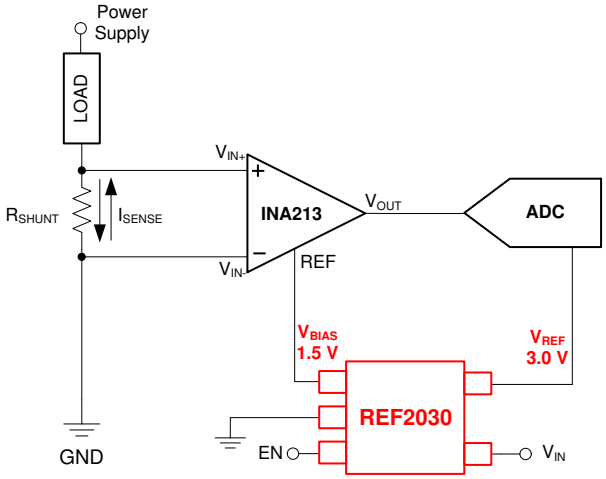
REF20xx 低ドリフト、低消費電力、デュアル出力、V_{REF} および $V_{REF}/2$ 基準電圧

1 特長

- V_{REF} および V_{REF} / 2 という 2 つの出力により、単一電源システムでの使用に便利
- 優れた温度ドリフト性能:
  - -40℃～125℃ について 8ppm/℃ (最大値)
- 高い初期精度:±0.05% (最大値)
- 温度範囲全体にわたる V_{REF} および V_{BIAS} トラッキング:
  - -40℃～85℃ について 6ppm/℃ (最大値)
  - -40℃～125℃ について 7ppm/℃ (最大値)
- 超小型パッケージ:SOT23-5
- 低いドロップアウト電圧:10mV
- 大きい出力電流:±20mA
- 低い静止電流:360µA
- ライン・レギュレーション: 3 ppm/V
- 負荷レギュレーション: 8ppm/mA
- マットスズメッキ・バージョン (REF2025AISDDCR) は、Battelle Class III および同様の過酷な環境で耐腐食性を強化

2 アプリケーション

- 電気メーター
- アナログ入力モジュール
- アナログ出力モジュール
- サーボ・ドライブ制御モジュール
- サーキット・ブレーカ (ACB、MCCB、VCB)
- 医療用デジタル温度計
- 計測機器:ラボ、フィールド
- バッテリ試験装置



アプリケーションの例

3 概要

正の電源電圧のみを使用するアプリケーションでは、入力バイポーラ信号をバイアスするため、多くの場合 A/D コンバータ (ADC) 入力範囲の中間に、追加の安定した電圧が必要になります。REF20xx は、ADC 用の基準電圧 (V_{REF})、および入力バイポーラ信号をバイアスするために使用する第 2 の高精度電圧 (V_{BIAS}) を供給します。

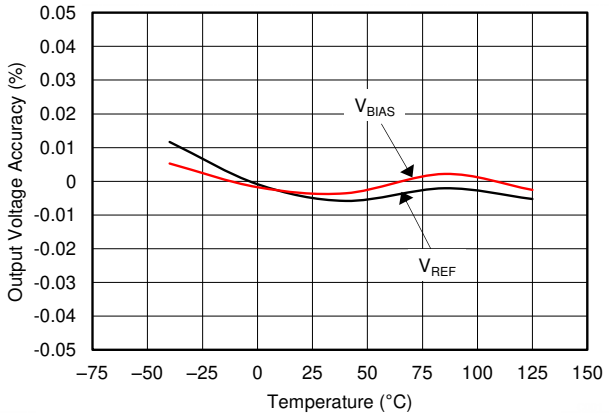
REF20xx は、V_{REF} および V_{BIAS} の出力に対する温度ドリフト (最大値 8ppm/℃) および初期精度 (0.05%) が非常に優れており、430µA 未満の静止電流で動作します。さらに、V_{REF} および V_{BIAS} 出力は、-40℃～125℃ の温度範囲にわたって、6ppm/℃ (最大値) の精度で相互にトラッキングします。これらの機能すべてによって、信号チェーンの精度向上、基板面積の削減、ディスクリート・ソリューションと比較してシステムのコスト低減を実現します。ドロップアウト電圧が 10mV と非常に低いため、非常に低い入力電圧で動作し、バッテリ動作のシステムでは非常に有用です。

V_{REF} および V_{BIAS} 電圧は、どちらも非常に優れた仕様を備えており、同様に電流を適切にシンクおよびソースできます。長期的な安定性が非常に優れており、ノイズ・レベルが低いため、これらのデバイスは高精度の産業用アプリケーションに最適です。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
REF20xx	SOT-23 (5)	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



V_{REF} および V_{BIAS} と温度との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (May 2018) to Revision E (January 2022) — **Page**

- 「アプリケーション」セクションを更新 ... 1
- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Changed *ESD Rating* table: changed HBM rating from ±4000 V to ±2500 V ... 4
- Updated Long-term stability value ... 5
- Added Long-Term Stability sub-section under Parameter Measurement Information section ... 14

Changes from Revision C (January 2017) to Revision D (May 2018) — **Page**

- Changed application information to include corrosion resistance advantages. ... 19

Changes from Revision B (July 2014) to Revision C (January 2017) — **Page**

- Added I/O column to *Pin Functions* table ... 3
- Added *Storage temperature* parameter to *Absolute Maximum Ratings* table (moved from *ESD Ratings* table) ... 4
- Changed *ESD Rating* table: changed title, updated table format ... 4

Changes from Revision A (June 2014) to Revision B (July 2014) — **Page**

- デバイス・ステータスを「事前情報」から「量産データ」に変更 ... 1
- 「製品情報」表から脚注 2 を削除 ... 1
- Deleted footnote from Device Comparison Table ... 3
- Added Thermal Information table ... 4

Changes from Revision * (May 2014) to Revision A (June 2014) — **Page**

- 製品プレビューのデータシートを変更 ... 1

5 Device Comparison Table

PRODUCT	V_{REF}	V_{BIAS}
REF2025	2.5 V	1.25 V
REF2030	3.0 V	1.5 V
REF2033	3.3 V	1.65 V
REF2041	4.096 V	2.048 V

6 Pin Configuration and Functions

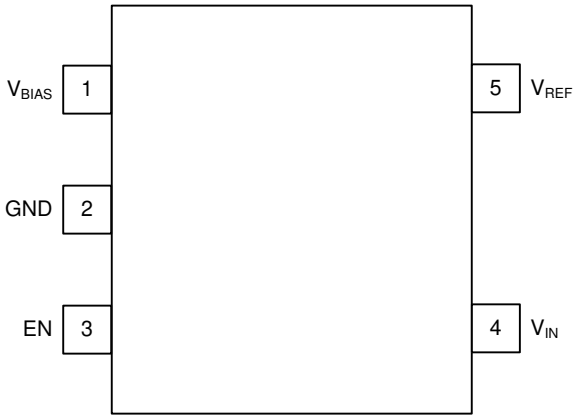


図 6-1. DDC Package SOT23-5 (Top View)

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{BIAS}	Output	Bias voltage output (V_{REF} / 2)
2	GND	—	Ground
3	EN	Input	Enable (EN ≥ V_{IN} – 0.7 V, device enabled)
4	V_{IN}	Input	Input supply voltage
5	V_{REF}	Output	Reference voltage output (V_{REF})

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	6	V
	EN	–0.3	V_{IN} + 0.3	
Temperature	Operating	–55	150	°C
	Junction, T_j		150	
	Storage, T_{stg}	–65	170	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range (I_L = 0 mA, T_A = 25°C)	V_{REF} + 0.02(1)		5.5	V

(1) See 図 7-28 in セクション 7.6 for minimum input voltage at different load currents and temperature

7.4 Thermal Information

THERMAL METRIC(1)		REF20xx DDC (SOT23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

At T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, unless otherwise noted. Both V_{REF} and V_{BIAS} have the same specifications.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT								
	Output voltage accuracy				–0.05%		0.05%	
	Output voltage temperature coefficient(1)		–40°C ≤ T_A ≤ 125°C			±3	±8	ppm/°C
	V_{REF} and V_{BIAS} tracking over temperature(2)		–40°C ≤ T_A ≤ 85°C			±1.5	±6	ppm/°C
			–40°C ≤ T_A ≤ 125°C			±2	±7	
LINE AND LOAD REGULATION								
$\Delta V_{O(\Delta VI)}$	Line regulation		V_{REF} + 0.02 V ≤ V_{IN} ≤ 5.5 V			3	35	ppm/V
$\Delta V_{O(\Delta IL)}$	Load regulation	Sourcing	0 mA ≤ I_L ≤ 20 mA , V_{REF} + 0.6 V ≤ V_{IN} ≤ 5.5 V			8	20	ppm/mA
		Sinking	0 mA ≤ I_L ≤ –20 mA, V_{REF} + 0.02 V ≤ V_{IN} ≤ 5.5 V			8	20	
POWER SUPPLY								
I_{CC}	Supply current	Active mode				360	430	µA
			–40°C ≤ T_A ≤ 125°C				460	
		Shutdown mode				3.3	5	
			–40°C ≤ T_A ≤ 125°C				9	
	Enable voltage		Device in shutdown mode (EN = 0)		0		0.7	V
			Device in active mode (EN = 1)		V_{IN} – 0.7		V_{IN}	
	Dropout voltage					10	20	mV
			I_L = 20 mA				600	
I_{SC}	Short-circuit current					50		mA
t_{on}	Turn-on time		0.1% settling, C_L = 1 µF			500		µs
NOISE								
	Low-frequency noise(3)		0.1 Hz ≤ f ≤ 10 Hz			12		ppm_{PP}
	Output voltage noise density		f = 100 Hz			0.25		ppm/√Hz
CAPACITIVE LOAD								
	Stable output capacitor range				0		10	µF
HYSTERESIS AND LONG TERM STABILITY								
	Long-term stability(4)		0 to 1000 hours			25		ppm
	Output voltage hysteresis(5)		25°C, –40°C, 125°C, 25°C	Cycle 1		60		ppm
				Cycle 2		35		

(1) Temperature drift is specified according to the box method. See the *セクション 9.3* section for more details.
(2) The V_{REF} and V_{BIAS} tracking over temperature specification is explained in more detail in the *セクション 9.3* section.
(3) The peak-to-peak noise measurement procedure is explained in more detail in the *セクション 8.4* section.
(4) Long-term stability measurement procedure is explained in more in detail in the セクション 8.2 section.
(5) The thermal hysteresis measurement procedure is explained in more detail in the *セクション 8.3* section.

7.6 Typical Characteristics

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.

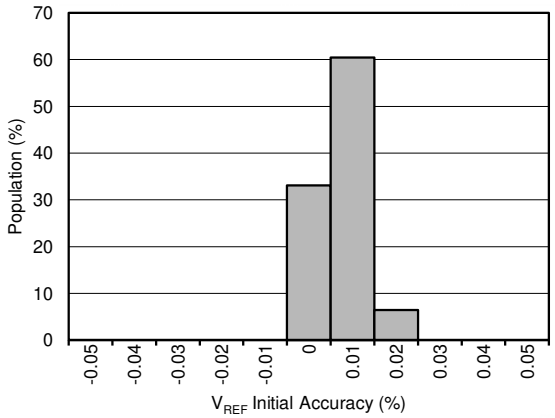
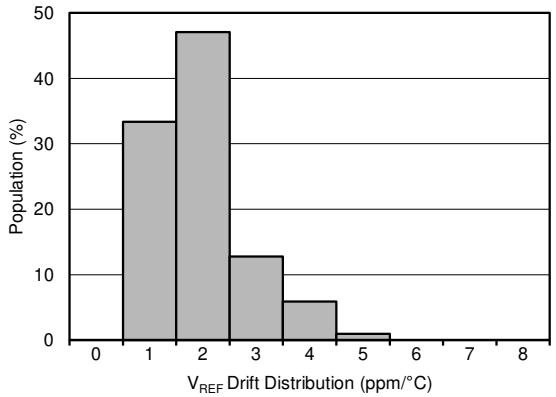


図 7-1. Initial Accuracy Distribution (V_{REF})



–40°C ≤ T_A ≤ 125°C

図 7-2. Drift Distribution (V_{REF})

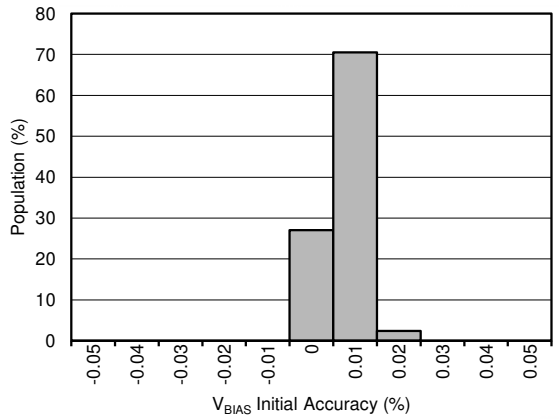
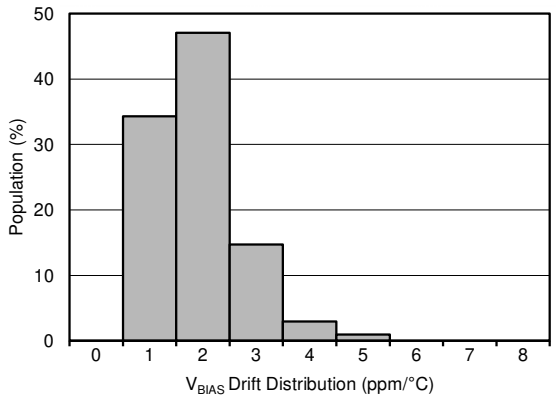


図 7-3. Initial Accuracy Distribution (V_{BIAS})



–40°C ≤ T_A ≤ 125°C

図 7-4. Drift Distribution (V_{BIAS})

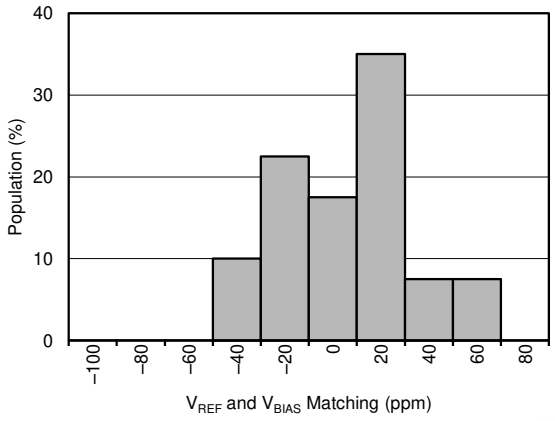
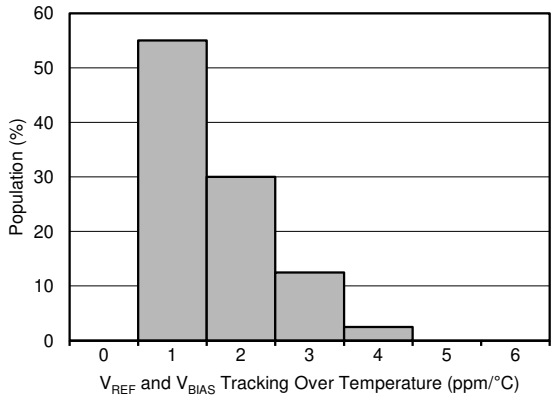


図 7-5. V_{REF} – 2 × V_{BIAS} Distribution

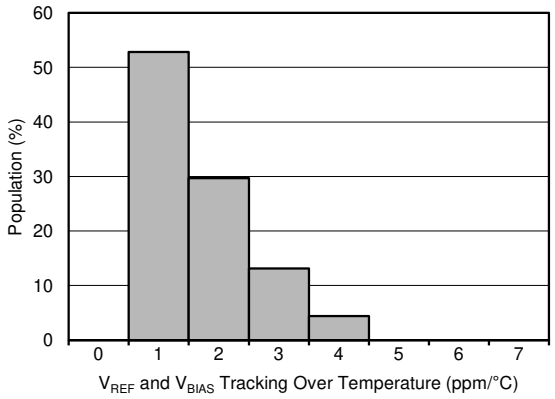


–40°C ≤ T_A ≤ 85°C

図 7-6. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature

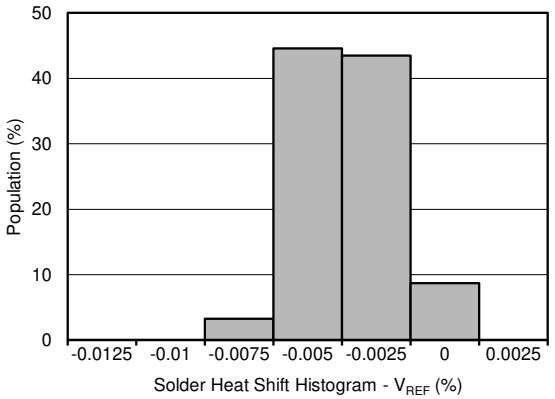
7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.



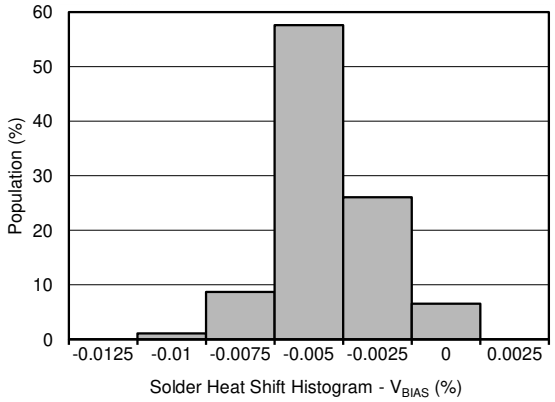
–40°C ≤ T_A ≤ 125°C

図 7-7. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature



Refer to the *セクション 8.1* section for more information.

図 7-8. Solder Heat Shift Distribution (V_{REF})



Refer to the *セクション 8.1* section for more information.

図 7-9. Solder Heat Shift Distribution (V_{BIAS})

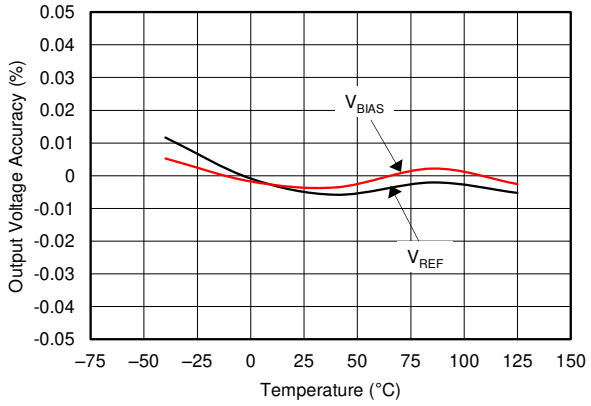


図 7-10. Output Voltage Accuracy (V_{REF}) vs Temperature

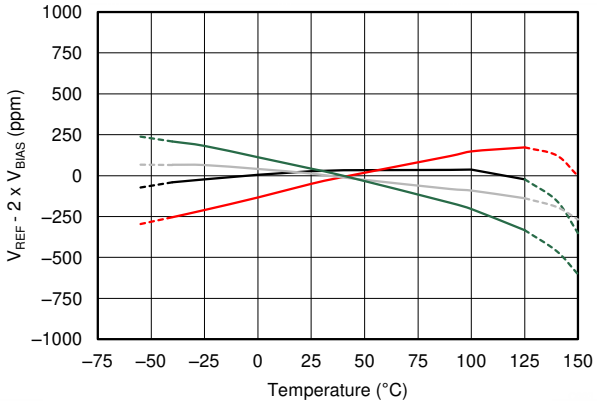
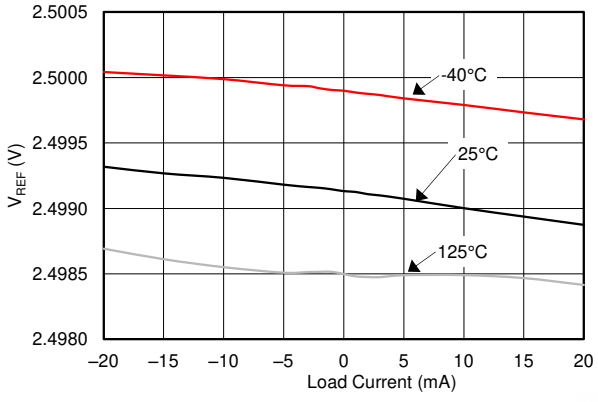


図 7-11. V_{REF} – 2 × V_{BIAS} Tracking vs Temperature

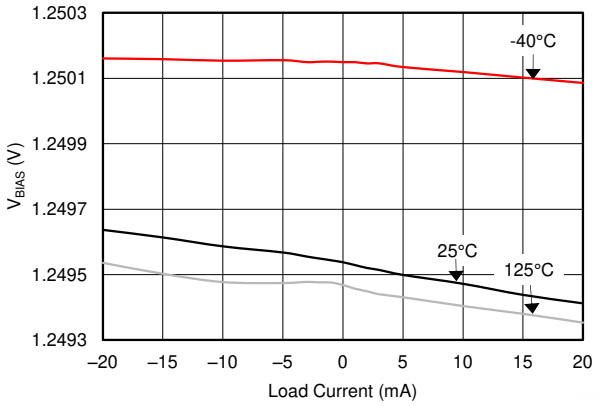


V_{REF} output

図 7-12. Output Voltage Change vs Load Current (V_{REF})

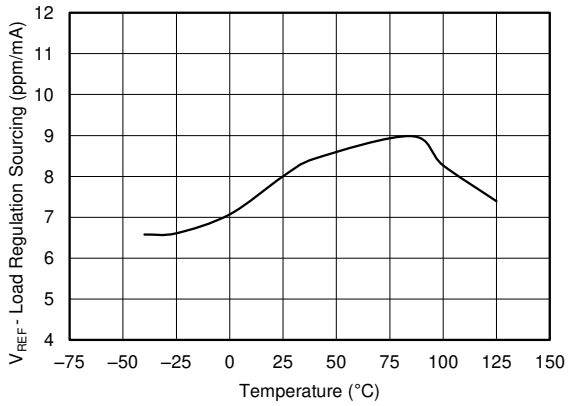
7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.



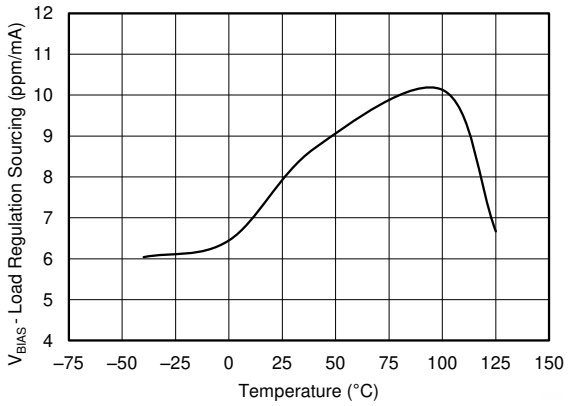
V_{BIAS} output

図 7-13. Output Voltage Change vs Load Current (V_{BIAS})



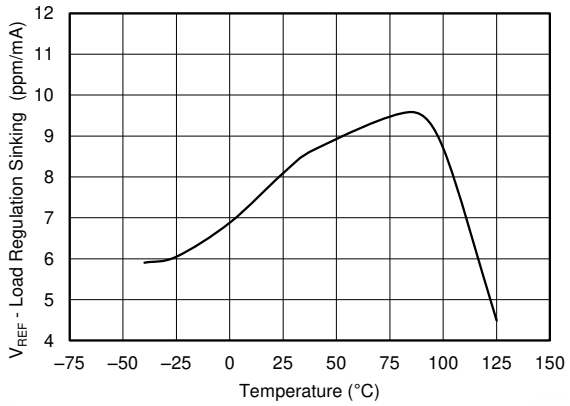
V_{REF} output I_L = 20 mA

図 7-14. Load Regulation Sourcing vs Temperature (V_{REF})



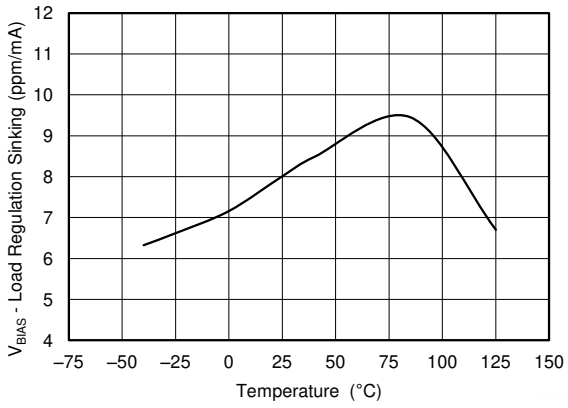
V_{BIAS} output I_L = 20 mA

図 7-15. Load Regulation Sourcing vs Temperature (V_{BIAS})



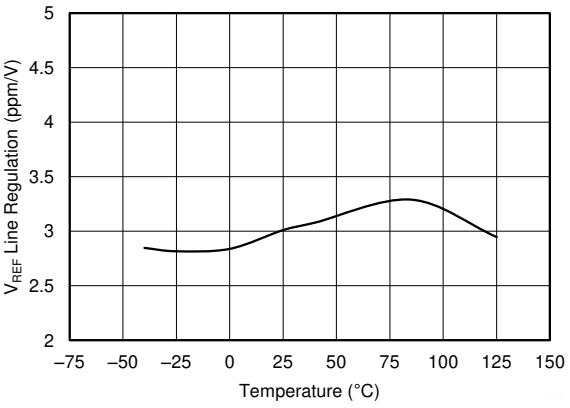
V_{REF} output I_L = –20 mA

図 7-16. Load Regulation Sinking vs Temperature (V_{REF})



V_{BIAS} output I_L = –20 mA

図 7-17. Load Regulation Sinking vs Temperature (V_{BIAS})

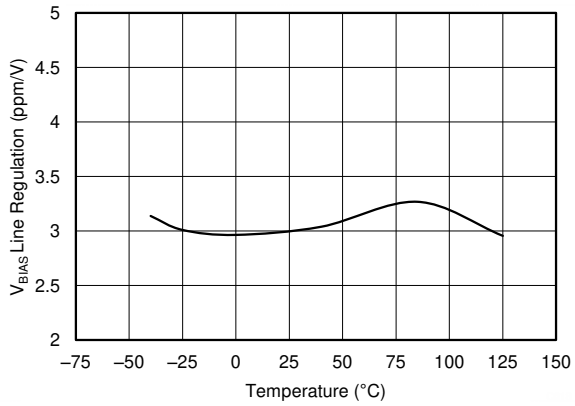


V_{REF} output

図 7-18. Line Regulation vs Temperature (V_{REF})

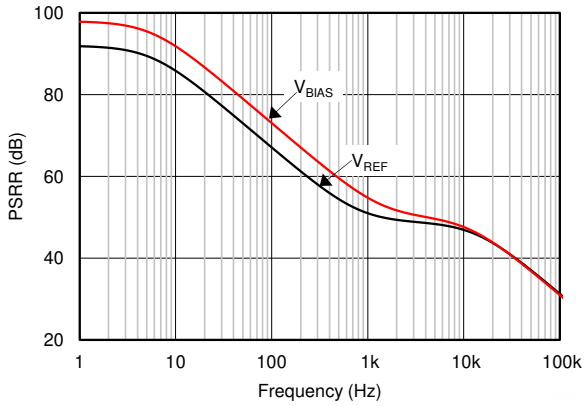
7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.



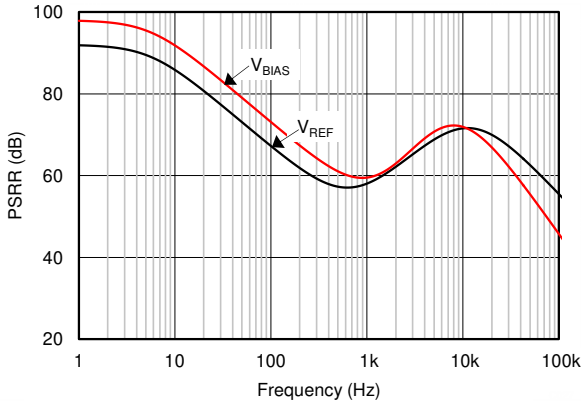
V_{BIAS} output

図 7-19. Line Regulation vs Temperature (V_{BIAS})



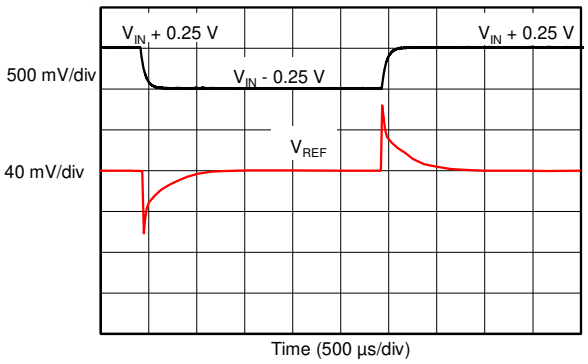
C_L = 0 µF

図 7-20. Power-Supply Rejection Ratio vs Frequency



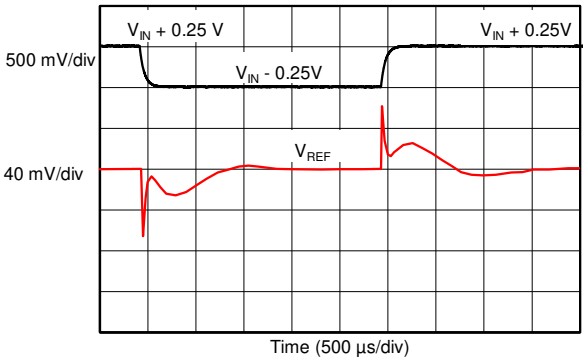
C_L = 10 µF

図 7-21. Power-Supply Rejection Ratio vs Frequency



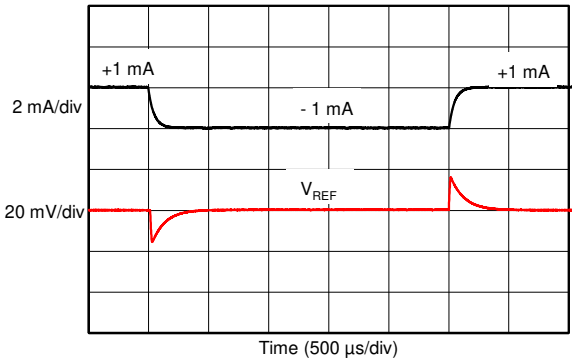
C_L = 1 µF

図 7-22. Line Transient Response



C_L = 10 µF

図 7-23. Line Transient Response

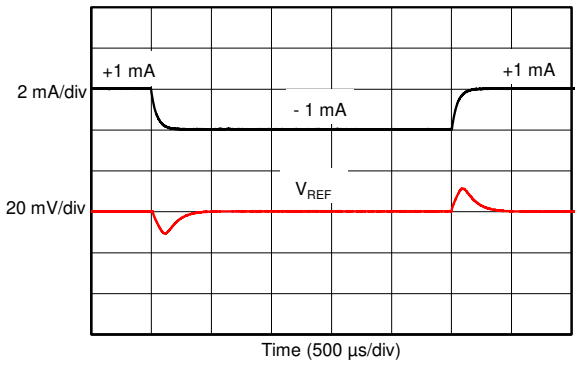


C_L = 1 µF I_L = ±1-mA step

図 7-24. Load Transient Response

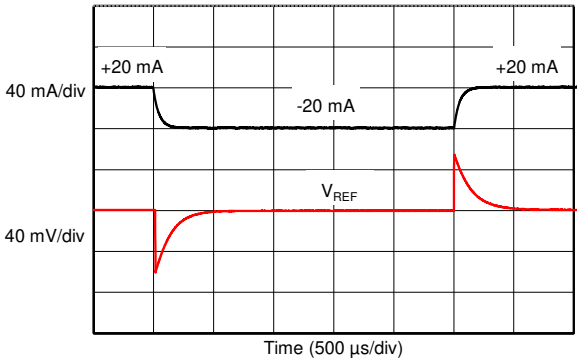
7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.



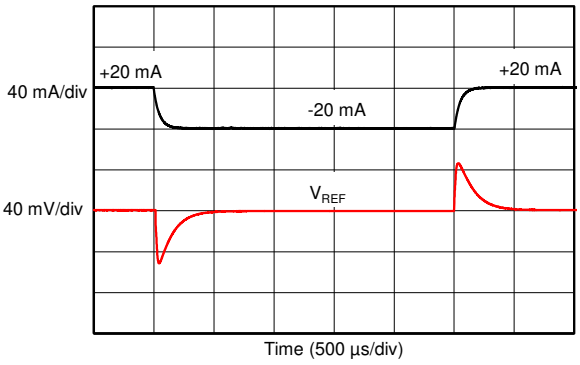
C_L = 10 µF I_L = ±1-mA step

図 7-25. Load Transient Response



C_L = 1 µF I_L = ±20-mA step

図 7-26. Load Transient Response



C_L = 10 µF I_L = ±20-mA step

図 7-27. Load Transient Response

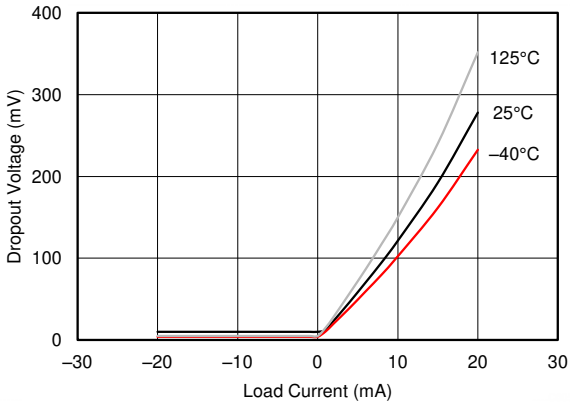
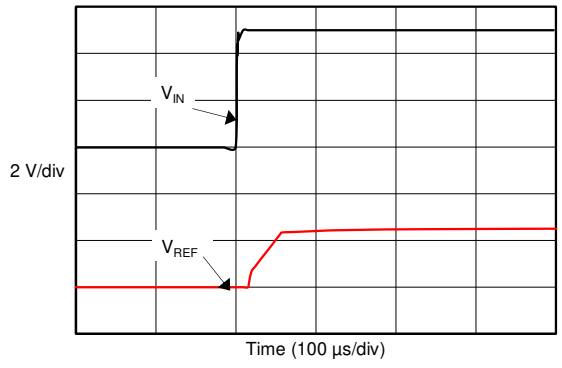
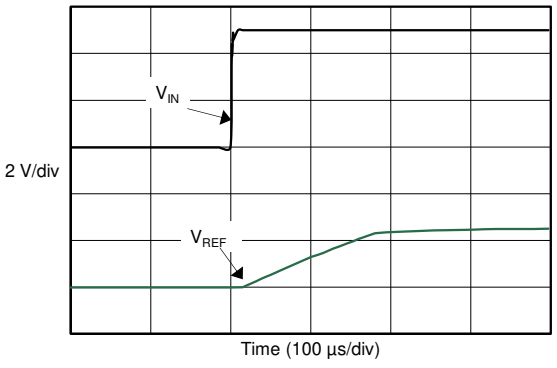


図 7-28. Minimum Dropout Voltage vs Load Current



C_L = 1 µF

図 7-29. Turn-On Settling Time



C_L = 10 µF

図 7-30. Turn-On Settling Time

7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.

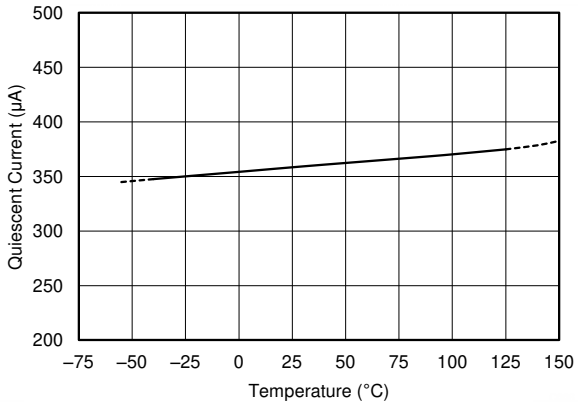


図 7-31. Quiescent Current vs Temperature

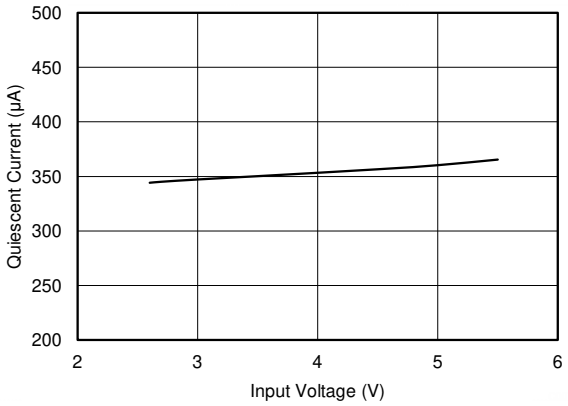
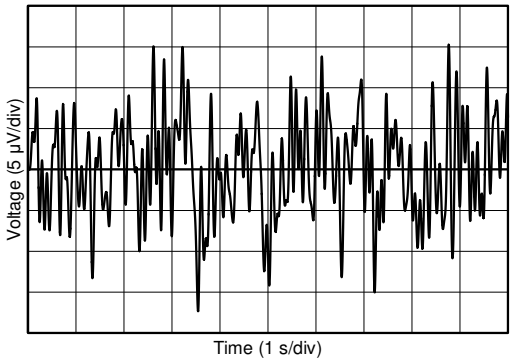
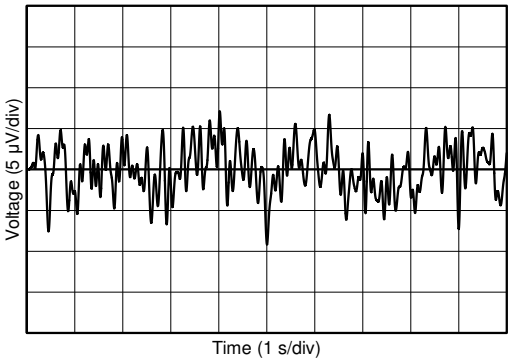


図 7-32. Quiescent Current vs Input Voltage



V_{REF} output

図 7-33. 0.1-Hz to 10-Hz Noise (V_{REF})



V_{BIAS} output

図 7-34. 0.1-Hz to 10-Hz Noise (V_{BIAS})

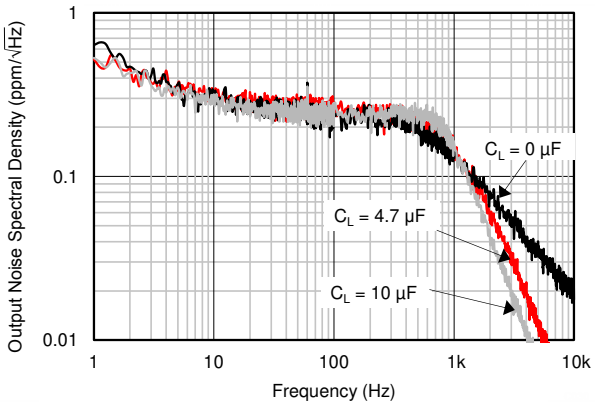
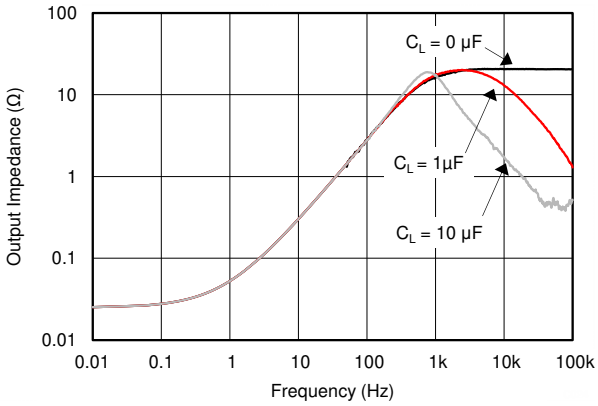


図 7-35. Output Voltage Noise Spectrum



V_{REF} output

図 7-36. Output Impedance vs Frequency (V_{REF})

7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.

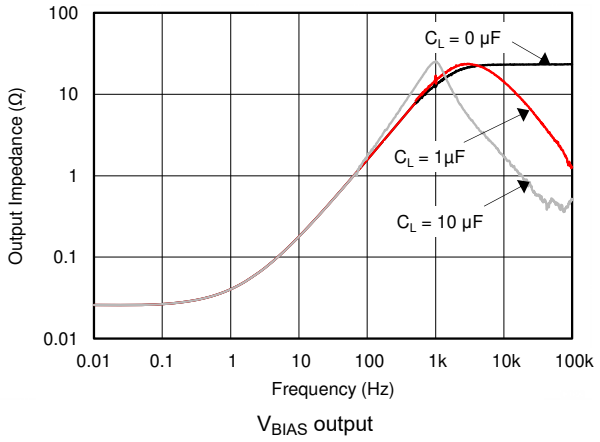


図 7-37. Output Impedance vs Frequency (V_{BIAS})

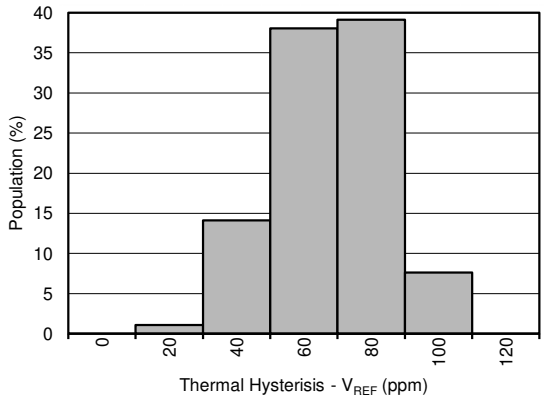


図 7-38. Thermal Hysteresis Distribution (V_{REF})

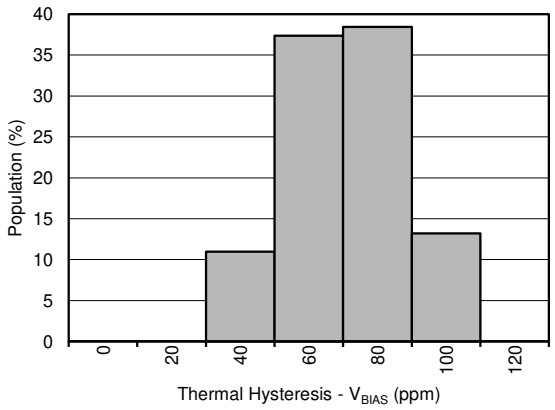


図 7-39. Thermal Hysteresis Distribution (V_{BIAS})

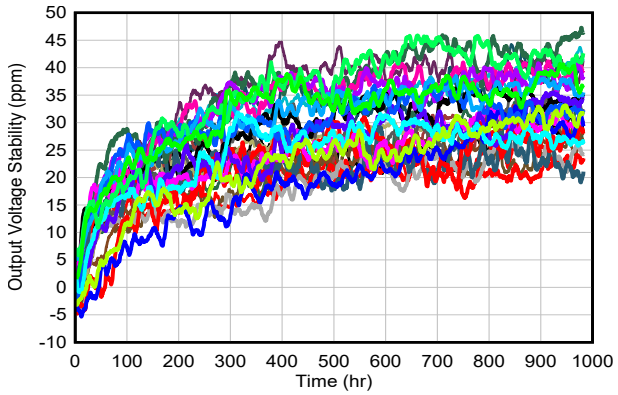


図 7-40. Long-Term Stability (First 1000 hours)

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF20xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 92 devices were soldered on four printed circuit boards [23 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in 図 8-1. The printed circuit board is comprised of FR4 material. The board thickness is 1.57 mm and the area is 171.54 mm × 165.1 mm.

The reference and bias output voltages are measured before and after the reflow process; the typical shift is displayed in 図 8-2 and 図 8-3. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device should be soldered in the second pass to minimize its exposure to thermal stress.

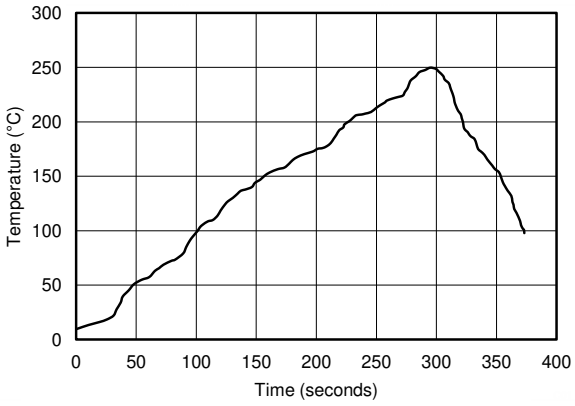


図 8-1. Reflow Profile

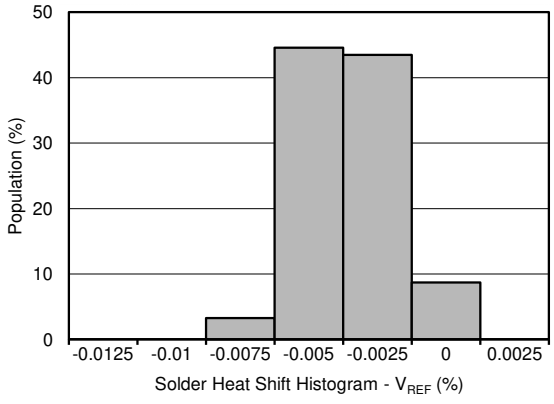


図 8-2. Solder Heat Shift Distribution, V_{REF} (%)

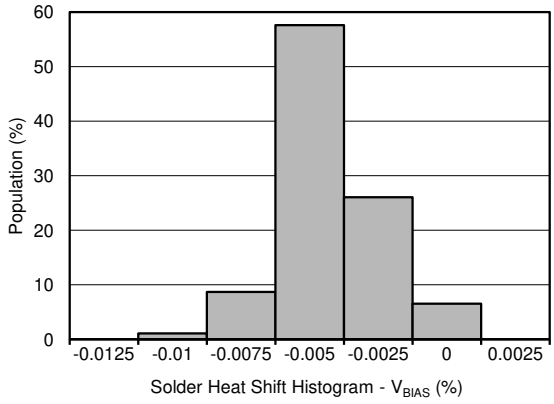


図 8-3. Solder Heat Shift Distribution, V_{BIAS} (%)

8.2 Long-Term Stability

The long term stability of the REF20xx was collected on 32 parts that were soldered onto Printed Circuit Boards without any slots or special layout considerations. The boards were then placed into an oven with air temperature maintained at T_A = 35°C. The V_{REF} output of the 32 parts was measured regularly. Typical long term stability is as shown in 図 8-4.

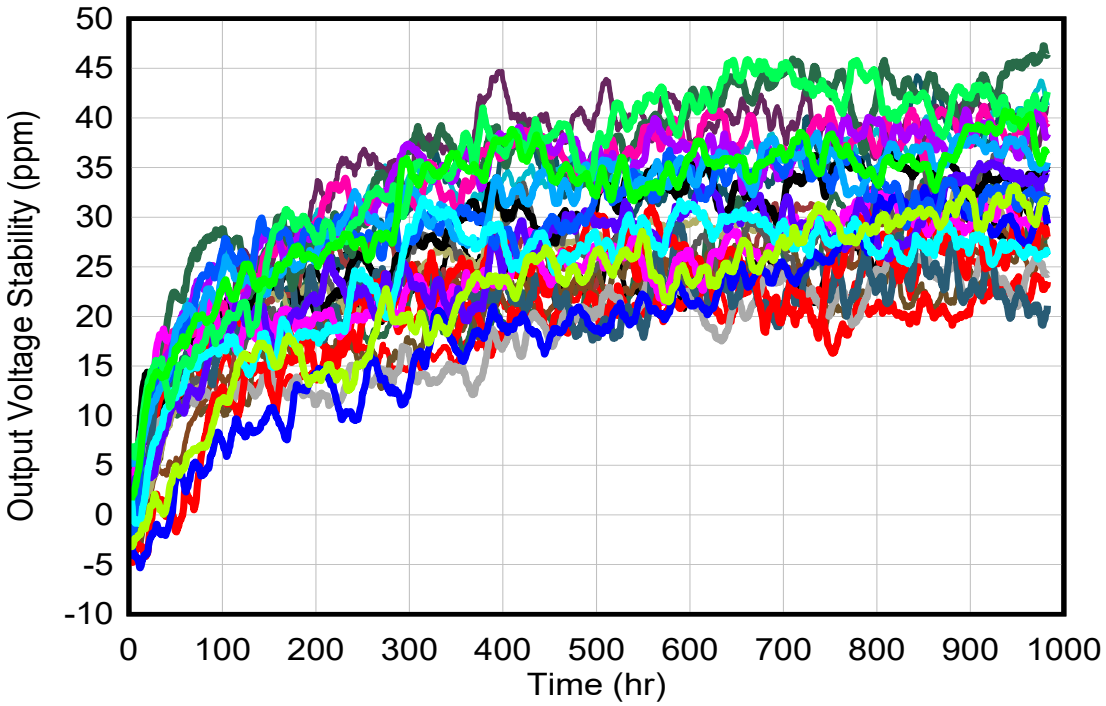


図 8-4. Long Term Stability – 1000 hours (V_{REF})

8.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF20xx soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by 式 1:

$$V_{HYST} = \left(\frac{\left| V_{PRE} - V_{POST} \right|}{V_{NOM}} \right) \bullet 10^6 \quad \text{(ppm)} \tag{1}$$

where

- V_{HYST} = thermal hysteresis (in units of ppm),
- V_{NOM} = the specified output voltage,
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling, and
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C.

Typical thermal hysteresis distribution is as shown in 図 8-5 and 図 8-6.

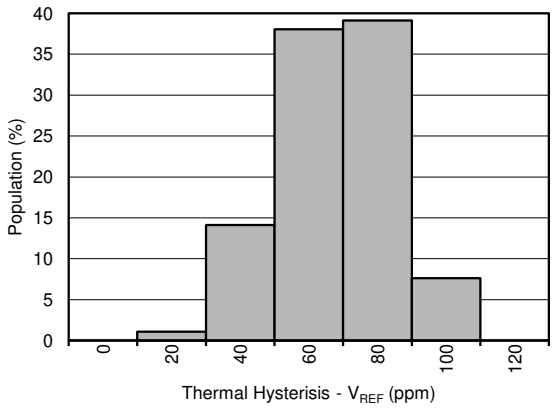


図 8-5. Thermal Hysteresis Distribution (V_{REF})

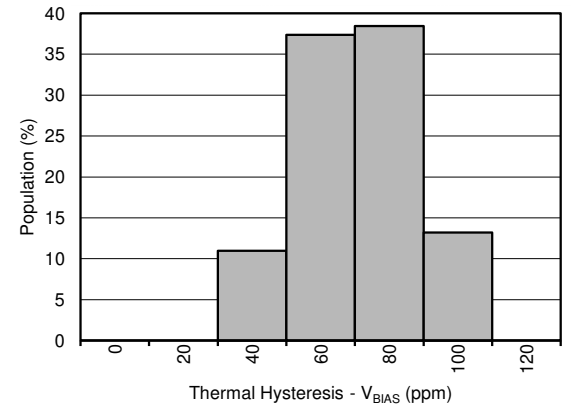


図 8-6. Thermal Hysteresis Distribution (V_{BIAS})

8.4 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in 図 8-7 and 図 8-8. Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in 図 8-9.

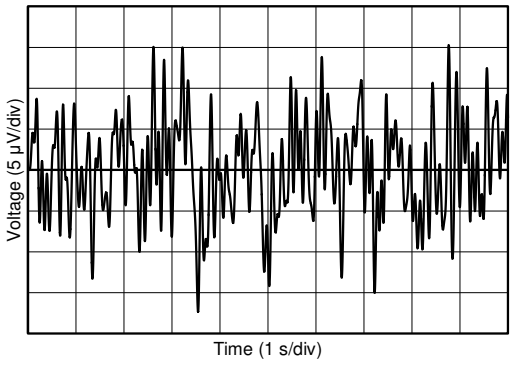


図 8-7. 0.1-Hz to 10-Hz Noise (V_{REF})

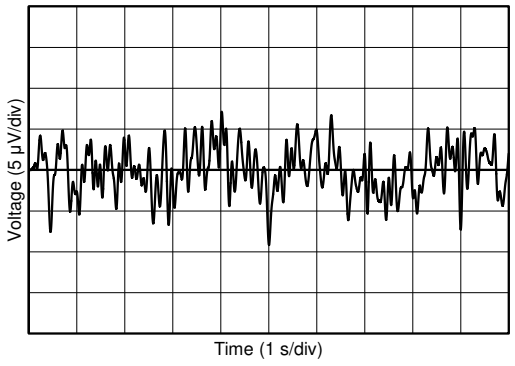


図 8-8. 0.1-Hz to 10-Hz Noise (V_{BIAS})

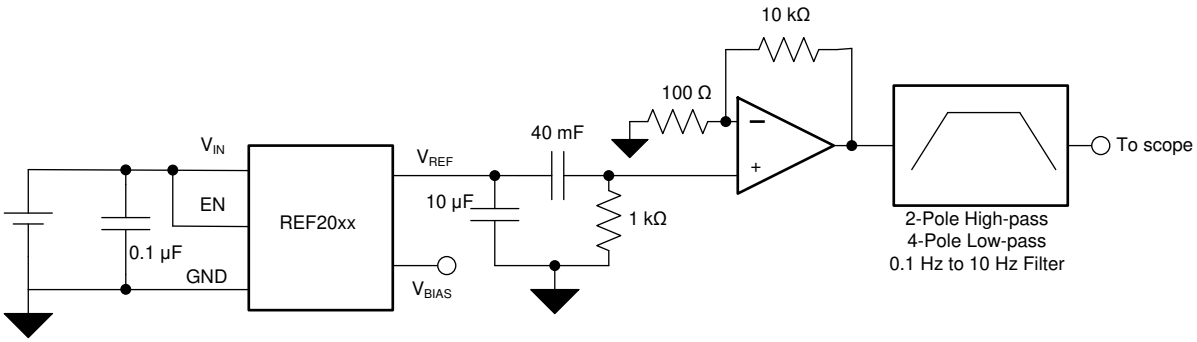


図 8-9. 0.1-Hz to 10-Hz Noise Measurement Setup

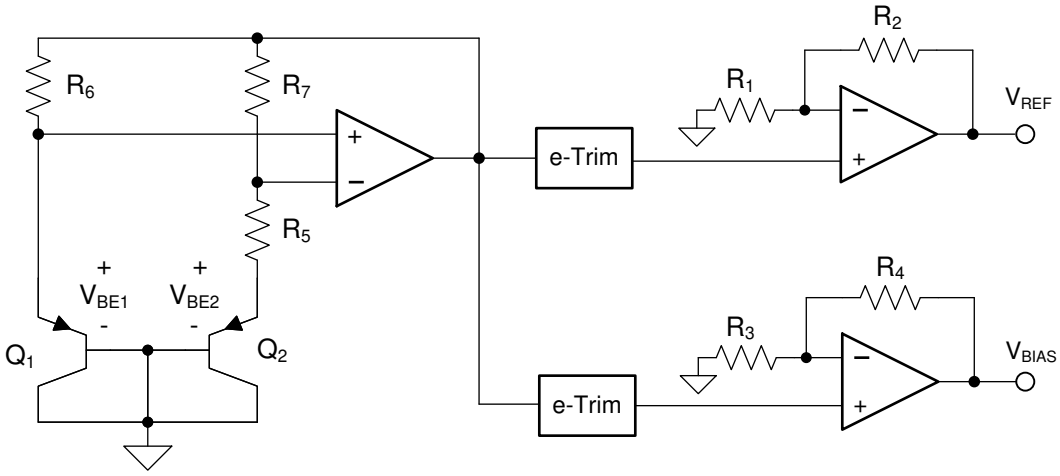
9 Detailed Description

9.1 Overview

The REF20xx are a family of dual-output, V_{REF} and V_{BIAS} (V_{REF} / 2) band-gap voltage references. The *セクション 9.2* section provides a block diagram of the basic band-gap topology and the two buffers used to derive the V_{REF} and V_{BIAS} outputs. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base emitter voltages (V_{BE1} – V_{BE2}) has a positive temperature coefficient and is forced across resistor R_5. The voltage is amplified and added to the base emitter voltage of Q_2, which has a negative temperature coefficient. The resulting band-gap output voltage is almost independent of temperature. Two independent buffers are used to generate V_{REF} and V_{BIAS} from the band-gap voltage. The resistors R_1, R_2 and R_3, R_4 are sized such that V_{BIAS} = V_{REF} / 2.

e-Trim™ is a method of package-level trim for the initial accuracy and temperature coefficient of V_{REF} and V_{BIAS}, implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent transistor mismatch, as well as errors induced during package molding. e-Trim is implemented in the REF20xx to minimize the temperature drift and maximize the initial accuracy of both the V_{REF} and V_{BIAS} outputs.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 V_{REF} and V_{BIAS} Tracking

Most single-supply systems require an additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The V_{REF} and V_{BIAS} outputs of the REF20xx are generated from the same band-gap voltage as shown in the *セクション 9.2* section. Hence, both outputs track each other over the full temperature range of –40°C to 125°C with an accuracy of 7 ppm/°C (maximum). The tracking accuracy increases to 6 ppm/°C (maximum) when the temperature range is limited to –40°C to 85°C. The tracking error is calculated using the box method, as described by *式 2*:

$$\text{Tracking Error} = \left(\frac{V_{DIFF(MAX)} - V_{DIFF\ (MIN)}}{V_{REF} \bullet \text{Temperature Range}} \right) \bullet 10^6 \quad \text{(ppm)} \tag{2}$$

where

- $V_{DIFF} = V_{REF} - 2 \bullet V_{BIAS}$

The tracking accuracy is as shown in 図 9-1.

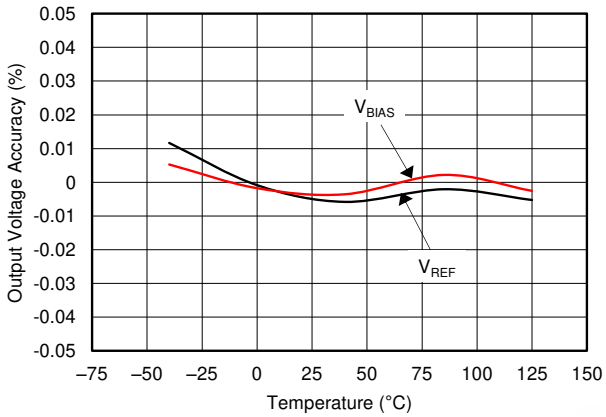


図 9-1. V_{REF} and V_{BIAS} Tracking vs Temperature

9.3.2 Low Temperature Drift

The REF20xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by 式 3:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \bullet \text{Temperature Range}} \right) \bullet 10^6 \quad \text{(ppm)} \tag{3}$$

9.3.3 Load Current

The REF20xx family is specified to deliver a current load of ±20 mA per output. Both the V_{REF} and V_{BIAS} outputs of the device are protected from short circuits by limiting the output short-circuit current to 50 mA. The device temperature increases according to 式 4:

$$T_J = T_A + P_D \bullet R_{\theta JA} \tag{4}$$

where

- T_J = junction temperature (°C),
- T_A = ambient temperature (°C),
- P_D = power dissipated (W), and
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The REF20xx maximum junction temperature must not exceed the absolute maximum rating of 150°C.

9.4 Device Functional Modes

When the EN pin of the REF20xx is pulled high, the device is in active mode. The device should be in active mode for normal operation. The REF20xx can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 5 µA in shutdown mode. See the *セクション 7.5* for logic high and logic low voltage levels.

10 Applications and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The low-drift, bidirectional, single-supply, low-side, current-sensing solution, described in this section, can accurately detect load currents from –2.5 A to 2.5 A. The linear range of the output is from 250 mV to 2.75 V. Positive current is represented by output voltages from 1.5 V to 2.75 V, whereas negative current is represented by output voltages from 250 mV to 1.5 V. The difference amplifier is the INA213 current-shunt monitor, whose supply and reference voltages are supplied by the low-drift REF2030.

Industrial applications with electronics in corrosive environments are susceptible to corrosive damage due to the exposure to heat, moisture, and corrosive gases. The combination of the following conditions in a given system lead to higher risk of corrosive damage:

1. Ventilated enclosures exposing underlying PCB.
2. PCBs not conformally coated.
3. Exposed-lead components with plating susceptible to corrosion.
4. Changes in plating techniques for RoHS compliance (e.g. removal of Pb (lead) and certain types of plating).

To improve resistance to corrosion in harsh environments, the REF2025AISDDCR uses Matte-Sn plating with improved assembly process to reduce exposed Cu, leading to improved corrosion resistance in the Battelle Class III and similar harsh environments. The “S” in the part number identifies this special plating option. REF2025 versions that do not have the “S” will continue to be available in industry standard NiPdAu processing technique.

10.2 Typical Application

10.2.1 Low-Side, Current-Sensing Application

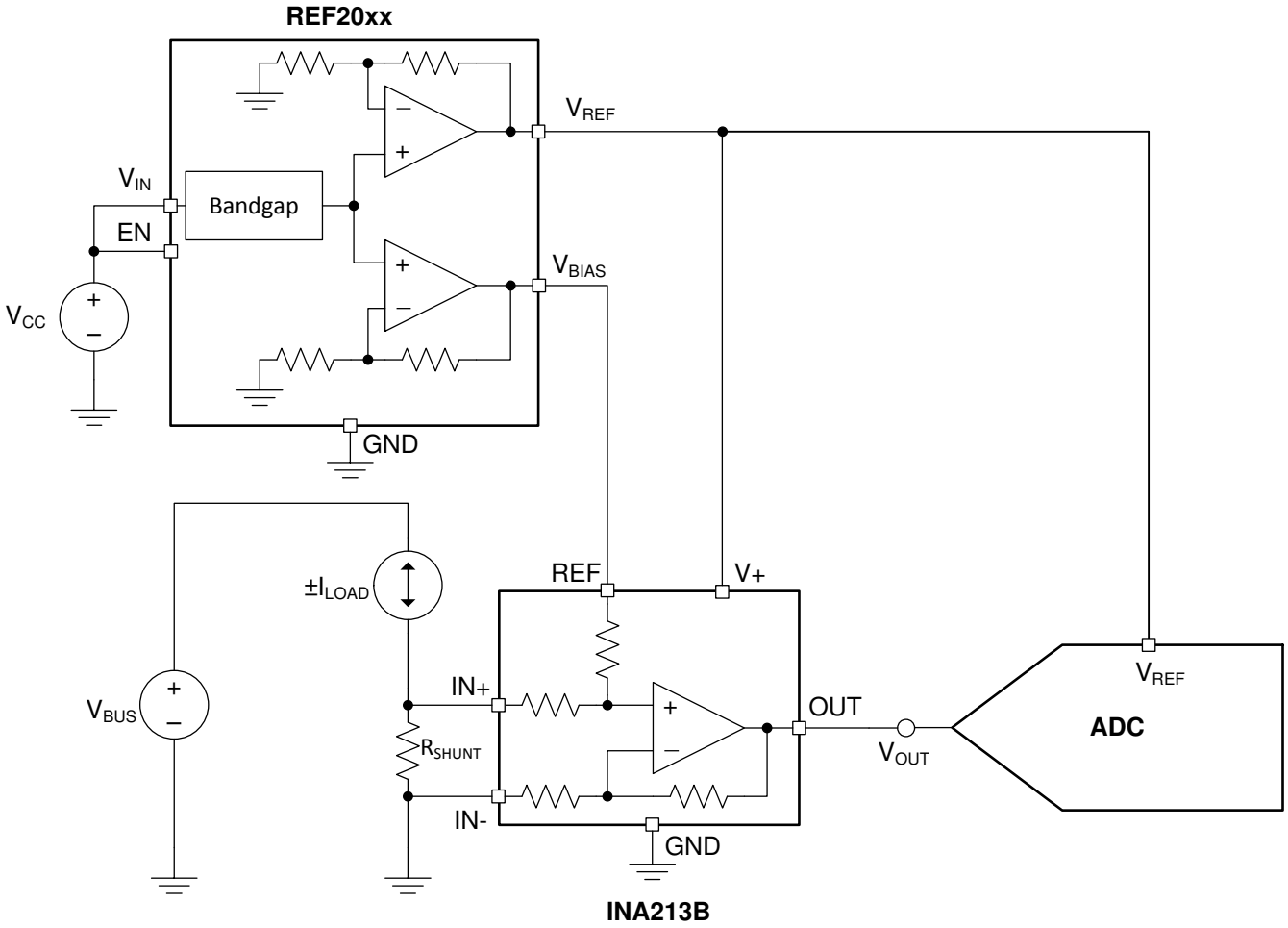


図 10-1. Low-Side, Current-Sensing Application

10.2.1.1 Design Requirements

The design requirements are as follows:

1. Supply voltage: 5.0 V
2. Load current: ±2.5 A
3. Output: 250 mV to 2.75 V
4. Maximum shunt voltage: ±25 mV

10.2.1.2 Detailed Design Procedure

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore, the current-sensing solution is independent of the bus voltage, V_{BUS}. When sensing bidirectional currents, use a differential amplifier with a reference pin. This procedure allows for the differentiation between positive and negative currents by biasing the output stage such that it can respond to negative input voltages. There are a variety of methods for supplying power (V+) and the reference voltage (V_{REF}, or V_{BIAS}) to the differential amplifier. For a low-drift solution, use a monolithic reference that supplies both power and the reference voltage. 図 10-2 shows the general circuit topology for a low-drift, low-side, bidirectional, current-sensing solution. This topology is particularly useful when interfacing with an ADC; see 図 10-1. Not only do V_{REF} and V_{BIAS} track over temperature, but their matching is much better than alternate topologies. For a more detailed version of the design procedure, refer to TIDU357.

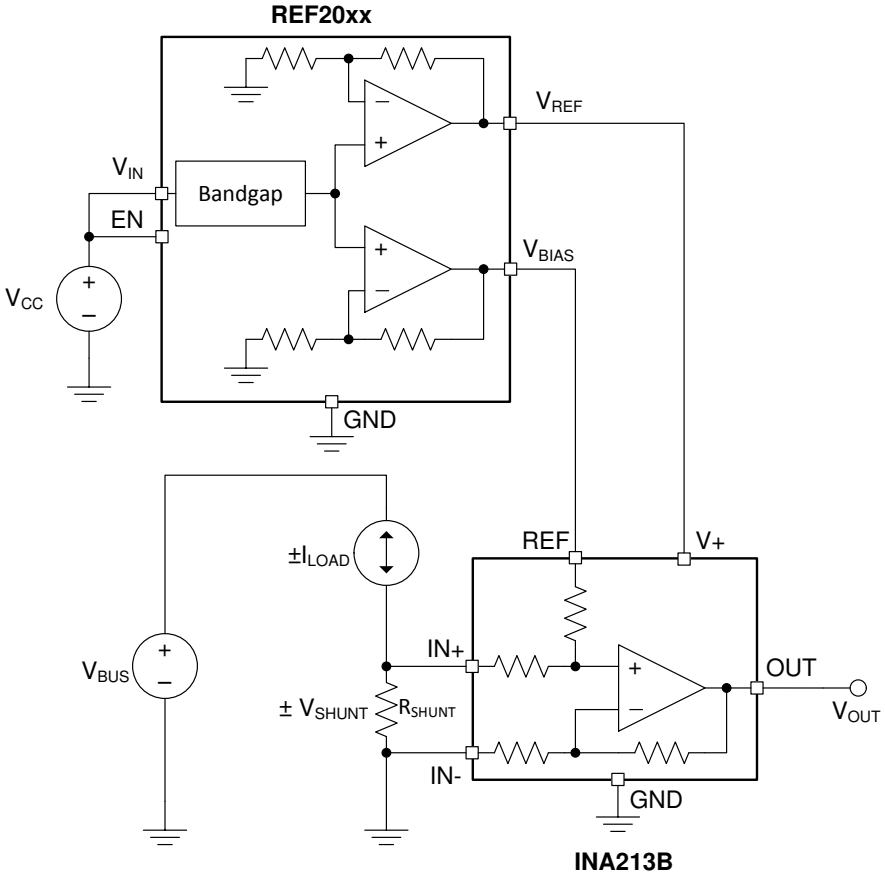


図 10-2. Low-Drift, Low-side, Bidirectional, Current-Sensing Circuit Topology

The transfer function for the circuit given in 図 10-2 is as shown in 式 5:

$$V_{OUT} = G \bullet (\pm V_{SHUNT}) + V_{BIAS}$$
$$= G \bullet (\pm I_{LOAD} \bullet R_{SHUNT}) + V_{BIAS} \quad (5)$$

10.2.1.2.1 Shunt Resistor

As illustrated in 図 10-2, the value of V_{SHUNT} is the ground potential for the system load. If the value of V_{SHUNT} is too large, issues may arise when interfacing with systems whose ground potential is actually 0 V. Also, a value of V_{SHUNT} that is too negative may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore, limiting the voltage across the shunt resistor is important. 式 6 can be used to calculate the maximum value of R_{SHUNT}.

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} \tag{6}$$

Given that the maximum shunt voltage is ±25 mV and the load current range is ±2.5 A, the maximum shunt resistance is calculated as shown in 式 7.

$$R_{SHUNT\,(max)} = \frac{V_{SHUNT\,(max)}}{I_{LOAD\,(max)}} = \frac{25mV}{2.5A} = 10m\Omega \tag{7}$$

To minimize errors over temperature, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. For this design, the Y14870R01000B9W resistor is used.

10.2.1.2.2 Differential Amplifier

The differential amplifier used for this design should have the following features:

1. Single-supply (3 V),
2. Reference voltage input,
3. Low initial input offset voltage (V_{OS}),
4. Low-drift,
5. Fixed gain, and
6. Low-side sensing (input common-mode range below ground).

For this design, a current-shunt monitor (INA213) is used. The INA21x family topology is shown in 図 10-3. The INA213B specifications can be found in the INA213 product data sheet.

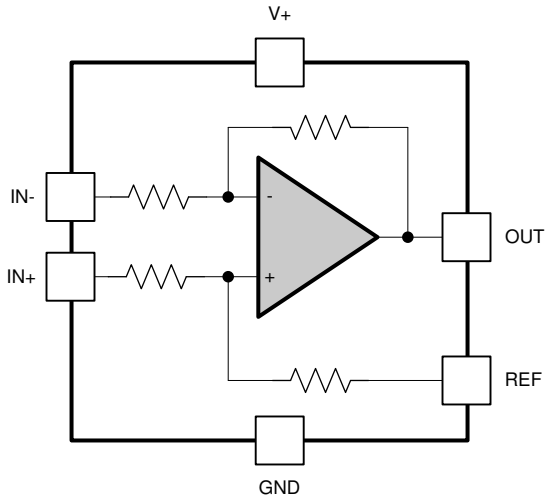


図 10-3. INA21x Current-Shunt Monitor Topology

The INA213B is an excellent choice for this application because all the required features are included. In general, instrumentation amplifiers (INAs) do not have the input common-mode swing to ground that is essential for this application. In addition, INAs require external resistors to set their gain, which is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce solution accuracy at

small load currents. Difference amplifiers typically have a gain of 1 V/V. When the gain is adjustable, these amplifiers use external resistors that are not conducive to low-drift applications.

10.2.1.2.3 Voltage Reference

The voltage reference for this application should have the following features:

1. Dual output (3.0 V and 1.5 V),
2. Low drift, and
3. Low tracking errors between the two outputs.

For this design, the REF2030 is used. The REF20xx topology is as shown in the *セクション 9.2* section.

The REF2030 is an excellent choice for this application because of its dual output. The temperature drift of 8 ppm/°C and initial accuracy of 0.05% make the errors resulting from the voltage reference minimal in this application. In addition, there is minimal mismatch between the two outputs and both outputs track very well across temperature, as shown in 図 10-4 and 図 10-5.

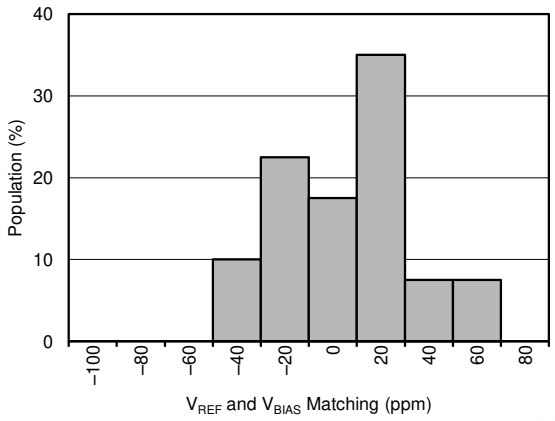


図 10-4. V_{REF} – 2 × V_{BIAS} Distribution (At T_A = 25°C)

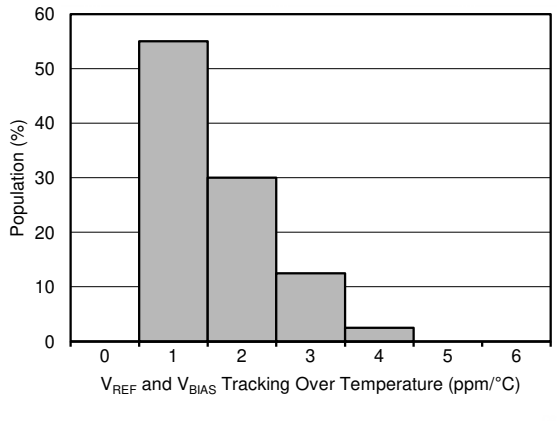


図 10-5. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature

10.2.1.2.4 Results

表 10-1 summarizes the measured results.

表 10-1. Measured Results

ERROR	UNCALIBRATED (%)	CALIBRATED (%)
Error across the full load current range (25°C)	±0.0355	±0.004
Error across the full load current range (–40°C to 125°C)	±0.0522	±0.0606

10.2.1.3 Application Curves

Performing a two-point calibration at 25°C removes the errors associated with offset voltage, gain error, and so forth. 図 10-6 to 図 10-8 show the measured error at different conditions. For a more detailed description on measurement procedure, calibration, and calculations, please refer to TIDU357.

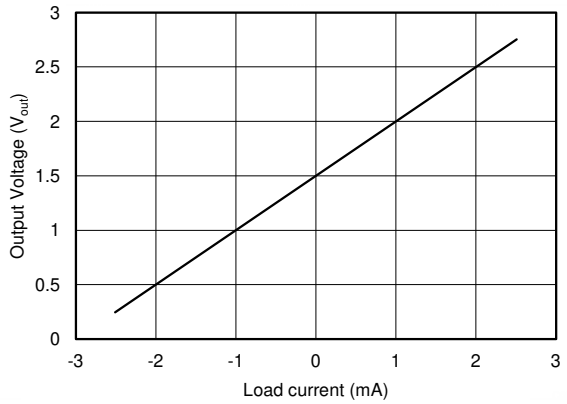


図 10-6. Measured Transfer Function

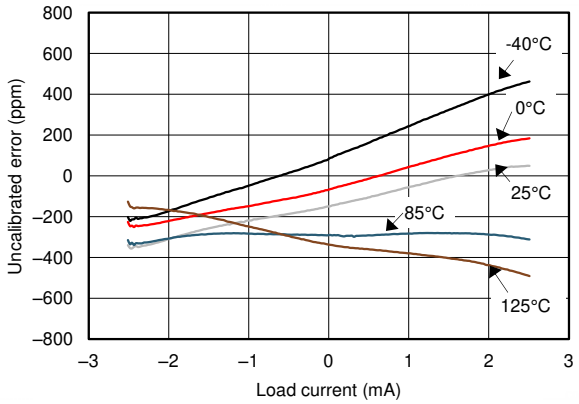


図 10-7. Uncalibrated Error vs Load Current

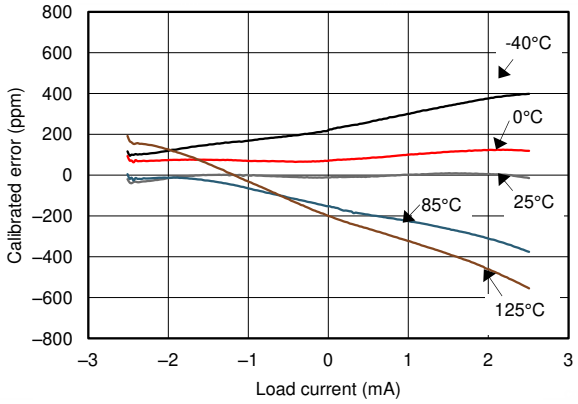


図 10-8. Calibrated Error vs Load Current

11 Power-Supply Recommendations

The REF20xx family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 20 mV above the output voltage. For loaded reference conditions, a typical dropout voltage versus load is shown in 図 11-1. A supply bypass capacitor ranging between 0.1 µF to 10 µF is recommended.

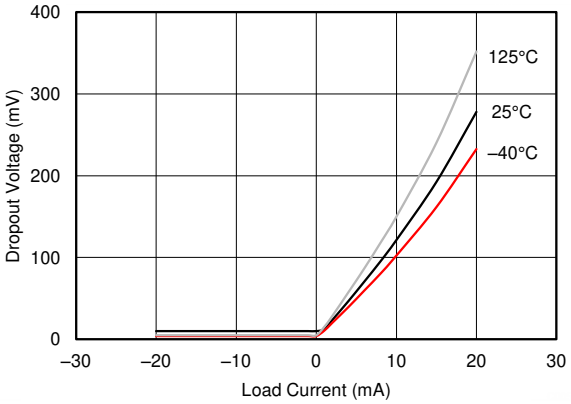


図 11-1. Dropout Voltage vs Load Current

12 Layout

12.1 Layout Guidelines

図 12-1 shows an example of a PCB layout for a data acquisition system using the REF2030. Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at V_{IN}, V_{REF}, and V_{BIAS} of the REF2030.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

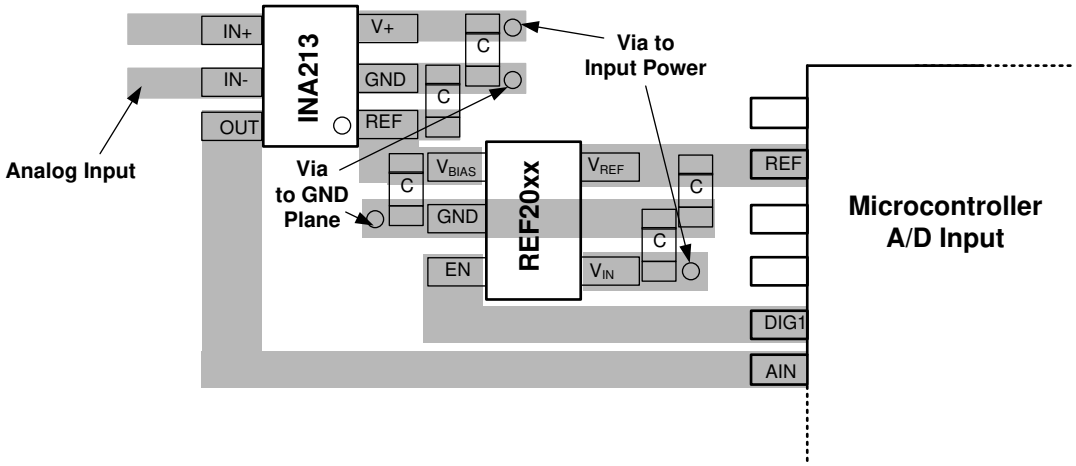


図 12-1. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors* (SBOS437)
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design* (TIDU357)

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF2025AIDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AIDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AIDDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AIDDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AIDDCTG4.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AISDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	1M98
REF2025AISDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	1M98
REF2030AIDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2030AIDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2030AIDDCRG4.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2030AIDDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2030AIDDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2033AIDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM
REF2033AIDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM
REF2033AIDDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM
REF2033AIDDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF2033AIDDCTG4.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM
REF2041AIDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM
REF2041AIDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM
REF2041AIDDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM
REF2041AIDDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM
REF2041AIDDCTG4.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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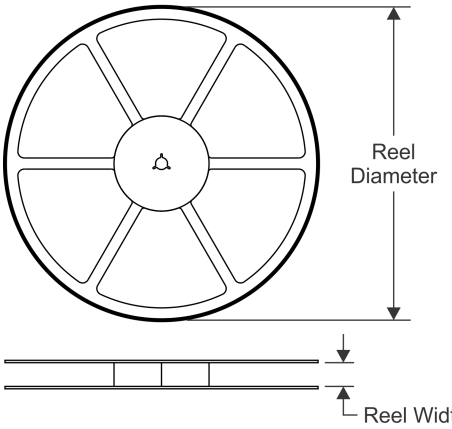
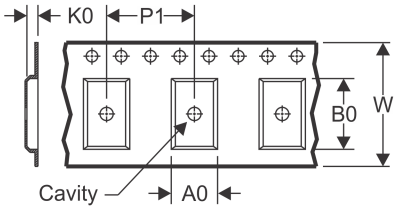
TAPE AND REEL INFORMATION

REEL DIMENSIONS

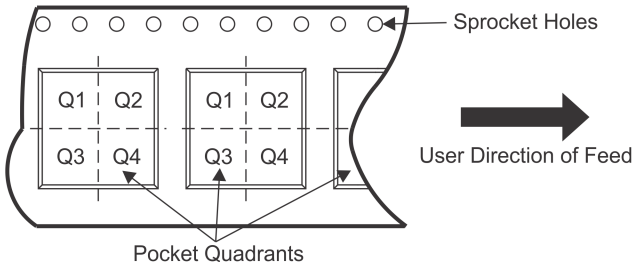


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

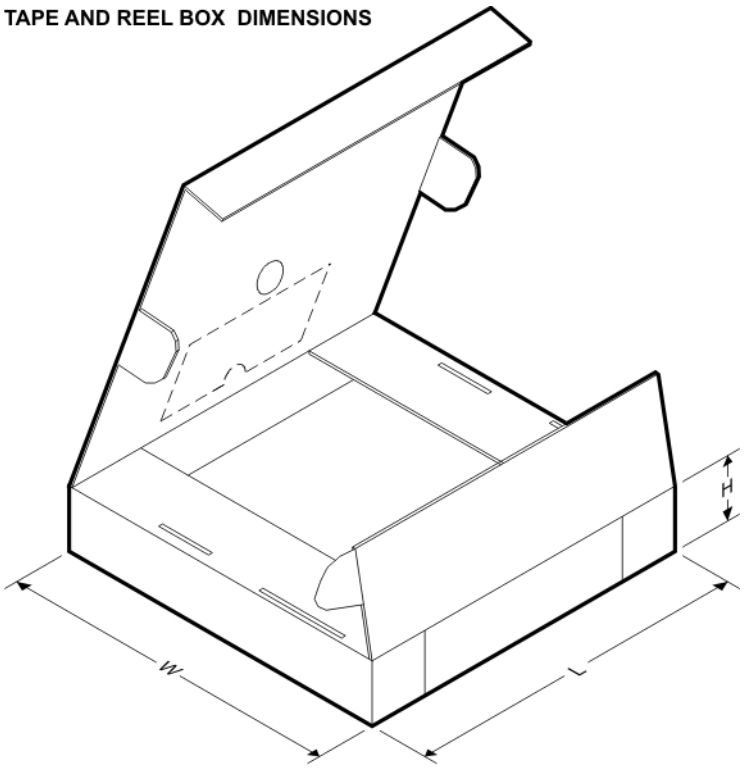
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

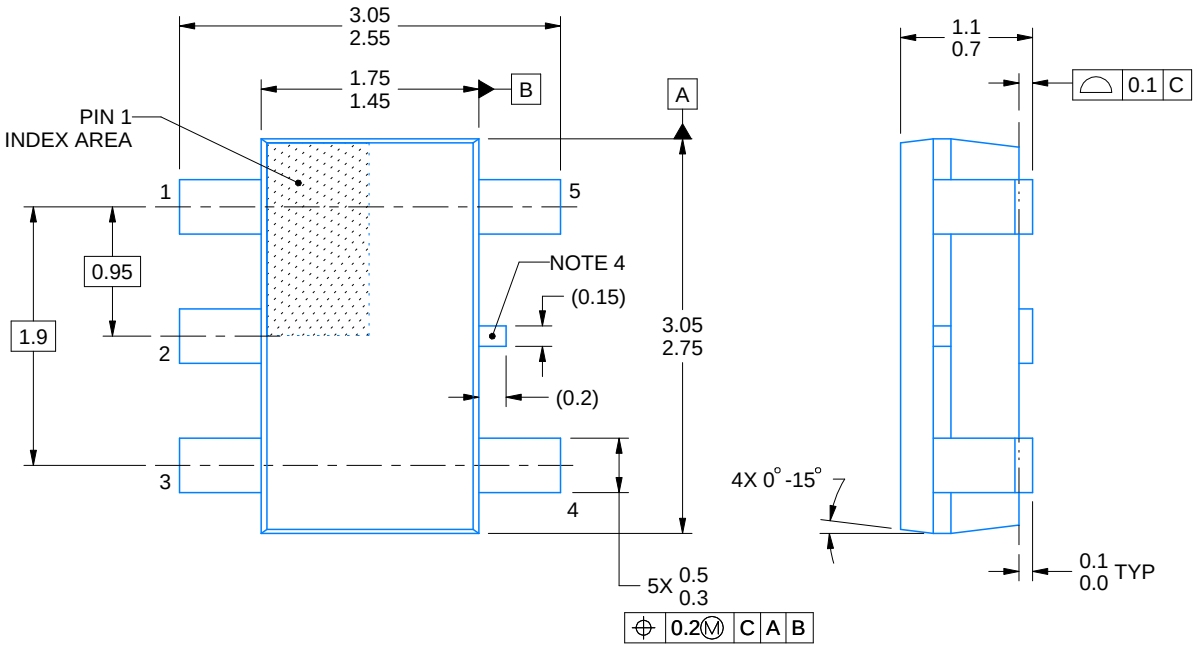
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0

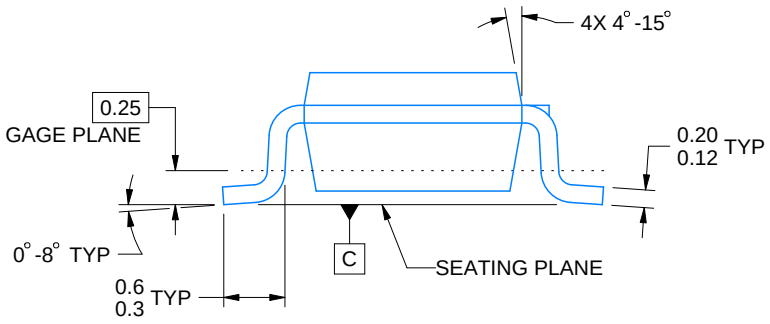
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR





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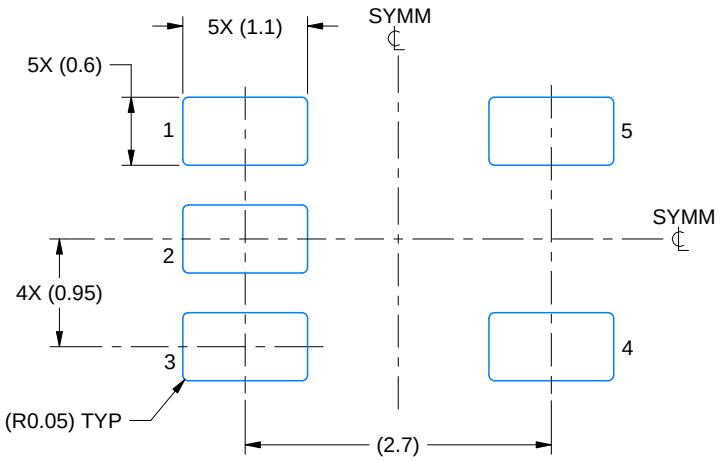
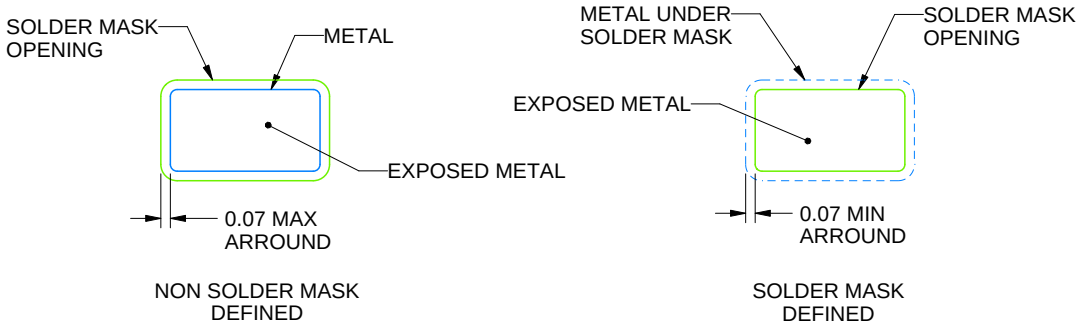
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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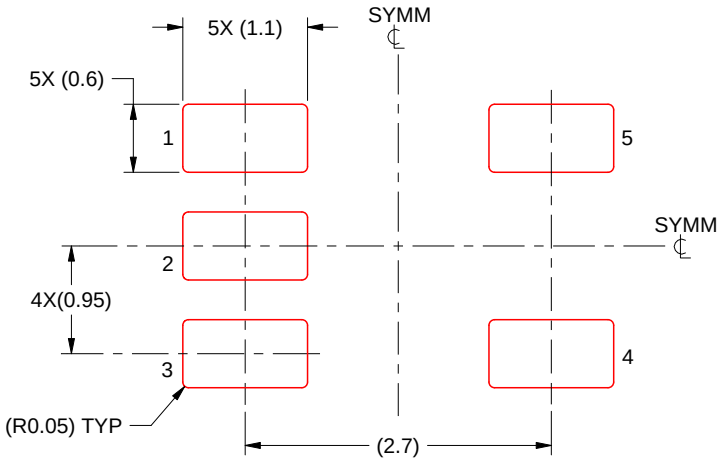
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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