

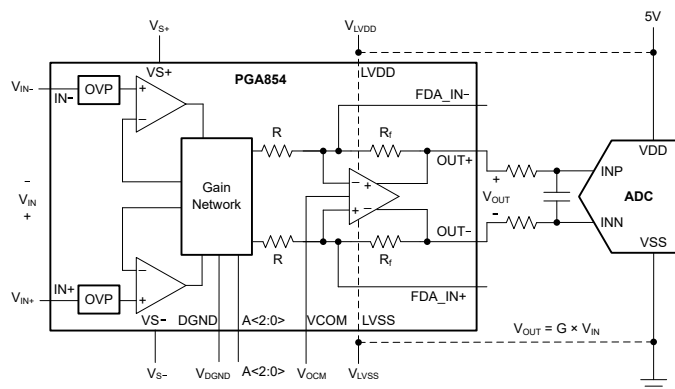
# PGA854 Low-Noise, Wide-Bandwidth, Decade Gain, Precision Programmable Gain Instrumentation Amplifier

## 1 Features

- Eight pin-programmable decade (scope) gains
  - $G (V/V) = \frac{1}{2}, 1, 2, 5, 10, 20, 50,$  and  $100$
- Fully differential outputs
- Output common-mode control
- Low gain error drift:  $\pm 2 \text{ppm}/^\circ\text{C}$  (maximum)
- Faster signal processing:
  - Wide bandwidth:  $6.2 \text{MHz}$  ( $G < 10$ ),  $2.4 \text{MHz}$  ( $G = 50, 100$ )
  - High slew rate:  $45 \text{V}/\mu\text{s}$  at all gains
  - Settling time:  $750 \text{ns}$  to  $0.01\%$  ( $G < 20$ )
  - Input stage noise:  $8.8 \text{nV}/\sqrt{\text{Hz}}$  at  $G > 10 \text{V/V}$
  - Filter option to achieve better SNR
- Input overvoltage protection to  $\pm 40 \text{V}$  beyond supplies
- Input-stage supply range:
  - Single supply:  $9 \text{V}$  to  $36 \text{V}$
  - Dual supply:  $\pm 4.5 \text{V}$  to  $\pm 18 \text{V}$
- Independent output power-supply pins
- Output-stage supply range:
  - Single supply:  $4.5 \text{V}$  to  $36 \text{V}$
  - Dual supply:  $\pm 2.25 \text{V}$  to  $\pm 18 \text{V}$
- Specified temperature range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Small package:  $3 \text{mm} \times 3 \text{mm}$  VQFN

## 2 Applications

- [Factory automation and control](#)
- [Analog input module](#)
- [Data acquisition \(DAQ\)](#)
- [Test and measurement](#)
- [Parametric measurement unit \(PMU\)](#)



PGA854 Simplified Application

## 3 Description

The PGA854 is a wide-bandwidth, high-voltage, low-noise programmable gain instrumentation amplifier with differential output. The PGA854 is equipped with eight decade (scope) gain settings, from an attenuating gain of  $0.5 \text{V/V}$  to a maximum of  $100 \text{V/V}$ . Gain is set using three digital gain selection pins.

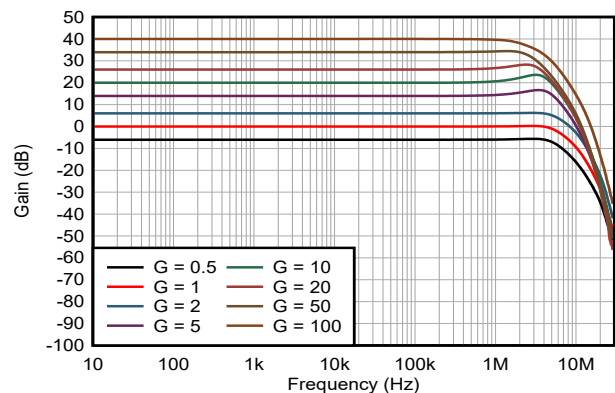
The PGA854 architecture is optimized to drive inputs of high-resolution, precision analog-to-digital converters (ADCs) with sampling rates up to  $1 \text{MSPS}$  without the need for an additional ADC driver. The output-stage power supplies are decoupled from the input stage to protect the ADC or downstream devices against overdrive damage.

The super-beta input transistors offer an impressively low input bias current, which in turn provides a very low input current noise density of  $0.3 \text{pA}/\sqrt{\text{Hz}}$ , making the PGA854 a versatile choice for virtually any sensor type. The low-noise current-feedback front-end architecture offers exceptional gain flatness even at high frequencies, making the PGA854 an excellent high-impedance sensor readout device. Integrated protection circuitry on the input pins handles overvoltages of up to  $\pm 40 \text{V}$  beyond the power-supply voltages.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
PGA854	RGT (VQFN, 16)	$3 \text{mm} \times 3 \text{mm}$

- (1) For more information, see [Section 11](#).
- (2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



Gain vs Frequency



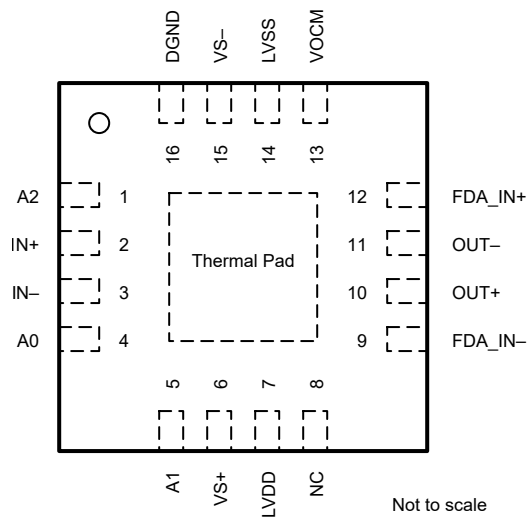
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## 4 Device Comparison Table

DEVICE	OUTPUT TYPE	GAIN (V/V)	BANDWIDTH (MHz)	SLEW RATE (V/ $\mu$ s)	NOISE (nV/ $\sqrt{\text{Hz}}$ )
<a href="#">PGA849</a>	Single-ended	$\frac{1}{8}, \frac{1}{4}, \frac{1}{2}, 1, 2, 4, 8, 16$	10	35	8.6
<a href="#">INA849</a>	Single-ended	$G = 1 + 6\text{k}\Omega / R_G$	28	35	1
<a href="#">PGA848</a>	Single-ended	$\frac{1}{2}, 1, 2, 5, 10, 20, 50, 100$	6.2	43	8.5
<a href="#">PGA854</a>	Differential	$\frac{1}{2}, 1, 2, 5, 10, 20, 50, 100$	6.2	45	8.8
<a href="#">PGA855</a>	Differential	$\frac{1}{8}, \frac{1}{4}, \frac{1}{2}, 1, 2, 4, 8, 16$	10	35	7.8
<a href="#">INA851</a>	Differential	$G = 1 + 6\text{k}\Omega / R_G$	22	37	3.2
<a href="#">INA821</a>	Single-ended	$G = 1 + 49.4\text{k}\Omega / R_G$	4.7	2	7
<a href="#">INA819</a>	Single-ended	$G = 1 + 50\text{k}\Omega / R_G$	2	0.9	8

## 5 Pin Configuration and Functions



**Figure 5-1. RGT Package, 16-Pin VQFN (Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	4	Input	Gain setting pin 0
A1	5	Input	Gain setting pin 1
A2	1	Input	Gain setting pin 2
DGND	16	Power	Ground reference for digital logic and gain setting pins
FDA_IN-	9	Input	Connection to output driver summing node
FDA_IN+	12	Input	Connection to output driver summing node
IN-	3	Input	Negative (inverting) input
IN+	2	Input	Positive (noninverting) input
LVDD	7	Power	Output driver positive supply. Connect this pin to the positive supply of the ADC to protect from overdriving.
LVSS	14	Power	Output driver negative supply. Connect this pin to the negative supply of the ADC to protect from overdriving.
NC	8	—	Do not connect
OUT-	11	Output	Output (inverting)
OUT+	10	Output	Output (noninverting)
VOCM	13	Input	output common mode control pin
VS+	6	Power	Input stage positive supply
VS-	15	Power	Input stage negative supply
Thermal Pad	Thermal pad	—	Solder the thermal pad to the printed-circuit board (PCB). Connect the thermal pad to a plane or large copper pour that is either floating or electrically connected to VS-. Make this connection even for applications that have low power dissipation.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage on VS+, VS– pins; V <sub>S</sub> = (V <sub>S+</sub> ) – (V <sub>S–</sub> )	0	40	V
V <sub>SOUT</sub>	Supply voltage on LVDD, LVSS pins; V <sub>SOUT</sub> = V <sub>LVDD</sub> – V <sub>LVSS</sub>	0	40	V
	Voltage on power pins LVDD, LVSS	(V <sub>S–</sub> ) – 0.5	(V <sub>S+</sub> ) + 0.5	V
	Voltage on signal-input pins IN+, IN–	(V <sub>S–</sub> ) – 40	(V <sub>S+</sub> ) + 40	V
	Voltage on pins DGND, FDA_IN+, FDA_IN–	(V <sub>S–</sub> ) – 0.5	(V <sub>S+</sub> ) + 0.5	V
	Voltage on gain-select pins A2, A1, A0	V <sub>DGND</sub> – 0.5	(V <sub>S+</sub> ) + 0.5	V
V <sub>O</sub>	Voltage on output pins OUT+, OUT–	V <sub>LVSS</sub> – 0.5	V <sub>LVDD</sub> + 0.5	V
V <sub>OCM</sub>	Output common-mode control voltage	V <sub>LVSS</sub> – 0.5	V <sub>LVDD</sub> + 0.5	V
I <sub>O</sub>	Output pins OUT+, OUT– current	–100	100	mA
I <sub>SC</sub>	Output short-circuit current <sup>(2)</sup>	Continuous		
T <sub>A</sub>	Operating temperature	–50	150	°C
T <sub>J</sub>	Junction temperature		175	°C
T <sub>stg</sub>	Storage temperature	–65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to V<sub>SOUT</sub> / 2.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>S</sub>	Input stage supply voltage	Single supply	9	36	V
		Dual supply	±4.5	±18	
V <sub>SOUT</sub>	Output stage supply voltage	Single supply	4.5	36	V
		Dual supply	±2.25	±18	
T <sub>A</sub>	Specified temperature		–40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		PGA854	UNIT
		RGT (VQFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM}$  at mid-supply,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>INPUT</b>							
$V_{OS}$	Differential offset voltage (RTI)	G = 5 to 100			±50	±300	μV
		G = 0.5, 1, 2			±100 / G	±700 / G	
	Differential offset voltage drift (RTI)	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	G > 1		±0.1	±1.0	μV/°C
			G = 0.5, 1		±0.2	±2.0	
PSRR	Power-supply rejection ratio	$\pm 4.5\text{V} \leq V_S \leq \pm 18\text{V}$ , RTI	G = 0.5	108	124	dB	
			G = 1	114	128		
			G = 2	118	130		
			G ≥ 5	120	134		
$Z_{id}$	Differential input impedance	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		100    1		GΩ    pF	
$Z_{ic}$	Common-mode input impedance			100    4.4			
$V_{ICM}$	Common-mode input voltage	$V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$(V_{S-}) + 3$		$(V_{S+}) - 3$	V
$V_{IN}$	Differential input voltage <sup>(1)</sup>			-16		+16	V
CMRR	Common-mode rejection ratio	At dc to 60Hz, $V_{ICM} = \pm 10\text{V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , RTI	G = 0.5	69	82	dB	
			G = 1	75	88		
			G = 2	80	94		
			G = 5	88	100		
			G = 10	95	106		
			G = 20	100	112		
			G = 50	108	116		
			G = 100	116	124		
<b>BIAS CURRENT</b>							
$I_B$	Input bias current			±0.5		±2	nA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			±1	±3.6	
	Input bias current drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$				±5	pA/°C
$I_{OS}$	Input offset current			±0.5		±1	nA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			±1	±2	
	Input offset current drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$				±5	pA/°C

## 6.5 Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = V_{\text{OCM}}$  at mid-supply,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>NOISE VOLTAGE</b>							
$e_{\text{NI}}$	Voltage noise density (RTI)	$f = 1\text{kHz}$	$G = 100$		8.5		$\text{nV}/\sqrt{\text{Hz}}$
			$G = 50$		8.5		
			$G = 20$		8.8		
			$G = 10$		8.8		
			$G = 5$		10.5		
			$G = 2$		20		
			$G = 1$		40		
			$G = 0.5$		80		
$E_{\text{NI}}$	Voltage noise (RTI)	$f_B = 0.1\text{Hz to } 10\text{Hz}$	$G = 100$		0.28		$\mu\text{V}_{\text{PP}}$
			$G = 50$		0.28		
			$G = 20$		0.30		
			$G = 10$		0.30		
			$G = 5$		0.30		
			$G = 2$		0.41		
			$G = 1$		0.76		
			$G = 0.5$		1.50		
$i_{\text{N}}$	Input current noise density	$f = 1\text{kHz}$			0.2		$\text{pA}/\sqrt{\text{Hz}}$
$I_{\text{N}}$	Input current noise	$f_B = 0.1\text{Hz to } 10\text{Hz}$			7.9		$\text{pA}_{\text{PP}}$
<b>GAIN</b>							
$G$	Differential gain			0.5		100	V/V
$G_E$	Differential gain error	$G = 0.5, 1, 2$			$\pm 0.005$	$\pm 0.035$	%
		$G = 5, 10, 20, 50$			$\pm 0.015$	$\pm 0.045$	
		$G = 100$			$\pm 0.025$	$\pm 0.055$	
	Differential gain drift	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	$G = 2$		$\pm 0.05$	$\pm 1$	$\text{ppm}/^\circ\text{C}$
			$G \neq 2$		$\pm 0.2$	$\pm 2$	
	Differential gain nonlinearity	$G = 0.5, V_{\text{OUT}} = 8\text{V}$ $G = 1 \text{ to } 20, V_{\text{OUT}} = 10\text{V}$			$\pm 4$	$\pm 5.5$	ppm
			$G = 50, 100, V_{\text{OUT}} = 10\text{V}$			$\pm 9$	
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$ , $G = 0.5, V_{\text{OUT}} = 8\text{V}$ $G = 1 \text{ to } 100, V_{\text{OUT}} = 10\text{V}$	$G \leq 20$		$\pm 5$	$\pm 7$	
			$G = 50, 100$		$\pm 12$	$\pm 30$	
<b>OUTPUT</b>							
$V_{\text{O}}$	Single-ended output voltage	No load, $V_{\text{SOUT}} = \pm 2.25\text{V}$  $R_L = 10\text{k}\Omega$		$V_{\text{LVSS}} + 0.1$		$V_{\text{LVDD}} - 0.1$	V
			$V_{\text{SOUT}} = \pm 2.25\text{V}$	$V_{\text{LVSS}} + 0.2$		$V_{\text{LVDD}} - 0.2$	
			$V_{\text{SOUT}} = \pm 18\text{V}$	$V_{\text{LVSS}} + 0.4$		$V_{\text{LVDD}} - 0.4$	
$V_{\text{OUT}}$	Differential output voltage	$V_{\text{ICM}}$ and $V_{\text{IN}}$ in valid linear operating range <sup>(2)</sup>			$G \times V_{\text{IN}}$		V
$C_L$	Differential load capacitance	Stable operation for differential load			50		pF
$I_{\text{SC}}$	Short-circuit current	Continuous to $V_{\text{SOUT}} / 2$			$\pm 45$		mA
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	$\pm 20$		$\pm 60$	

## 6.5 Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = V_{\text{OCM}}$  at mid-supply,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>FREQUENCY RESPONSE</b>							
BW	Bandwidth, $-3\text{dB}$	$G < 10$		6.2		MHz	
		$G = 10, 20$		5.0			
		$G = 50, 100$		2.4			
SR	Slew rate	$G = 0.5$ , $V_{\text{OUT}} = 8\text{V}$ $G = 1$ to $100$ , $V_{\text{OUT}} = 10\text{V}$		45		$\text{V}/\mu\text{s}$	
$t_s$	Settling time	$G = 0.5$ , $V_{\text{IN}} = 10\text{V}$ step or $G = 1$ to $20$ , $V_{\text{OUT}} = 10\text{V}$ step	To 0.01%	0.75		$\mu\text{s}$	
			To 0.0015%	0.9		$\mu\text{s}$	
		$G = 50$ $V_{\text{OUT}} = 10\text{V}$ step	To 0.01%	1.3		$\mu\text{s}$	
			To 0.0015%	1.4		$\mu\text{s}$	
		$G = 100$ $V_{\text{OUT}} = 10\text{V}$ step	To 0.01%	2		$\mu\text{s}$	
		To 0.0015%	2.3		$\mu\text{s}$		
	Gain switching time			1.5		$\mu\text{s}$	
THD+N	Total harmonic distortion and Noise	Differential input, $f = 10\text{kHz}$ , $V_{\text{OUT}} = 10\text{V}_{\text{PP}}$		-99		dB	
		Single-ended input, $f = 10\text{kHz}$ , $V_{\text{OUT}} = 10\text{V}_{\text{PP}}$		-93			
HD2	Second-order harmonic distortion	Differential input, $f = 10\text{kHz}$ , $V_{\text{OUT}} = 10\text{V}_{\text{PP}}$		-121		dB	
		Single-ended input, $f = 10\text{kHz}$ , $V_{\text{OUT}} = 10\text{V}_{\text{PP}}$		-112			
HD3	Third-order harmonic distortion	Differential input, $f = 10\text{kHz}$ , $V_{\text{OUT}} = 10\text{V}_{\text{PP}}$		-105		dB	
		Single-ended input, $f = 10\text{kHz}$ , $V_{\text{OUT}} = 10\text{V}_{\text{PP}}$		-104			
<b>OUTPUT COMMON-MODE VOLTAGE (<math>V_{\text{OCM}}</math>) CONTROL</b>							
$V_{\text{OCM}}$	Output common-mode control voltage <sup>(3)</sup>	$V_S = \pm 4.5\text{V}$		$V_{\text{LVSS}} + 1.5$	$V_{\text{LVDD}} - 1.5$	V	
		$V_S = \pm 18\text{V}$		$V_{\text{LVSS}} + 2$	$V_{\text{LVDD}} - 2$		
	Small-signal bandwidth V <sub>OCM</sub> pin	$V_{\text{OCM}} = 100\text{mV}_{\text{PP}}$		14		MHz	
	Large-signal bandwidth V <sub>OCM</sub> pin	$V_{\text{OCM}} = 0.6\text{V}_{\text{PP}}$		14		MHz	
	DC output balance <sup>(4)</sup>	$V_{\text{OCM}}$ fixed at mid-supply ( $V_{\text{OUT}} = \pm 1\text{V}$ )		95		dB	
	Input impedance V <sub>OCM</sub> pin			250    1		$\text{k}\Omega$    $\text{pF}$	
	$V_{\text{OUTCM}}$ offset from mid-supply	V <sub>OCM</sub> pin floating		$\pm 1$	$\pm 4.5$	mV	
	$V_{\text{OUTCM}}$ offset voltage <sup>(5)</sup>	$V_{\text{OCM}} = V_{\text{ICM}}$ , $V_{\text{OUT}} = 0\text{V}$		$\pm 1$	$\pm 4.5$	mV	
	$V_{\text{OUTCM}}$ offset voltage drift	$V_{\text{OCM}} = V_{\text{ICM}}$ , $V_{\text{OUT}} = 0\text{V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 20$	$\pm 40$	$\mu\text{V}/^\circ\text{C}$	
<b>INPUT STAGE POWER SUPPLY</b>							
$I_{\text{Q\_input}}$	Input stage quiescent current $V_{\text{S+}}$ , $V_{\text{S-}}$	$V_{\text{IN}} = 0\text{V}$ , $V_{\text{ICM}} = 0\text{V}$		3.2		3.9	mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	4.9			
<b>OUTPUT STAGE POWER SUPPLY</b>							
$I_{\text{Q\_output}}$	Output stage quiescent current LVDD, LVSS	$V_{\text{IN}} = 0\text{V}$ , $V_{\text{OCM}}$ fixed at mid-supply		2.3		2.8	mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	3.5			
<b>DIGITAL LOGIC</b>							
$V_{\text{IL}}$	Digital input logic low	A0, A1, A2 pins, referred to DGND		$V_{\text{DGND}}$	$V_{\text{DGND}} + 0.8$	V	
$V_{\text{IH}}$	Digital input logic high	A0, A1, A2 pins, referred to DGND		$V_{\text{DGND}} + 1.8$	$V_{\text{S+}}$	V	
	Digital input pin current	A0, A1, A2 pins		1.5		3	$\mu\text{A}$
$V_{\text{DGND}}$	DGND voltage			$V_{\text{S-}}$	$(V_{\text{S+}}) - 4$	V	
	DGND reference current			4		10	$\mu\text{A}$

- (1) Differential Input voltage of the PGA854 amplifier ( $V_{\text{IN}} = V_{\text{IN+}} - V_{\text{IN-}}$ ). The valid input range depends on input common-mode voltage  $V_{\text{ICM}}$ , gain  $G$ , and output common-mode voltage  $V_{\text{OCM}}$ . See [Section 8.1.1](#).
- (2) Differential output voltage  $V_{\text{OUT}} = V_{\text{OUT+}} - V_{\text{OUT-}}$ . See [Section 8.1.1](#) for valid linear operating range of the amplifier.
- (3)  $V_{\text{OCM}}$  is the Voltage on V<sub>OCM</sub> pin. Actual output common-mode voltage is calculated from single-ended output voltages  $V_{\text{OUTCM}} = (V_{\text{OUT+}} + V_{\text{OUT-}}) / 2$ .
- (4) DC output balance is defined as  $|V_{\text{OUTCM}}(\text{at } V_{\text{IN}} = +1) - V_{\text{OUTCM}}(\text{at } V_{\text{IN}} = -1)| / 2$ .
- (5)  $V_{\text{OUTCM}}$  offset voltage is defined as  $V_{\text{OUTCM}} - V_{\text{OCM}}$ .



## 6.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)

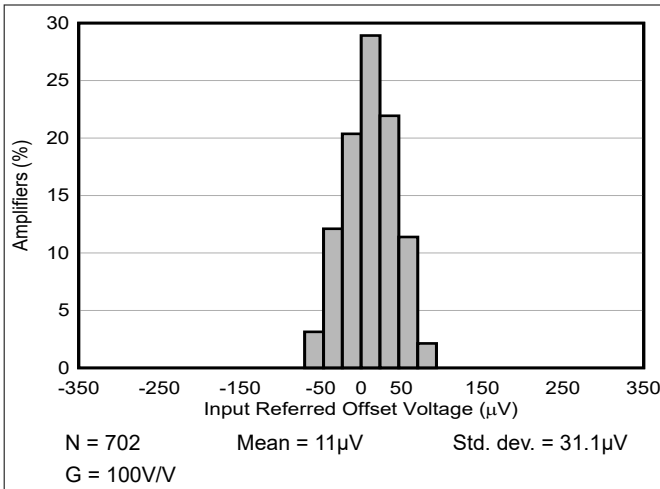


Figure 6-1. Distribution of Offset Voltage (RTI)

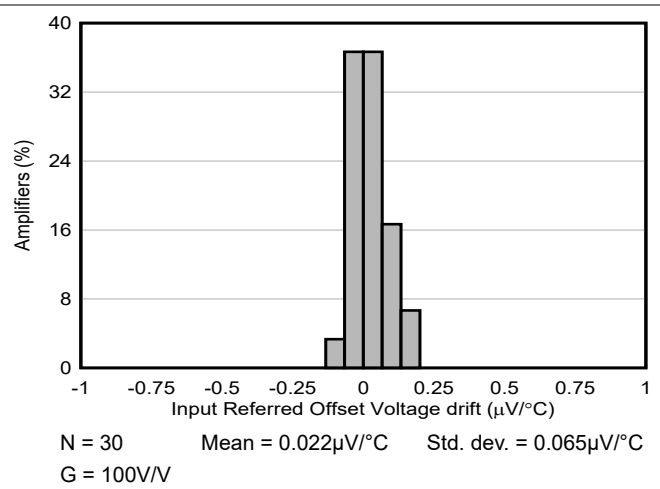


Figure 6-2. Distribution of Offset Voltage Drift (RTI)

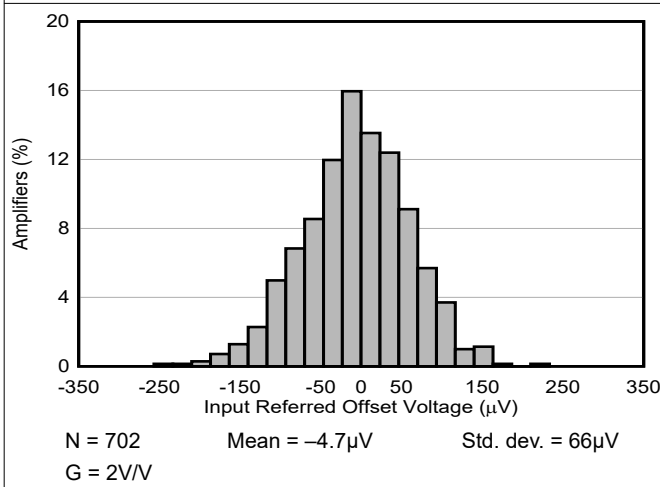


Figure 6-3. Distribution of Offset Voltage (RTI)

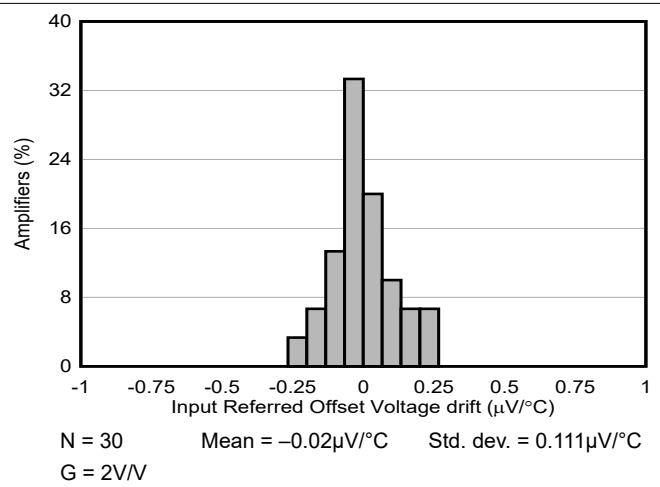


Figure 6-4. Distribution of Offset Voltage Drift (RTI)

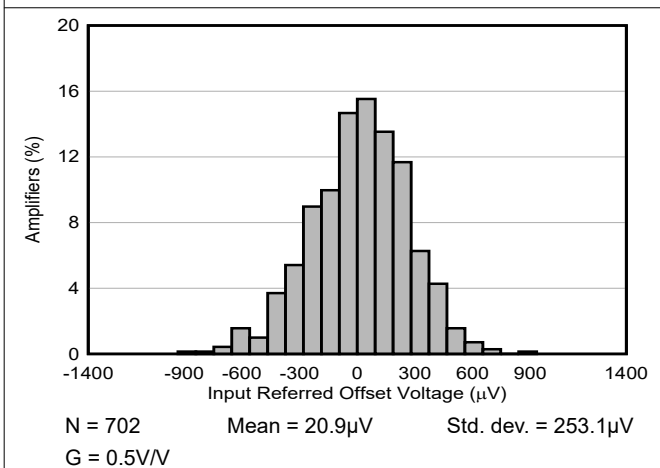


Figure 6-5. Distribution of Offset Voltage (RTI)

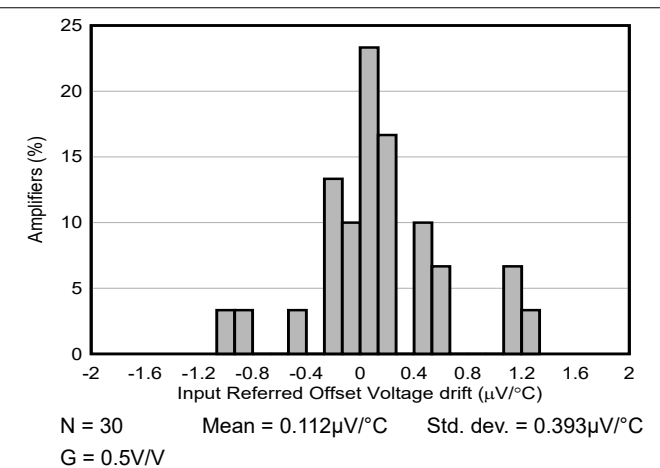
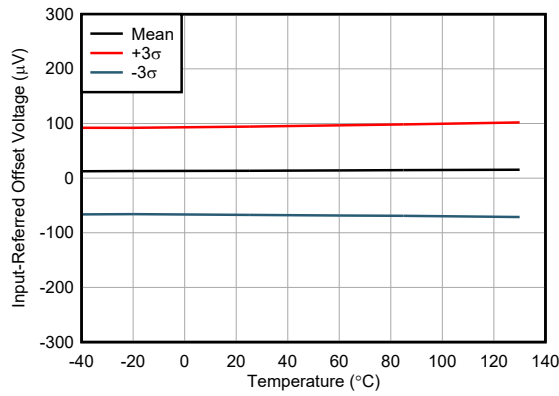


Figure 6-6. Distribution of Offset Voltage Drift (RTI)

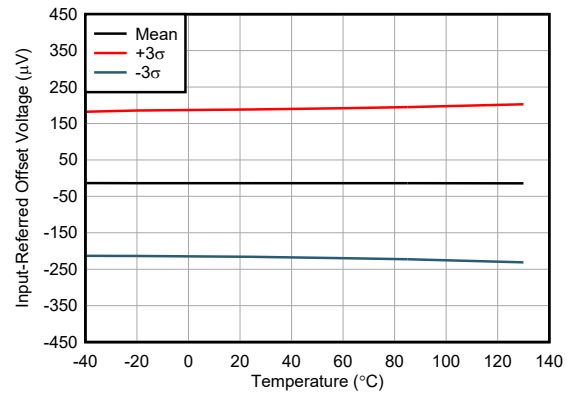
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)



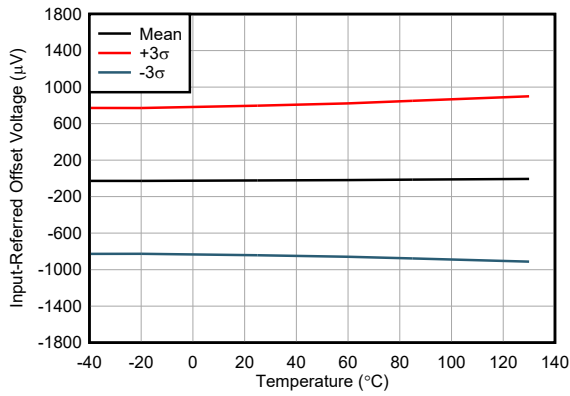
N = 30  
G = 100V/V

Figure 6-7. Offset Voltage (RTI) vs Temperature



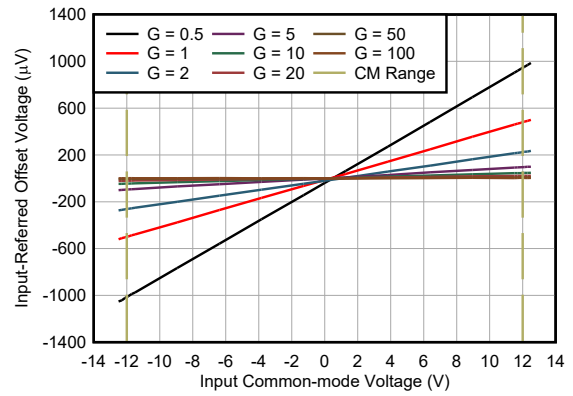
N = 30  
G = 2V/V

Figure 6-8. Offset Voltage (RTI) vs Temperature



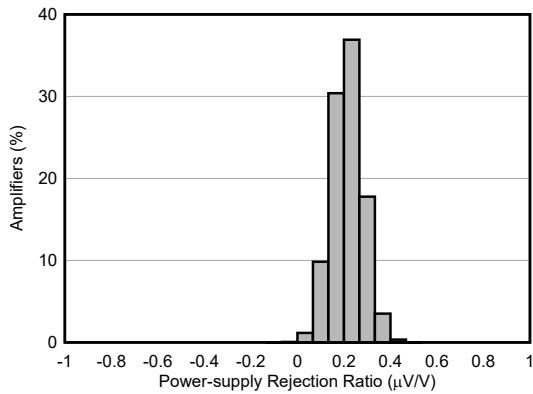
N = 30  
G = 0.5V/V

Figure 6-9. Offset Voltage (RTI) vs Temperature



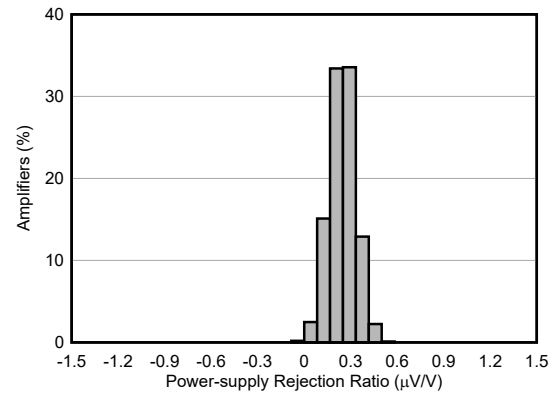
Typical unit shown

Figure 6-10. Offset Voltage (RTI) vs  $V_{ICM}$



N = 8126    Mean = 0.214µV/V    Std. dev. = 0.0668µV/V  
G = 100V/V

Figure 6-11. PSRR Distribution

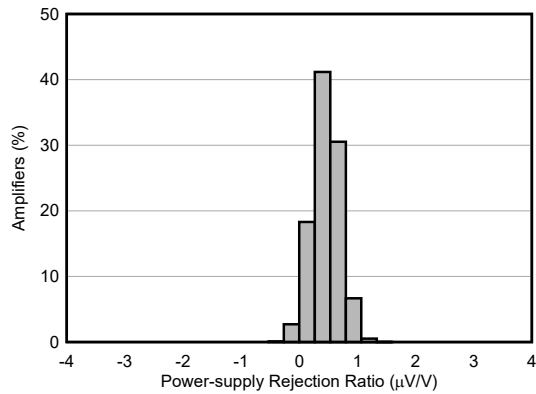


N = 8126    Mean = 0.247µV/V    Std. dev. = 0.0852µV/V  
G = 2V/V

Figure 6-12. PSRR Distribution

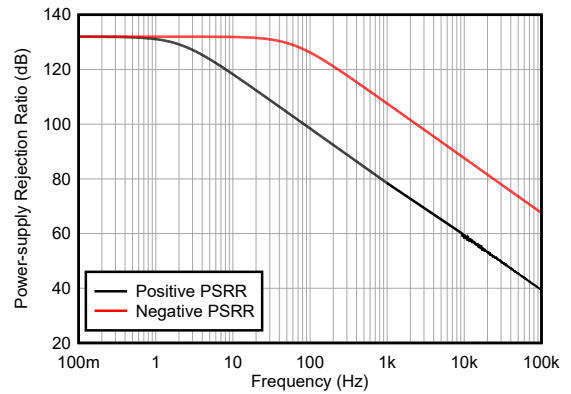
### 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)



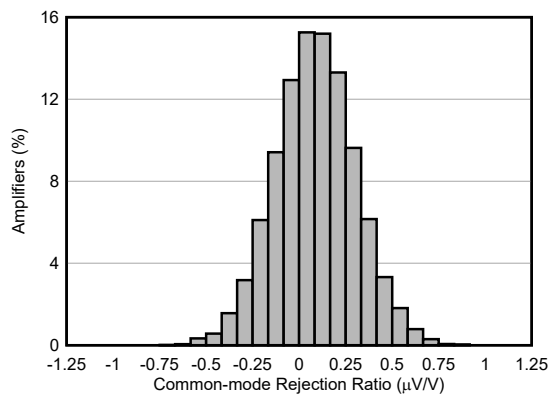
N = 8126    Mean =  $0.459\mu\text{V/V}$     Std. dev. =  $0.237\mu\text{V/V}$   
G =  $0.5\text{V/V}$

**Figure 6-13. PSRR Distribution**



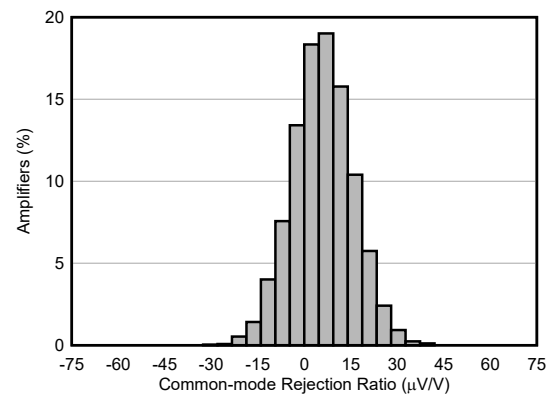
Typical unit shown  
G =  $1\text{V/V}$

**Figure 6-14. Positive and Negative PSRR vs Frequency**



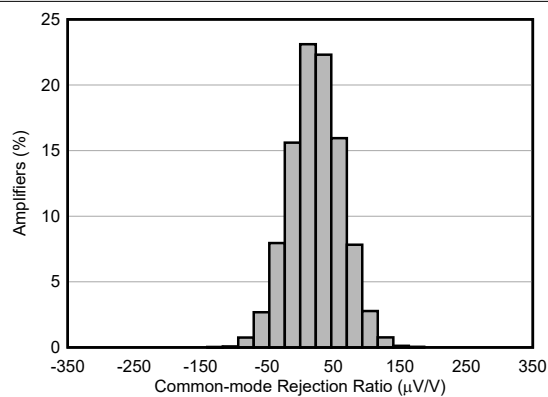
N = 8126    Mean =  $0.0868\mu\text{V/V}$     Std. dev. =  $0.216\mu\text{V/V}$   
G =  $100\text{V/V}$

**Figure 6-15. CMRR Distribution**



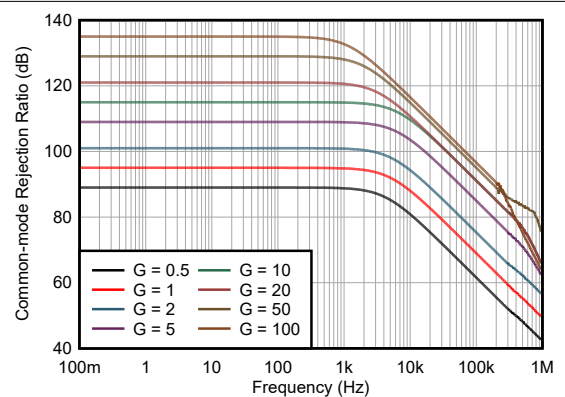
N = 8126    Mean =  $5.79\mu\text{V/V}$     Std. dev. =  $9.74\mu\text{V/V}$   
G =  $2\text{V/V}$

**Figure 6-16. CMRR Distribution**



N = 8126    Mean =  $23.08\mu\text{V/V}$     Std. dev. =  $38.97\mu\text{V/V}$   
G =  $0.5\text{V/V}$

**Figure 6-17. CMRR Distribution**

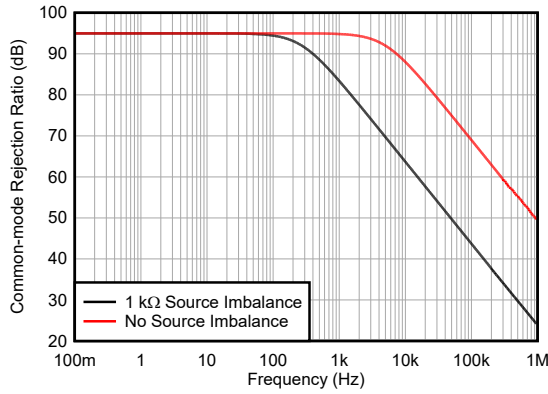


Typical unit shown

**Figure 6-18. CMRR vs Frequency (RTI)**

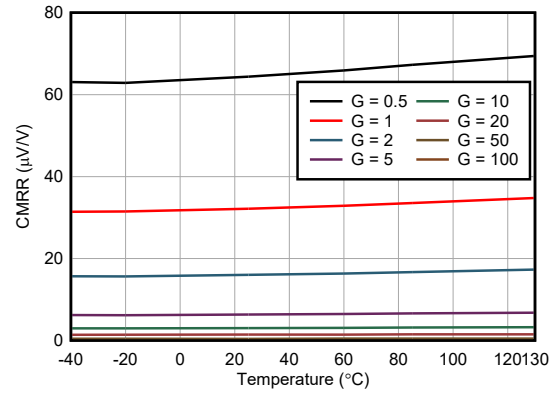
### 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)



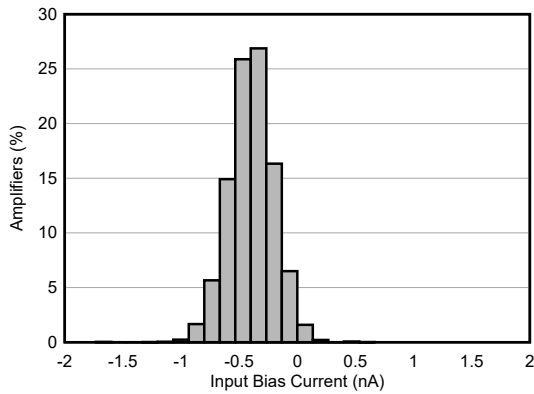
Typical unit shown  
 $G = 1\text{V/V}$

**Figure 6-19. CMRR vs Frequency (Unbalanced)**



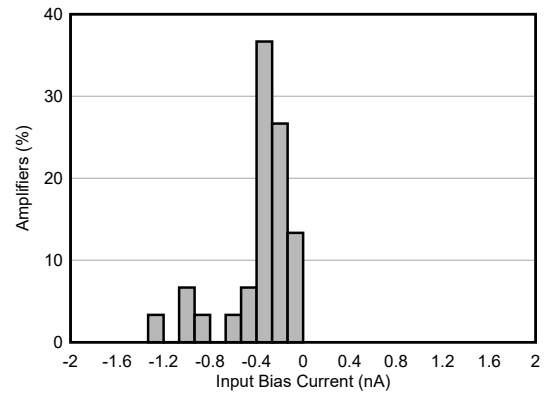
Typical unit shown

**Figure 6-20. CMRR vs Temperature**



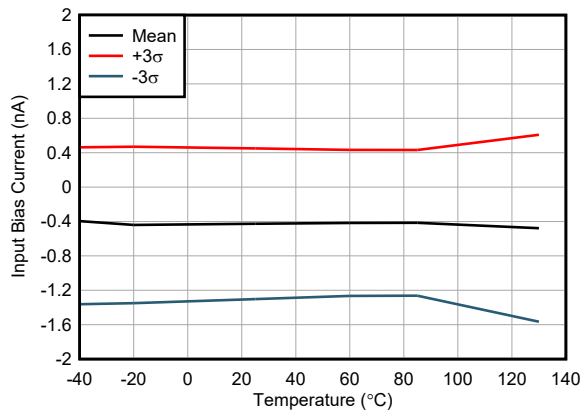
$N = 8126$  Mean =  $-0.392\text{nA}$  Std. dev. =  $0.191\text{nA}$   
 $G = 1\text{V/V}$

**Figure 6-21. Distribution of Input Bias Current**



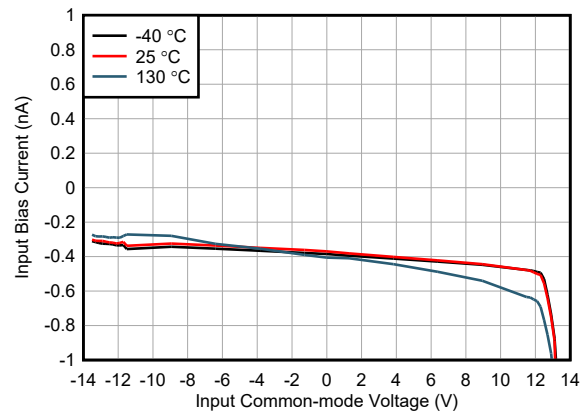
$N = 30$  Mean =  $-0.313\text{nA}$  Std. dev. =  $0.282\text{nA}$   
 $G = 1\text{V/V}$   $T_A = 85^\circ\text{C}$

**Figure 6-22. Distribution of Input Bias Current**



$N = 30$  1 wafer lot  
 $G = 1\text{V/V}$

**Figure 6-23. Input Bias Current vs Temperature**

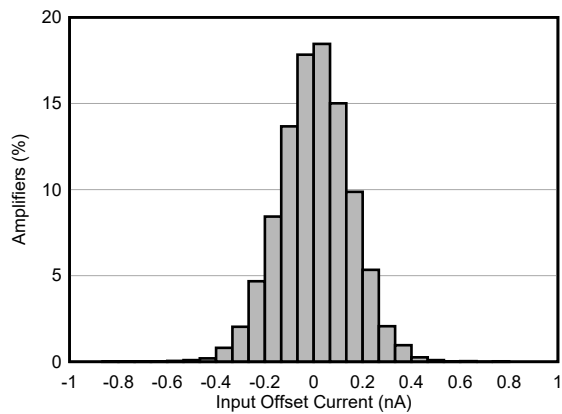


Typical unit shown  
 $G = 1\text{V/V}$

**Figure 6-24. Input Bias Current vs  $V_{ICM}$**

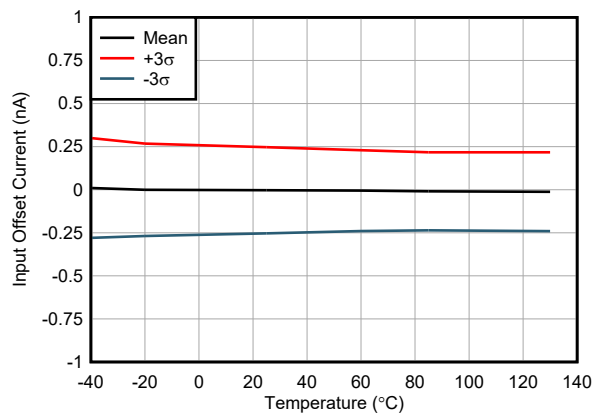
### 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)



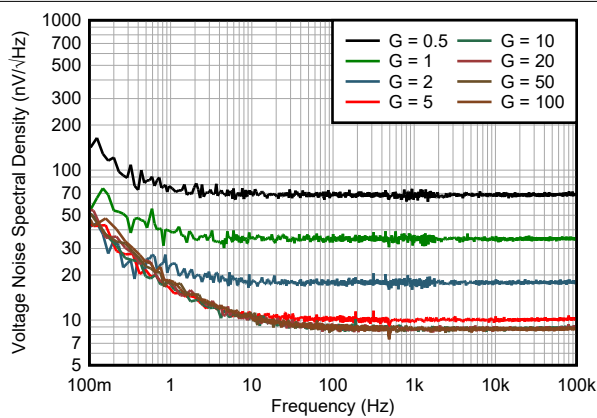
N = 8126      Mean = 0.0067nA      Std. dev = 0.1473nA  
G = 1V/V

**Figure 6-25. Distribution of Input Offset Current**



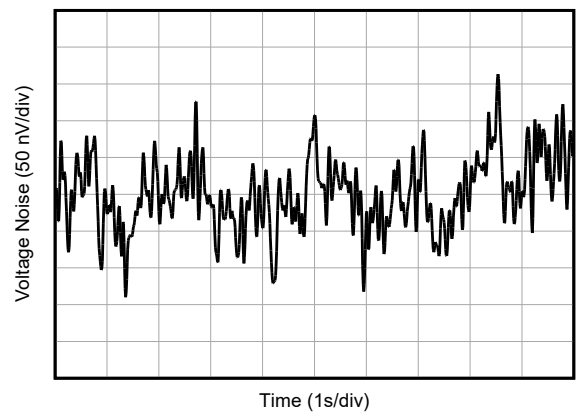
N = 30      1 wafer lot  
G = 1V/V

**Figure 6-26. Input Offset Current vs Temperature**



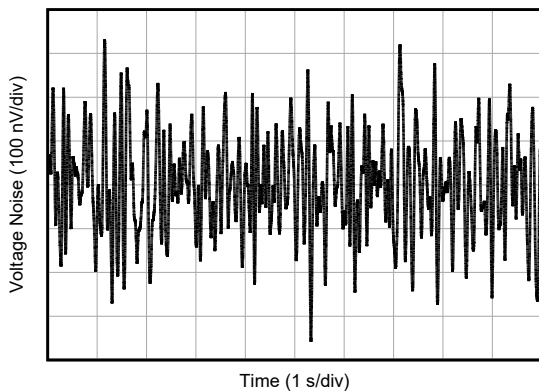
Typical unit shown

**Figure 6-27. Voltage Noise Spectral Density (RTI) vs Frequency**



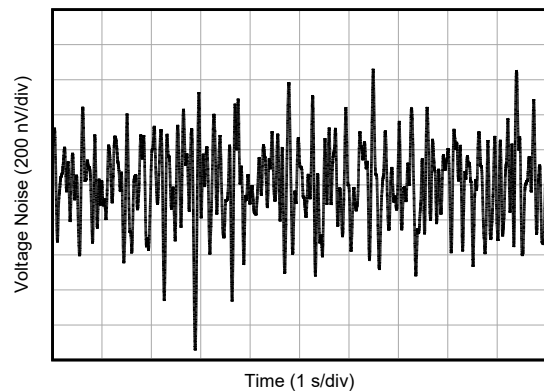
Typical unit shown  
G = 100V/V

**Figure 6-28. 0.1Hz to 10Hz Voltage Noise (RTI)**



Typical unit shown  
G = 1V/V

**Figure 6-29. 0.1Hz to 10Hz Voltage Noise (RTI)**

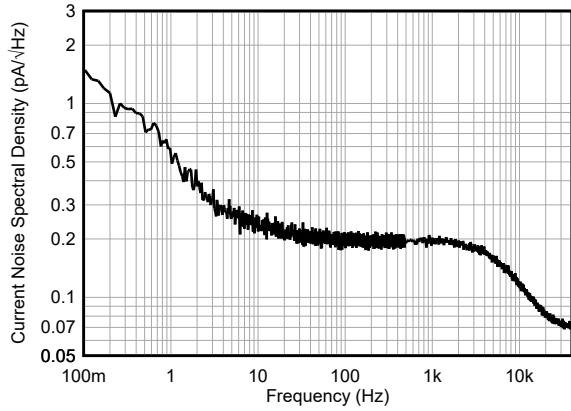


Typical unit shown  
G = 0.5V/V

**Figure 6-30. 0.1Hz to 10Hz Voltage Noise (RTI)**

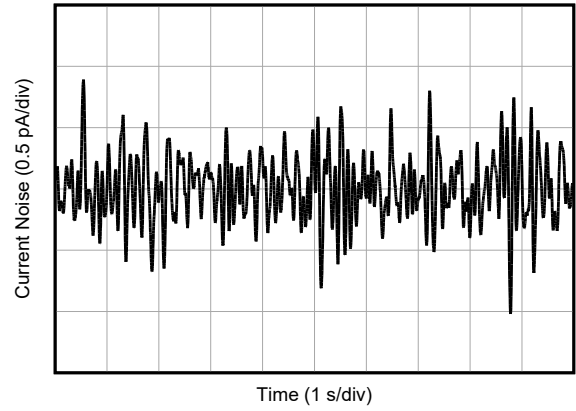
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)



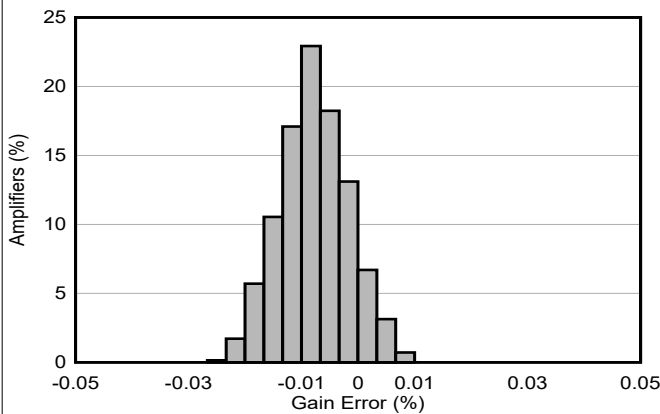
Typical unit shown  
 $G = 1\text{V/V}$

Figure 6-31. Current Noise Spectral Density vs Frequency



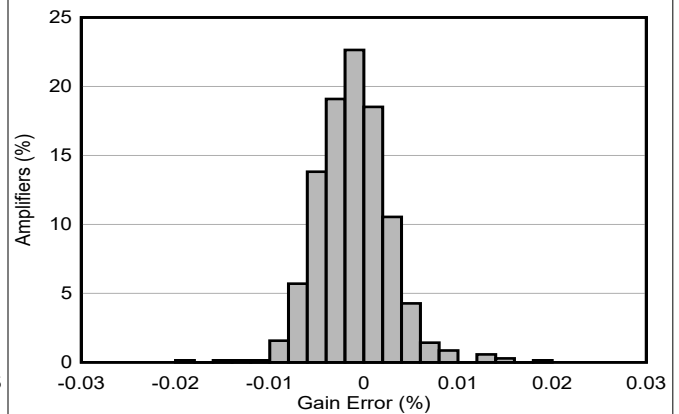
Typical unit shown  
 $G = 1\text{V/V}$

Figure 6-32. 0.1Hz to 10Hz Current Noise



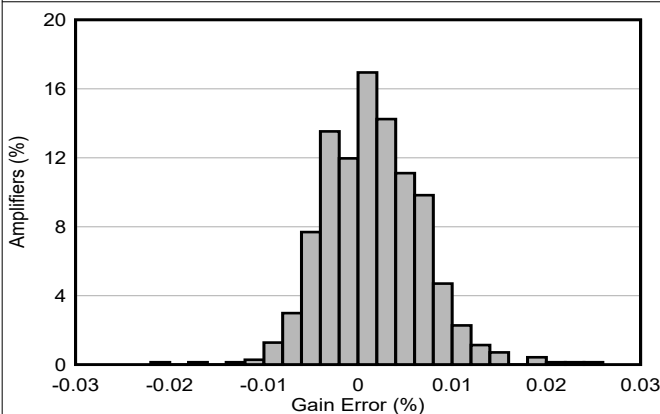
$N = 702$  Mean =  $-0.008\%$  Std. dev. =  $0.006\%$   
 $G = 100\text{V/V}$

Figure 6-33. Distribution of Differential Gain Error



$N = 702$  Mean =  $-0.001\%$  Std. dev. =  $0.004\%$   
 $G = 2\text{V/V}$

Figure 6-34. Distribution of Differential Gain Error



$N = 702$  Mean =  $0.001\%$  Std. dev. =  $0.005\%$   
 $G = 0.5\text{V/V}$

Figure 6-35. Distribution of Differential Gain Error

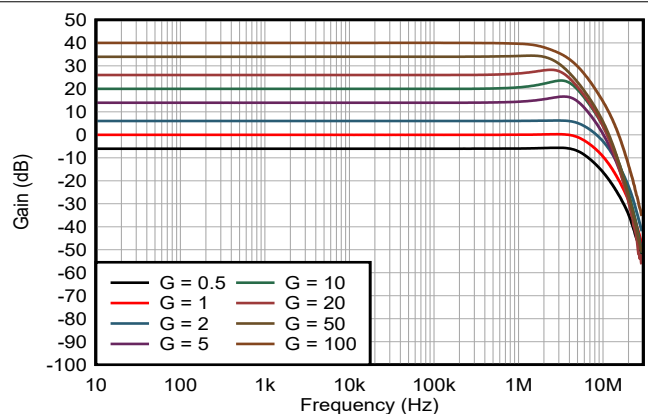
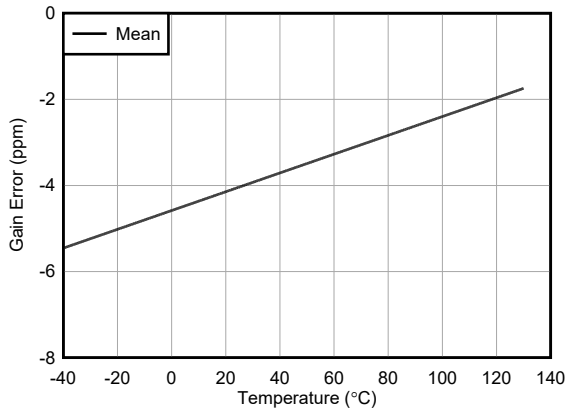


Figure 6-36. Gain vs Frequency

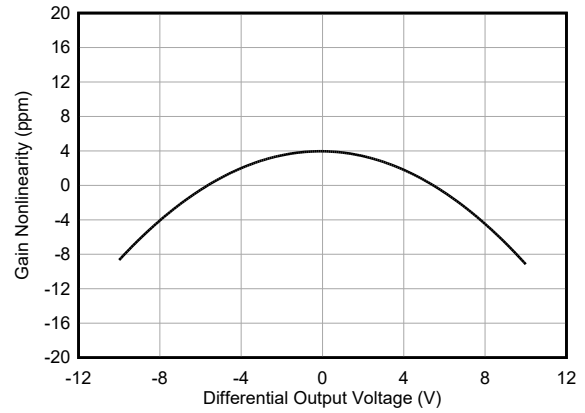
### 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)



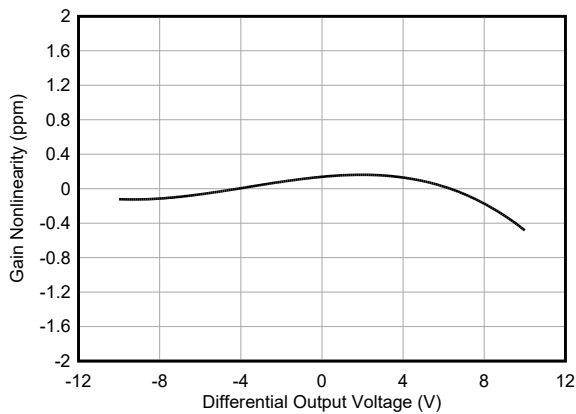
Typical unit shown  
 $G = 2\text{V/V}$

**Figure 6-37. Gain Error vs Temperature**



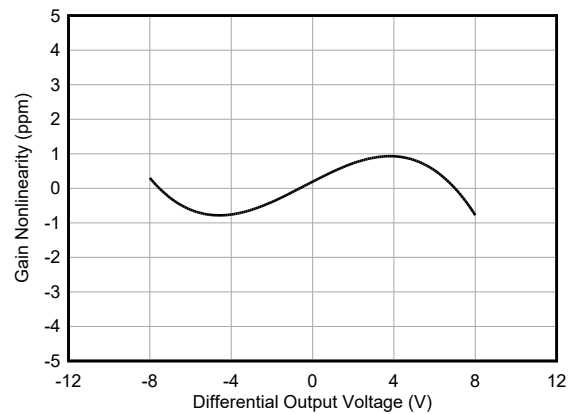
$V_{OUT} = \pm 10\text{V}$   
Typical unit shown  
 $G = 100\text{V/V}$

**Figure 6-38. Gain Nonlinearity**



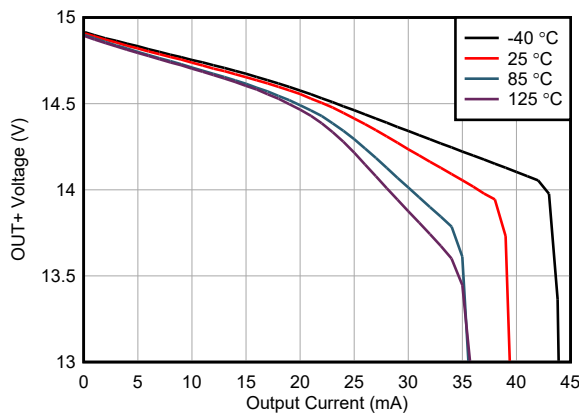
$V_{OUT} = \pm 10\text{V}$   
Typical unit shown  
 $G = 2\text{V/V}$

**Figure 6-39. Gain Nonlinearity**



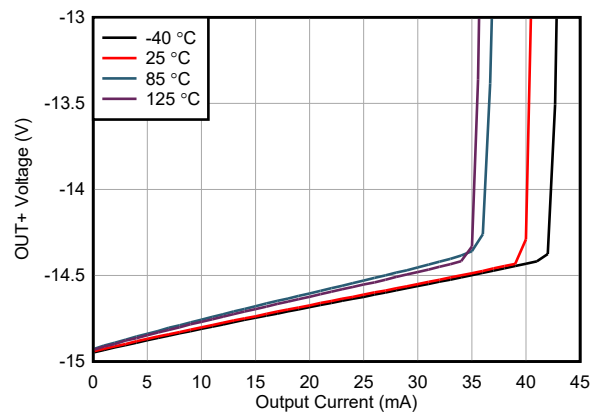
$V_{OUT} = \pm 8\text{V}$   
Typical unit shown  
 $G = 0.5\text{V/V}$

**Figure 6-40. Gain Nonlinearity**



$V_S = \pm 18\text{V}$      $V_{OUT} = \pm 15\text{V}$      $G = 100\text{V/V}$

**Figure 6-41. Positive Output Voltage vs Output Current**

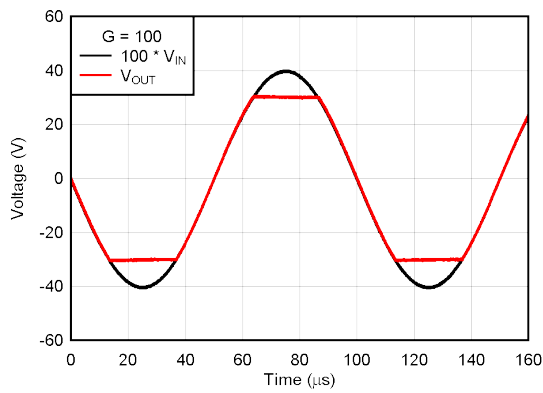


$V_S = \pm 18\text{V}$      $V_{OUT} = \pm 15\text{V}$      $G = 100\text{V/V}$

**Figure 6-42. Negative Output Voltage vs Output Current**

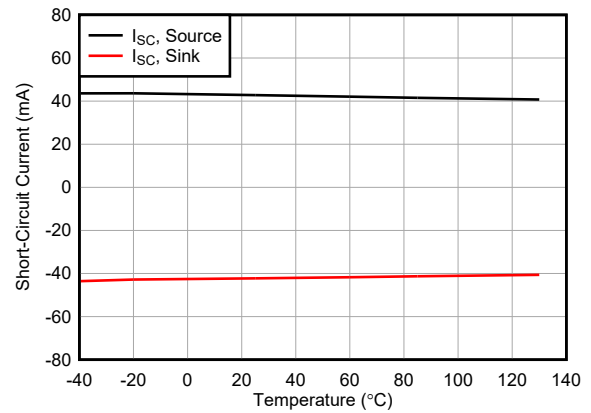
### 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)



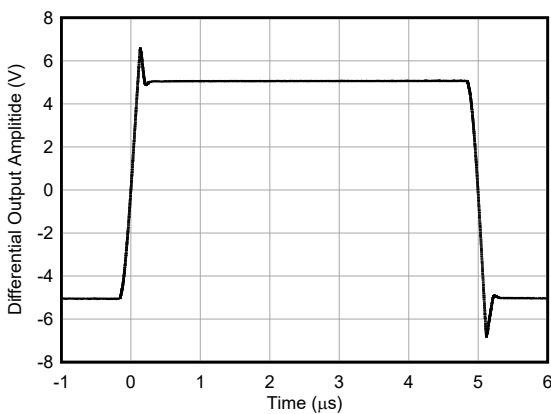
$G = 100\text{V/V}$

Figure 6-43. Overload Recovery



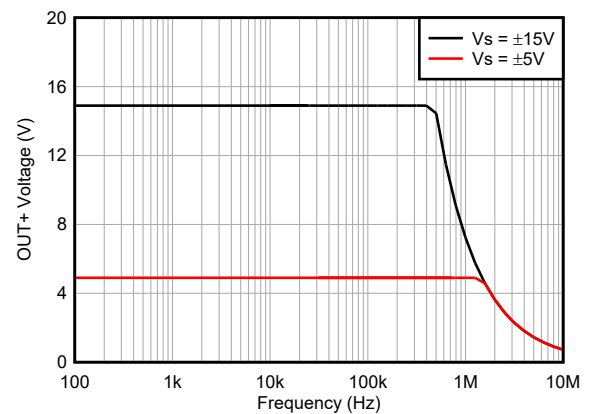
Short to  $V_{SOUT}/2$   
 $G = 1\text{V/V}$

Figure 6-44. Output Short-Circuit Current vs Temperature



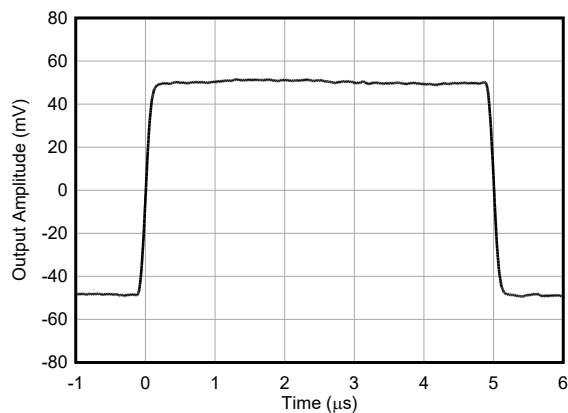
$G = 1\text{V/V}$

Figure 6-45. Large-Signal Step Response



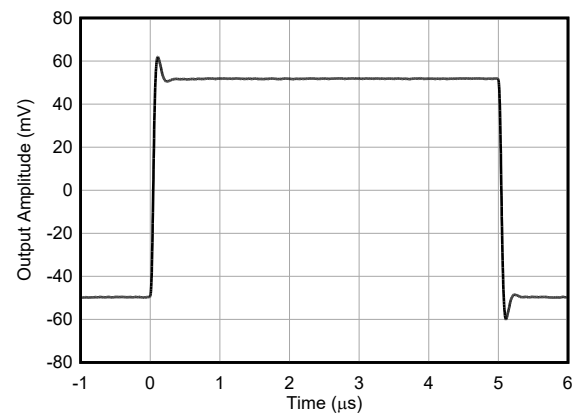
$G = 1\text{V/V}$

Figure 6-46. Large-Signal Step Response vs Frequency



$G = 100\text{V/V}$   $C_L = 50\text{pF}$

Figure 6-47. Small-Signal Step Response



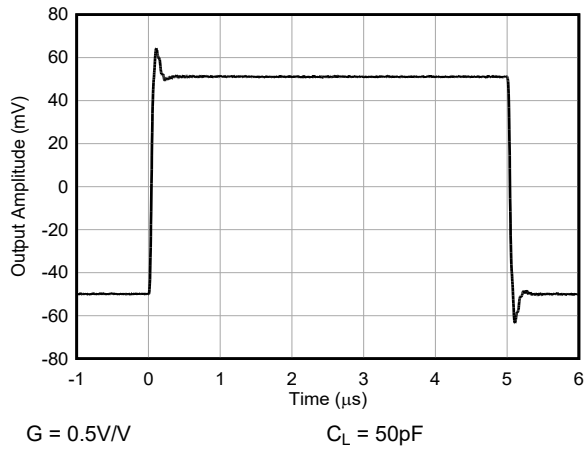
$G = 1\text{V/V}$   $C_L = 50\text{pF}$

Figure 6-48. Small-Signal Step Response

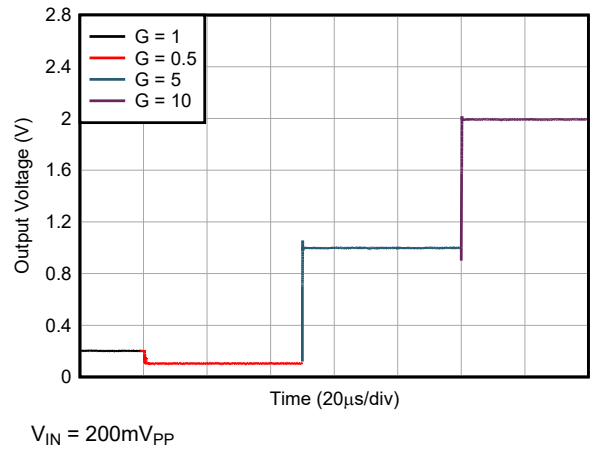


### 6.6 Typical Characteristics (continued)

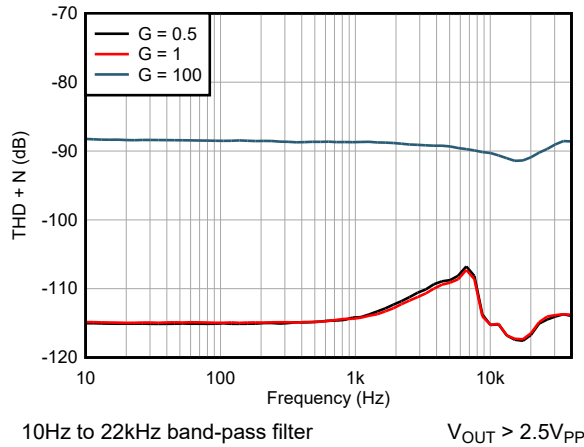
at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)



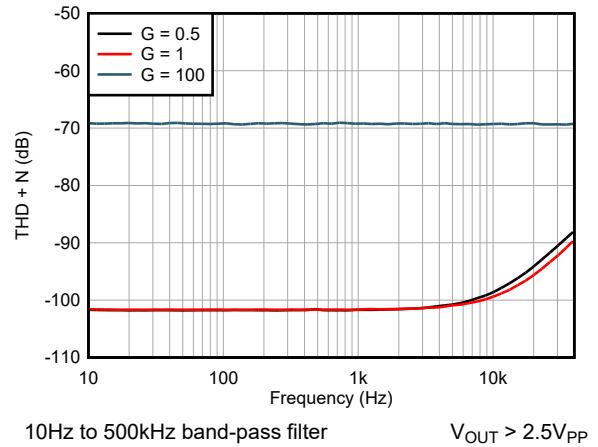
**Figure 6-49. Small-Signal Step Response**



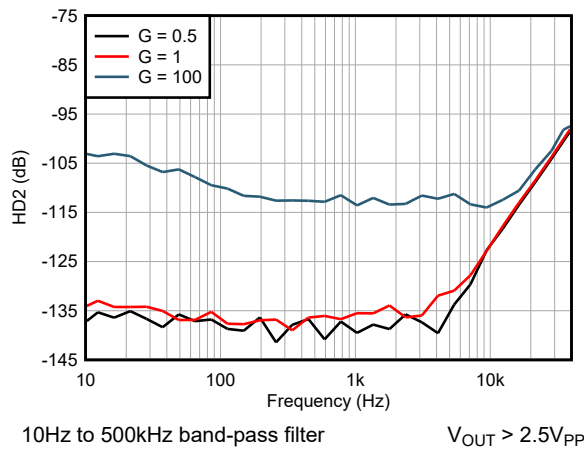
**Figure 6-50. Gain Switching Transient Response**



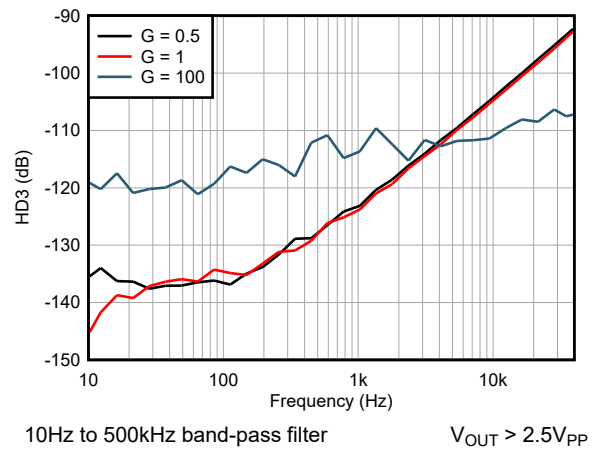
**Figure 6-51. Total Harmonic Distortion + Noise vs Frequency**



**Figure 6-52. Total Harmonic Distortion + Noise vs Frequency**



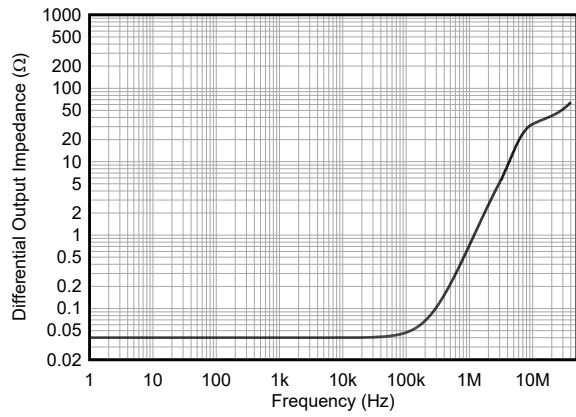
**Figure 6-53. 2nd Harmonic Distortion vs Frequency**



**Figure 6-54. 3rd Harmonic Distortion vs Frequency**

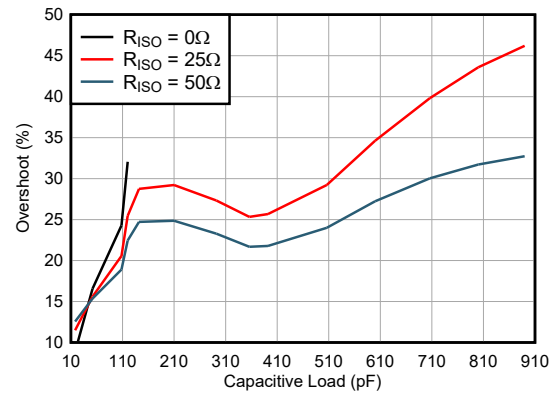
### 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{OCM} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ , and  $G = 1\text{V/V}$  (unless otherwise noted)



$G = 1\text{V/V}$

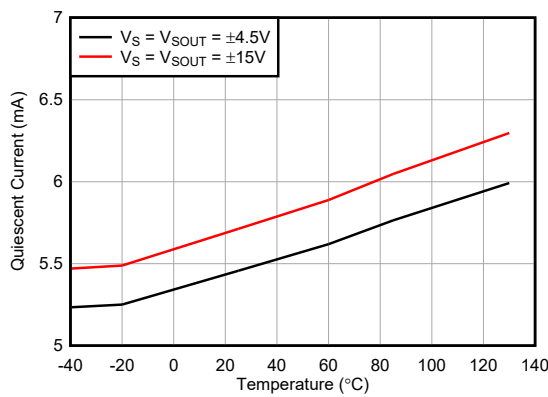
Figure 6-55. Closed-Loop Output Impedance vs Frequency



$G = 1\text{V/V}$

$V_{OUT} = 100\text{mV}_{PP}$

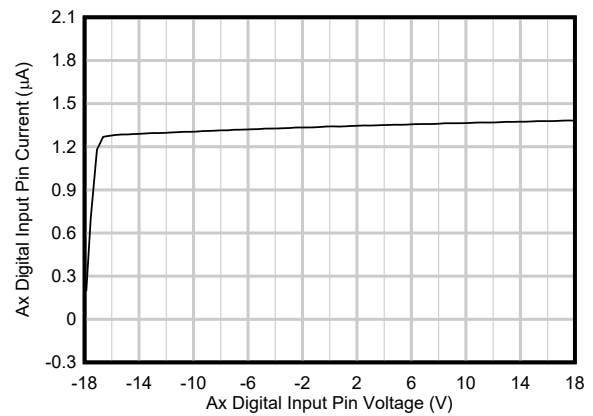
Figure 6-56. Overshoot vs Capacitive Load



Input stage

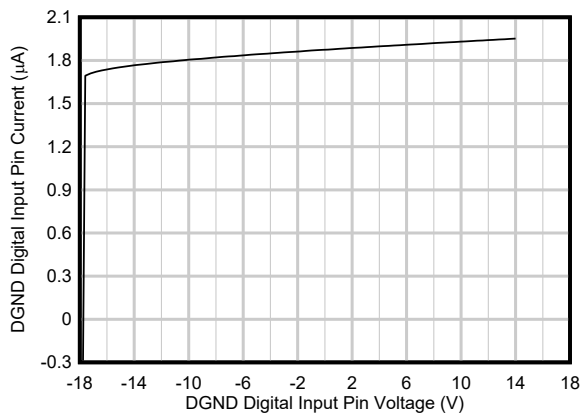
$G = 0.5\text{V/V}$

Figure 6-57. Quiescent Current vs Temperature



DGND = -18V

Figure 6-58. Ax Digital Input Pin Current vs Ax Digital Input Pin Voltage



Ax = DGND

Figure 6-59. DGND Digital Input Pin Current vs DGND Digital Input Pin Voltage

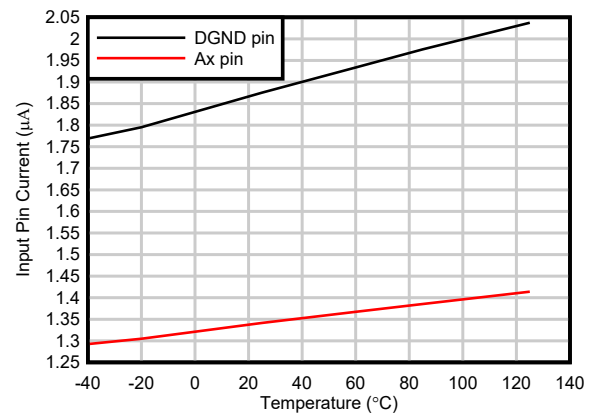


Figure 6-60. Digital Input Pin Current vs Temperature

## 7 Detailed Description

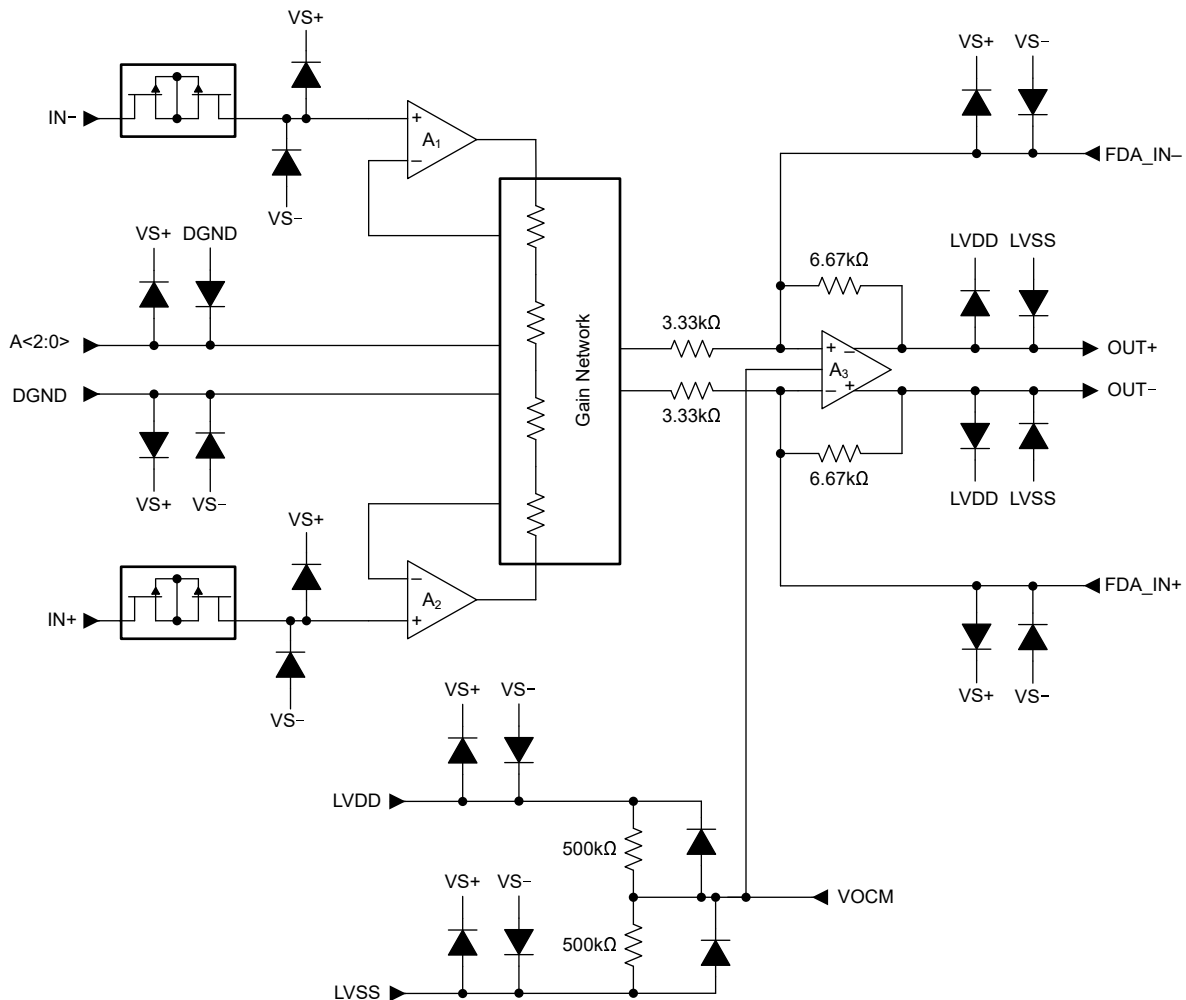
### 7.1 Overview

The PGA854 is a monolithic, high-voltage, precision programmable-gain instrumentation amplifier. The PGA854 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, difference amplifier output stage. Eight preprogrammed decade gains are selectable using gain-select pins A0, A1, A2. Gains range from 0.5V/V to 100V/V; see also [Section 7.3.1](#).

A functional block diagram for the PGA854 is shown in the next section. The differential input voltage is fed into a pair of matched, high-impedance input, current-feedback amplifiers. An integrated precision-matched gain resistor network is used to amplify the differential input voltage. An output difference amplifier, A<sub>3</sub>, rejects the input common-mode component and refers the output signal to the voltage level set by the V<sub>OCM</sub> pin.

The PGA854 output amplifier bandwidth is optimized to drive high-performance analog-to-digital converters (ADCs) with sampling rates up to 1MSPS without additional ADC drivers. The output amplifier uses a separate power supply that is independent of the input-stage power supply. When driving an ADC, use a low-impedance connection from LVDD and LVSS to the ADC power supplies. This configuration protects the ADC inputs from damage resulting from inadvertent overvoltage conditions.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Gain Control

The PGA854 uses three pins to set the amplifier gain. These gain select pins are set with respect to DGND. This configuration simplifies the design when compared to programmable-gain amplifiers requiring a SPI or other digital interface options for gain changes. Figure 7-1 shows the gain-setting block diagram. Table 7-1 lists the gain options. Any gain select pin that is not driven by an external source is automatically biased at DGND using internal pull-down options.

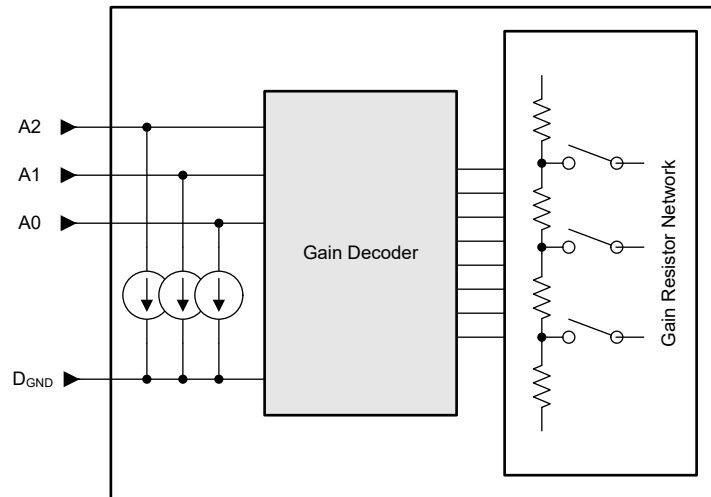


Figure 7-1. PGA854 Gain Setting Block Diagram

Table 7-1. Gain Options

A2:A0	GAIN
000	0.5
001	1
010	2
011	5
100	10
101	20
110	50
111	100

### 7.3.2 Input Protection

The inputs of the PGA854 are individually protected for voltages up to  $\pm 40V$  beyond either supply. For example, an input common-mode voltage anywhere between  $-55V$  and  $+55V$  does not cause damage when powered from  $\pm 15V$  supplies. Internal circuitry on each input provides low series impedance under normal signal conditions, thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8mA. Figure 7-2 shows the input protection functionality during an overvoltage condition on IN+ or IN- inputs.

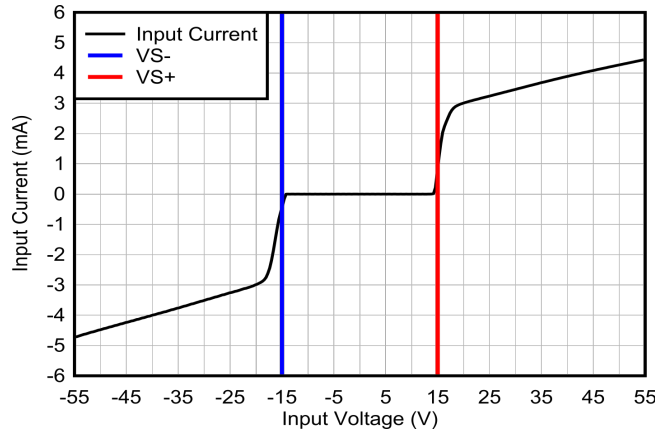


Figure 7-2. Input Current vs Input Overvoltage

Figure 7-3 shows that during an input overvoltage condition, current flows through the input protection diodes into the power supplies. In applications where the power supplies are unable to sink current, place Zener diode clamps (ZD1 and ZD2) on the power supplies to provide a current pathway to ground.

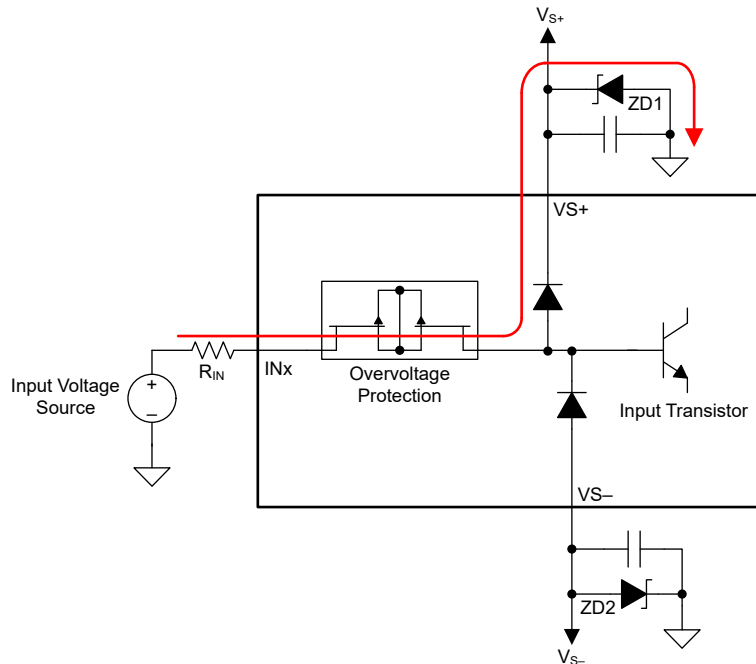


Figure 7-3. Input Current Path During an Overvoltage Condition

### 7.3.3 Output Common-Mode Pin

The output voltages of the PGA854 are balanced with respect to the voltage on the output common-mode pin, VO<sub>CM</sub>. The starting point for most designs is to assign an output common-mode voltage for the PGA854. For ac-coupled signal paths, this voltage is often the default mid-supply voltage, so as to retain the most available output swing around the voltage centered at VO<sub>CM</sub>. For dc-coupled signal paths, and low voltage output supply, set this voltage between a maximum of  $V_{LVDD} - 1.5V$  and minimum of  $V_{LVSS} + 1.5V$ . For higher voltage supplies, set VO<sub>CM</sub> between  $V_{LVDD} - 2V$  and minimum of  $V_{LVSS} + 2V$ . Note that For precision ADC applications, this voltage is typically the input common-mode voltage of the ADC.

The voltage at the VO<sub>CM</sub> pin is internally buffered to bias the fully differential output amplifier, eliminating the need for an external VO<sub>CM</sub> buffer. In the event that the VO<sub>CM</sub> pin is left floating, the output common-mode control voltage is biased at output mid-supply using an internal 500k $\Omega$ -500k $\Omega$  resistor divider network connected between the output-stage power-supply pins.

### 7.3.4 Using the Fully Differential Output Amplifier to Shape Noise

Section 7.2 shows that the PGA854 output-stage fully-differential amplifier uses 6.67k $\Omega$  feedback resistors between the OUT+ output and the inverting input, and the OUT– output and the noninverting input. External direct access to inverting input is provided through the FDA\_IN+ pin, and to the noninverting input through the FDA\_IN– pin. This option allows circuit designers to add external feedback capacitors in parallel with the internal feedback resistors to implement noise-filtering or noise-shaping techniques. These pins are also usable to implement customized attenuating gains for the output stage. Consider the following important factors when designing parallel circuits with the internal feedback resistors:

- The accuracy of the internal resistor network is 0.01% or better. This accuracy results in a common-mode rejection ratio (CMRR) of 80dB or better. Mismatched leakage currents on these pins potentially causes CMRR degradation.
- The internal resistors have  $\pm 15\%$  absolute resistance variation; consider this variation when implementing custom attenuating gains or noise filters.

#### CAUTION

Do not treat these pins as outputs, nor use the pins to source or sink current. Excessive currents through the feedback resistors potentially cause permanent damage to internal circuitry.

## 7.4 Device Functional Modes

The PGA854 has a single functional mode and operates when the input-stage power supply is greater than  $\pm 4.5V$  (9V) and the output-stage power supply is greater than  $\pm 2.25V$  (4.5V); see also Section 6.3.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

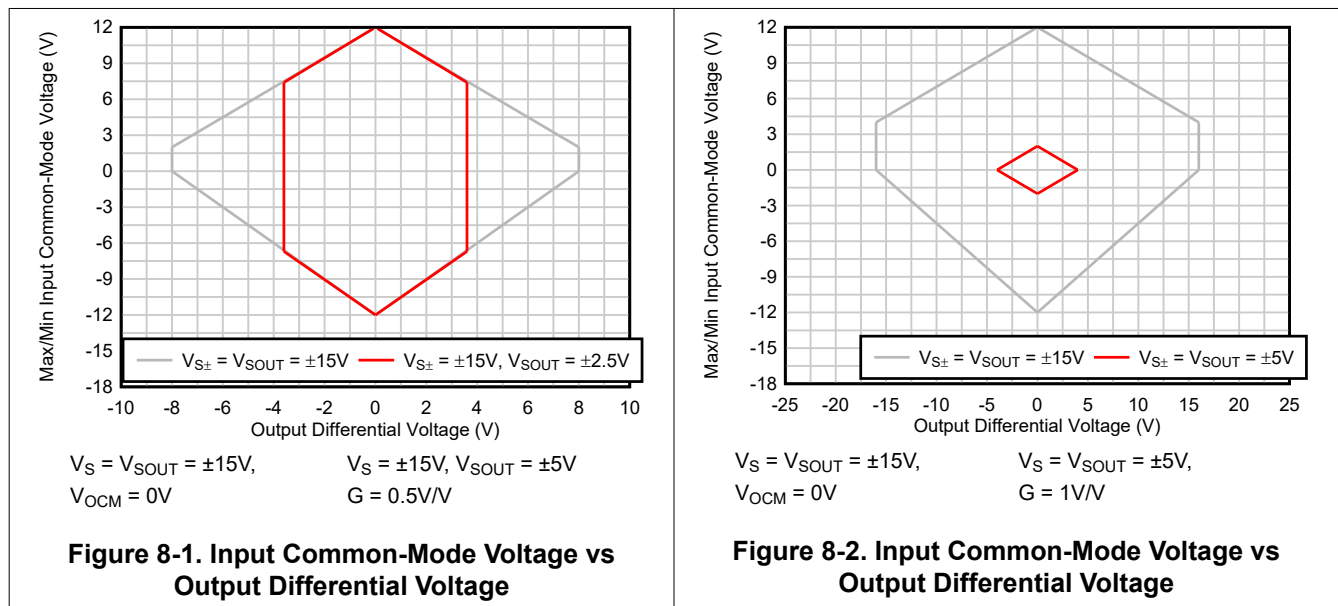
The PGA854 is a monolithic, high-voltage, high-bandwidth, precision programmable gain instrumentation amplifier with fully differential outputs. The PGA854 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, differential amplifier output stage. The PGA854 is equipped with eight decade-gain settings, from 0.5V/V to 100V/V, using three digital gain-selection pins: A0, A1, and A2.

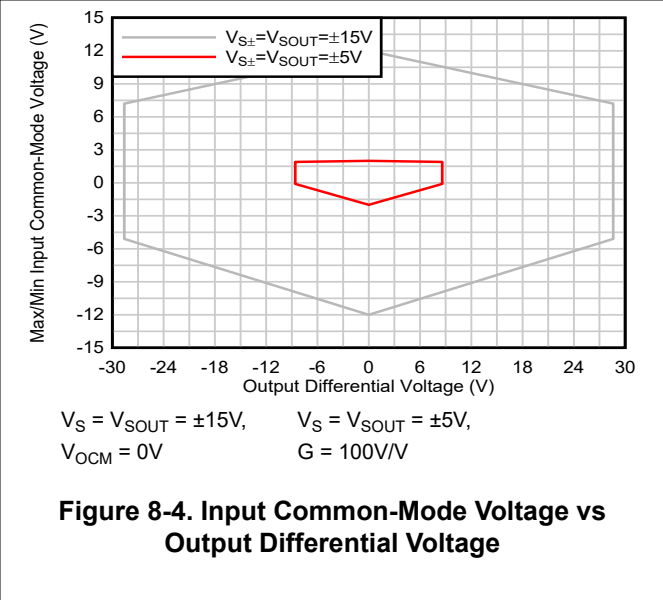
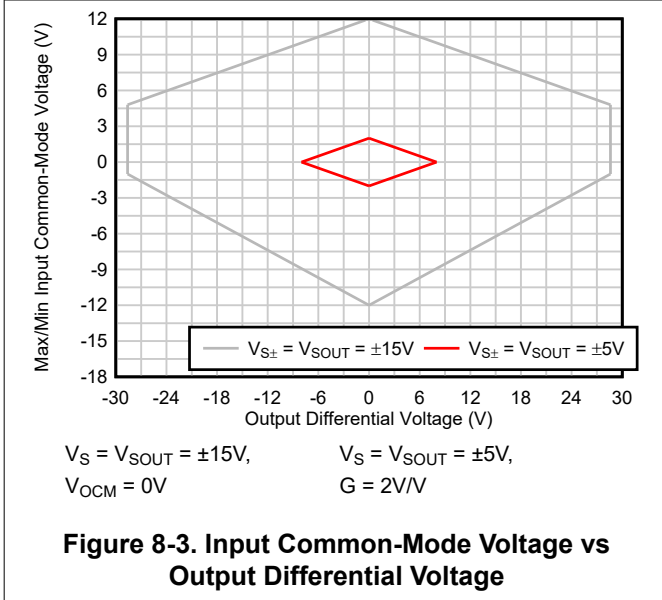
The PGA854 is designed for applications such as factory automation and control, analog input modules, data acquisition, test and measurement, and semiconductor test.

#### 8.1.1 Linear Operating Input Range

The linear operating input voltage range of the PGA854 input circuitry extends within 3V (maximum) of either power supply. This device maintains excellent common-mode rejection throughout this range at all temperatures. The linear operating input common-mode range is a function of the input common-mode voltage, input differential voltage, gain, and output common-mode voltage.

Figure 8-1 to Figure 8-4 show the valid common-mode range to enable valid output voltage at no load condition.



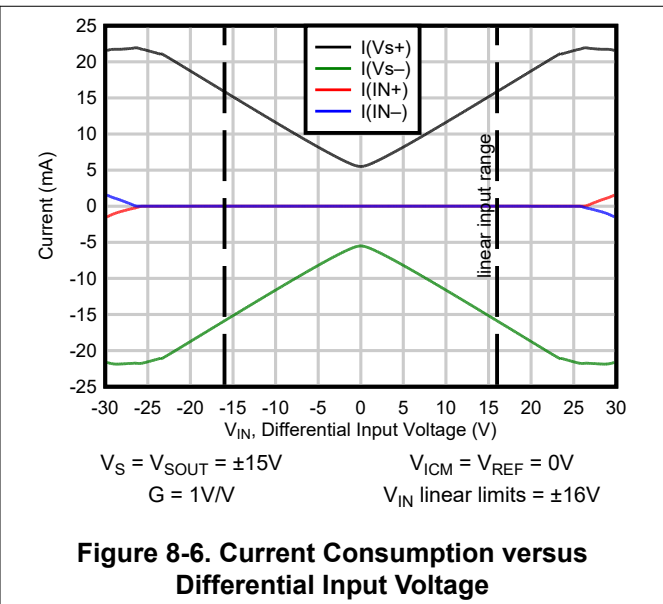
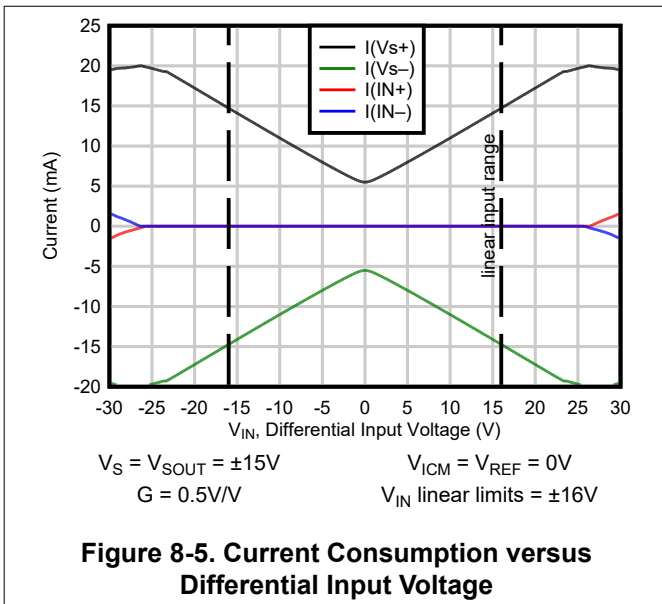


### 8.1.2 Current Consumption with Differential Inputs

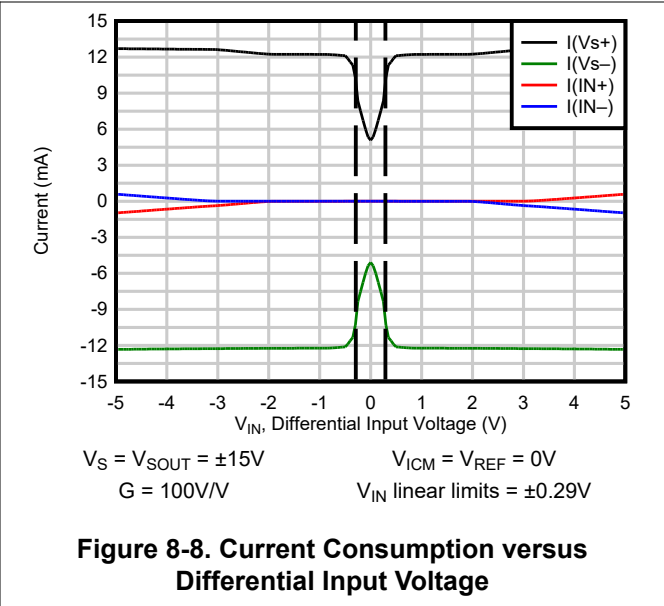
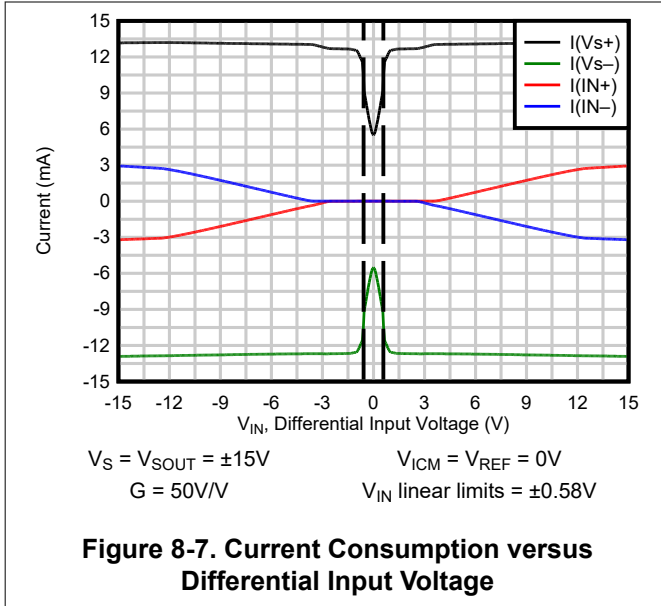
Programmable gain amplifiers such as the PGA854 use internal resistors to set the gain. Consequently, the current consumption is increased by the current that passes through these resistors. The largest supply current consumption occurs at  $G = 2V/V$  when applying large amplitude differential signals.

Note that  $I_Q$  values in the specifications section are under the condition  $V_{IN} = 0V$ . Higher supply current is to be expected for higher differential input levels. Same goes to bias current  $I_B$ , which is specified with zero differential input. Input bias current increases slightly with increased differential inputs up to the linear input range limit (see Section 8.1.1 for details), If the input exceeds the linear input range limit (inputs are overdriven), the input bias current significantly increases.

Figure 8-5 to Figure 8-8 show typical current consumption versus input differential voltage for the input stage supply, and the current drawn by the PGA854 inputs when the device is overdriven. The dashed vertical reference lines outline the linear operating region of the device at that given gain ( $V_{IN}$ ), outside of this region is when the inputs of the device are overdriven.



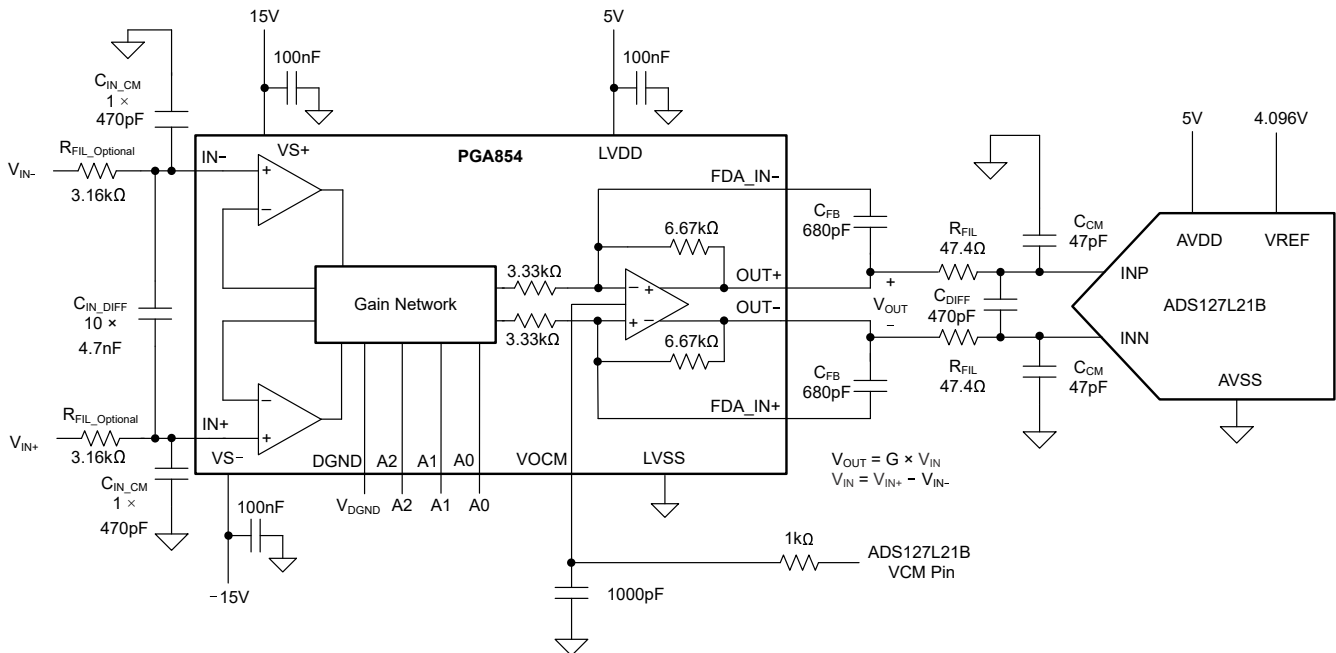




## 8.2 Typical Application

### 8.2.1 ADS127L11 and ADS127L21B, 24-Bit, Delta-Sigma ADC Driver Circuit

The application circuit in [Figure 8-9](#) shows a schematic for a 24-bit wide-bandwidth, delta-sigma ADC. The [ADS127Lx1](#) ADC offers two digital filters to optimize ac applications (wideband filter) or dc applications (sinc4 filter). [Table 8-2](#) and [Table 8-3](#) show measurement results in both filter settings. For a detailed design procedure to operate the ADS127Lx1 ADC, see the [ADS127Lx1EVM-PDK evaluation module user's guide](#).



### 8.2.1.1 Design Requirements

The design requirements for the application driving the ADS127Lx1 ADC are listed in [Table 8-1](#).

**Table 8-1. Design Parameters**

PARAMETER	VALUE
Differential-to-differential conversion	$V_{IN}$ to $V_{OUT}$
Supply voltages	$V_{S\pm} = \pm 15V$ , $V_{LVDD} = 5V$ , $V_{LVSS} = GND$ , $V_{REF} = 4.096V$
Full-scale range of ADC	$FSR = \pm 4.096V$
Data rate of ADC	$f_{DATA} = 187.5kSPS$
ADC filter configuration	(1) High-speed mode, Sinc4 filter, OSR = 64
	(2) High-speed mode, Wideband filter, OSR = 64
Signal frequency	Tested at $f_{IN} = 1kHz$
RC kickback filter <sup>(1)</sup>	$R_{FIL} = 47.4\Omega$ , $C_{DIFF} = 470pF$ , $C_{CM} = 47pF$

- (1) Consider a trade-off between THD, frequency response, and drift. The differential current drift into the ADC can interact with the filter resistors and result in higher drift errors. However, lower resistance degrades the phase margin of the PGA854. For low drift applications, keep  $R_{FIL} < 50\Omega$ .

### 8.2.1.2 Detailed Design Procedure

[Table 8-2](#) and [Table 8-3](#) show the typical signal-to-noise (SNR) and total harmonic distortion (THD) of the PGA854 driving the ADS127Lx1 delta-sigma ADC using a sinc4 or wideband filter. A 1kHz differential signal is applied to the input. The signal amplitude is adjusted to produce a PGA854 output at  $-0.2dBFS$  of the ADC full-scale range. For a list of the equivalent input voltage amplitude signals for the different PGA854 gain configurations, see [Table 8-2](#) and [Table 8-3](#). At gain =  $1V/V$ , the design achieves  $-94dB$  THD and  $80.2dB$  SNR for Sinc4 filter.

**Table 8-2. PGA854 and ADS127Lx1 FFT Data Summary, OSR = 64, Sinc4 Filter**

PGA GAIN (V/V)	INPUT AMPLITUDE (V <sub>PP</sub> )	SNR (dB)	THD (dB)	ENOB (Bits)
0.5	16.6	107.28	-110.4	17.24
1	8.28	106.42	-109.17	17.08
2	4.14	106.79	-109.93	17.16
5	1.66	103.48	-108.83	16.71
10	0.83	99.03	-108.35	16.08
20	0.41	92.75	-106.19	15.08
50	0.17	86.32	-101.12	14.02
100	0.08	80.21	-94.02	13

**Table 8-3. PGA854 and ADS127Lx1 FFT Data Summary, OSR = 64, Wideband Filter**

PGA GAIN (V/V)	INPUT AMPLITUDE (V <sub>PP</sub> )	SNR (dB)	THD (dB)	ENOB (Bits)
0.5	16.6	105.36	-110.12	17.00
1	8.28	105.22	-109.12	16.94
2	4.14	105.45	-109.96	17.01
5	1.66	102.83	-108.62	16.62
10	0.83	98.7	-108.64	16.03
20	0.41	93.15	-104.83	15.13
50	0.17	85.67	-99.43	13.91
100	0.08	79.8	-93.67	12.93

The R-C-R differential low-pass filter at the input of the instrumentation amplifier helps reduce EMI/RFI high-frequency extrinsic noise. This filter is customizable per the bandwidth and application requirements. This design example (see [Figure 8-9](#)) suggests a filter with the capacitor ratio of  $C_{IN\_DIFF} = 10 \times C_{IN\_CM}$ . Using

the 10:1 ratio for differential capacitor  $C_{IN\_DIFF}$  versus common-mode capacitors  $C_{IN\_CM}$  offers good differential and common-mode noise rejection. This arrangement tends to be less sensitive to the tolerance variation and mismatch of the filter capacitors. In the measurement above a narrow-band input filter is used to limit the noise and harmonics from the source waveform generator.

The feedback capacitor,  $C_{FB}$ , is in parallel with the PGA854 output-stage 6.67k $\Omega$  feedback resistors to help implement additional noise filtering. The internal resistors have  $\pm 15\%$  absolute resistance variation; take this variation into account when implementing noise filtering. In this example,  $C_{FB}$  is set to 680pF, providing a typical  $f_{-3dB}$  corner frequency of 35kHz. The estimated minimum  $f_{-3dB}$  corner frequency for this circuit is approximately 30kHz when accounting for the feedback-resistor variation.

The filter at the ADS127Lx1 inputs works as a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion and low gain error that otherwise potentially degrade because of incomplete amplifier settling. The ADC input filter values are  $R_{FIL} = 47.4\Omega$ ,  $C_{DIFF} = 470\text{pF}$ , and  $C_{CM} = 47\text{pF}$ . The ADC input precharge buffers significantly reduce the sample-phase input charge that raises the ADC input impedance to decrease gain error.

High-grade COG (NPO) are used everywhere in the signal path ( $C_{IN\_DIFF}$ ,  $C_{IN\_CM}$ ,  $C_{FB}$ ,  $C_{DIFF}$ ,  $C_{CM}$ ) for low distortion. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance accuracy. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

## 8.3 Power Supply Recommendations

The nominal performance of the PGA854 is specified with input-stage supply and output-stage supply voltages of  $\pm 15\text{V}$ , and  $V_{\text{ICM}}$  and  $V_{\text{OCM}}$  at mid-supply. Within the specified limits, custom input common-mode and output common-mode voltages are usable without compromising performance; see also [Section 6.3](#). To prevent damage to internal circuitry, the output-stage power supplies are clamped to stay within the input-stage supply voltage levels; see also [Section 7.2](#).

### CAUTION

Supply voltages greater than 40V ( $\pm 20\text{V}$ ) permanently damage the device. Parameters that vary over supply voltage or temperature are shown in [Section 6.6](#) of this data sheet.

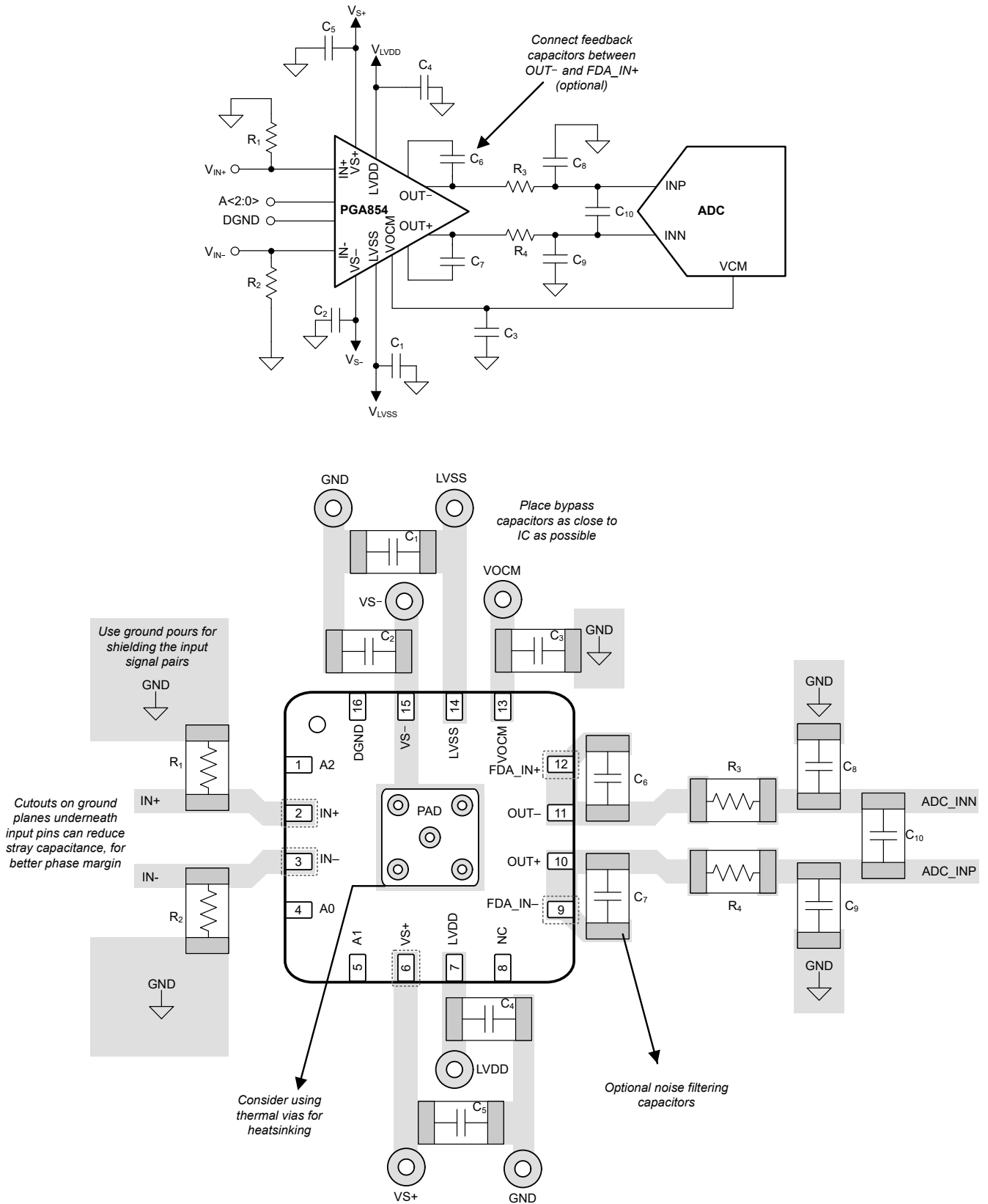
## 8.4 Layout

### 8.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), verify both input paths are symmetrical and well-matched for source impedance and capacitance.
- Noise potentially propagates into analog circuitry through the power pins of the device and of the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1  $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from  $V+$  to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Leakage on the  $\text{FDA\_IN+}$  and  $\text{FDA\_IN-}$  pins potentially causes a dc offset error in the output voltages. Additionally, excessive parasitic capacitance at these pins potentially results in decreased phase margin and affects the stability of the output stage. If these pins are not used to implement deliberate capacitive feedback, follow best practices to minimize leakage and parasitic capacitance.
- Follow best practices to minimize leakage and parasitic capacitance, which includes implementing *keep-out* areas in any ground planes located immediately below the input pins.
- Minimize the number of thermal junctions. If possible, route the signal path using a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device so that the thermal energy source effects on both sides of the differential signal path are evenly matched.
- Keep the traces as short as possible.

### 8.4.2 Layout Example



**Figure 8-10. Example Schematic and Associated PCB Layout**

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Development Support

##### 9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype designs before committing to layout and fabrication, reducing development cost and time to market.

##### 9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design and simulation tools](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

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### 9.2 Documentation Support

#### 9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Comprehensive Error Calculation for Instrumentation Amplifiers application note](#)
- Texas Instruments, [Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications application note](#)
- Texas Instruments, [ADS127L21 512kSPS, Programmable Filter, 24-Bit, Wideband Delta-Sigma ADC data sheet](#)

### 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.5 Trademarks

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TINA™ is a trademark of DesignSoft, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

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## 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2025) to Revision A (December 2025)	Page
• Changed the document status from <i>Advance Information</i> to <i>Production Data</i> .....	1
• Changed common mode input impedance from 7pF to 4.4pF.....	6
• Changed differential input voltage limits from $\pm 20V$ to $\pm 16V$ .....	6
• Modified CMRR for G = 2, 10, and 20 from 81dB, 96dB, and 102dB to 80dB, 95dB, and 100dB respectively. 6	6
• Added the Voltage Noise section.....	6
• Modified GE maximum values for different gains from 0.03% to 0.035%, from 0.04% to 0.045%, and from 0.05% to 0.055% respectively.....	6
• Modified Nonlinearity test conditions for G=0.5 from VOUT=10V to 8V.....	6
• Added the differential gain nonlinearity parameter values.....	6
• Changed the BW parameter value for G=10,20 from 4.2MHz to 5MHz.....	6
• Modified slew rate test conditions for G=0.5 from VOUT=10V to 8V.....	6
• Added Slew Rate , and Gain Switching Time parameter values, and Settling Time parameter.....	6
• Added the THD and HD2, and HD3 parameters.....	6
• Added VCOM small signal and large signal parameters values.....	6
• Changed IQ_input parameter typical value from 3mA to 3.2mA, and maximum value from 3.7mA to 3.9mA... 6	6
• Changed IQ_input over temprature parameter maximum value from 4.5mA to 4.9mA.....	6
• Added all typical characteristics figures apart from gain error, offset and offset drift distribution, and Gain vs. frequency which existed already in previous version.....	9
• Modified the gain settings block diagram to have current sources at the input instead of resistors.....	20
• Updated the valid ranges for VOVM.....	22
• updated Input common mode vs. output differential voltage curves for G=0.5, G=1, and G=2.....	23
• Added current consumption with differential inputs section.....	24
• Updated the ADS127L11 driver circuit application section. circuit modified, and added measurement results table.....	25
• Modified the RC kickback filter component values.....	26
• Added reference to the typical characteristics section in the caution statement.....	28

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">XPGA854RGTR</a>	Active	Preproduction	VQFN (RGT)   16	5000   LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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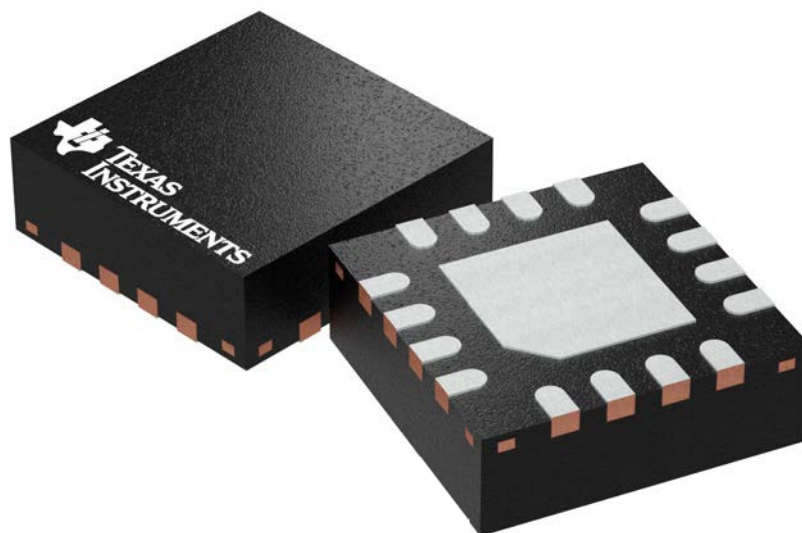


**RGT 16**

**GENERIC PACKAGE VIEW**

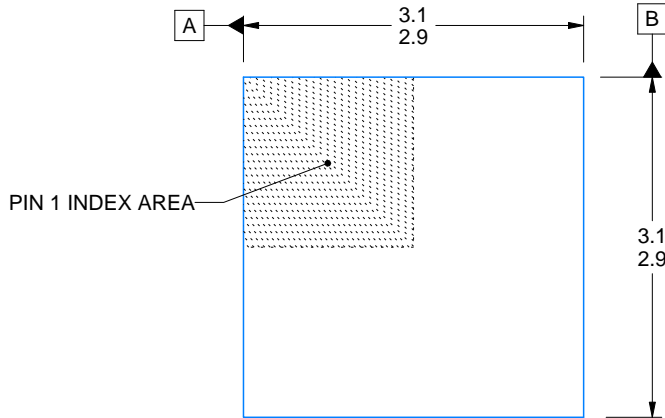
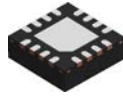
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

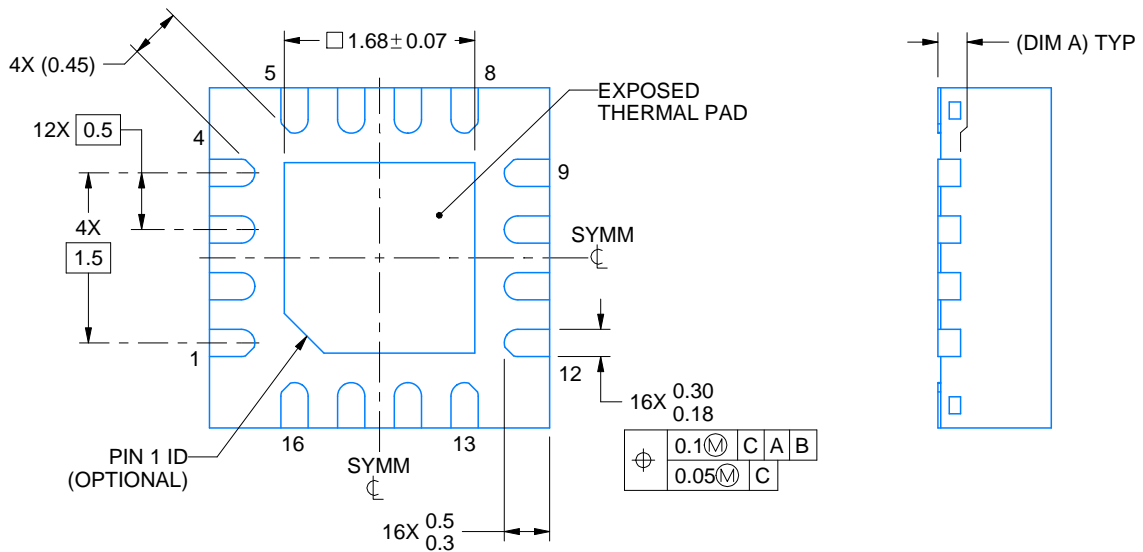
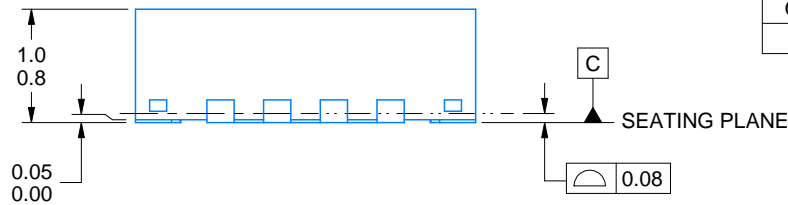


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



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NOTES:

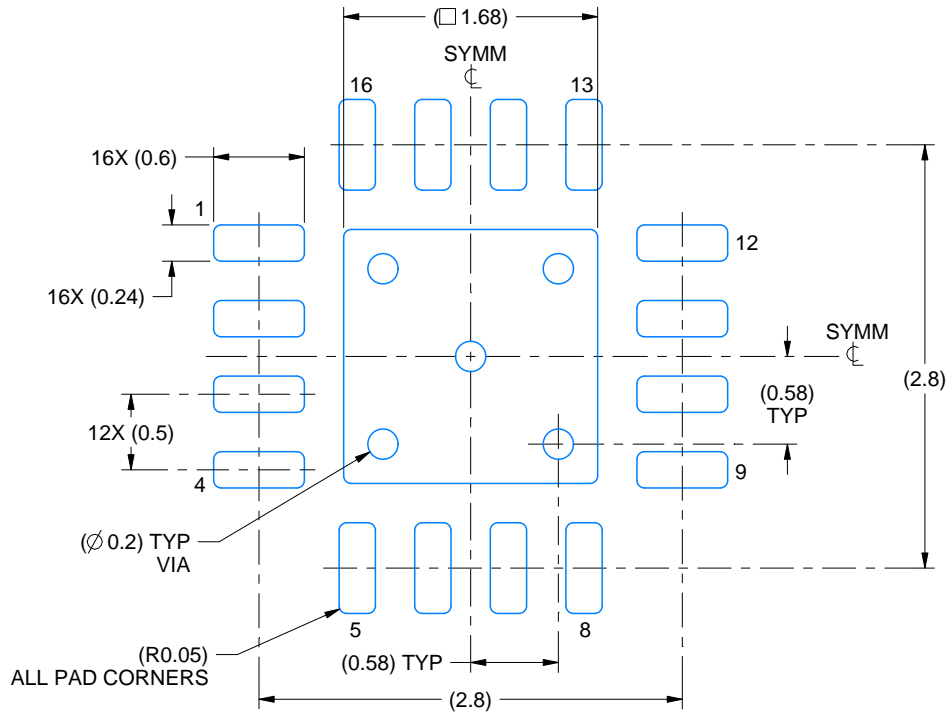
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

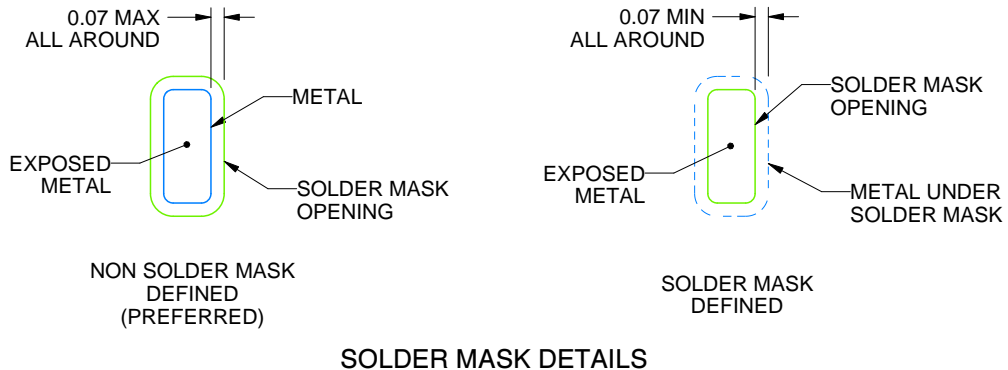
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:20X



**SOLDER MASK DETAILS**

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NOTES: (continued)

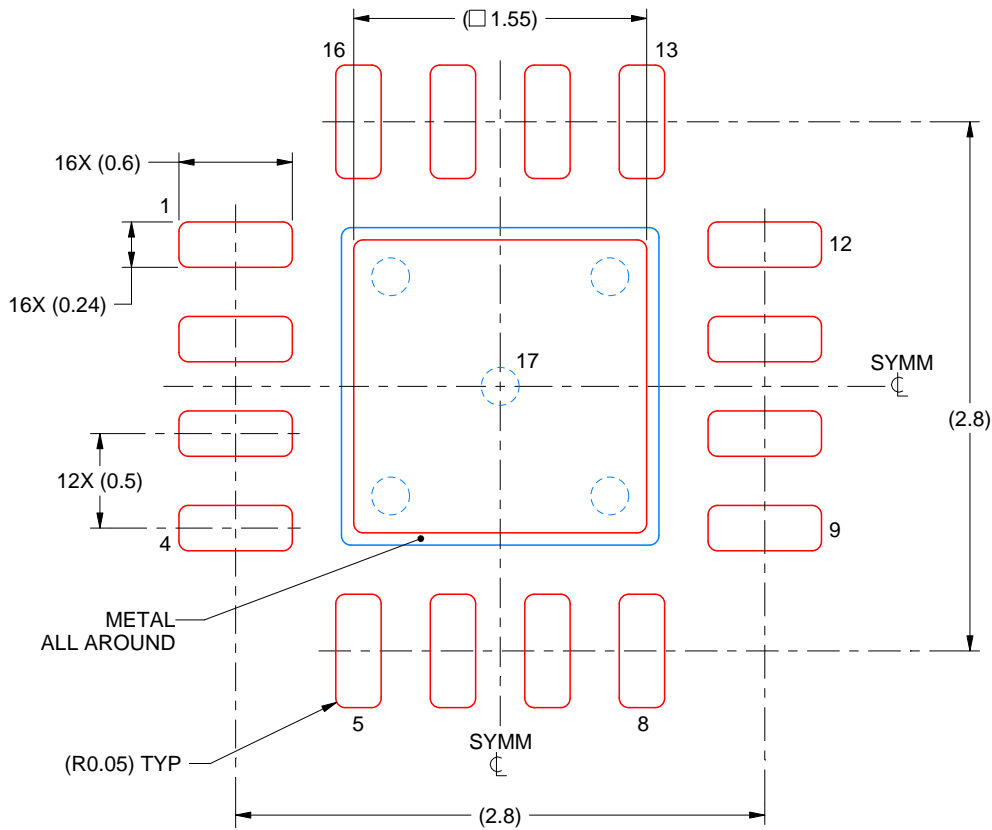
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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