PCM1841-Q1 クワッド チャネル、32 ビット、192kHz、Burr-Brown™ オーディオ ADC

1 特長

- マルチチャネルの高性能 ADC:
  - 4 チャネルのアナログ マイクロフォンまたはライン入力
- ADC ラインおよびマイクロフォンの差動入力性能:
  - ダイナミック レンジ:
    - ダイナミック レンジ エンハンサが有効な状態で 123dB
    - ダイナミック レンジ エンハンサが無効な状態で 113dB
  - THD+N:-98dB
- ADC 差動 $2V_{RMS}$ フルスケール入力
- ADC サンプル・レート (f_S):8kHz～192kHz
- ハードウェア ピン制御構成
- 線形位相または低レイテンシ フィルタを選択可能
- 柔軟なオーディオ シリアル データ インターフェイス
  - コントローラまたはターゲットのインターフェイス選択
  - 32 ビット、4 チャネル TDM
  - 32 ビット、2 チャネル TDM
  - 32 ビット、2 チャネル I^2S
  - 32 ビット、2 チャネル LJ (左揃え)
- オーディオ クロック喪失時の自動パワーダウン
- 高性能オーディオ PLL を内蔵
- 低ノイズ MICBIAS 2.75V 出力
- 単一電源動作:3.3V
- I/O 電源動作:3.3V または 1.8V
- 3.3V AVDD 電源での消費電力:
  - 17.0 mW/チャネル (サンプル レート:16kHz)
  - 18.4 mW/チャネル (サンプル レート:48kHz)

2 アプリケーション

- テレマティクス制御ユニット
- 車載用ヘッド ユニット
- デジタル コックピット処理装置
- 車載ディスプレイ モジュール

3 概要

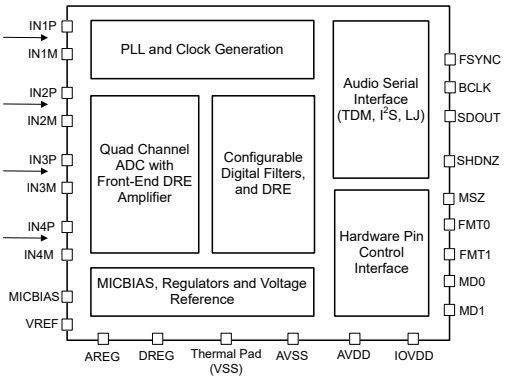
PCM1841-Q1 は、最大 4 つのアナログ チャネルの同時サンプリングをサポートする高性能 Burr-Brown™ オーディオ A/D コンバータ (ADC) です。本デバイスは、$2V_{RMS}$ フルスケール信号の差動ラインおよびマイクロフォン入力をサポートしています。マイクロフォン バイアス電圧、位相ロック ループ (PLL)、DC 除去ハイパス フィルタ (HPF) を内蔵し、最高 192kHz のサンプル レートに対応しています。TDM (時分割多重)、I^2S、LJ (左揃え) オーディオ フォーマットをサポートしており、これらのフォーマットはハードウェア ピンのレベルで選択できます。また PCM1841-Q1 は、オーディオ バス インターフェイス動作をコントローラ モードまたはターゲット モードに選択できます。これらの高性能な機能を内蔵し、かつ 3.3V 単一電源で動作できることから、本デバイスは、低コストと省スペースが求められる遠距離マイクロフォン録音アプリケーションのオーディオ システムに理想的な選択肢です。

PCM1841-Q1 は -40℃～+125℃で動作が規定されており、24 ピンの VQFN パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)	本体サイズ (公称)
PCM1841-Q1	RGE (VQFN、24)	4.00mm × 4.00mm	4.00mm × 4.00mm(3)

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 0.5mm ピッチを含みます。



概略ブロック図

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4 Pin Configuration and Functions

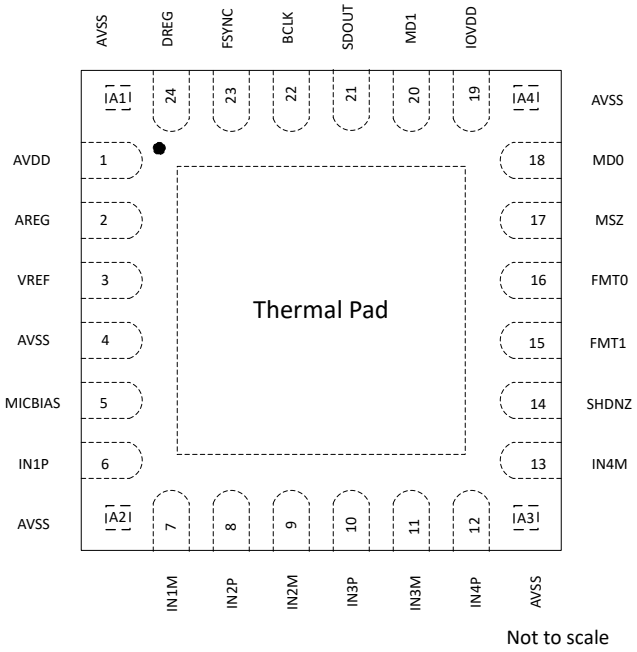

図 4-1. RGE Package, 24-Pin VQFN With Exposed Thermal Pad, Top View

表 4-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	AVDD	P	Analog power (3.3V, nominal)
2	AREG	P	Analog on-chip regulator output voltage for analog supply (1.8V, nominal)
3	VREF	O	Analog reference voltage filter output
4	AVSS	GND	Analog ground. Short this pin directly to the board ground plane.
5	MICBIAS	O	MICBIAS output
6	IN1P	I	Analog input 1P pin
7	IN1M	I	Analog input 1M pin
8	IN2P	I	Analog input 2P pin
9	IN2M	I	Analog input 2M pin
10	IN3P	I	Analog input 3P pin
11	IN3M	I	Analog input 3M pin
12	IN4P	I	Analog input 4P pin
13	IN4M	I	Analog input 4M pin
14	SHDNZ	I	Digital input. Device hardware shutdown and reset (active low)
15	FMT1	I	Digital input. Audio interface format select 1 pin
16	FMT0	I	Digital input. Audio interface format select 0 pin
17	MSZ	I	Digital input. Audio interface bus controller or target select pin
18	MD0	I	Digital input. Device configuration mode select 0 pin
19	IOVDD	P	Digital I/O power supply (1.8V or 3.3V, nominal)
20	MD1	I	Digital input. Device configuration mode select 1 pin
21	SDOUT	O	Digital output. Audio serial data interface bus output
22	BCLK	I/O	Audio serial data interface bus bit clock

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表 4-1. Pin Functions (続き)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
23	FSYNC	I/O	Audio serial data interface bus frame synchronization signal
24	DREG	P	Digital regulator output voltage for digital core supply (1.5V, nominal)
A1, A2,A3, A4	AVSS	GND	Analog ground. Short this pin directly to the board ground plane.
Thermal Pad (VSS)		GND	Thermal pad shorted to internal device ground. Short thermal pad directly to board ground plane.

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

5 Specifications

5.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AVSS	–0.3	3.9	V
	AREG to AVSS	–0.3	2.0	
	IOVDD to VSS (thermal pad)	–0.3	3.9	
Ground voltage differences	AVSS to VSS (thermal pad)	–0.3	0.3	V
Analog input voltage	Analog input pins voltage to AVSS	–0.3	AVDD + 0.3	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charge device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD, AREG(1)	Analog supply voltage AVDD to AVSS (AREG is generated using onchip regulator) - AVDD 3.3V operation	3.0	3.3	3.6	V
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8V operation	1.65	1.8	1.95	
INPUTS					
	Analog input pins voltage to AVSS	0		AVDD	V
	Digital input pins voltage to VSS (thermal pad)	0		IOVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C
OTHERS					
	Digital input pin used as MCLK input clock frequency			36.864	MHz

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5.3 Recommended Operating Conditions (続き)

		MIN	NOM	MAX	UNIT
C_L	Digital output load capacitance		20	50	pF

(1) AVSS and VSS (thermal pad): all ground pins must be tied together and must not differ in voltage by more than 0.2V.

5.4 Thermal Information

THERMAL METRIC(1)		PCM1841-Q1 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32 bit audio data, BCLK = 256 × f_S, TDM target mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC CONFIGURATION						
	AC input impedance	Input pins INxP or INxM		2.5		kΩ
ADC PERFORMANCE FOR LINE/MICROPHONE INPUT RECORDING : AVDD 3.3V OPERATION						
	Differential input full-scale AC signal voltage	AC-coupled input		2		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	IN1 differential input selected and AC signal shorted to ground, DRE enabled (DRE_LVL = –36dB, DRE_MAXGAIN = 24dB)	115	122		dB
		IN1 differential input selected and AC signal shorted to ground, DRE disabled	106	112		
DR	Dynamic range, A-weighted(2)	IN1 differential input selected and –60dB full-scale AC signal input, DRE enabled (DRE_LVL = –36dB, DRE_MAXGAIN = 24dB)		123		dB
		IN1 differential input selected and –60dB full-scale AC signal input, DRE disabled		113		
THD+N	Total harmonic distortion(2) (3)	IN1 differential input selected and –1dB full-scale AC signal input, DRE enabled (DRE_LVL = –36dB, DRE_MAXGAIN = 24dB)		–98	–80	dB
		IN1 differential input selected and –1dB full-scale AC signal input, DRE disabled		–98		
ADC OTHER PARAMETERS						
	Output data sample rate		7.35		192	kHz
	Output data sample word length				32	Bits
	Interchannel isolation	–1dB full-scale AC-signal input to non measurement channel		–124		dB
	Interchannel gain mismatch	–6dB full-scale AC-signal input		0.1		dB
	Gain drift	across temperature range 15°C to 35°C		–4.4		ppm/°C
	Interchannel phase mismatch	1kHz sinusoidal signal		0.02		Degrees

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5.5 Electrical Characteristics (続き)

at T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32 bit audio data, BCLK = 256 × f_S, TDM target mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Phase drift	1kHz sinusoidal signal, across temperature range 15°C to 35°C		0.0005		Degrees/°C
PSRR	Power-supply rejection ratio	100mV_{PP}, 1kHz sinusoidal signal on AVDD, differential input selected, 0dB channel gain		102		dB
CMRR	Common-mode rejection ratio	Differential microphone input selected, 100mV_{PP}, 1kHz signal on both pins and measure level at output		60		dB
MICROPHONE BIAS						
	MICBIAS noise	BW = 20Hz to 20kHz, A-weighted, 1µF capacitor between MICBIAS and AVSS		1.6		μV_{RMS}
	MICBIAS voltage			VREF		V
	MICBIAS current drive				20	mA
	MICBIAS load regulation	Measured up to max load	0	0.6	1.8	%
	MICBIAS over current protection threshold		22			mA
DIGITAL I/O						
$V_{IL(SHDNZ)}$	Low-level digital input logic voltage threshold	SHDNZ pin	–0.3		0.25 × IOVDD	V
$V_{IH(SHDNZ)}$	High-level digital input logic voltage threshold	SHDNZ pin	0.75 × IOVDD		IOVDD + 0.3	V
V_{IL}	Low-level digital input logic voltage threshold	All digital pins, IOVDD 1.8V operation	–0.3		0.3 × IOVDD	V
		All digital pins, IOVDD 3.3V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins, IOVDD 1.8V or 3.3V operation	0.7 × IOVDD		IOVDD + 0.3	V
V_{OL}	Low-level digital output voltage	All digital pins, I_{OL} = –2mA, IOVDD 1.8V operation			0.45	V
		All digital pins, I_{OL} = –2mA, IOVDD 3.3V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins, I_{OH} = 2mA, IOVDD 1.8V operation	IOVDD – 0.45			V
		All digital pins, I_{OH} = 2mA, IOVDD 3.3V operation	2.4			
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, input = IOVDD	–5	0.1	5	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, input = 0V	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in hardware shutdown mode	SHDNZ = 0, AVDD = 3.3V, internal AREG		1		µA
I_{IOVDD}		SHDNZ = 0, all external clocks stopped, IOVDD = 3.3V		0.2		
I_{IOVDD}		SHDNZ = 0, all external clocks stopped, IOVDD = 1.8V		0.15		
I_{AVDD}	Current consumption with ADC 4 channel operating at f_S 16kHz, BCLK = 256 × f_S and DRE disable	AVDD = 3.3V, internal AREG		21.3		mA
I_{IOVDD}		IOVDD = 3.3V		0.15		
I_{IOVDD}		IOVDD = 1.8V		0.04		
I_{AVDD}	Current consumption with ADC 4 channel operating at f_S 48kHz, BCLK = 256 × f_S and DRE disable	AVDD = 3.3V, internal AREG		22.9		mA
I_{IOVDD}		IOVDD = 3.3V		0.25		
I_{IOVDD}		IOVDD = 1.8V		0.1		
I_{AVDD}	Current consumption with ADC 4 channel operating at f_S 48kHz, BCLK = 256 × f_S and DRE enable	AVDD = 3.3V, internal AREG		25.0		mA
I_{IOVDD}		IOVDD = 3.3V		0.25		
I_{IOVDD}		IOVDD = 1.8V		0.1		

(1) Ratio of output level with 1kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

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(3) For best distortion performance, use input AC-coupling capacitors with low-voltage-coefficient.

5.6 Timing Requirements: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see 図 5-1 for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period		40			ns
$t_{H(BCLK)}$	BCLK high pulse duration (1)		18			ns
$t_{L(BCLK)}$	BCLK low pulse duration (1)		18			ns
$t_{SU(FSYNC)}$	FSYNC setup time		8			ns
$t_{HLD(FSYNC)}$	FSYNC hold time		8			ns
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time			10	ns
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time			10	ns

(1) The BCLK minimum high or low pulse duration must be higher than 25ns (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

5.7 Switching Characteristics: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see 図 5-1 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDOUT-BCLK)}$	BCLK to SDOUT delay	50% of BCLK to 50% of SDOUT			18	ns
$t_{d(SDOUT-FSYNC)}$	FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0)	50% of FSYNC to 50% of SDOUT			18	ns
$f_{(BCLK)}$	BCLK output clock frequency: controller mode (1)				24.576	MHz
$t_{H(BCLK)}$	BCLK high pulse duration: controller mode		14			ns
$t_{L(BCLK)}$	BCLK low pulse duration: controller mode		14			ns
$t_{d(FSYNC)}$	BCLK to FSYNC delay: controller mode	50% of BCLK to 50% of FSYNC			18	ns
$t_{r(BCLK)}$	BCLK rise time: controller mode	10% - 90% rise time			8	ns
$t_{f(BCLK)}$	BCLK fall time: controller mode	90% - 10% fall time			8	ns

(1) The BCLK output clock frequency must be lower than 18.5MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

5.8 Timing Diagram

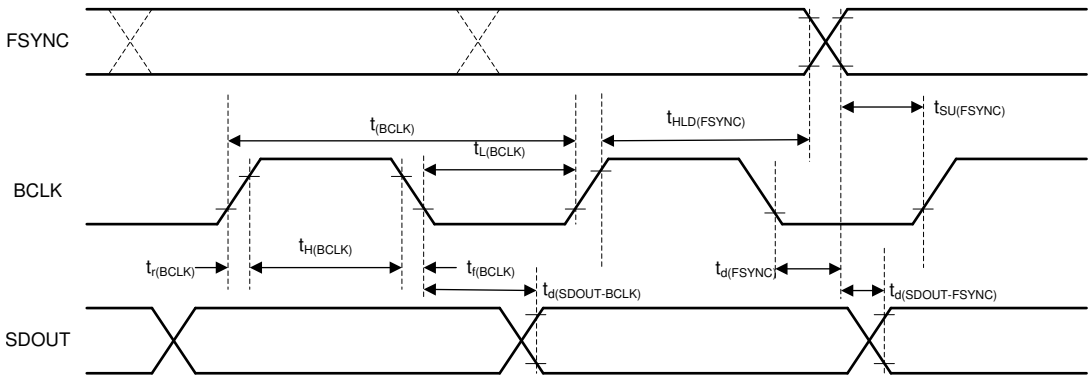

図 5-1. TDM, I²S, and LJ Interface Timing Diagram

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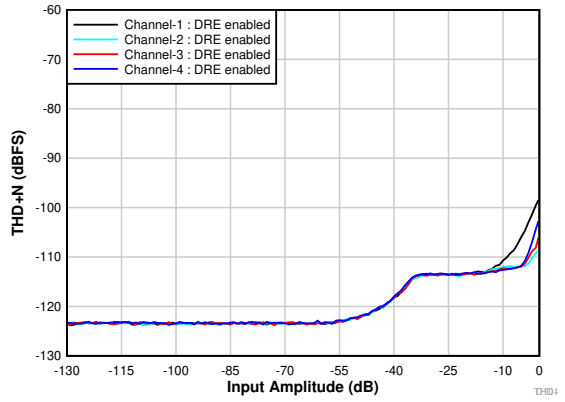
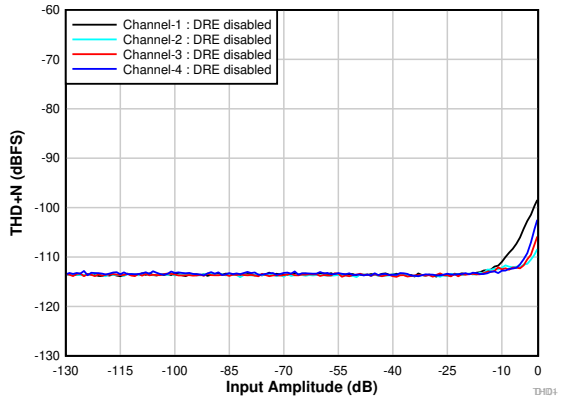
5.9 Typical Characteristics

at T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode, PLL on, DRE_LVL = –36dB, channel gain = 0dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20kHz, low-pass filter, and an A-weighted filter



Differential input

図 5-2. THD+N vs Input Amplitude With DRE Enabled



Differential input

図 5-3. THD+N vs Input Amplitude With DRE Disabled

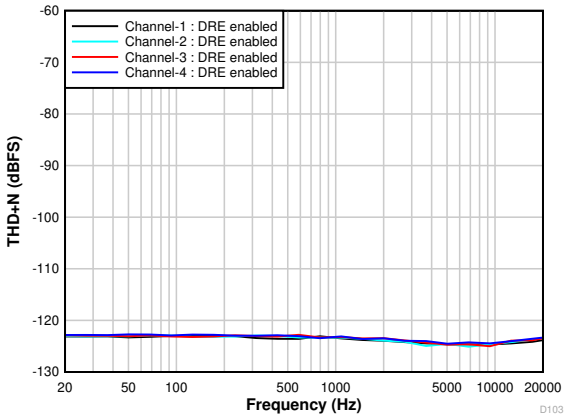


図 5-4. THD+N vs Input Frequency With a –60dBr Input

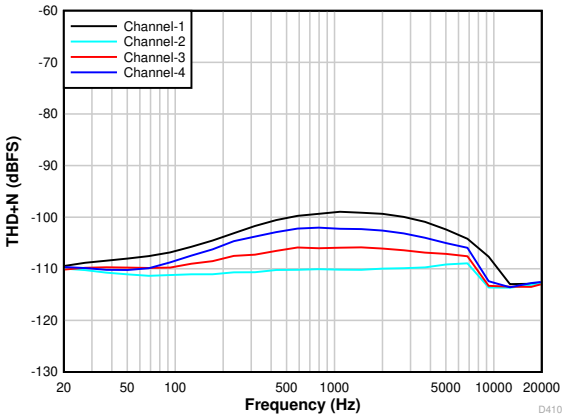


図 5-5. THD+N vs Input Frequency With a –1dBr Input

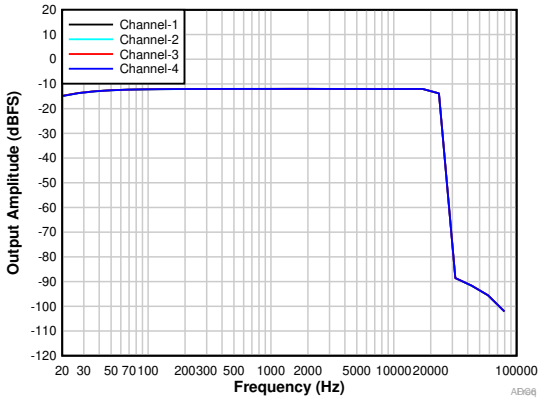


図 5-6. Frequency Response With a –12dBr Input

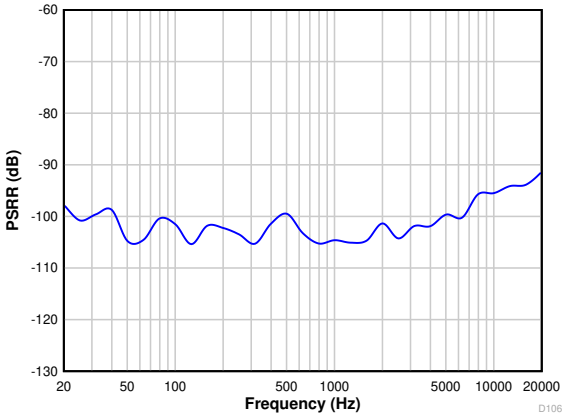


図 5-7. Power-Supply Rejection Ratio vs Ripple Frequency With 100mV$_{PP}$ Amplitude

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode, PLL on, DRE_LVL = –36dB, channel gain = 0dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20kHz, low-pass filter, and an A-weighted filter

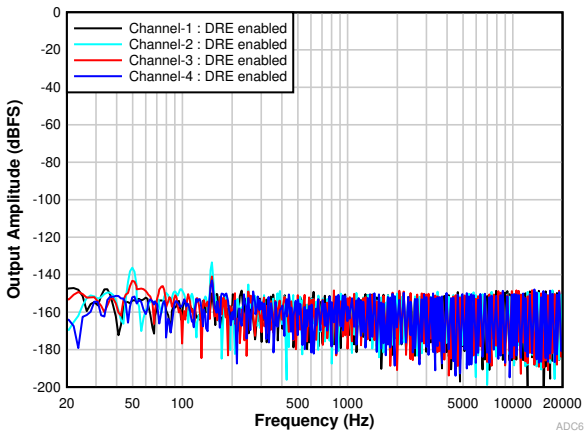


図 5-8. FFT With Idle Input With DRE Enabled

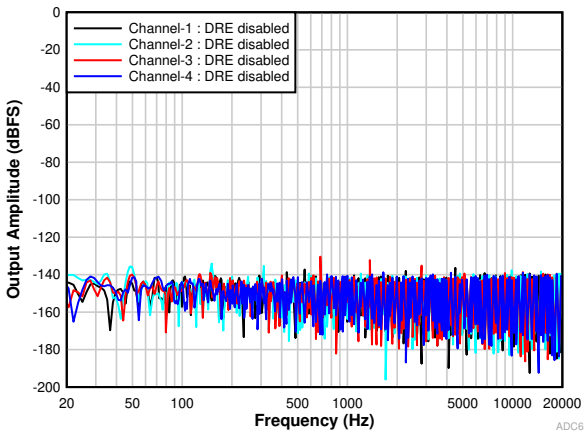


図 5-9. FFT With Idle Input With DRE Disabled

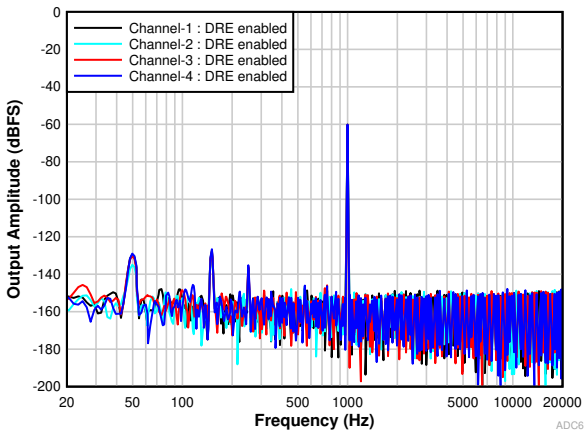


図 5-10. FFT With a –60dBr Input With DRE Enabled

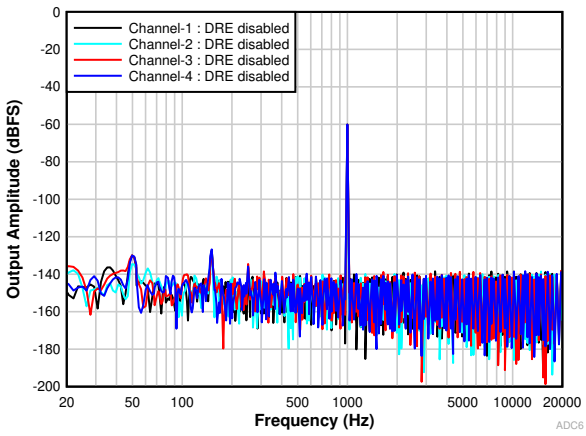


図 5-11. FFT With a –60dBr Input With DRE Disabled

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5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode, PLL on, DRE_LVL = –36dB, channel gain = 0dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20kHz, low-pass filter, and an A-weighted filter

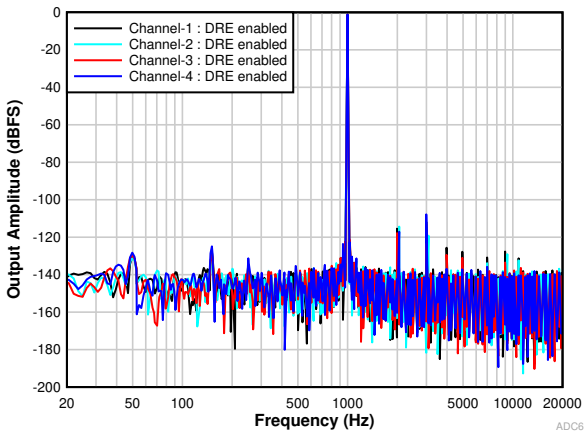

図 5-12. FFT With a –1dBr Input With DRE Enabled

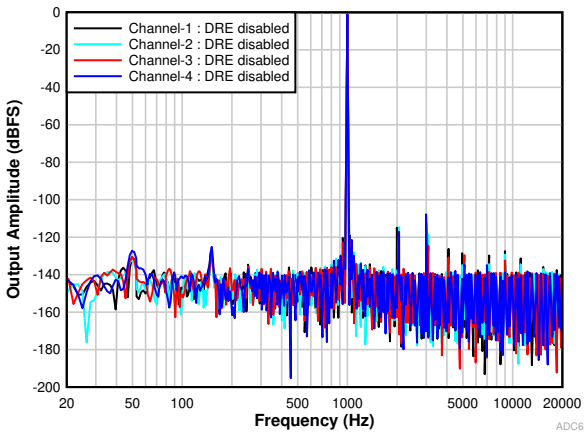

図 5-13. FFT With a –1dBr Input With DRE Disabled

6 Detailed Description

6.1 Overview

The PCM1841-Q1 is a high-performance, low-power, quad-channel, audio analog-to-digital converter (ADC) with flexible audio interface control options. This device is intended for applications in voice-activated systems, AV receivers, TV and blu-ray players, professional microphones, audio conferencing, portable computing, communication, and entertainment applications. The high dynamic range of the device enables far-field audio recording with high fidelity. This device integrates a host of features that reduce costs, board space, and power consumption in space-constrained, battery-powered, consumer, home, and industrial applications. The device features are controlled through hardware by pulling pins high or low with resistors or a controller GPIO. The PCM1841-Q1 also supports a power-down and reset function by means of halting the system clock.

The PCM1841-Q1 consists of the following blocks and features:

- Quad-channel, multibit, high-performance delta-sigma (ΔΣ) ADC
- Differential audio inputs with a $2V_{RMS}$ full-scale signal
- Low-noise, $1.6\mu V_{RMS}$, microphone bias output
- Hardware pin control operation to select the device features
- Audio bus serial interface controller or target select option
- Audio bus serial interface format select option
- Audio bus serial interface supported up to 192kHz sampling
- Target mode supports dynamic range enhancer (DRE) with 123dB dynamic range
- Target mode supports decimation filters with linear-phase or low-latency filter selection
- Controller mode operation supported using system clock of 256 × f_S or 512 × f_S
- Power-down function by means of halting the audio clocks
- Integrated high-pass filter (HPF) that removes the DC component of the input signal
- Integrated low-jitter phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply 3.3V operation

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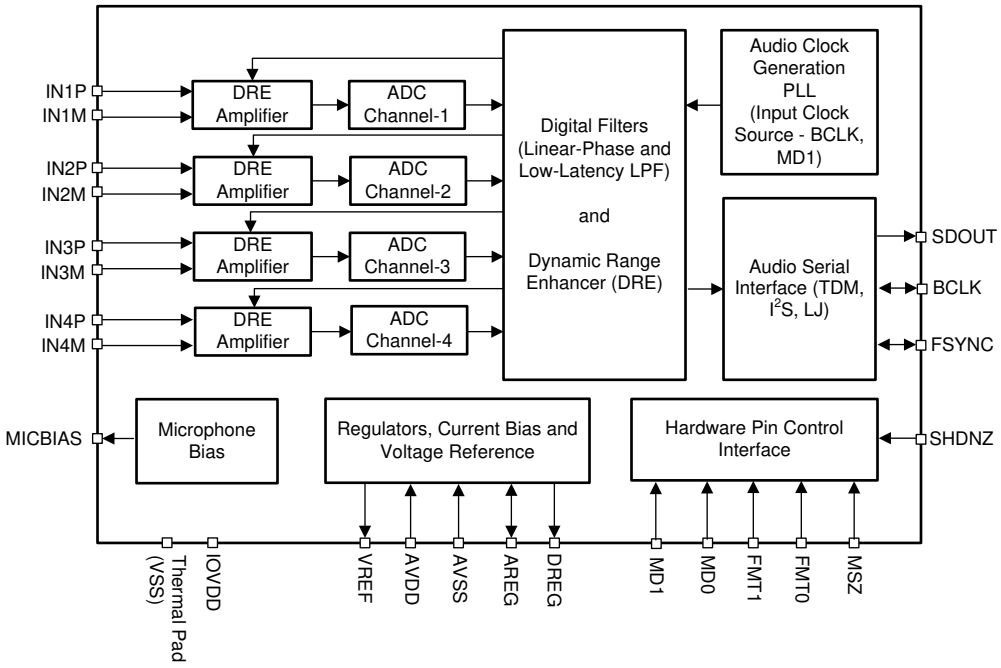
6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Hardware Control

This device enables simple, pin-controlled hardware select a specific mode of operation and audio interface for a given system. The MSZ, MD0, MD1, FMT0, and FMT1 pins allow the device to be controlled by either pullup or pulldown resistors as well as the GPIO from a digital device.

6.3.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the PCM1841-Q1 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for I^2S or left-justified protocols format, and the pin-selectable controller-target configuration for bus clock lines.

The device supports audio bus controller or target mode of operation using the hardware pin MSZ. FSYNC and BCLK work as input pins in target mode, whereas, FSYNC and BCLK work as output pins generated by the device in controller mode.表 6-1 shows the controller and target mode selection using the MSZ pin.

表 6-1. Controller and Target Mode Selection

MSZ	CONTROLLER AND TARGET SELECTION
LOW	Target mode of operation
HIGH	Controller ode of operation

The FMT0 and FMT1 pins can be used to select the bus protocol TDM, I^2S, or left-justified (LJ) format. As shown in 表 6-2, these modes are most significant byte (MSB)-first, pulse code modulation (PCM) data format, with the output channel data word-length of 32 bits.

表 6-2. Audio Serial Interface Format

FMT1	FMT0	AUDIO SERIAL INTERFACE FORMAT
LOW	LOW	4-channel output with time division multiplexing (TDM) mode
LOW	HIGH	2-channel output with time division multiplexing (TDM) mode
HIGH	LOW	2-channel output with left-justified (LJ) mode

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表 6-2. Audio Serial Interface Format (続き)

FMT1	FMT0	AUDIO SERIAL INTERFACE FORMAT
HIGH	HIGH	2-channel output with inter IC sound (I^2S) mode

6.3.2.1 Time Division Multiplexed Audio (TDM) Interface

The rising edge of FSYNC starts the data transfer in TDM mode (also known as DSP mode) with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit is transmitted on the rising edge of BCLK (except the MSB of slot 0 when TX_OFFSET equals 0). 図 6-1 to 図 6-4 illustrate the protocol timing for TDM operation with various configurations.

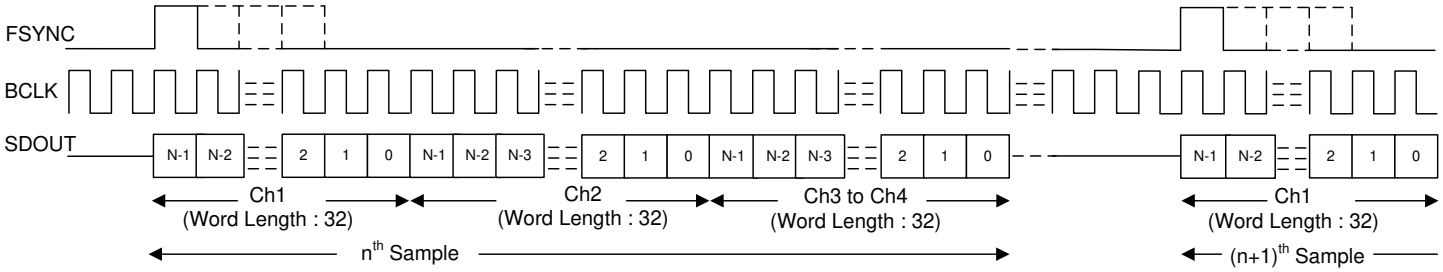

図 6-1. TDM Mode Protocol Timing (FMT0 = LOW) In Target Mode

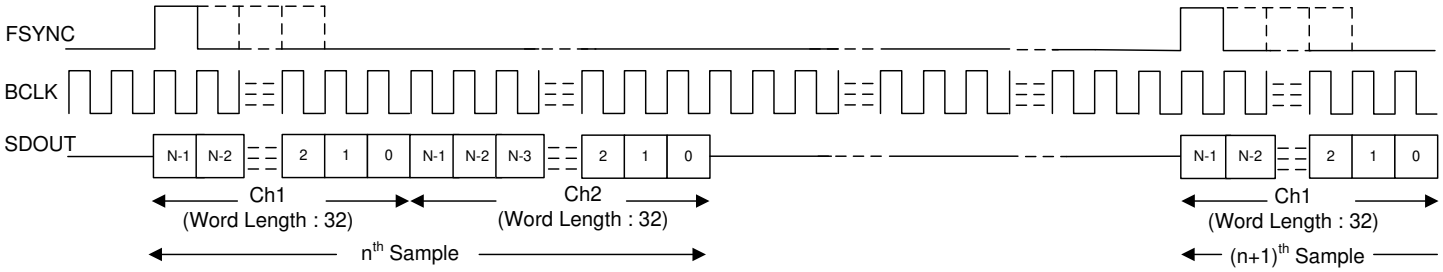

図 6-2. TDM Mode Protocol Timing (FMT0 = HIGH) In Target Mode

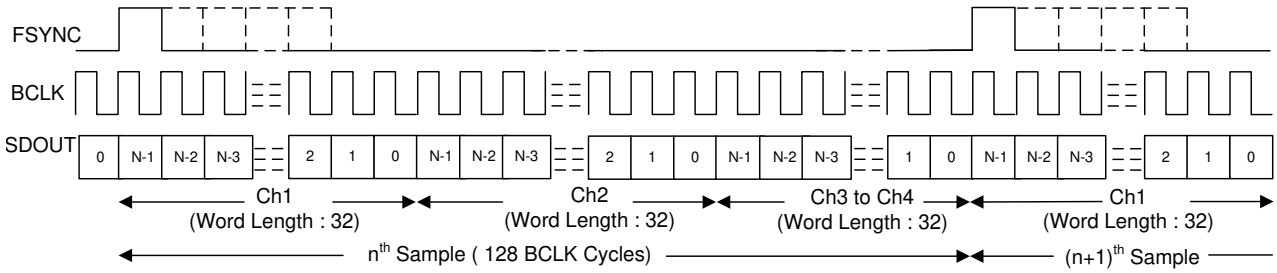

図 6-3. TDM Mode Protocol Timing (FMT0 = LOW) In Controller Mode

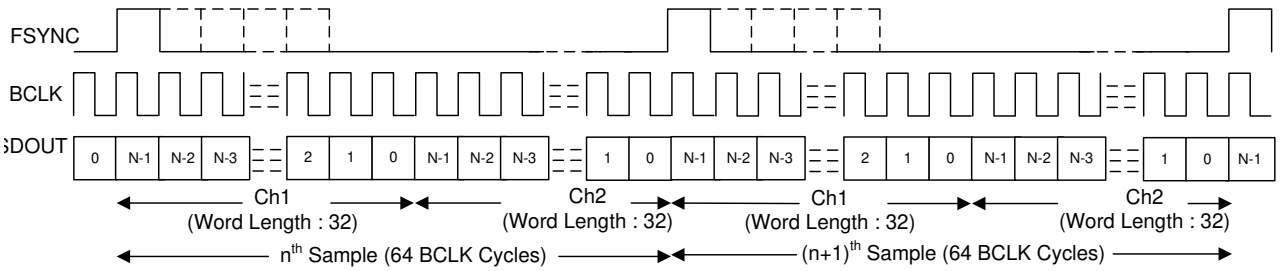

図 6-4. TDM Mode Protocol Timing (FMT0 = HIGH) In Controller Mode

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For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than, or equal to, the number of active output channels times the 32-bits word length of the output channel data. The device transmits a zero data value on SDOUT for the extra unused bit clock cycles. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well.

6.3.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. In I^2S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. In controller mode, FSYNC is transmitted on the rising edge of BCLK. 図 6-5 and 図 6-6 illustrate the protocol timing for I^2S operation in target and controller mode of operation.

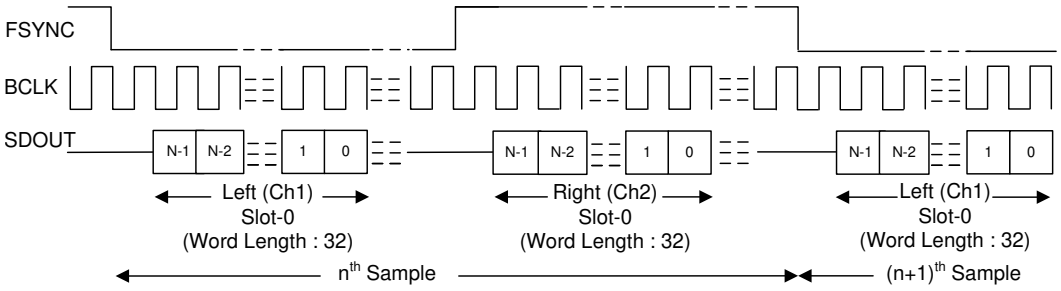

図 6-5. I^2S Mode Protocol Timing in Target Mode

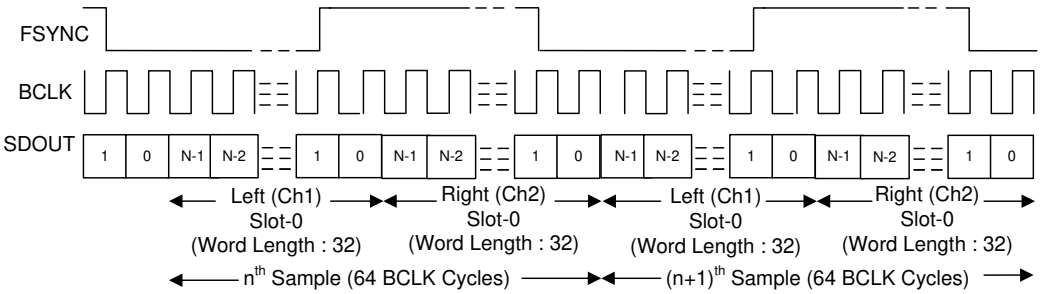

図 6-6. I^2S Protocol Timing In Controller Mode

For proper operation of the audio bus in I^2S mode, the number of bit clocks per frame must be greater than, or equal to, the number of active output channels (including left and right slots) times the 32-bits word length of the output channel data. The device FSYNC low pulse must be atleast Word length(32-bits) times number of active left channels, BCLK cycles wide. Similarly, the FSYNC high pulse must be atleast Word length(32-bits) times number of active right channels, BCLK cycles wide. The device transmits zero data value on SDOUT for the extra unused bit clock cycles.

6.3.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. The MSB of the right slot 0 is transmitted in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. In controller mode, FSYNC is transmitted on the rising edge of BCLK. 図 6-7 and 図 6-8 illustrate the protocol timing for LJ operation in target and controller mode of operation.

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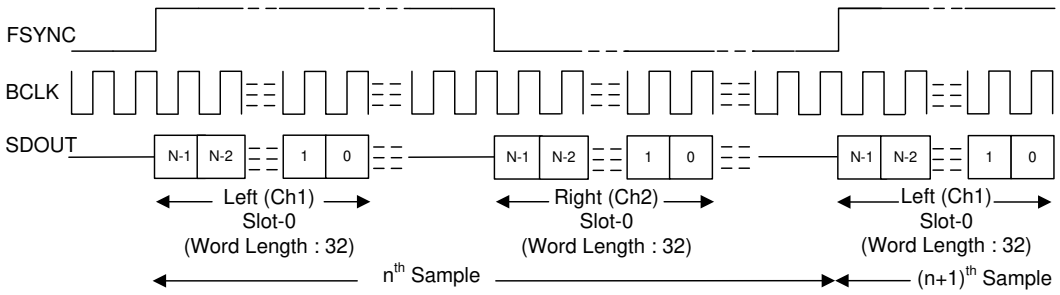

図 6-7. LJ Mode Protocol Timing In Target Mode

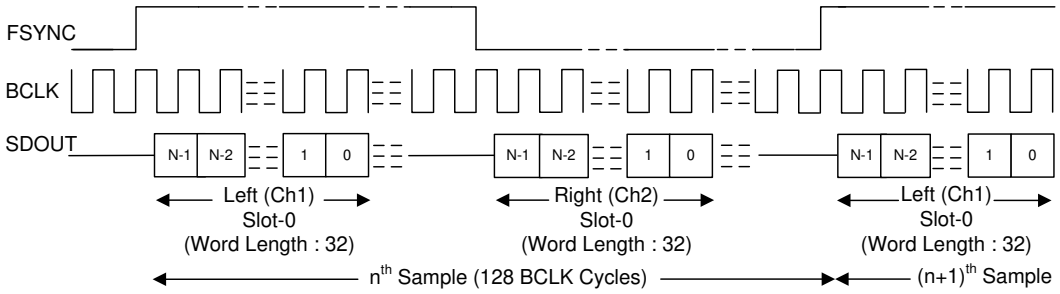

図 6-8. LJ Mode Protocol Timing In Controller Mode

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than, or equal to, the number of active output channels (including left and right slots) times the 32-bit word length of the output channel data. The device FSYNC high pulse must be atleast Word length(32-bits) times number of active left channels, BCLK cycles wide. Similarly, the FSYNC low pulse must be atleast Word length(32-bits) times number of active right channels, BCLK cycles wide. The device transmits zero data value on SDOUT for the extra unused bit clock cycles.

6.3.3 Phase-Locked Loop (PLL) and Clock Generation

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC modulator and digital filter engine, as well as other control blocks.

In target mode of operation, the device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. 表 6-3 and 表 6-4 list the supported FSYNC and BCLK frequencies.

表 6-3. Supported FSYNC (Multiples or Submultiples of 48kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8kHz)	FSYNC (16kHz)	FSYNC (24kHz)	FSYNC (32kHz)	FSYNC (48kHz)	FSYNC (96kHz)	FSYNC (192kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**

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表 6-3. Supported FSYNC (Multiples or Submultiples of 48kHz) and BCLK Frequencies (続き)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8kHz)	FSYNC (16kHz)	FSYNC (24kHz)	FSYNC (32kHz)	FSYNC (48kHz)	FSYNC (96kHz)	FSYNC (192kHz)
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**

表 6-4. Supported FSYNC (Multiples or Submultiples of 44.1kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35kHz)	FSYNC (14.7kHz)	FSYNC (22.05kHz)	FSYNC (29.4kHz)	FSYNC (44.1kHz)	FSYNC (88.2kHz)	FSYNC (176.4kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**

In the controller mode of operation, the device uses the MD1 pin (as system clock, MCLK) as the reference input clock source with supported system clock frequency option of either 256 × f_S or 512 × f_S as configured using the MD0 pin. 表 6-5 shows the system clock selection for the controller mode using the MD0 pin.

表 6-5. System Clock Selection for the Controller Mode

MD0	SYSTEM CLOCK SELECTION (Valid for Controller Mode Only)
LOW	System clock with frequency 256 × f_S connected to pin MD1 as MCLK
HIGH	System clock with frequency 512 × f_S connected to pin MD1 as MCLK

See 表 6-7 and 表 6-20 for the MD0 and MD1 pin function in the target mode of operation.

6.3.4 Input Channel Configurations

The device consists of four pairs of analog input pins (INxP and INxM) as differential inputs for the recording channel. The device supports simultaneous recording of up to four channels using the high-performance multichannel ADC. The input source for the analog pins can be from the electret condenser analog microphones, micro electrical-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board.

The voice or audio signal inputs must be capacitively coupled (AC-coupled) to the device. For better distortion performance, use the low-voltage coefficient capacitors for AC coupling. The device has the typical input impedance on INxP or INxM as 2.5kΩ on each pin. The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power-up. The device has a quick charge scheme that increases the charging speed of the coupling capacitor at power-up. The default value of the quick-charge timing is set for a coupling capacitor up to 1µF.

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6.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The PCM1841-Q1 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1µF capacitor connected from the VREF pin to analog ground (AVSS). The value of this reference voltage, VREF, is set to 2.75V, which in turn supports a $2V_{RMS}$ differential full-scale input to the device. The required minimum AVDD voltage for this VREF voltage is 3V. Do not connect any external load to a VREF pin.

6.3.6 Microphone Bias

The device integrates a built-in, low-noise, $1.6\mu V_{RMS}$ microphone bias pin with an output voltage of 2.75V that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphone. The integrated bias amplifier supports up to 20mA of load current that can be used for multiple microphones and is designed to provide a combination of high PSRR and low noise bias voltages to bias microphones for high-end audio applications. When using this MICBIAS pin for biasing or supplying to multiple microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones.

6.3.7 Signal-Chain Processing

The PCM1841-Q1 signal chain is comprised of very-low-noise, high-performance, low-power analog blocks and highly flexible, programmable digital processing blocks. This high performance and flexibility, combined with a compact package, makes the PCM1841-Q1 excellent for a variety of end-equipments and applications that require multichannel audio capture. 図 6-9 shows a conceptual block diagram that highlights the various building blocks used in the signal chain and how the blocks interact in the signal chain.

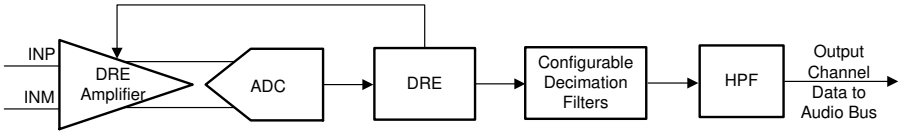

図 6-9. Signal-Chain Processing Flowchart

The front-end, dynamic range enhancer (DRE) gain amplifier is very low noise, with a 123dB dynamic range performance. The front-end DRE gain amplifier enables the PCM1841-Q1 to record a far-field audio signal with very high fidelity along with a low-noise and low-distortion, multibit, delta-sigma ADC, in both quiet and loud environments. Moreover, the ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further along the signal chain, an integrated, high-performance multistage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The device supports an input signal bandwidth up to 80kHz, which allows the high-frequency non-audio signal to be recorded by using a 176.4kHz (or higher) sample rate.

6.3.7.1 Digital High-Pass Filter

The device supports a fixed high-pass filter (HPF) with –3dB cut-off frequency of $0.00002083 \times f_S$ to remove the DC offset component and attenuate the undesired low-frequency noise content in the record data. The HPF is not a channel-independent filter but is globally applicable for all ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter and is efficient enough to filter out possible DC components of the signal. 表 6-6 shows the fixed –3-dB cutoff frequency value.

表 6-6. HPF Cutoff Frequency Value

-3dB CUTOFF FREQUENCY VALUE	-3dB CUTTOFF FREQUENCY AT 16kHz SAMPLE RATE	-3dB CUTTOFF FREQUENCY AT 48kHz SAMPLE RATE
$0.00002083 \times f_S$	0.33Hz	1Hz

6.3.7.2 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range and built-in digital decimation filter to process the oversampled data from the multibit delta-sigma (ΔΣ) modulator, which generates digital data at the same Nyquist sampling rate as the FSYNC rate. The decimation filter can be chosen from セクション 6.3.7.2.1 and セクション 6.3.7.2.2 only in target mode, depending on the required frequency response, group delay, and phase linearity requirements for the target application. The MD0 pin can select the decimation filter option. 表 6-7 shows the decimation filter mode selection for the record channel.

表 6-7. Decimation Filter Mode Selection for the Record Channel

MD0	DECIMATION FILTER MODE SELECTION (Supported Only in Target Mode)
LOW	Linear phase filters are used for the decimation in target mode. For controller mode, the device always uses linear phase filters for the decimation.
HIGH	Low latency filters are used for the decimation in target mode. For controller mode, the device always uses linear phase filters for the decimation.

6.3.7.2.1 Linear Phase Filters

The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in セクション 6.3.7.2.1.1 through セクション 6.3.7.2.1.7.

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6.3.7.2.1.1 Sampling Rate: 8kHz or 7.35kHz

図 6-10 and 図 6-11 show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 8kHz or 7.35kHz. 表 6-8 lists the specifications for a decimation filter with an 8kHz or 7.35kHz sampling rate.

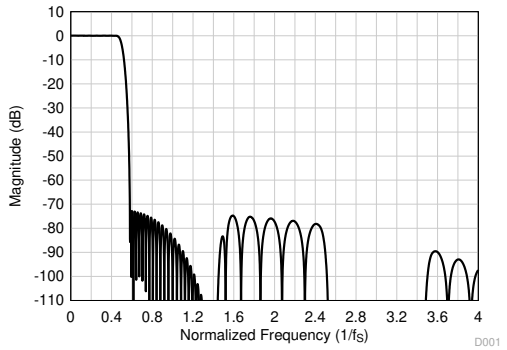

図 6-10. Linear Phase Decimation Filter Magnitude Response

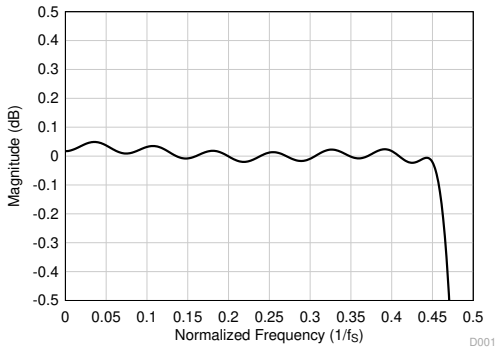

図 6-11. Linear Phase Decimation Filter Pass-Band Ripple

表 6-8. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	72.7			dB
	Frequency range is 4 × f_S onwards	81.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

6.3.7.2.1.2 Sampling Rate: 16kHz or 14.7kHz

図 6-12 and 図 6-13 show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 16kHz or 14.7kHz. 表 6-9 lists the specifications for a decimation filter with an 16kHz or 14.7kHz sampling rate.

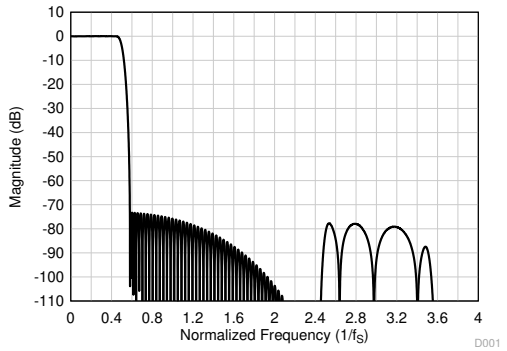

図 6-12. Linear Phase Decimation Filter Magnitude Response

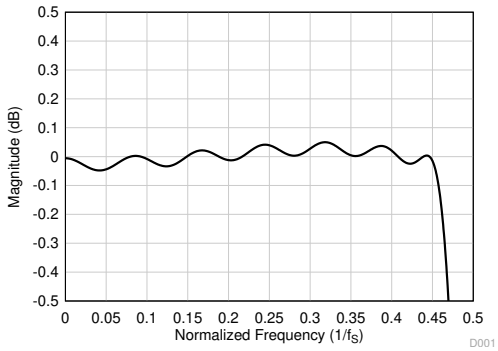

図 6-13. Linear Phase Decimation Filter Pass-Band Ripple

表 6-9. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.3			dB
	Frequency range is 4 × f_S onwards	95.0			

表 6-9. Linear Phase Decimation Filter Specifications (続き)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay or latency	Frequency range is 0 to 0.454 × f_S		15.7		$1/f_S$

6.3.7.2.1.3 Sampling Rate: 24kHz or 22.05kHz

図 6-14 and 図 6-15 show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 24kHz or 22.05kHz. 表 6-10 lists the specifications for a decimation filter with an 24kHz or 22.05kHz sampling rate.

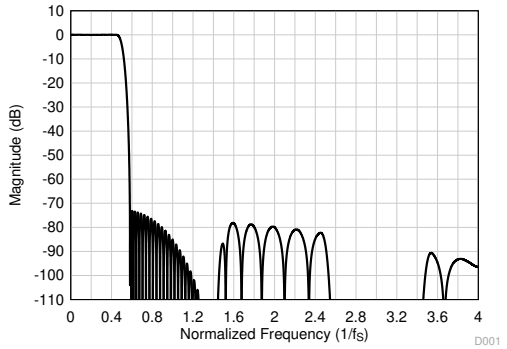

図 6-14. Linear Phase Decimation Filter Magnitude Response

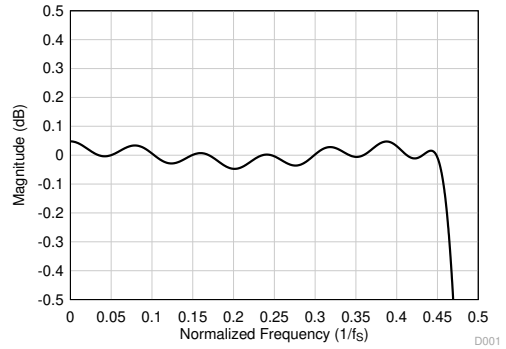

図 6-15. Linear Phase Decimation Filter Pass-Band Ripple

表 6-10. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.0			dB
	Frequency range is 4 × f_S onwards	96.4			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.6		$1/f_S$

6.3.7.2.1.4 Sampling Rate: 32kHz or 29.4kHz

図 6-16 and 図 6-17 show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 32kHz or 29.4kHz. 表 6-11 lists the specifications for a decimation filter with an 32kHz or 29.4kHz sampling rate.

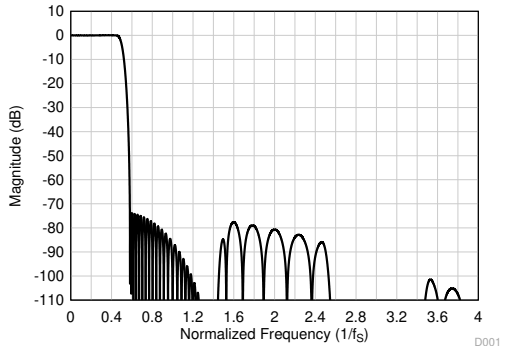

図 6-16. Linear Phase Decimation Filter Magnitude Response

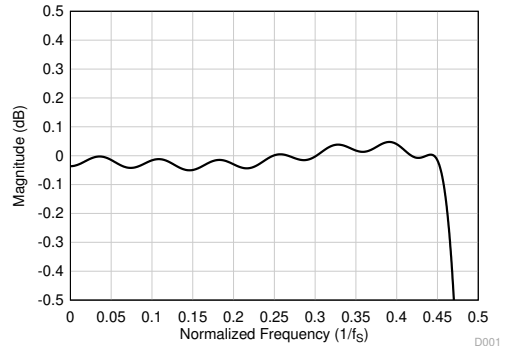

図 6-17. Linear Phase Decimation Filter Pass-Band Ripple

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表 6-11. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.7			dB
	Frequency range is 4 × f_S onwards	107.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.9		1/f_S

6.3.7.2.1.5 Sampling Rate: 48kHz or 44.1kHz

図 6-18 and 図 6-19 show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 48kHz or 44.1kHz. 表 6-12 lists the specifications for a decimation filter with an 48kHz or 44.1kHz sampling rate.

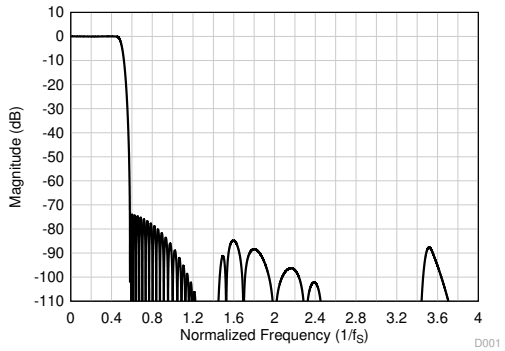

図 6-18. Linear Phase Decimation Filter Magnitude Response

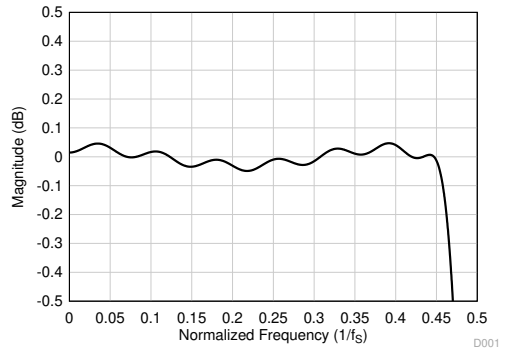

図 6-19. Linear Phase Decimation Filter Pass-Band Ripple

表 6-12. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.8			dB
	Frequency range is 4 × f_S onwards	98.1			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

6.3.7.2.1.6 Sampling Rate: 96kHz or 88.2kHz

図 6-20 and 図 6-21 show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 96kHz or 88.2kHz. 表 6-13 lists the specifications for a decimation filter with an 96-kHz or 88.2-kHz sampling rate.

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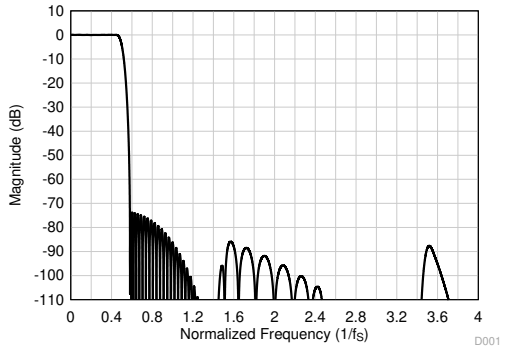

図 6-20. Linear Phase Decimation Filter Magnitude Response

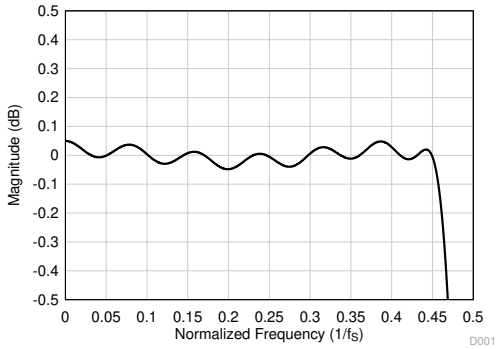

図 6-21. Linear Phase Decimation Filter Pass-Band Ripple

表 6-13. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.6			dB
	Frequency range is 4 × f_S onwards	97.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

6.3.7.2.1.7 Sampling Rate: 192kHz or 176.4kHz

図 6-22 and 図 6-23 show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 192kHz or 176.4kHz. 表 6-14 lists the specifications for a decimation filter with an 192kHz or 176.4kHz sampling rate.

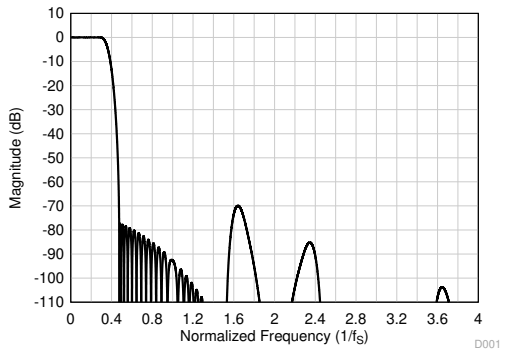

図 6-22. Linear Phase Decimation Filter Magnitude Response

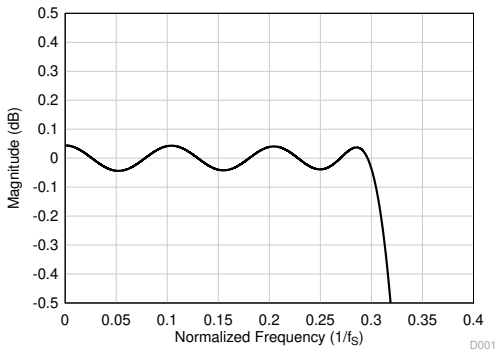

図 6-23. Linear Phase Decimation Filter Pass-Band Ripple

表 6-14. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.3 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.473 × f_S to 4 × f_S	70.0			dB
	Frequency range is 4 × f_S onwards	111.0			
Group delay or latency	Frequency range is 0 to 0.3 × f_S		11.9		1/f_S

6.3.7.2.2 Low-Latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the PCM1841-Q1 can be used. The device supports these filters with a group delay

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of approximately seven samples with an almost linear phase response within the 0.365 × f_S frequency band. セクション 6.3.7.2.2.1 through セクション 6.3.7.2.2.5 provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

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6.3.7.2.2.1 Sampling Rate: 16kHz or 14.7kHz

図 6-24 shows the magnitude response and 図 6-25 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 16kHz or 14.7kHz. 表 6-15 lists the specifications for a decimation filter with a 16kHz or 14.7kHz sampling rate.

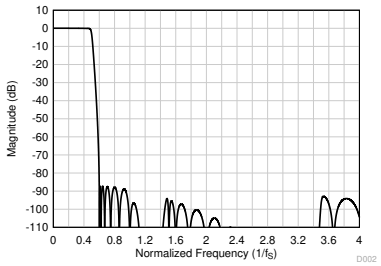

図 6-24. Low-Latency Decimation Filter Magnitude Response

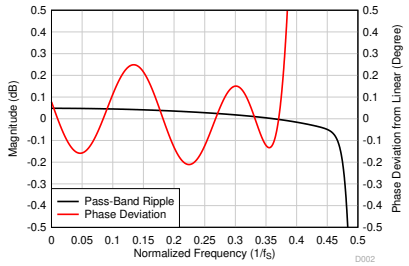

図 6-25. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-15. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.451 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.61 × f_S onwards	87.3			dB
Group delay or latency	Frequency range is 0 to 0.363 × f_S		7.6		1/f_S
Group delay deviation	Frequency range is 0 to 0.363 × f_S	–0.022		0.022	1/f_S
Phase deviation	Frequency range is 0 to 0.363 × f_S	–0.21		0.25	Degrees

6.3.7.2.2.2 Sampling Rate: 24kHz or 22.05kHz

図 6-26 shows the magnitude response and 図 6-27 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 24kHz or 22.05kHz. 表 6-16 lists the specifications for a decimation filter with a 24kHz or 22.05kHz sampling rate.

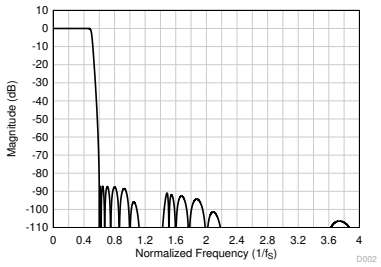

図 6-26. Low-Latency Decimation Filter Magnitude Response

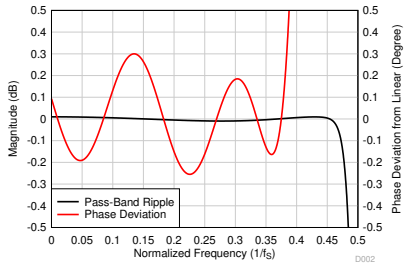

図 6-27. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-16. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.459 × f_S	–0.01		0.01	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.2			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.5		1/f_S
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.026		0.026	1/f_S
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

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6.3.7.2.2.3 Sampling Rate: 32kHz or 29.4kHz

図 6-28 shows the magnitude response and 図 6-29 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 32kHz or 29.4kHz. 表 6-17 lists the specifications for a decimation filter with a 32kHz or 29.4kHz sampling rate.

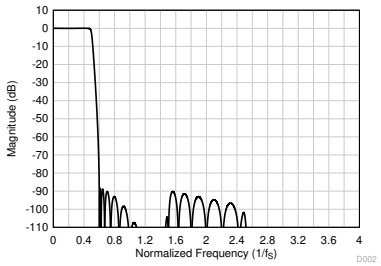

図 6-28. Low-Latency Decimation Filter Magnitude Response

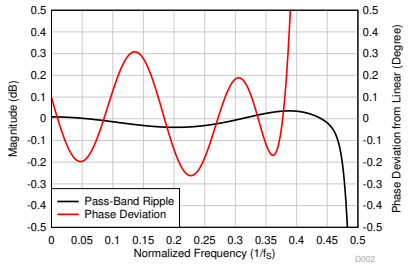

図 6-29. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-17. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.457 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	88.3			dB
Group delay or latency	Frequency range is 0 to 0.368 × f_S		8.7		1/f_S
Group delay deviation	Frequency range is 0 to 0.368 × f_S	–0.026		0.026	1/f_S
Phase deviation	Frequency range is 0 to 0.368 × f_S	–0.26		0.31	Degrees

6.3.7.2.2.4 Sampling Rate: 48kHz or 44.1kHz

図 6-30 shows the magnitude response and 図 6-31 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 48kHz or 44.1kHz. 表 6-18 lists the specifications for a decimation filter with a 48kHz or 44.1kHz sampling rate.

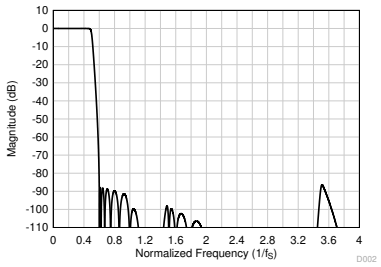

図 6-30. Low-Latency Decimation Filter Magnitude Response

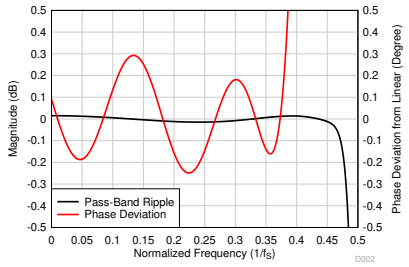

図 6-31. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-18. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.015		0.015	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.4			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		1/f_S
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	1/f_S
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.25		0.30	Degrees

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6.3.7.2.2.5 Sampling Rate: 96kHz or 88.2kHz

図 6-32 shows the magnitude response and 図 6-33 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 96kHz or 88.2kHz. 表 6-19 lists the specifications for a decimation filter with a 96kHz or 88.2kHz sampling rate.

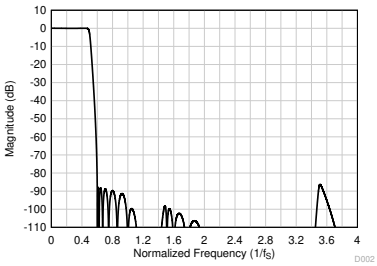

図 6-32. Low-Latency Decimation Filter Magnitude Response

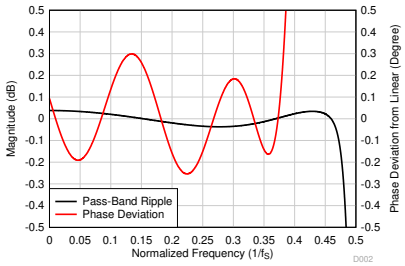

図 6-33. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-19. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.466 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.3			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		1/f_S
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	1/f_S
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

6.3.8 Dynamic Range Enhancer (DRE)

The device integrates an ultra-low noise, front-end DRE gain amplifier with 123dB dynamic range performance with a low-noise, low-distortion, multibit delta-sigma (ΔΣ) ADC with a 113dB dynamic range. The dynamic range enhancer (DRE) is a digitally assisted algorithm to boost the overall channel performance. The DRE monitors the incoming signal amplitude and accordingly adjusts the internal DRE amplifier gain automatically. The DRE achieves a complete-channel dynamic range as high as 123dB. At a system level, the DRE scheme enables far-field, high-fidelity recording of audio signals in very quiet environments and low-distortion recording in loud environments.

The DRE is enabled only in target mode by driving high to the MD1 pin. 表 6-20 shows the DRE selection for the record channel.

表 6-20. DRE Selection for the Record Channel

MD1	DRE SELECTION (Supported Only in Target Mode)
LOW	DRE is disabled in target mode. For controller mode, DRE is always disabled.
HIGH	DRE is enabled with DRE_LVL = –36dB and DRE_MAXGAIN = 24dB in target mode. For controller mode, DRE is always disabled.

This algorithm is implemented with very low latency and all signal chain blocks are designed to minimize any audible artifacts that may occur resulting from dynamic gain modulation. The target signal threshold level, DRE_LVL, at which DRE is triggered is fixed to the –36dB input signal level. The DRE gain range can be dynamically modulated by using DRE_MAXGAIN, which is fixed to 24dB to maximize the benefit of the DRE in real-world applications and to minimize any audible artifacts.

Enabling the DRE for processing increases the power consumption of the device because of increased signal processing. Therefore, disable the DRE for low-power critical applications. Furthermore, the DRE is not supported for output sample rates greater than 48kHz.

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6.4 Device Functional Modes

6.4.1 Hardware Shutdown

The device enters hardware shutdown mode when the SHDNZ pin is asserted low or the AVDD supply voltage is not applied to the device. In hardware shutdown mode, the device consumes the minimum quiescent current from the AVDD supply. If the SHDNZ pin is asserted low when the device is in active mode, the device ramps down volume on the record data, powers down the analog and digital blocks, and puts the device into hardware shutdown mode in 25ms (typical).

6.4.2 Active Mode

In the hardware shutdown state, when the SHDNZ pin goes high, the device starts the internal boot-up sequence and then enters into active mode in less than 20ms (typical). Assert the SHDNZ pin high only when the IOVDD supply settles to a steady voltage level and all hardware control pins (MSZ, MD0, MD1, FMT0, and FMT1) are driven to the voltage level for the device desired mode of operation.

In active mode, when the audio clocks are available, the device powers up all the ADC channels and starts transmitting the data over the audio serial interface. If the clocks are stopped then the device auto powers down the ADC channels.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The PCM1841-Q1 is a multichannel, high-performance audio analog-to-digital converter (ADC) that supports output sample rates of up to 192kHz. The device supports up to four analog microphones for simultaneous recording applications.

The PCM1841-Q1 configuration is supported using various hardware pin control options. The device supports a highly flexible, audio serial interface (TDM, I^2S, and LJ) to transmit audio data seamlessly in the system across devices.

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7.2 Typical Application

図 7-1 shows a typical configuration of the PCM1841-Q1 for an application using four analog microelectrical-mechanical system (MEMS) microphones for simultaneous recording operation with a time-division multiplexing (TDM) audio data target interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

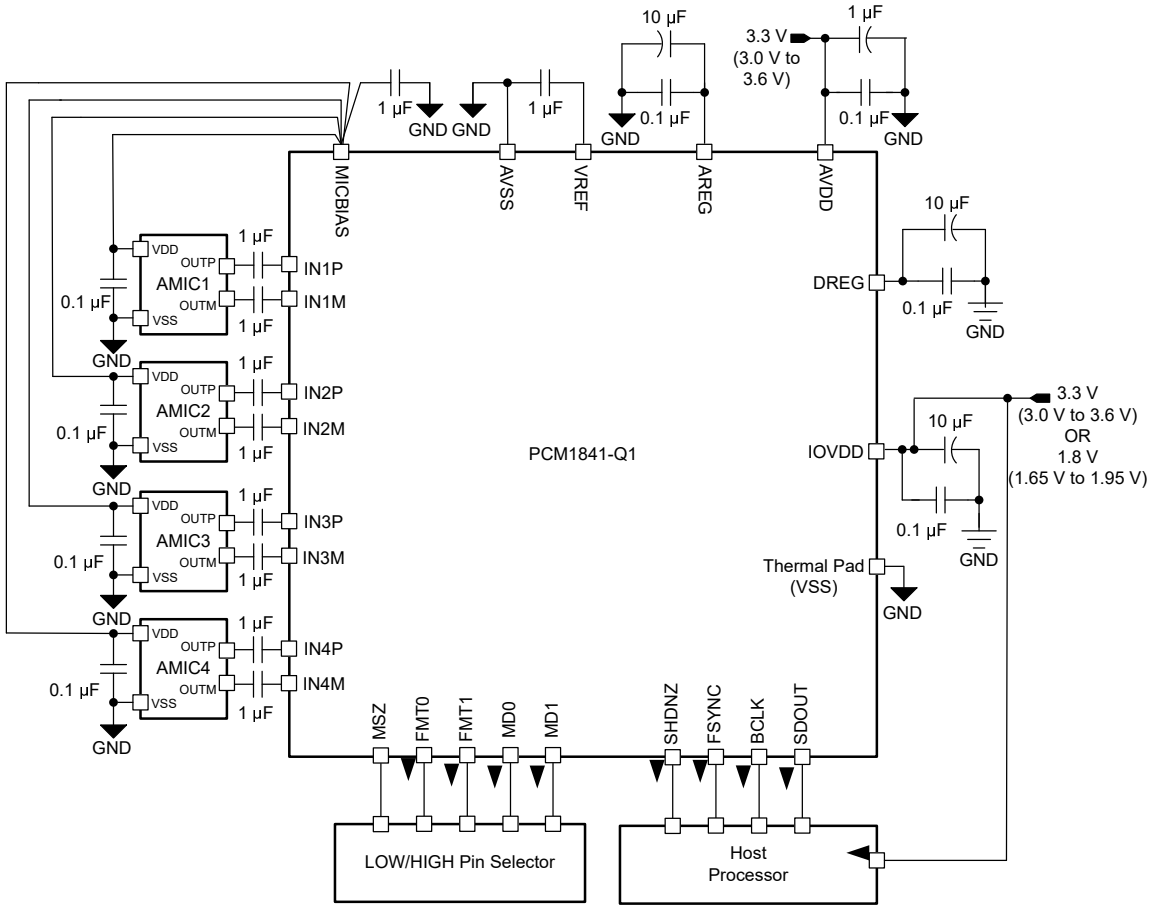

図 7-1. Four-Channel Analog Microphone Recording Diagram for 3.3V AVDD Operation

7.2.1 Design Requirements

表 7-1 lists the design parameters for this application.

表 7-1. Design Parameters

KEY PARAMETER	SPECIFICATION: 3.3V AVDD OPERATION
AVDD	3.3V
AVDD supply current consumption	> 23mA (PLL on, four-channel recording, f_S = 48kHz)
IOVDD	1.8V or 3.3V
Maximum MICBIAS current	10mA (MICBIAS voltage is the same as VREF)

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7.2.2 Detailed Design Procedure

This section describes the necessary steps to configure the PCM1841-Q1 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
   a. Power-up the IOVDD and AVDD power supplies, keeping the SHDNZ pin voltage low
   b. The device now goes into hardware shutdown mode (ultra-low-power mode < 1µA)
2. Transition from hardware shutdown mode to active mode whenever required for the recording operation:
   a. Connect the MSZ, FMT0, and FMT1 pins voltage low to configure the device in 4 channel TDM target mode
   b. Release SHDNZ only when the IOVDD and AVDD power supplies settle to the steady-state operating voltage
   c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

      This specific step can be done at any point in the sequence after step a

      See the *Phase-Locked Loop (PLL) and Clock Generation* section for supported sample rates and the BCLK to FSYNC ratio
   d. The device recording data are now sent to the host processor via the TDM audio serial data bus
3. Assert the SHDNZ pin low to enter hardware shutdown mode (again) at any time
4. Follow step 2 onwards to exit hardware shutdown mode (again)

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7.2.3 Application Curves

Measurements are done on the EVM by feeding the device analog input signal using audio precision and with a 3.3V AVDD supply.

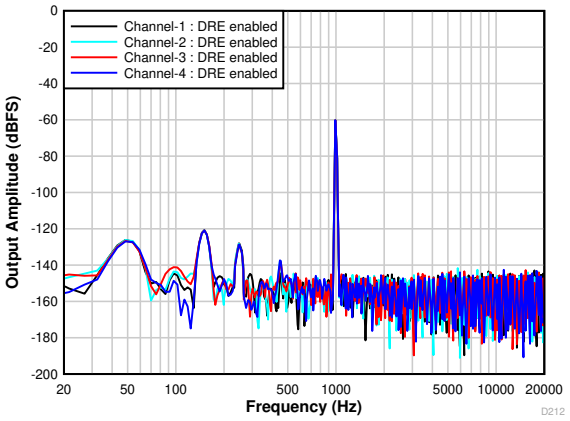

図 7-2. FFT With a –60dBr Input With DRE Enabled

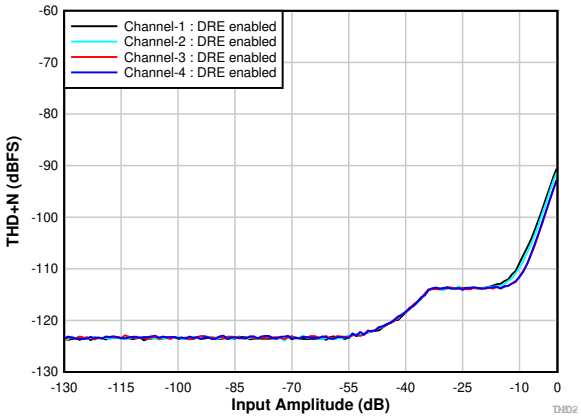

図 7-3. THD+N vs Input Amplitude With DRE Enabled

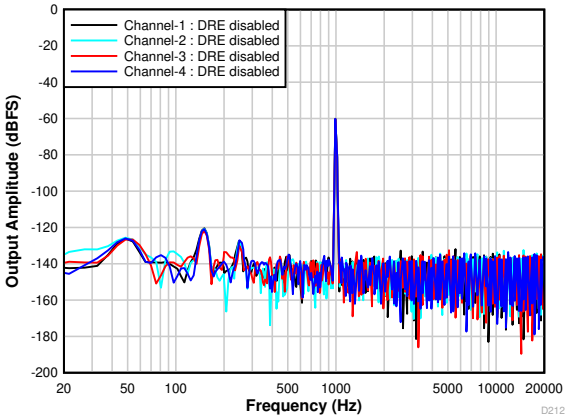

図 7-4. FFT With a –60dBr Input With DRE Disabled

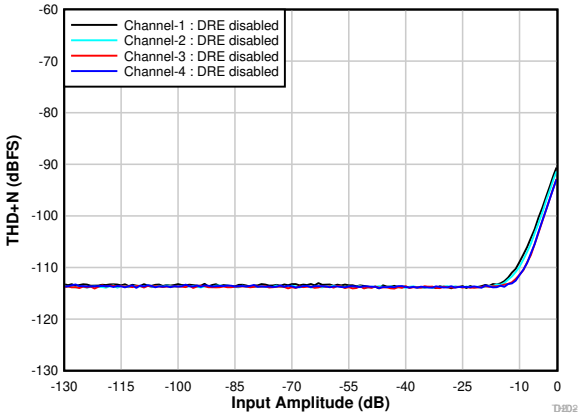

図 7-5. THD+N vs Input Amplitude With DRE Disabled

ADVANCE INFORMATION

7.3 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, keep the SHDNZ pin low until the IOVDD supply voltage settles to a stable and supported operating voltage range. After all supplies are stable, set the SHDNZ pin high to initialize the device. Assert the SHDNZ pin high only when all hardware control pins (MSZ, MD0, MD1, FMT0, and FMT1) are driven to the voltage level for the device desired mode of operation.

For the supply power-up requirement, t_1 and t_2 must be at least 100µs. For the supply power-down requirement, t_3 and t_4 must be at least 10ms. This timing (as shown in 図 7-6) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into hardware shutdown mode.

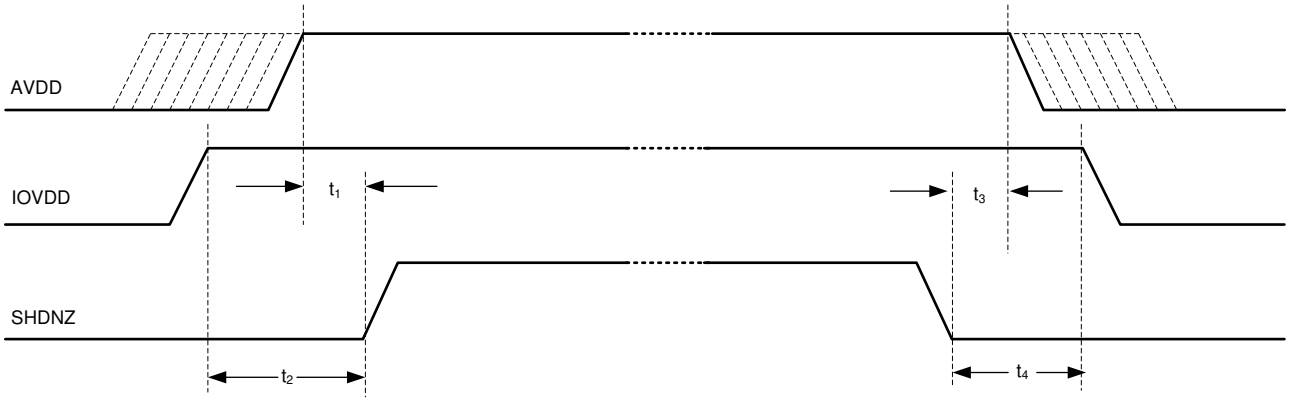

図 7-6. Power-Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 1V/µs and that the wait time between a power-down and a power-up event is at least 100ms.

The PCM1841-Q1 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG. However, if the AVDD voltage is less than 1.98V in the system, then short the AREG and AVDD pins onboard.

7.4 Layout

7.4.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can maximize device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- Route the analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for optimal performance.
- Directly tap the MICBIAS pin to avoid common impedance when routing the biasing or supply traces for multiple microphones to avoid coupling across microphones.
- Directly short the VREF and MICBIAS external capacitors ground terminal to the AVSS pin without using any vias for this connection trace.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

ADVANCE INFORMATION

7.4.2 Layout Example

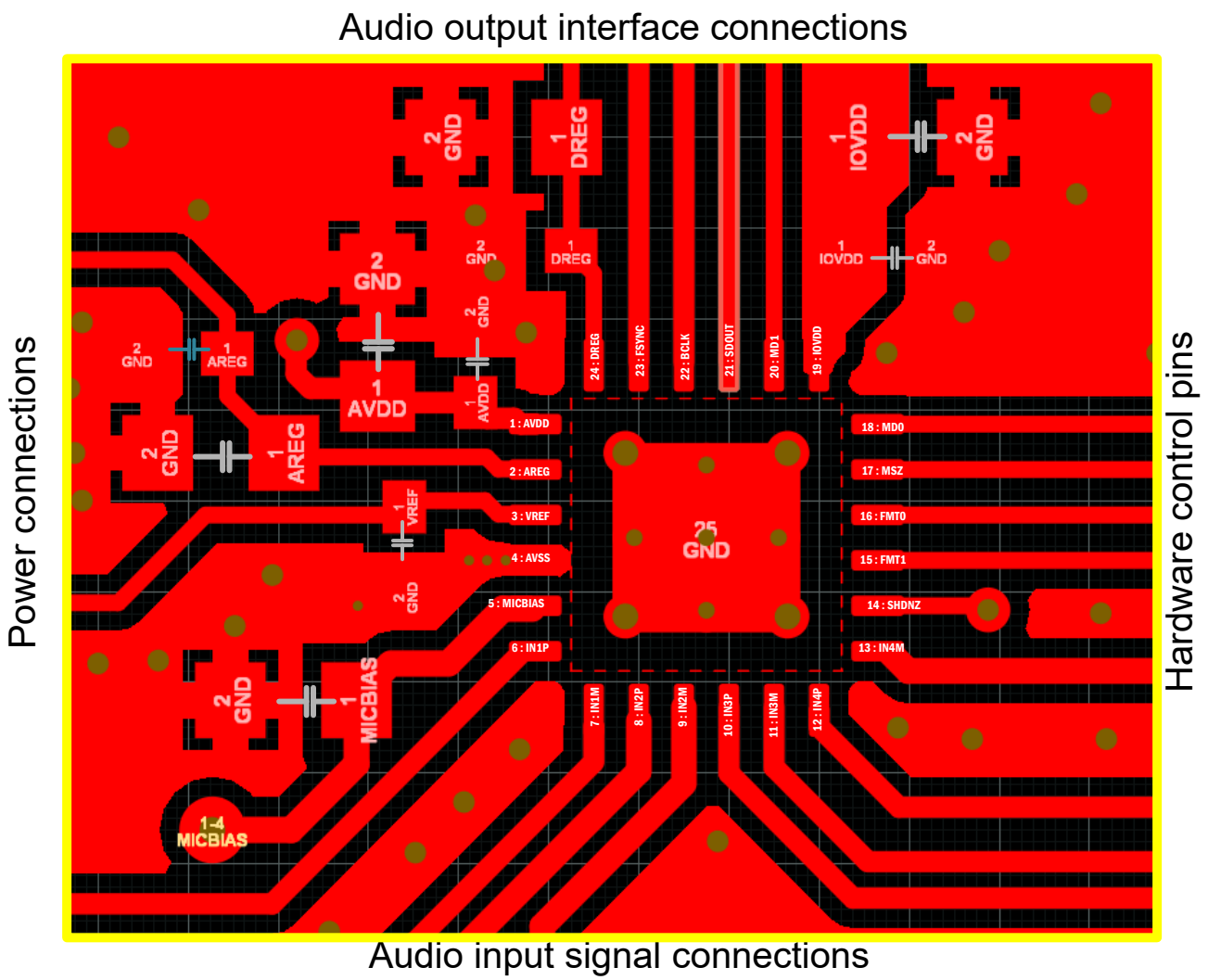

図 7-7. Example Layout

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

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8.3 Trademarks

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8.4 静電気放電に関する注意事項

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8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
May 2024	*	Initial Release

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

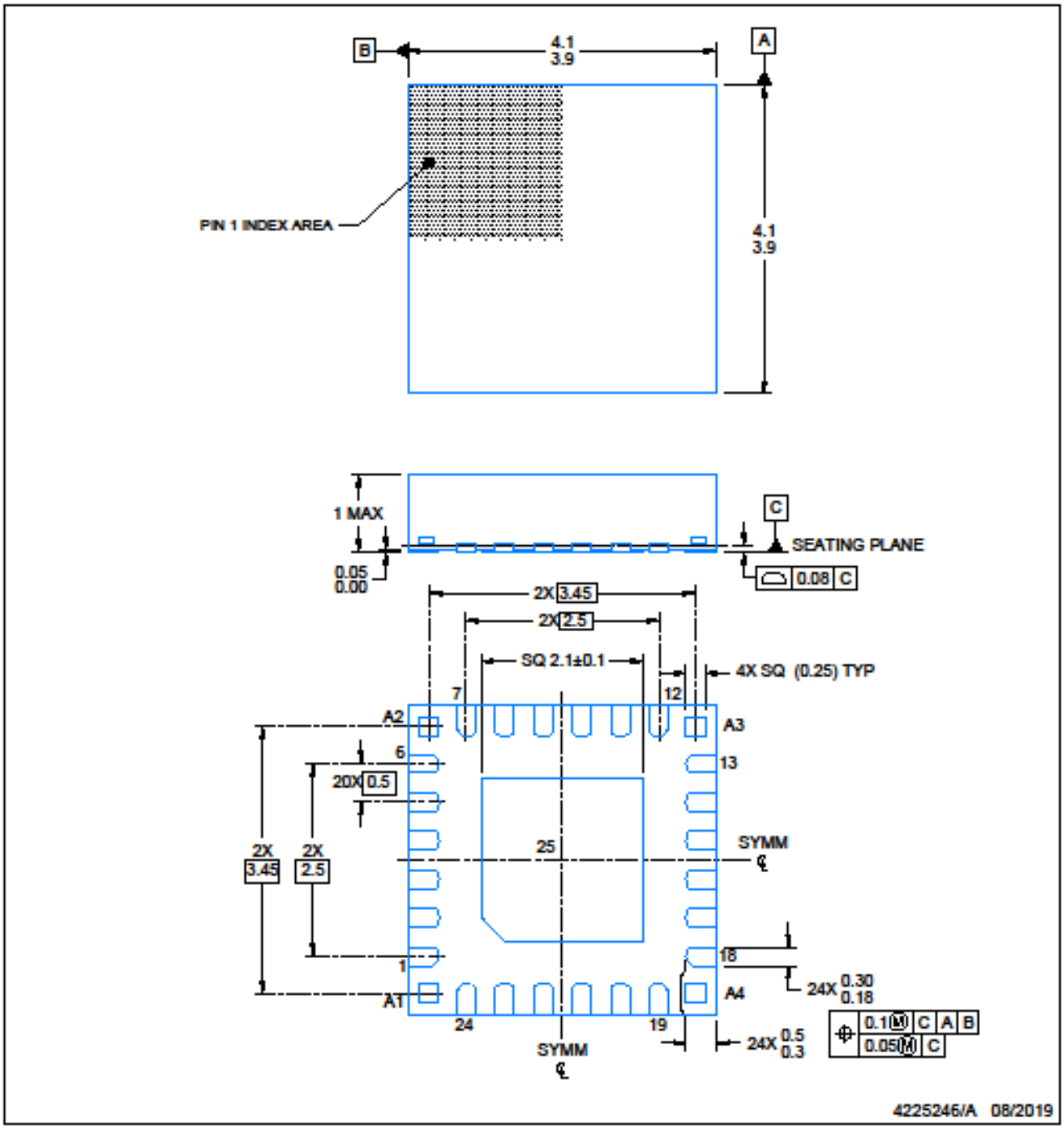
ADVANCE INFORMATION

PACKAGE OUTLINE

RGE0024R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

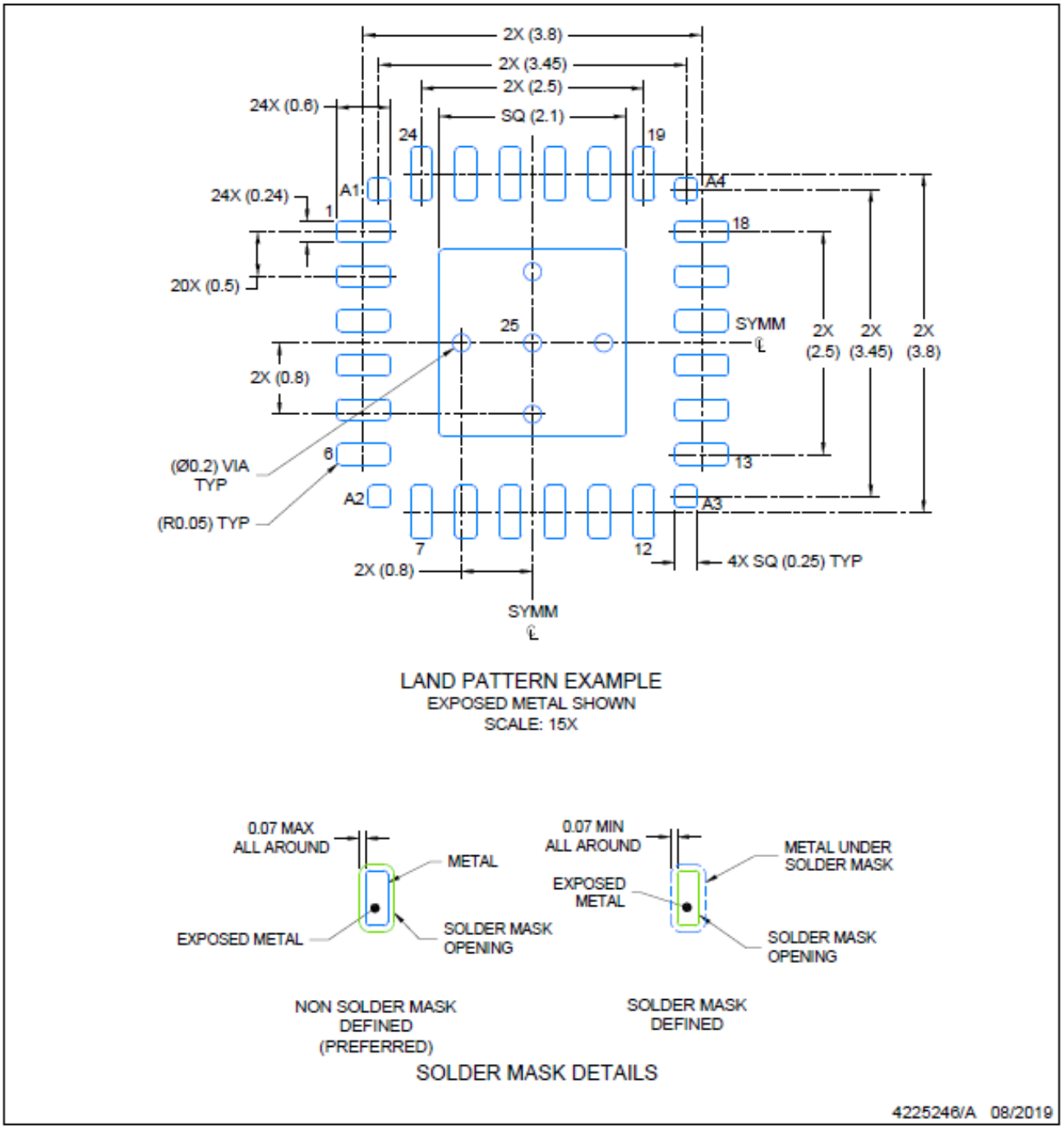
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RGE0024R — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

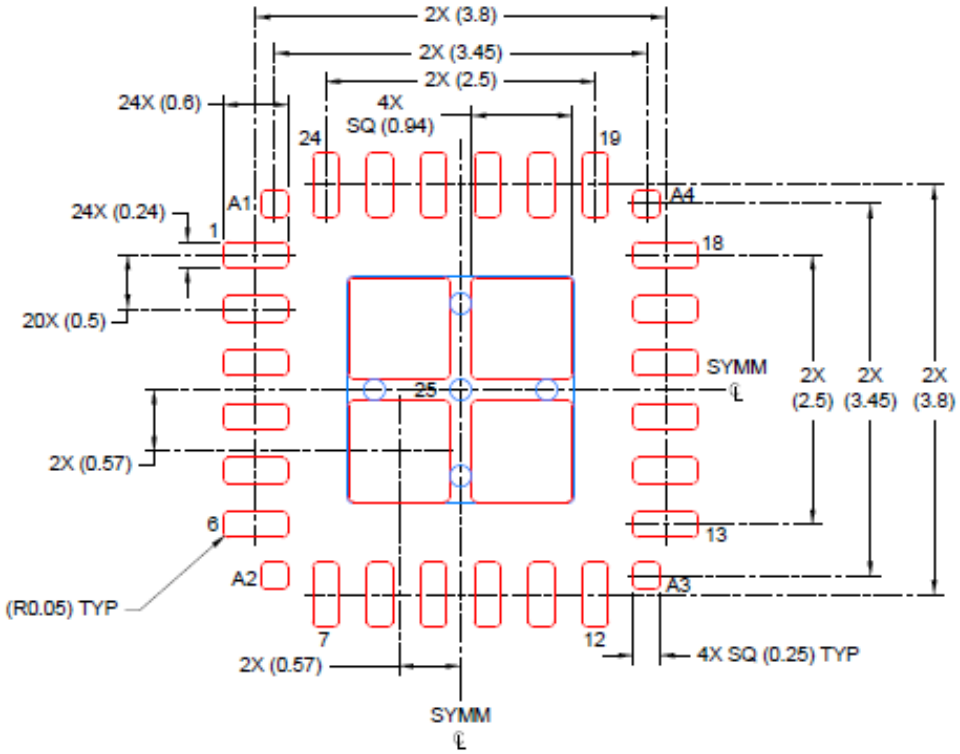
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

4225246/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

重要なお知らせと免責事項

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM1841QRGERQ1	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PCM1841 Q1
PCM1841QRGERQ1.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PCM1841 Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

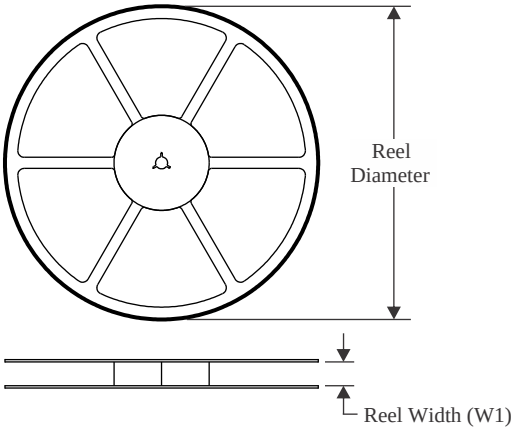
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

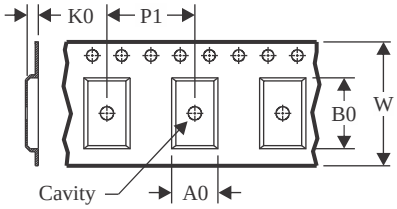
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

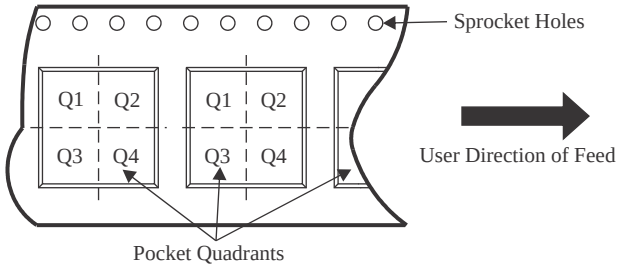


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

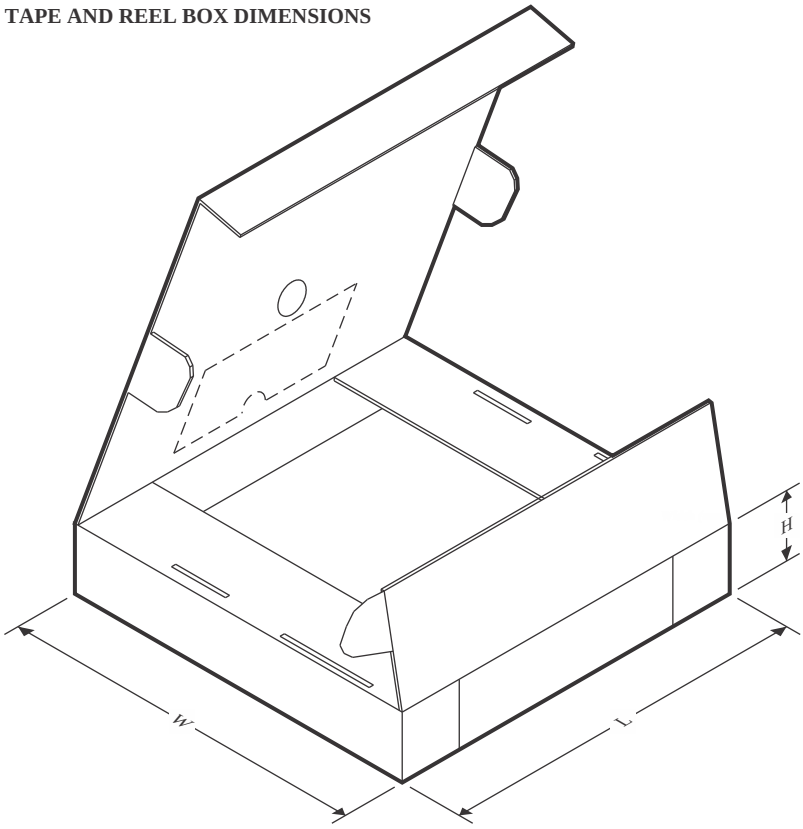
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1841QRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



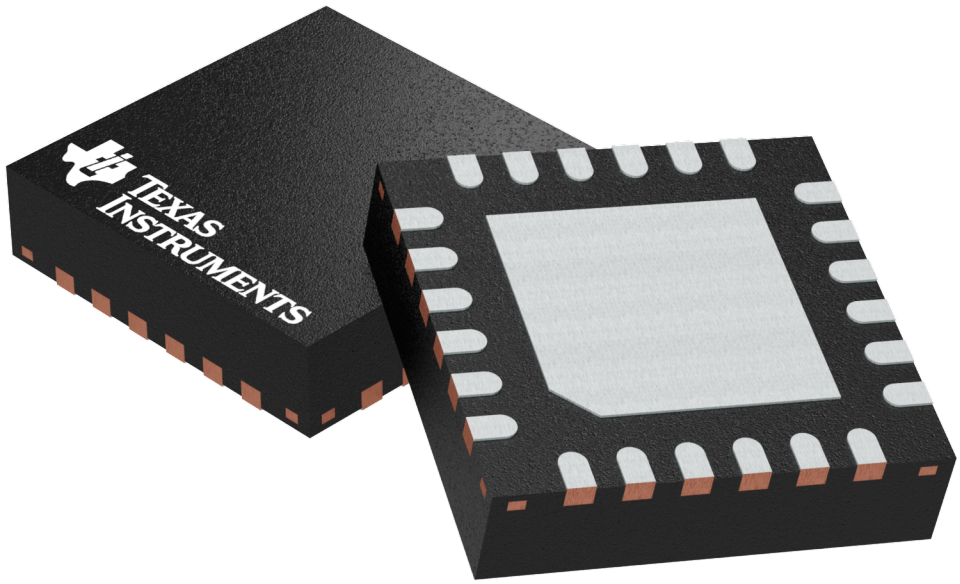
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1841QRGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

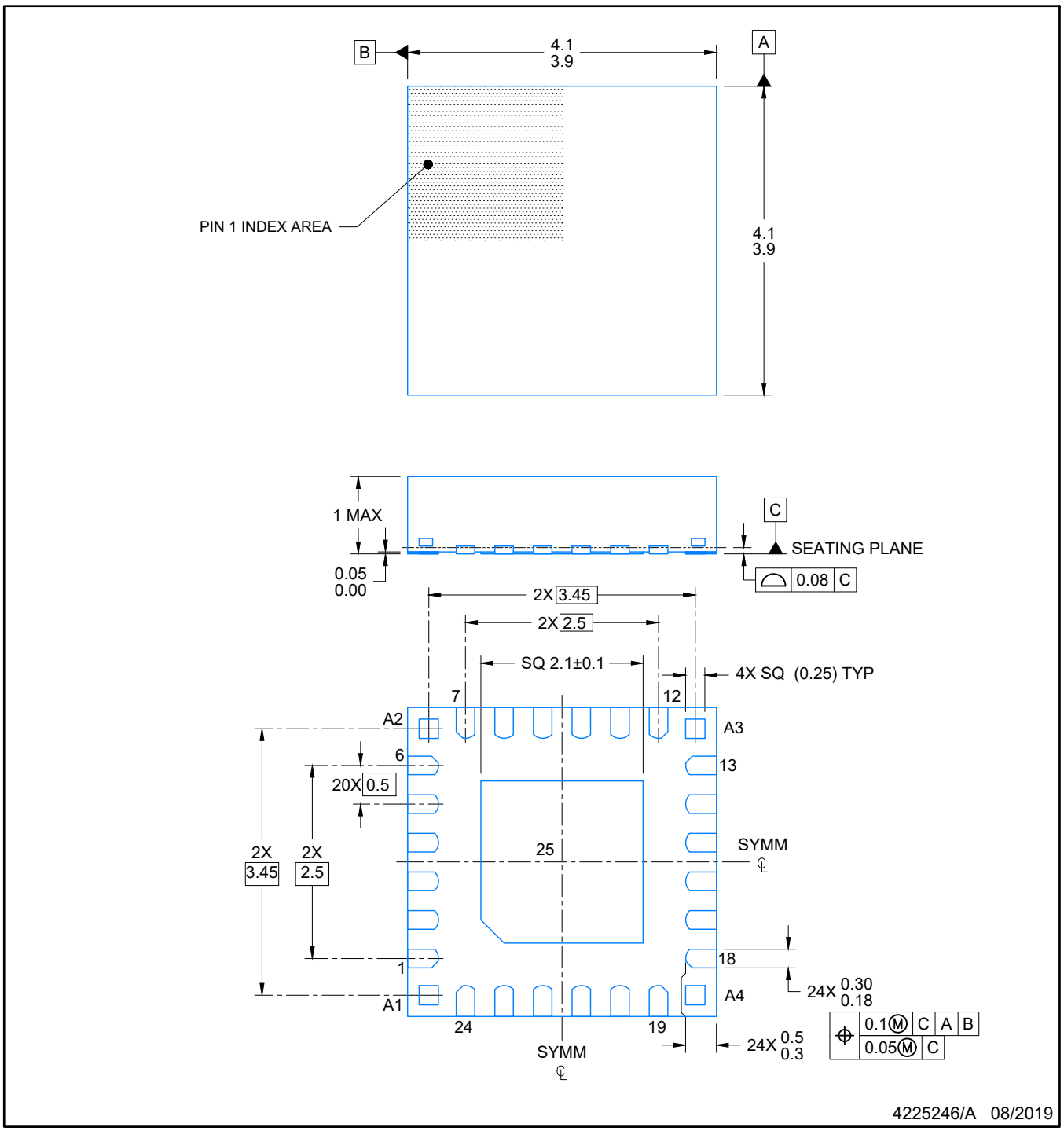
4204104/H

PACKAGE OUTLINE

RGE0024R

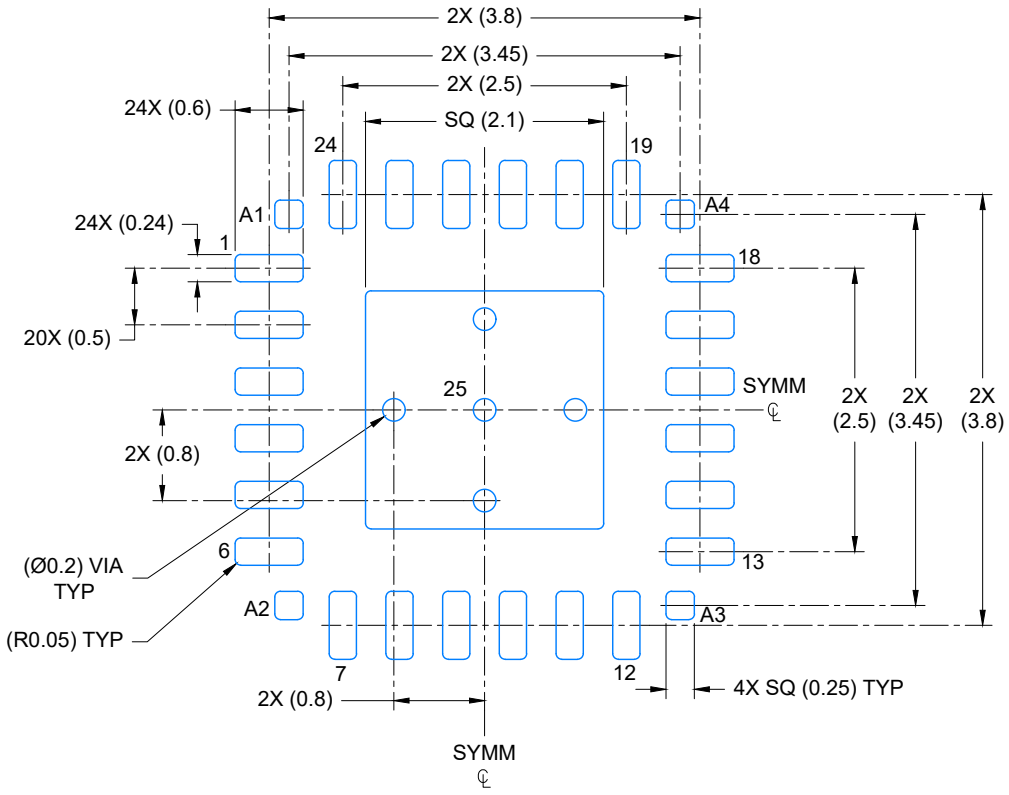
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

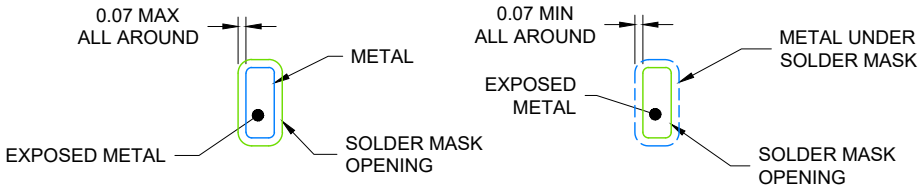


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

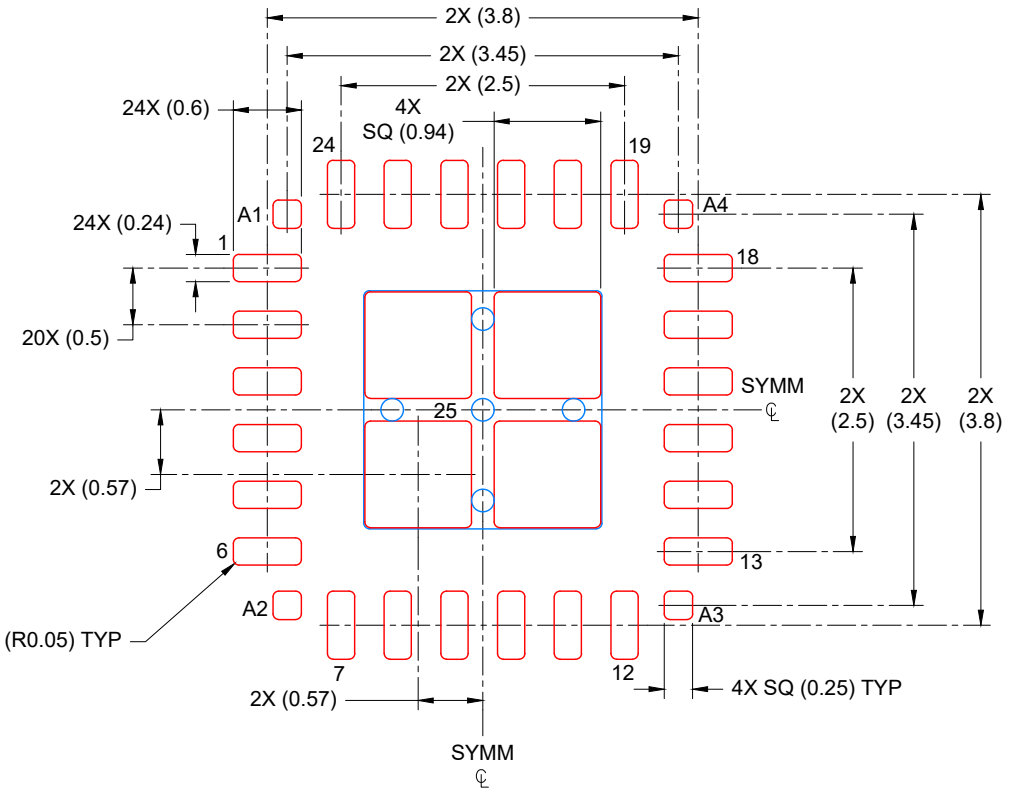
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4225246/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

4225246/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月