TEXAS INSTRUMENTS
PCM1753, PCM1754, PCM1755
JAJS199E – APRIL 2003 – REVISED JULY 2019

PCM175x 24 ビット、192kHz サンプリング、拡張マルチレベル、デルタ・シグマ、オーディオ、デジタル/アナログ・コンバータ

1 特長

- 24 ビット分解能
- アナログ性能 (V_{CC} = 5V)
  - ダイナミック・レンジ：106dB
  - SNR：106dB (標準値)
  - THD+N：0.002% (標準値)
  - フルスケール出力：$4V_{PP}$ (標準値)
- 4x または 8x のオーバーサンプリング・デジタル・フィルタ
  - ストップ・バンド減衰：-50dB
  - パスバンド・リップル：±0.04dB
- サンプリング周波数：5kHz～200kHz
- システム・クロック：128 f_S、192 f_S、256 f_S、384 f_S、512 f_S、768 f_S、1152 f_S、自動検出付き
- ハードウェア制御 (PCM1754)
  - I^2S および 16 ビット・ワード、右揃え
  - 44.1kHz のデジタル・ディエンファシス
  - ソフト・ミュート
  - L、R チャネル共通出力のゼロ・フラグ
- 電源：5V 単一電源
- 小型 16 ピン SSOP パッケージ、鉛フリー

2 アプリケーション

- A/V レシーバ
- HDTV レシーバ
- 車載用オーディオ・システム
- 24 ビット・オーディオを必要とするアプリケーション

3 概要

PCM1753、PCM1754、PCM1755 (PCM175x) デバイスは、TI の拡張デルタ・シグマ・アーキテクチャに基づくステレオ・デジタル/アナログ・コンバータ (DAC) です。この強化されたアーキテクチャは 4 次のノイズ・シェーピングと、8 レベルの振幅量子化を採用し、非常に優れた動的性能とクロック・ジッタ耐性の強化を実現しています。PCM175x デバイスは、業界標準のオーディオ・データ・フォーマットと 16 ビットおよび 24 ビット・データに対応しているため、オーディオ DSP およびデコーダ・チップと簡単に接続できます。PCM175x デバイスはハードウェア・モードで制御することも、レジスタ書き込み機能対応 3 線式シリアル制御ポートからアクセスできる一連のユーザー・プログラマブル機能で制御することもできます。

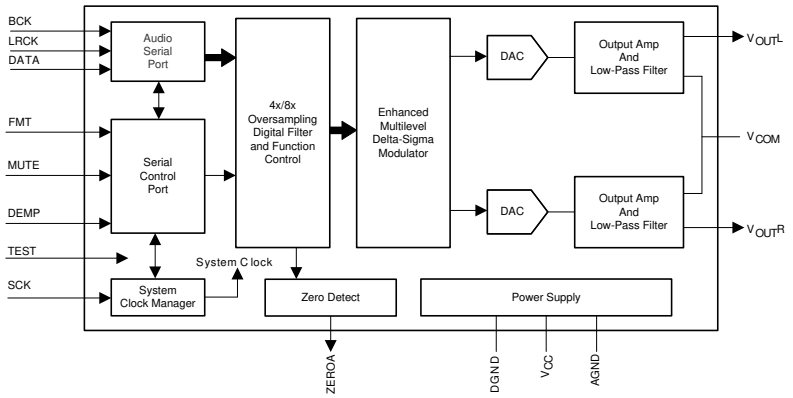
PCM1753 は、ピン 5 を除いて PCM1748、PCM1742、PCM1741 とピン互換です。

製品情報(1)

型番	パッケージ	本体サイズ (公称)
PCM1753	SSOP (16)	3.90mm × 4.90mm
PCM1754		
PCM1755		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

機能ブロック図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (August 2015) から **Revision E** に変更 **Page**

- Added text to pin 11 description to clarify operation for PCM1755 ... 3
- Added text to pin 12 description to clarify operation for PCM1755 ... 3
- Added new row for PCM1755 temperature range to *Absolute Maximum Ratings* table ... 4
- Changed location of operating temperature from *Electrical Characteristics* table to *Recommended Operating Conditions* table ... 4
- Changed operating temperature MAX value for PCM1753 and PCM1754 from 105°C to 85°C in the *Recommended Operating Conditions* table ... 4
- Added new row for PCM1755 temperature range to the *Recommended Operating Conditions* table ... 4
- Changed output voltage value from MIN to TYP in the *Electrical Characteristics* table ... 6
- Changed center voltage value from MIN to TYP in the *Electrical Characteristics* table ... 6

Revision C (February 2009) から **Revision D** に変更 **Page**

- 「*ESD 定格*」表、「*推奨動作条件*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1

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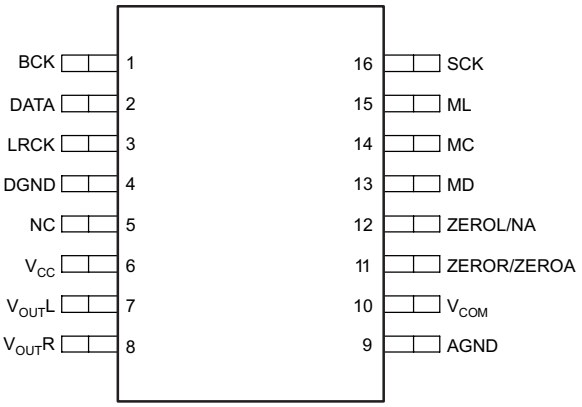
5 Device Comparison Table

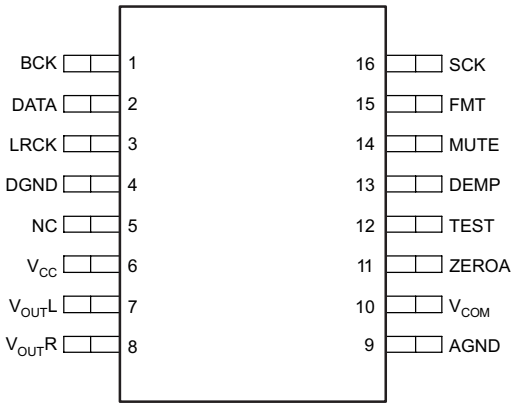
FEATURE	PCM1753, PCM1755	PCM1754
Audio data interface format	I^2S, standard, left-justified	I^2S, standard
Audio data bit length	16-bit, 18-bit, 20-bit, and 24-bit selectable	16-bit and 24-bit I^2S, 16-bit standard
Audio data format	MSB first, 2's complement	

6 Pin Configuration and Functions

PCM1753, PCM1755 DBQ Package
16-Pin SSOP
Top View



PCM1754 DBQ Package
16-Pin SSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	PCM1753, PCM1755	PCM1754		
AGND	9	9	—	Analog ground
BCK	1	1	I	Audio-data bit-clock input
DATA	2	2	I	Audio-data digital input
DEMP	-	13	I	De-emphasis control
DGND	4	4	—	Digital ground
FMT	-	15	I	Data format select
LRCK	3	3	I	L-channel and R-channel audio data latch enable input
MC	14	-	I	Mode control clock input
MD	13	-	I	Mode control data input
ML	15	-	I	Mode control latch input
MUTE	-	14	I	Analog mixing control
NC	5	5	—	No connection
SCK	16	16	I	System clock input
TEST	-	12	I	Test pin, ground or open
VCC	6	6	—	Analog power supply, 5 V
VCOM	10	10	—	Common voltage decoupling
VOUTL	7	7	O	Analog output for L-channel
VOUTR	8	8	O	Analog output for R-channel
ZEROR/ZEROA	11	11	O	Zero flag output for R-channel / Zero flag output for L-/R-channel. Open-drain output for PCM1755.
ZEROL/NA	12	-	O	Zero flag output for L-channel / Not assigned. Open-drain output for PCM1755.

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7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.3	6.5	V
Ground voltage differences	AGND, DGND		±0.1	V
Input voltage		–0.3	6.5	V
Input current (any pins except supplies)			±10	mA
Ambient temperature under bias	PCM1753, PCM1754	–40	85	°C
	PCM1755	–25	85	
Junction temperature			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating temperature	PCM1753, PCM1754	–40		85	°C
		PCM1755	–25		85	

7.4 Thermal Information

THERMAL METRIC(1)		PCM175x DBQ (SSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

all specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			24		Bits
DATA FORMAT						
f_S	Sampling frequency		5		200	kHz
	System clock frequency			128 f_S 192 f_S 256 f_S 384 f_S 512 f_S 768 f_S 1152 f_S		kHz
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	Input logic level, high		2			VDC
V_{IL}	Input logic level, low				0.8	VDC
I_{IH}	Input logic current, high (SCK, BCK, DATA, and LRCK pins)	$V_{IN} = V_{CC}$			10	µA
I_{IL}	Input logic current, low (SCK, BCK, DATA, and LRCK pins)	V_{IN} = 0 V			-10	µA
I_{IH}	Input logic current, high (TEST, DEMP, MUTE, and FMT pins)	$V_{IN} = V_{CC}$		65	100	µA
I_{IL}	Input logic current, low (TEST, DEMP, MUTE, and FMT pins)	V_{IN} = 0 V			-10	µA
V_{OH}	Output logic level, high (ZEROA pin)	I_{OH} = –1 mA	2.4			VDC
V_{OL}	Output logic level, low (ZEROA pin)	I_{OL} = 1 mA			0.4	VDC
DYNAMIC PERFORMANCE(1)(2)						
	THD+N at VOUT = 0 dB	f_S = 44.1 kHz		0%	0.01%	
		f_S = 96 kHz		0%		
		f_S = 192 kHz		0%		
	THD+N at VOUT = -60 dB	f_S = 44.1 kHz		0.65%		
		f_S = 96 kHz		0.80%		
		f_S = 192 kHz		0.95%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
		A-weighted, f_S = 96 kHz		104		
		A-weighted, f_S = 192 kHz		102		
	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
		A-weighted, f_S = 96 kHz		104		
		A-weighted, f_S = 192 kHz		102		
	Channel separation	f_S = 44.1 kHz	97	103		dB
		f_S = 96 kHz		101		
		f_S = 192 kHz		100		
	Level linearity error	VOUT = -90 dB		±0.5		dB
DC ACCURACY						
	Gain error			±1	±6	% of FSR
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Bipolar zero error	VOUT = 0.5 V_{CC} at BPZ		±30	±60	mV

(1) Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.
(2) Conditions in 192-kHz operation are system clock = 128 f_S and oversampling rate = 64 f_S of register 18.

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Electrical Characteristics (continued)

all specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
	Output voltage	Full scale (0 dB)		80% of V_{CC}		V_{PP}
	Center voltage			50% of V_{CC}		VDC
	Load impedance	AC-coupled load	5			kΩ
DIGITAL FILTER PERFORMANCE FILTER CHARACTERISTICS (SHARP ROLLOFF)						
	Pass band	±0.04 dB			0.454 f_S	
	Stop band		0.546 fs			
	Pass-band ripple				±0.04	dB
	Stop-band attenuation	Stop band = 0.546 f_S	–50			dB
ANALOG FILTER PERFORMANCE						
	Frequency response	At 20 kHz		–0.03		dB
		At 44 kHz		–0.2		
POWER SUPPLY REQUIREMENTS(2)						
I_{CC}	Supply current	f_S = 44.1 kHz		16	21	mA
		f_S = 96 kHz		25		
		f_S = 192 kHz		30		
	Power dissipation	f_S = 44.1 kHz		80	105	mW
		f_S = 96 kHz		125		
		f_S = 192 kHz		150		
TEMPERATURE						
$R_{\theta JA}$	Thermal Resistance	16-pin DBQ		104.1		°C/W

7.6 System Clock Input Timing

for more information, see the *System Clock Input* section

			MIN	NOM	MAX	UNIT
$t_{(SCKH)}$	System clock pulse duration, high	See Figure 20.	7			ns
$t_{(SCKL)}$	System clock pulse duration, low		7			ns
$t_{(SCY)}$	System clock pulse cycle time		See (1)			ns

(1) 1/128 f_S, 1/256 f_S, 1/384 f_S, 1/512 f_S, 1/768 f_S, or 1/1152 f_S.

7.7 Audio Interface Timing

for more information, see the *Audio Data Formats and Timing* section

			MIN	MAX	UNIT
$t_{(BCY)}$	BCK pulse cycle time	See Figure 22.	1/(32 f_S) 1/(48 f_S) 1/(64 f_S)(1)		
$t_{(BCH)}$	BCK high–level time		35		ns
$t_{(BCL)}$	BCK low–level time		35		ns
$t_{(BL)}$	BCK rising edge to LRCK edge		10		ns
$t_{(LB)}$	LRCK falling edge to BCK rising edge		10		ns
$t_{(DS)}$	DATA setup time		10		ns
$t_{(DH)}$	DATA hold time		10		ns

(1) f_S is the sampling frequency (for example, 44.1 kHz, 48 kHz, 96 kHz, and so on).

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7.8 Control Interface Timing Requirements

these timing parameters are critical for proper control port operation

			MIN	NOM	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	See Figure 1.	100			ns
$t_{(MCL)}$	MC low-level time		50			ns
$t_{(MCH)}$	MC high-level time		50			ns
$t_{(MCH)}$	ML high-level time		See (1)			ns
$t_{(MLS)}$	ML falling edge to MC rising edge		20			ns
$t_{(MLH)}$	ML hold time (2)		20			ns
$t_{(MDH)}$	MD hold time		15			ns
$t_{(MCS)}$	MD setup time		20			ns

(1) $\frac{3}{256 \times f_S}$ seconds (min); f_S: sampling rate.
(2) MC rising edge for LSB to ML rising edge.

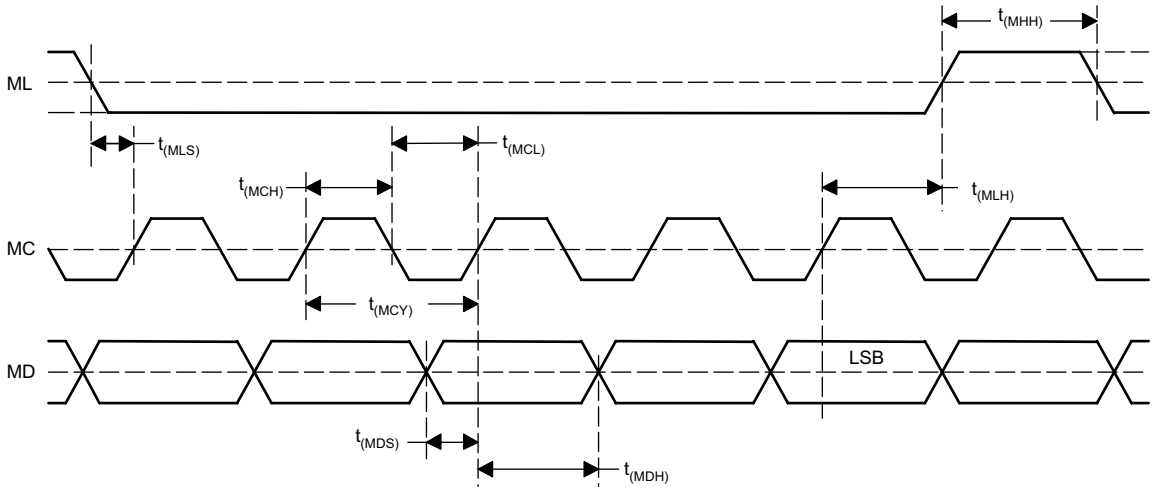

Figure 1. Control Interface Timing

7.9 Typical Characteristics

7.9.1 Digital Filter (De-Emphasis Off)

all specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

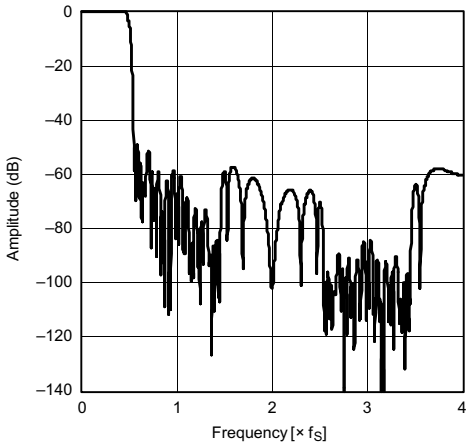

Figure 2. Frequency Response, Sharp Rolloff

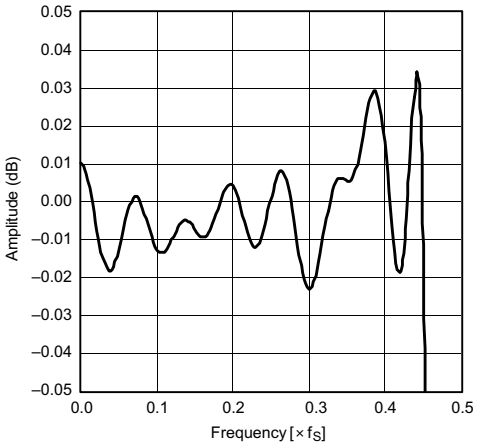

Figure 3. Pass-Band Ripple, Sharp Rolloff

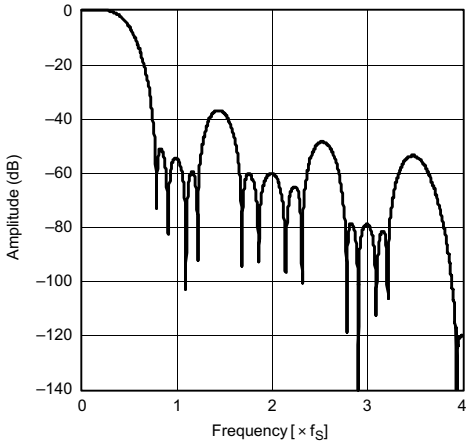

Figure 4. Frequency Response, Slow Rolloff

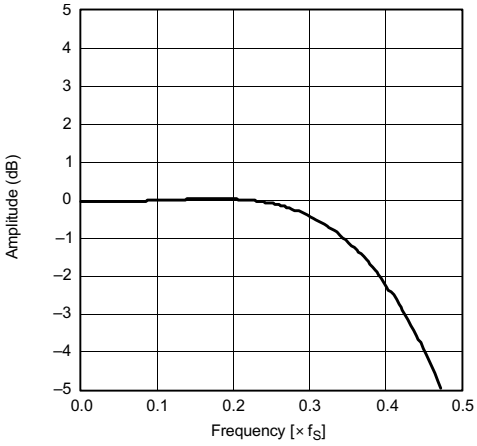

Figure 5. Transition Characteristics, Slow Rolloff

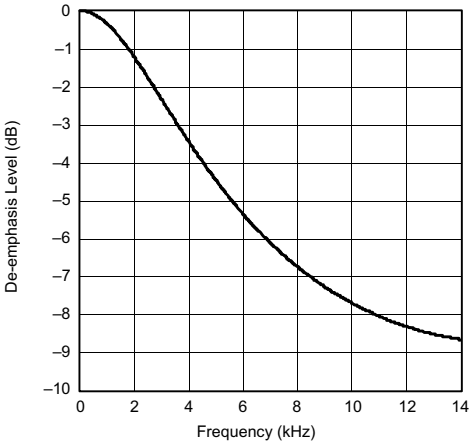

Figure 6. De-Emphasis Level vs Frequency

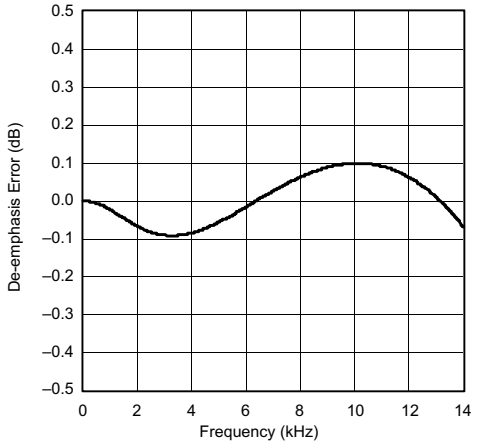

Figure 7. De-Emphasis Error vs Frequency

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Digital Filter (De-Emphasis Off) (continued)

all specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

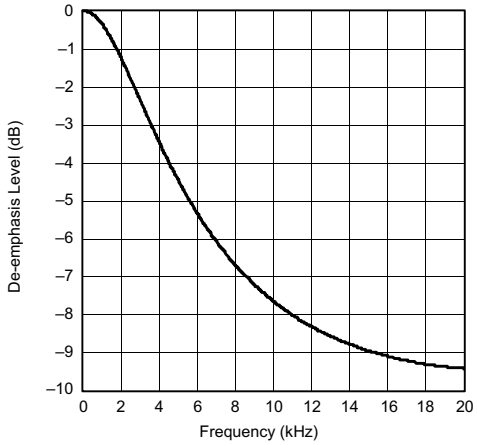

Figure 8. De-Emphasis Level vs Frequency

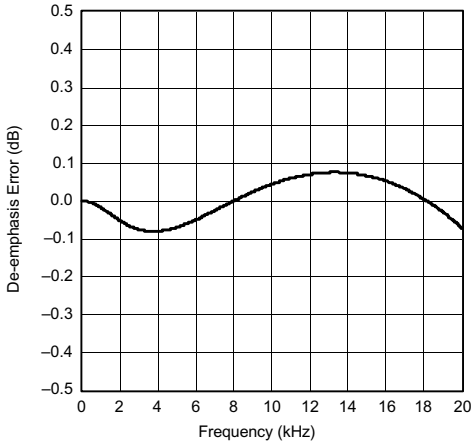

Figure 9. De-Emphasis Error vs Frequency

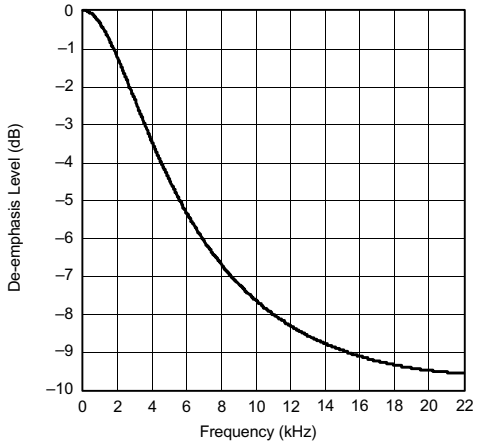

Figure 10. De-Emphasis Level vs Frequency

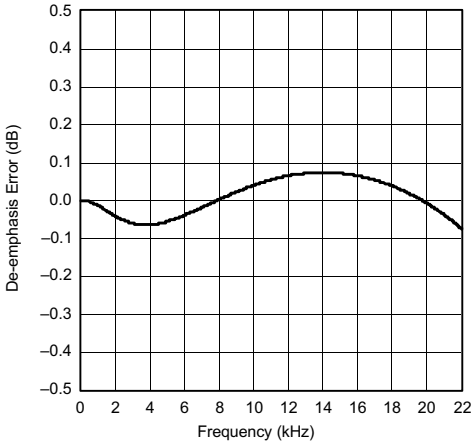

Figure 11. De-Emphasis Error vs Frequency

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7.9.2 Analog Dynamic Performance (Supply Voltage Characteristics)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

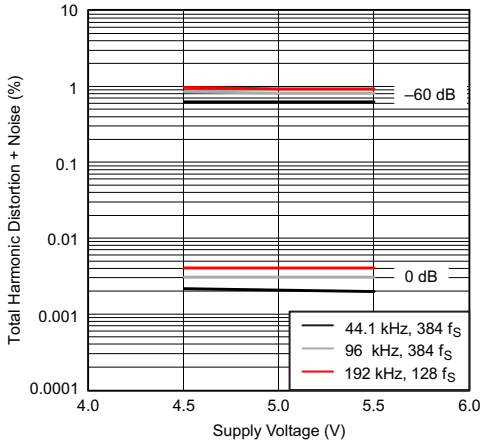

Figure 12. Total Harmonic Distortion + Noise vs Supply Voltage

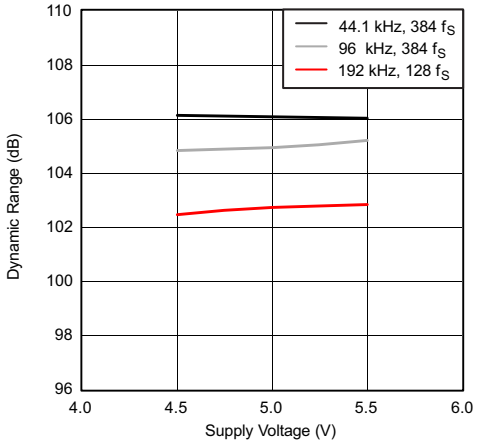

Figure 13. Dynamic Range vs Supply Voltage

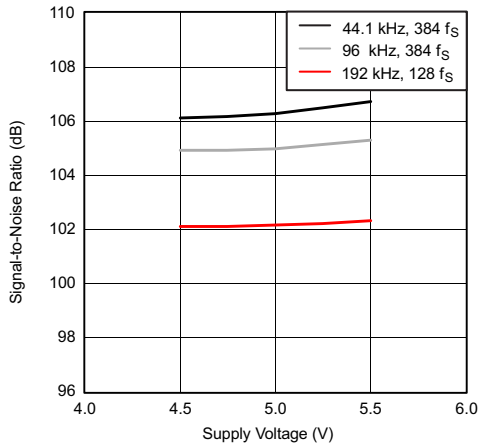

Figure 14. Signal-to-Noise Ratio vs Supply Voltage

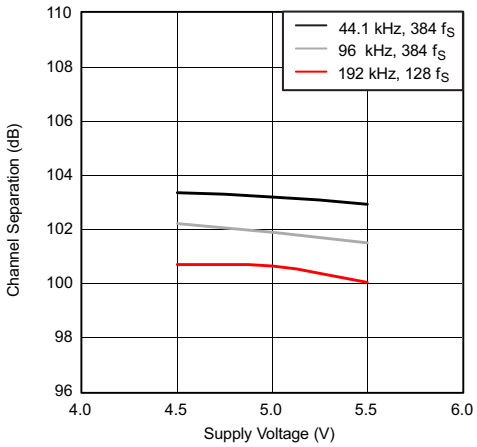

Figure 15. Channel Separation vs Supply Voltage

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7.9.3 Analog Dynamic Performance (Temperature Characteristics)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

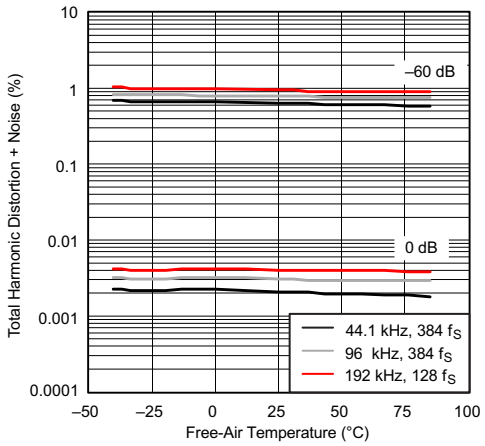

Figure 16. Total Harmonic Distortion + Noise vs Free-Air Temperature

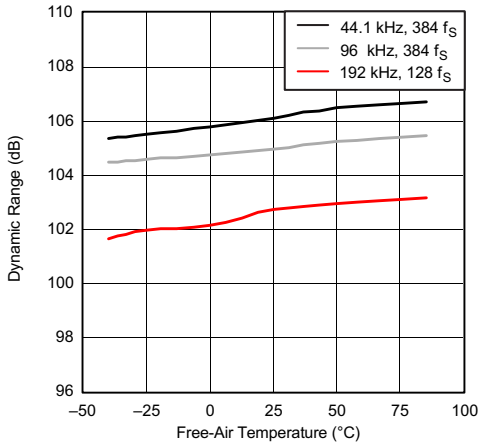

Figure 17. Dynamic Range vs Free-Air Temperature

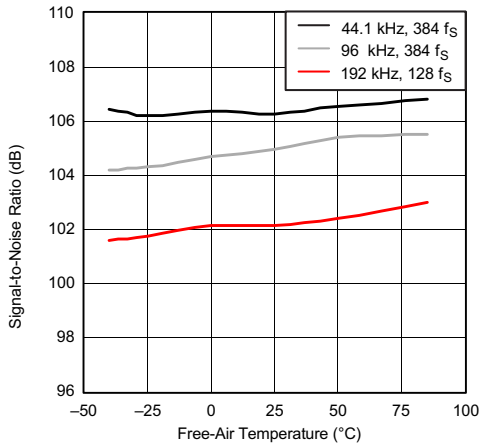

Figure 18. Signal-to-Noise Ratio vs Free-Air Temperature

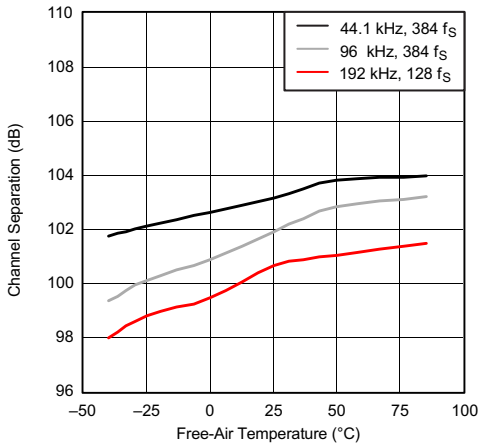

Figure 19. Channel Separation vs Free-Air Temperature

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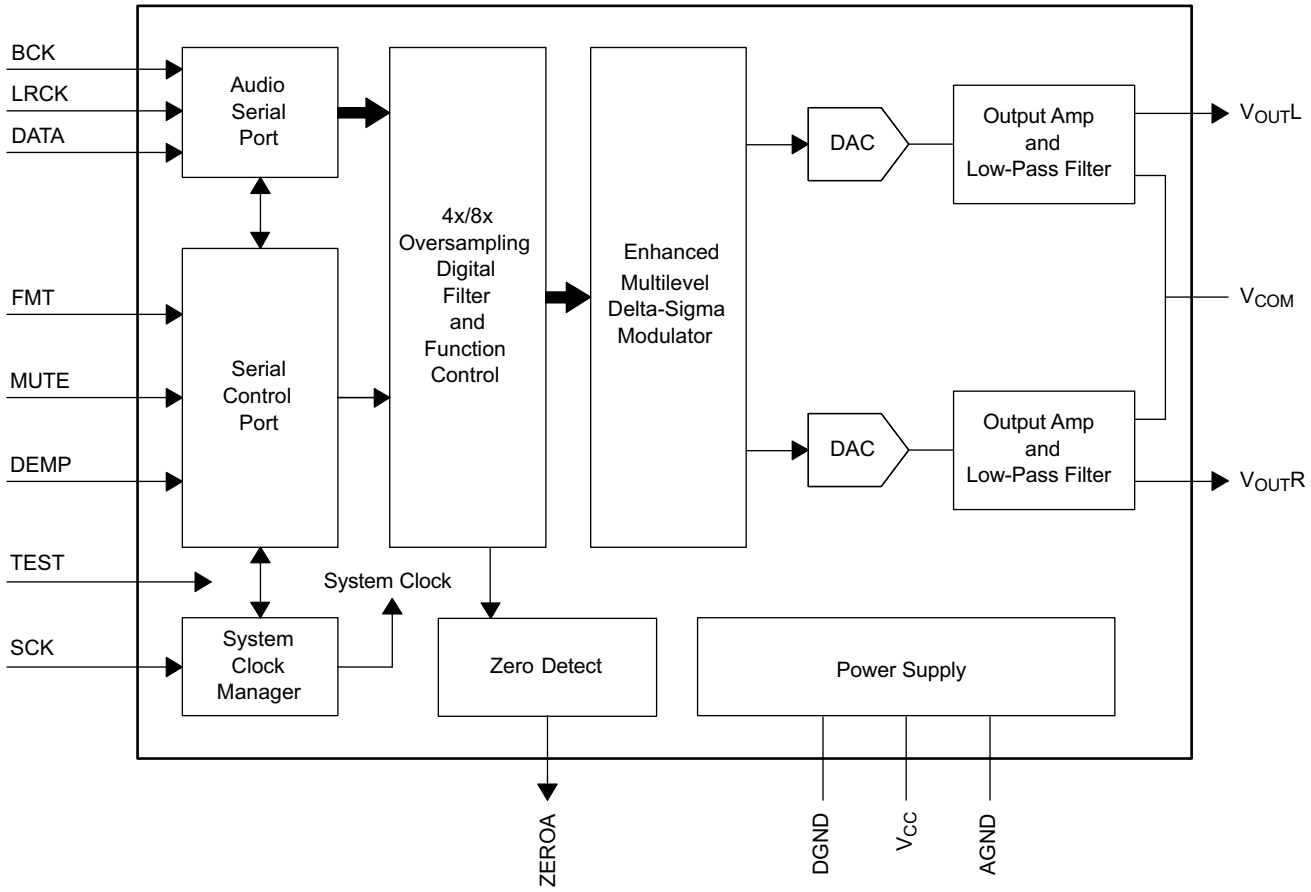
8 Detailed Description

8.1 Overview

The PCM175x devices are stereo digital-to-analog converters (DACs) based on TI's enhanced delta-sigma architecture which employ 4th-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved clock jitter tolerance. The PCM175x devices easily interface with audio DSP and decoder chips because of the devices' support of industry-standard audio data formats with 16- and 24-bit data. The PCM175x devices can be controlled in a hardware mode, or a full set of user-programmable functions is accessible through a three-wire serial control port, which supports register-write functions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 System Clock and Reset Functions

8.3.1.1 System Clock Input

The PCM175x devices require a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCK input (pin 16). Table 1 lists examples of system clock frequencies for common audio sampling rates.

Figure 20 shows and the *System Clock Input Timing* table lists he timing requirements for the system clock input. For optimal performance, use a clock source with low phase-jitter and noise. TI's PLL170x family of multiclock generators is an excellent choice for providing the PCM175x system clock.

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Feature Description (continued)

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)						
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1152 f_S
8 kHz	1.024	1.536	2.048	3.072	4.096	6.144	9.216
16 kHz	2.048	3.072	4.096	6.144	8.192	12.288	18.432
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576	36.864
44.1 kHz	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	(1)
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864	(1)
88.2 kHz	11.2896	16.9344	22.5792	33.8688	45.1584	(1)	(1)
96 kHz	12.288	18.432	24.576	36.864	49.152	(1)	(1)
192 kHz	24.576	36.864	(1)	(1)	(1)	(1)	(1)

(1) This system clock rate is not supported for the given sampling frequency.

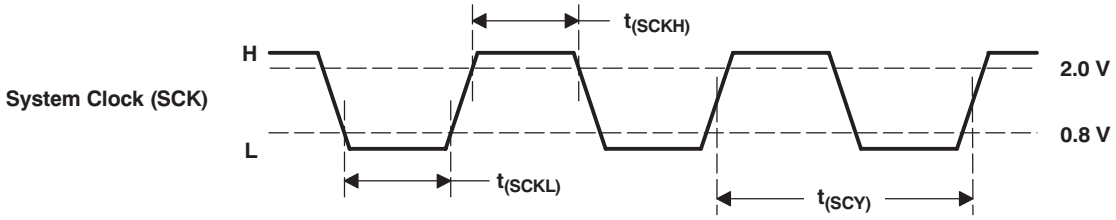

Figure 20. System Clock Input Timing

8.3.1.2 Power-On Reset Functions

The PCM175x devices include a power-on reset function. Figure 21 shows the operation of this function. With the system clock active and V_{CC} > 3 V (typical, 2.2 V to 3.7 V), the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{CC} > 3 V (typical, 2.2 V to 3.7 V).

During the reset period (1024 system clocks), the analog output is forced to the bipolar zero level, or $V_{CC}/2$. After the reset period, an internal register is initialized in the next $1/f_S$ period and if SCK, BCK, and LRCK are provided continuously, the PCM175x devices provide proper analog output with unit group delay against the input data.

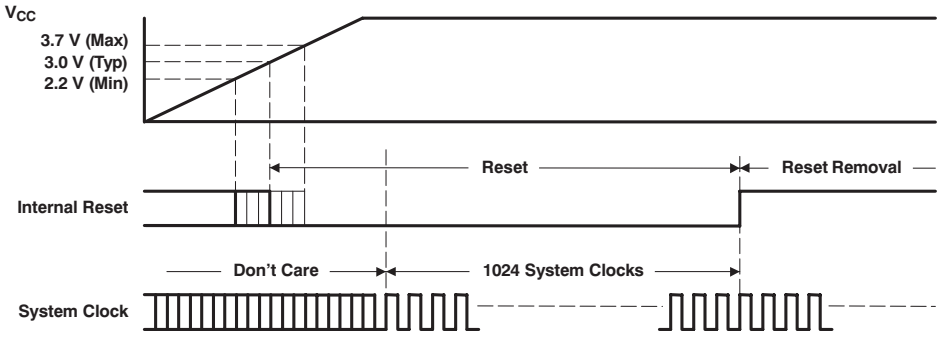

Figure 21. Power-On Reset Timing

8.3.2 Audio Serial Interface

The audio serial interface for the PCM175x devices consists of a 3-wire synchronous serial port. The interface includes LRCK (pin 3), BCK (pin 1), and DATA (pin 2). The BCK pin is the serial audio bit clock, and it is used to clock the serial data present on the DATA pin into the serial shift register of the audio interface. Serial data is clocked into the PCM175x on the rising edge of the BCK pin. The LRCK pin is the serial audio left and right word clock. This pin is used to latch serial data into the internal registers of the serial audio interface.

Both the LRCK and BCK pins should be synchronous to the system clock. Ideally, TI recommendeds that the LRCK and BCK pins be derived from the system clock input, SCK. The LRCK pin is operated at the sampling frequency, f_S. The BCK pin can be operated at 32, 48, or 64 times the sampling frequency for standard (right-justified) format, and 32 times the sampling frequency of the BCK pin is limited to 16-bit right-justified format only. The BCK pin can be operated at 48 or 64 times the sampling frequency for the I^2S and left-justified formats. 48 times the sampling frequency of BCK is limited to 192/384/768 f_S SCKI.

Internal operation of the PCM175x devices is synchronized with the LRCK pin. Accordingly, internal operation is held when the sampling rate clock of the LRCK pin is changed or when the SCK pin and/or BCK pin is interrupted for a 3-bit clock cycle or longer. If th SCK, BCK, and LRCK pins are provided continuously after this held condition, the internal operation is re-synchronized automatically in a period of less than $3/f_S$. External resetting is not required.

8.3.2.1 Audio Data Formats and Timing

The PCM1753 device supports industry-standard audio data formats, including right-justified, I2S, and left-justified. The PCM1754 device supports I^2S and 16-bit-word right-justified audio data formats. Figure 23 shows the data formats. Data formats are selected using the format bits, FMT[2:0], located in control register 20 of the PCM1753 device, and are selected using the FMT pin on the PCM1754 device. The default data format is 24-bit left-justified. All formats require binary 2s-complement MSB-first audio data. The *Audio Interface Timing* table shows a detailed timing diagram for the serial audio interface.

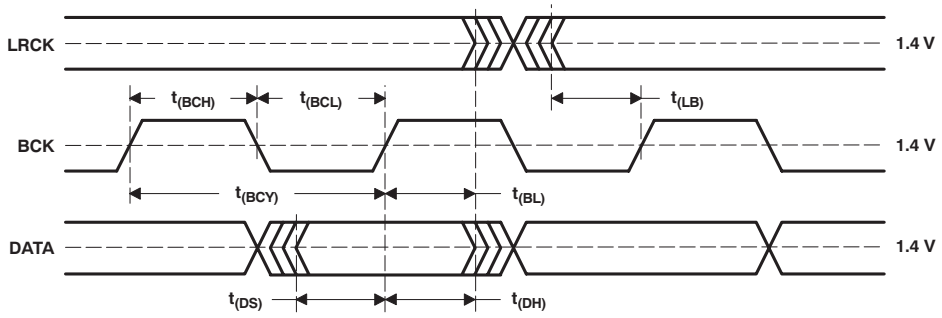

Figure 22. Audio Interface Timing

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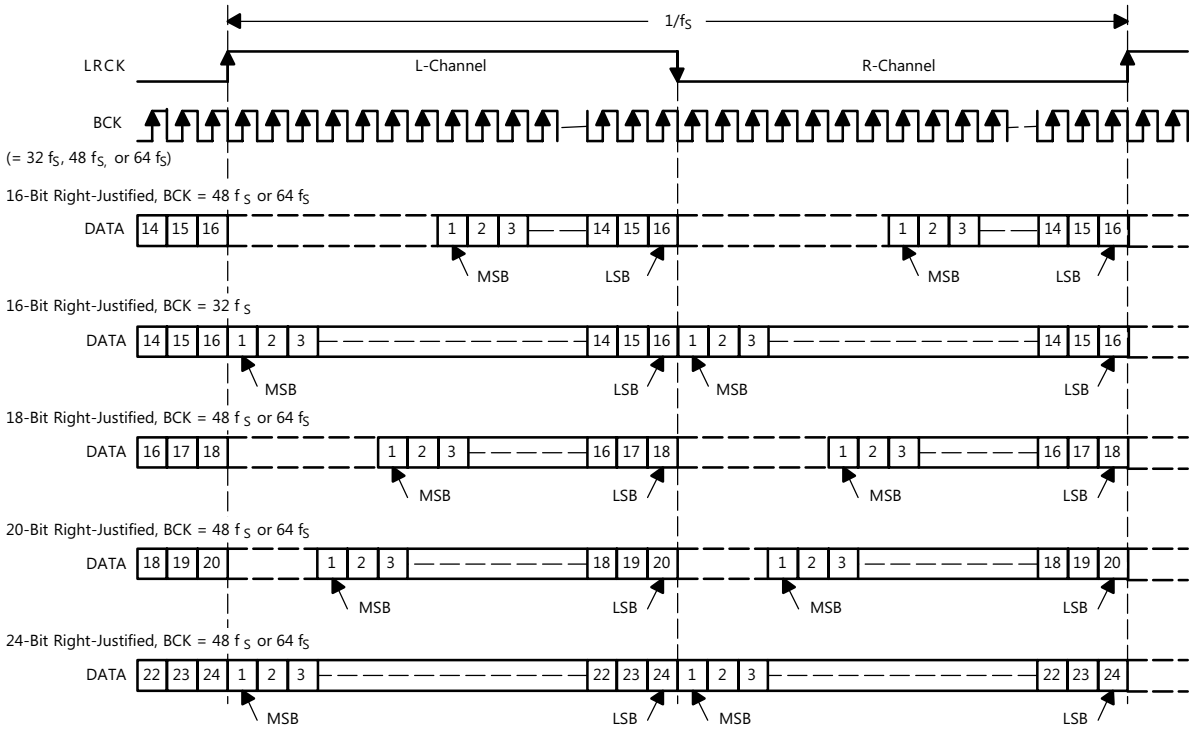
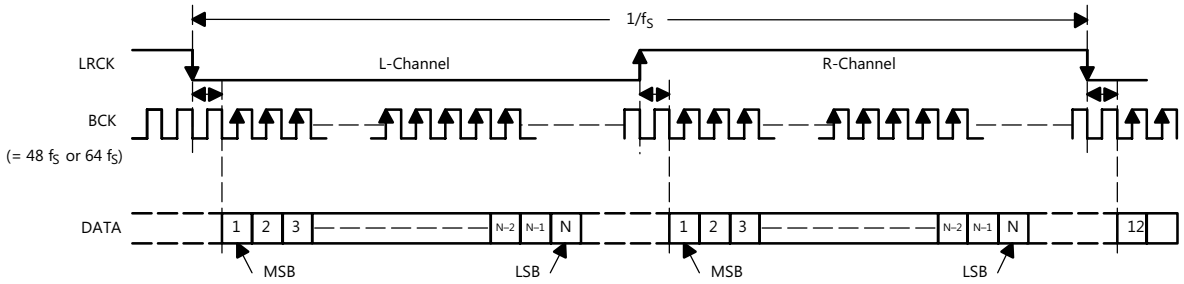
(1) Standard Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW

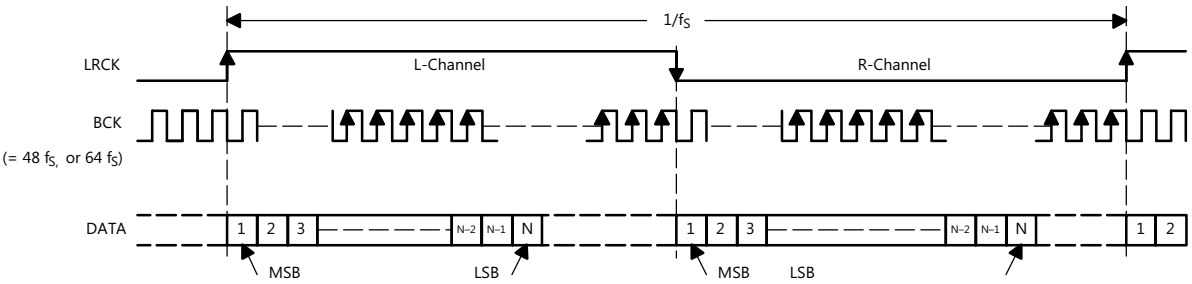


Figure 23. Audio Data Input Formats

8.3.3 Zero Flag (PCM1754)

The PCM1754 device has a ZERO flag pin, ZEROA (pin 11). ZEROA is the L-channel and R-channel common zero flag pin. If the data for L-channel and R-channel remains at a 0 level for 1024 sampling periods (or LRCK clock periods), ZEROA is set to a logic 1 state.

8.3.4 Zero Flag (PCM1753)

Zero-Detect Condition

Zero detection for either output channel is independent from the other channel. If the data for a given channel remains at a 0 level for 1024 sample periods (or LRCK clock periods), a zero-detect condition exists for that channel.

8.3.5 Zero Flag Outputs

If a zero-detect condition exists for one or more channels, the zero flag pins for those channels are set to a logic 1 state. There are zero flag pins for each channel, ZEROL (pin 12) and ZEROR (pin 11). These pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally controlled function. The active polarity of zero flag outputs can be inverted by setting the ZREV bit of control register 22 to 1. The reset default is active-high output, or ZREV = 0. The L-channel and R-channel common zero flag can be selected by setting the AZRO bit of control register 22 to 1. The reset default is independent zero flags for L-channel and R-channel, or AZRO = 0.

8.3.6 Analog Outputs

The PCM1753 device includes two independent output channels, $V_{OUT}L$ and $V_{OUT}R$. These are unbalanced outputs, each capable of driving 4 V_{PP} typical into a 5-kΩ ac-coupled load. The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are biased to the dc common-mode (or bipolar zero) voltage, equal to 0.5 V_{CC}.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM1754 delta-sigma D/A converters. The frequency response of this filter is shown in Figure 24. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for many applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Applications Information section of this data sheet.

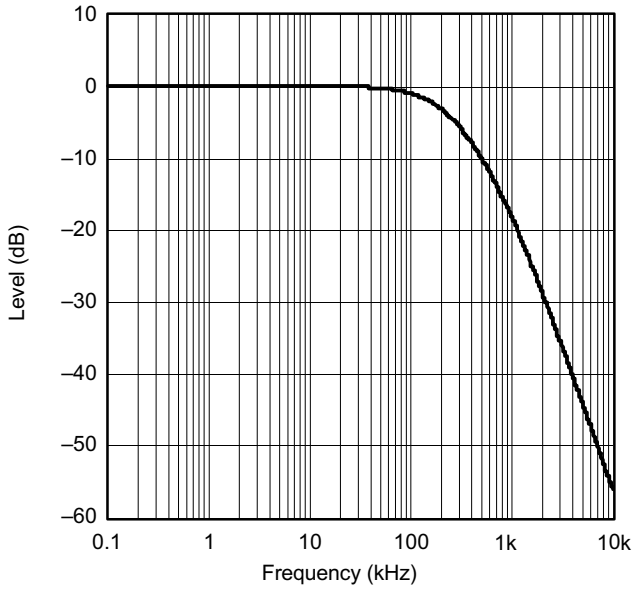


Figure 24. Output Filter Frequency Response

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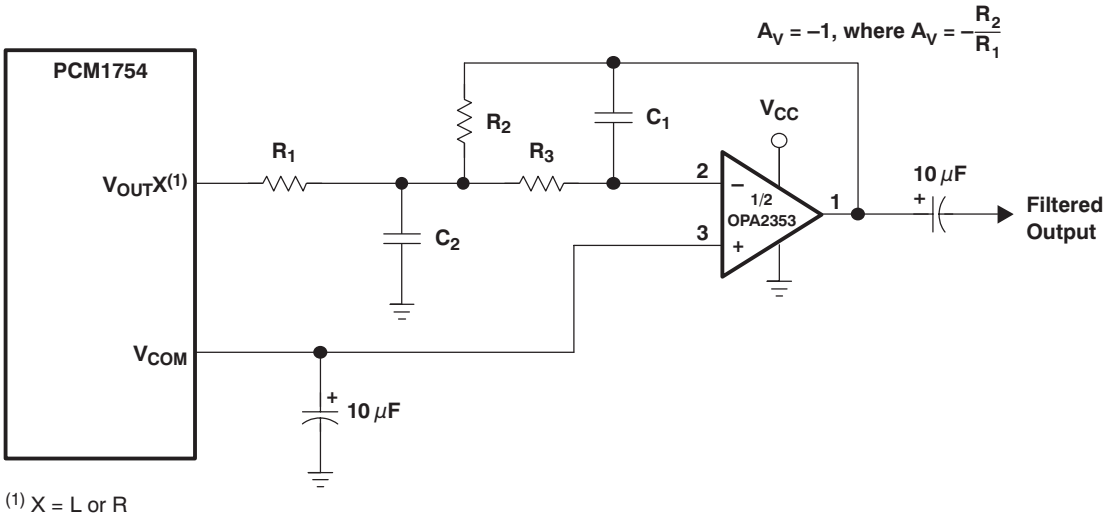
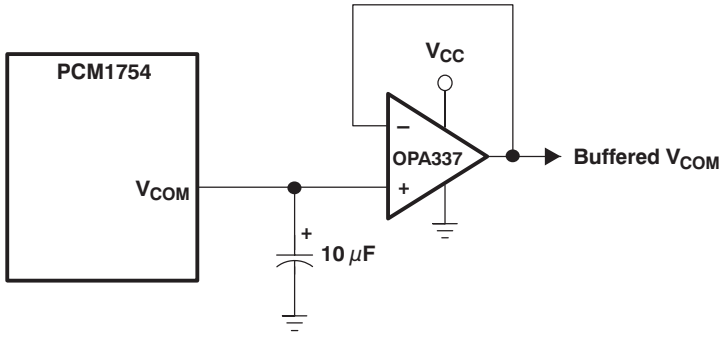
8.3.6.1 V_{COM} Output

One unbuffered common-mode voltage output pin, V_{COM} (pin 10) is brought out for decoupling purposes. This pin is nominally biased to a dc voltage level equal to 0.5 V_{CC}. This pin can be used to bias external circuits. Figure 25 shows an example of using the V_{COM} pin for external biasing applications.



(a) Using V_{COM} to Bias a Single-Supply Filter Stage



(b) Using a Voltage Follower to Buffer V_{COM} When Biasing Multiple Nodes

Figure 25. Biasing External Circuits Using the V_{COM} Pin

8.4 Device Functional Modes

8.4.1 Hardware Control (PCM1754)

The digital functions of the PCM1754 are capable of hardware control. Table 2 lists selectable formats, Table 3 shows de-emphasis control, and Table 4 lists mute control.

Table 2. Data Format Select

FMT (PIN 15)	DATA FORMAT
LOW	16– to 24–bit, I^2S format
HIGH	16–bit right–justified

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Table 3. De-Emphasis Control

DEMP (PIN 13)	DE–EMPHASIS FUNCTION
LOW	44.1 kHz de–emphasis OFF
HIGH	44.1 kHz de–emphasis ON

Table 4. Mute Control

MUTE (PIN 14)	MUTE
LOW	Mute OFF
HIGH	Mute ON

8.4.2 Oversampling Rate Control (PCM1754)

The PCM1754 automatically controls the oversampling rate of the delta-sigma DACs with the system clock rate. The oversampling rate is set to 64× oversampling with every system clock and sampling frequency.

8.5 Programming

8.5.1 Software Control (PCM1753/55)

The PCM1753 and PCM1755 devices have many programmable functions which can be controlled in the software control mode. The functions are controlled by programming the internal registers using the ML, MC, and MD pins.

The serial control interface is a 3-wire serial port, which operates asynchronously to the audio serial interface. The serial control interface is used to program the on-chip mode registers. The control interface includes MD (pin 13), MC (pin 14), and ML (pin 15). The MD pin is the serial data input, used to program the mode registers. The MC pin is the serial bit clock, used to shift data into the control port. The ML pin is the control port latch clock.

8.5.1.1 Register Write Operation

All write operations for the serial control port use 16-bit data words. Figure 26 lists the control data word format. The most significant bit must be a 0. There are seven bits, labeled IDX[6:0], that set the register index (or address) for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 27 lists the functional timing diagram for writing to the serial control port. ML is held at a logic 1 state until a register needs to be written. To start the register write cycle, ML is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the sixteenth clock cycle has completed, ML is set to logic 1 to latch the data into the indexed mode control register.

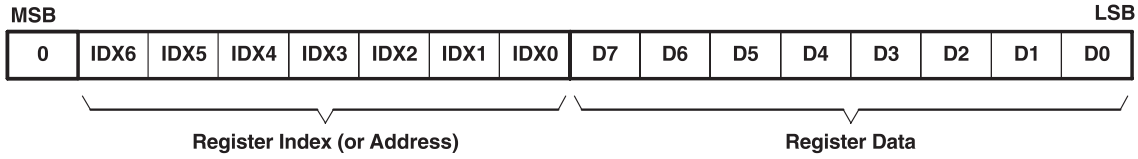

Figure 26. Control Data Word Format for MD

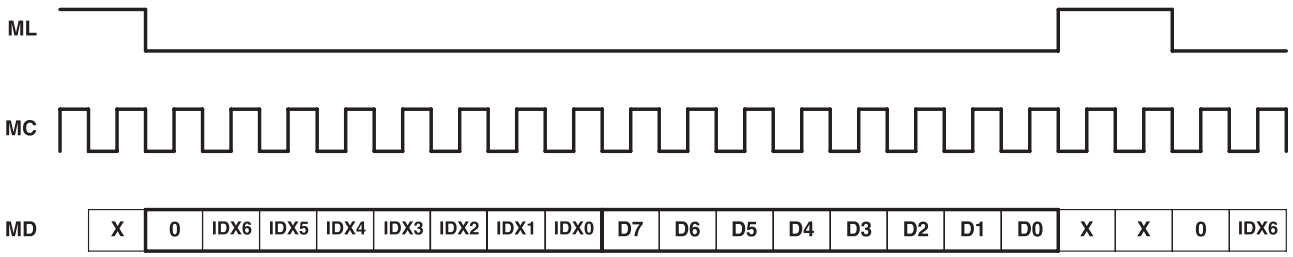

Figure 27. Register Write Operation

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8.6 Register Maps

8.6.1 Mode Control Registers (PCM1753/55)

8.6.1.1 User-Programmable Mode Controls

The PCM1753/55 devices include a number of user-programmable functions, which are accessed via control registers. The registers are programmed using the serial control interface, which was previously discussed in this data sheet. Table 5 lists the available mode control functions, along with their reset default conditions and associated register index.

Table 5. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER	BIT(s)
Digital attenuation control, 0 dB to –63 dB in 0.5-dB steps	0 dB, no attenuation	16 and 17	AT1[7:0], AT2[7:0]
Soft mute control	Mute disabled	18	MUT[2:0]
Oversampling rate control (64 f_S or 128 f_S)	64 f_S oversampling	18	OVER
Soft reset control	Reset disabled	18	SRST
DAC operation control	DAC1 and DAC2 enabled	19	DAC[2:1]
De-emphasis function control	De-emphasis disabled	19	DM12
De-emphasis sample rate selection	44.1 kHz	19	DMF[1:0]
Audio data format control	24-bit left-justified	20	FMT[2:0]
Digital filter rolloff control	Sharp rolloff	20	FLT
Zero flag function select	L-, R-channel independent	22	AZRO
Output phase select	Normal phase	22	DREV
Zero flag polarity select	High	22	ZREV

The mode control register map is shown in Table 6. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 6. Mode Control Register Map(1)

IDX (B8–B14)	REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
10h	Register 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
11h	Register 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
12h	Register 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1
13h	Register 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1
14h	Register 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0
16h	Register 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	AZRO	ZREV	DREV

(1) RSV: Reserved for test operation. It should be set to 0 for regular operation.

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8.6.1.2 Register Definitions

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

8.6.1.2.1 ATx[7:0]: Digital Attenuation Level Setting

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 1111 1111b

Each DAC channel ($V_{OUT}L$ and $V_{OUT}R$) includes a digital attenuation function. The attenuation level can be set from 0 dB to –63 dB in 0.5-dB steps. Changes in attenuator levels are made by incrementing or decrementing one step (0.5 dB) for every 8/fS time internal until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

The attenuation data for each channel can be set individually. The attenuation level is set using the following formula:

Attenuation level (dB) = 0.5 × ($ATx[7:0]_{DEC}$ – 255)

where $ATx[7:0]_{DEC}$ = 0 through 255.

For ATx[7:0]DEC = 0 through 128, attenuation is set to infinite attenuation.

The table in Figure 28 shows the attenuation levels for various settings:

ATx[7:0]	DECIMAL VALUE	ATTENUATION LEVEL SETTING
1111 1111b	255	0 dB, No Attenuation. (default)
1111 1110b	254	–0.5 dB
1111 1101b	253	–1.0 dB
⋮	⋮	⋮
1000 0011b	131	–62.0 dB
1000 0010b	130	–62.5 dB
1000 0001b	129	–63.0 dB
1000 0000b	128	Mute
⋮	⋮	⋮
$0000\ 0000_B$	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1

Figure 28. ATx[7:0]: Digital Attenuation Level Setting Table

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8.6.1.2.2 MUTx: Soft Mute Control

where x = 1 or 2, corresponding to the DAC outputs $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 0

MUTx = 0	Mute disabled (default)
MUTx = 1	Mute enabled

The mute bits, MUT1 and MUT2, are used to enable or disable the soft mute function for the corresponding DAC outputs, VOUTL and VOUTR. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation, one attenuator step (0.5 dB) for every 8/fS seconds. This provides pop-free muting of the DAC output.

By setting MUTx = 0, the attenuator is increased one step for every 8/fS seconds to the previously programmed attenuation level.

8.6.1.2.3 OVER: Oversampling Rate Control

Default value: 0

System clock rate = 256 f_S, 384 f_S, 512 f_S, 768 f_S, or 1152 f_S:

OVER = 0	64· oversampling (default)
OVER = 1	128· oversampling

System clock rate = 128 f_S or 192 f_S:

OVER = 0	32· oversampling (default)
OVER = 1	64· oversampling

The OVER bit is used to control the oversampling rate of the delta-sigma D/A converters. The OVER = 1 setting is recommended when the sampling rate is 192 kHz (system clock rate is 128 f_S or 192 f_S).

8.6.1.2.4 SRST: Reset

Default value: 0

SRST = 0	Reset disabled (default)
SRST = 1	Reset enabled

The SRST bit is used to enable or disable the soft reset function. The operation is the same as power-on reset. All registers are initialized.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1

8.6.1.2.5 DACx: DAC Operation Control

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) or $V_{OUT}R$ (x = 2).

Default value: 0

DACx = 0	DAC operation enabled (default)
DACx = 1	DAC operation disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. When DACx = 0, the corresponding output generates the audio waveform dictated by the data present on the DATA pin. When DACx = 1, the corresponding output is set to the bipolar zero level, or 0.5 V_{CC}.

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8.6.1.2.6 DM12: Digital De-Emphasis Function Control

Default value: 0

DM12 = 0	De-emphasis disabled (default)
DM12 = 1	De-emphasis enabled

The DM12 bit is used to enable or disable the digital de-emphasis function. See the plots shown in the *Typical Characteristics* section of this data sheet.

8.6.1.2.7 DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

Default value: 00

The DMF[1:0] bits are used to select the sampling frequency used for the digital de-emphasis function when it is enabled.

DMF[1:0]	De-Emphasis Sample Rate Selection
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0

8.6.1.2.8 FMT[2:0]: Audio Interface Data Format

Default value: 101

The FMT[2:0] bits are used to select the data format for the serial audio interface. The table in Figure 29 shows the available format options.

FMT[2:0]	Audio Data Format Selection
000	24-bit standard format, right-justified data
001	20-bit standard format, right-justified data
010	18-bit standard format, right-justified data
011	16-bit standard format, right-justified data
100	16- to 24-bit I^2S format
101	16- to 24-bit left-justified format (default)
110	Reserved
111	Reserved

Figure 29. FMT[2:0]: Audio Interface Data Format Table

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8.6.1.2.9 FLT: Digital Filter Rolloff Control

Default value: 0

FLT = 0	Sharp rolloff (default)
FLT = 1	Slow rolloff

The FLT bit allows the user to select the digital filter rolloff that is best suited to the application. Two filter rolloff selections are available, sharp and slow. The filter responses for these selections are shown in the *Typical Characteristics* section of this data sheet.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	AZRO	ZREV	DREV

8.6.1.2.10 DREV: Output Phase Select

Default value: 0

DREV = 0	Normal output (default)
DREV = 1	Inverted output

The DREV bit is the output analog signal phase control.

8.6.1.2.11 ZREV: Zero Flag Polarity Select

Default value: 01h

ZREV = 0	High on zero flag pins indicates a zero detect (default)
ZREV = 1	Low on zero flag pins indicates a zero detect

The ZREV bit allows the user to select the polarity of zero flag pins.

8.6.1.2.12 AZRO: Zero Flag Function Select

Default value: 0

AZRO = 0	L-/R-channel independent zero flags (default)
AZRO = 1	L-/R-channel common zero flag

The AZRO bit allows the user to select the function of zero flag pins.

AZRO = 0:	Pin 11: ZEROR, zero flag output for R-channel
	Pin 12: ZEROL, zero flag output for L-channel
AZRO = 1:	Pin 11: ZEROA, zero flag output for L-/R-channels
	Pin 12: NA, not assigned

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The delta-sigma section of the PCM175x device is based on an 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format. A block diagram of the 8-level delta-sigma modulator is shown in Figure 32. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the interpolation filter is 64 f_S.

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 35 and Figure 36. The enhanced multilevel delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multilevel quantizer, with the simulated jitter sensitivity shown in Figure 37.

The PCM175X devices are suitable for a wide variety of cost-sensitive consumer applications requiring good performance and operation with a single 5-V supply.

9.2 Typical Application

A basic connection diagram is shown in Figure 30, with the necessary power supply bypassing and decoupling components. TI recommends using the component values shown in Figure 30 for all designs.

The use of series resistors (22 Ω to 100 Ω) is recommended for the SCK, LRCK, BCK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter, which reduces high-frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

For this design example, use the parameters listed in Table 7.

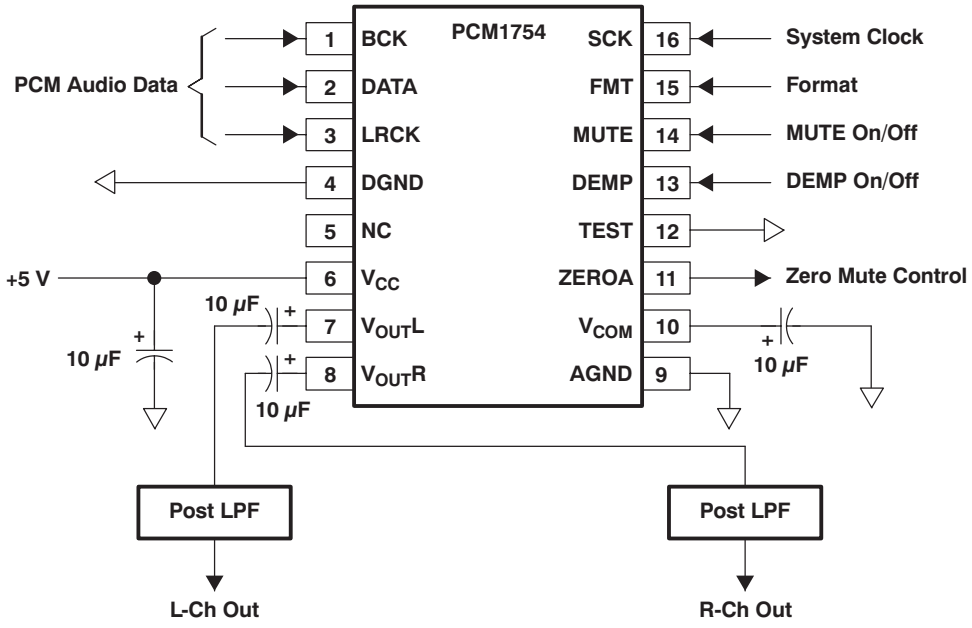

Figure 30. Basic Connection Diagram

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Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Design Parameters

Table 7 lists the design parameters and example values for the PCM175x devices.

Table 7. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Audio input	PCM audio data
Analog output	0 V_{PP} - 4 V_{PP}
Part configuration	Hardware

9.2.1.2 Power Supplies and Grounding

The PCM1754 device requires 5 V for V_{CC}.

Proper power supply bypassing is shown in Figure 30. The 10-μF capacitors should be tantalum or aluminum electrolytic.

9.2.1.3 D/A Output Filter Circuits

Delta-sigma D/A converters use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide the optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figure 25(a) and Figure 31 show the recommended external low-pass active filter circuits for single- and dual-supply applications. These circuits are 2nd-order Butterworth filters using the multiple feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, see Burr-Brown applications bulletin (SBAA055), available from the TI Web site at http://www.ti.com.

Because the overall system performance is defined by the quality of the D/A converters and their associated analog output circuitry, high-quality audio operational amplifiers are recommended for the active filters. TI's OPA2353 and OPA2134 dual operational amplifiers are shown in Figure 25(a) and Figure 31, and are recommended for use with the PCM1754 device.

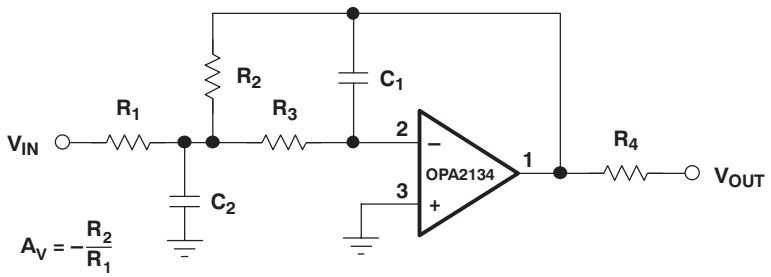

Figure 31. Dual-Supply Filter Circuit

9.2.2 Detailed Design Procedure

9.2.2.1 Total Harmonic Distortion + Noise

Total harmonic distortion + noise (THD+N) is a significant figure of merit for audio D/A converters because it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The average value of the distortion and noise is referred to as THD+N.

For the PCM175x, THD+N is measured with a full-scale, 1-kHz digital sine wave as the test stimulus at the input of the DAC (see Figure 33). The digital generator is set to 24-bit audio word length and a sampling frequency of 44.1 kHz or 96 kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via a coaxial cable to the digital audio receiver on the DEM-DAI1753 demonstration board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

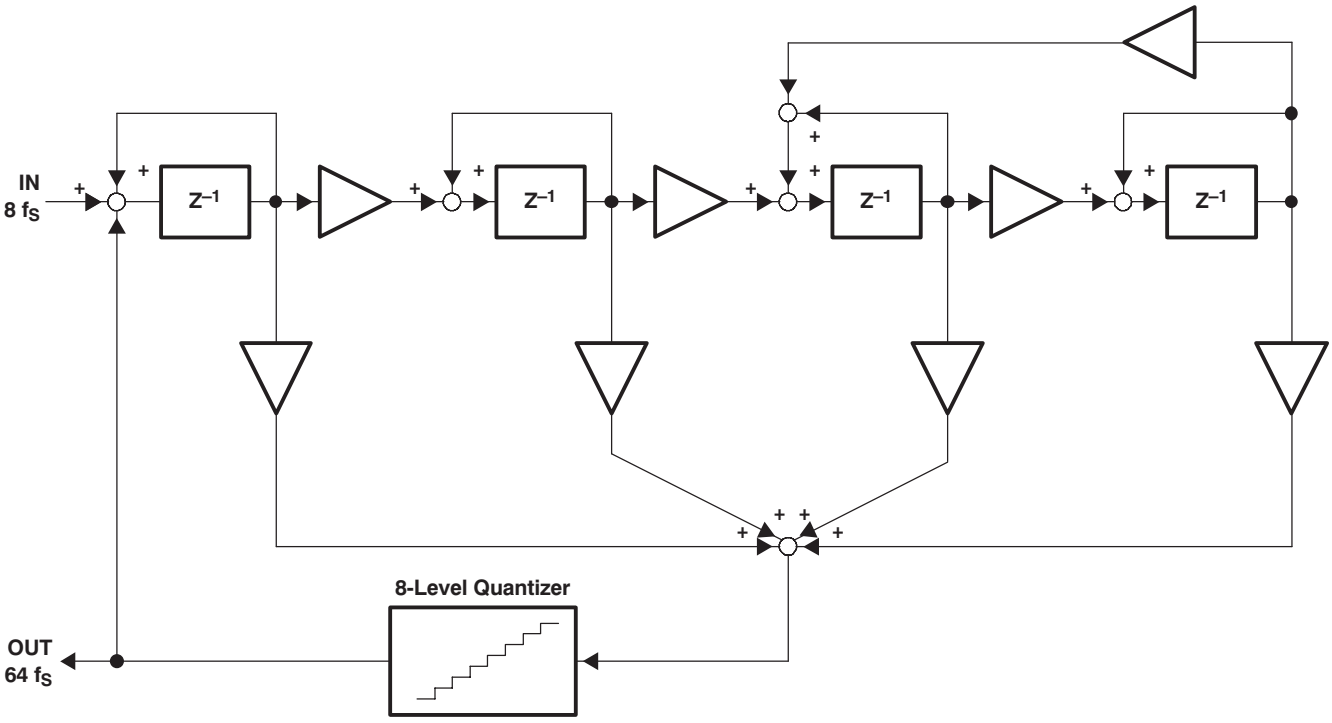

Figure 32. Eight-Level Delta-Sigma Modulator

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9.2.2.2 Dynamic Range

Dynamic range is specified as A-weighted THD+N measured with a –60-dB full-scale, 1-kHz digital sine wave stimulus at the input of the D/A converter. This measurement is designed to give a good indicator of how the DAC performs given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 34, and is similar to the THD+N test setup discussed previously. The differences include the band limit filter selection, the additional A-weighting filter, and the –60-dB full-scale input level.

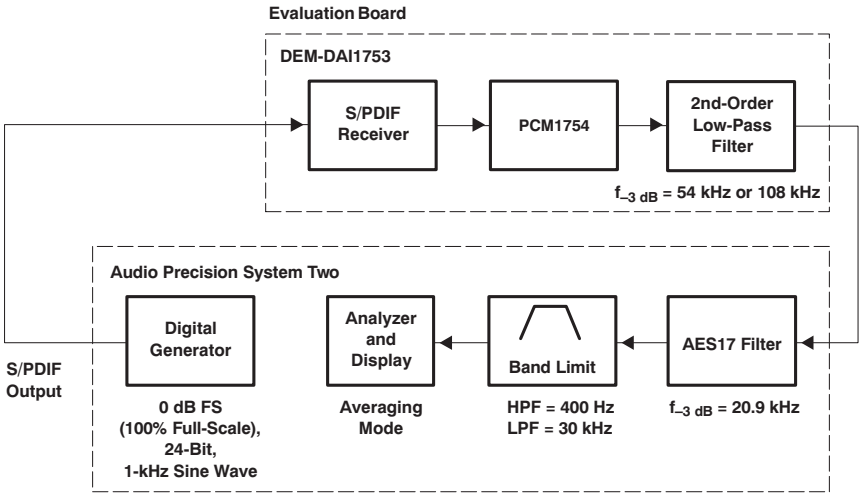


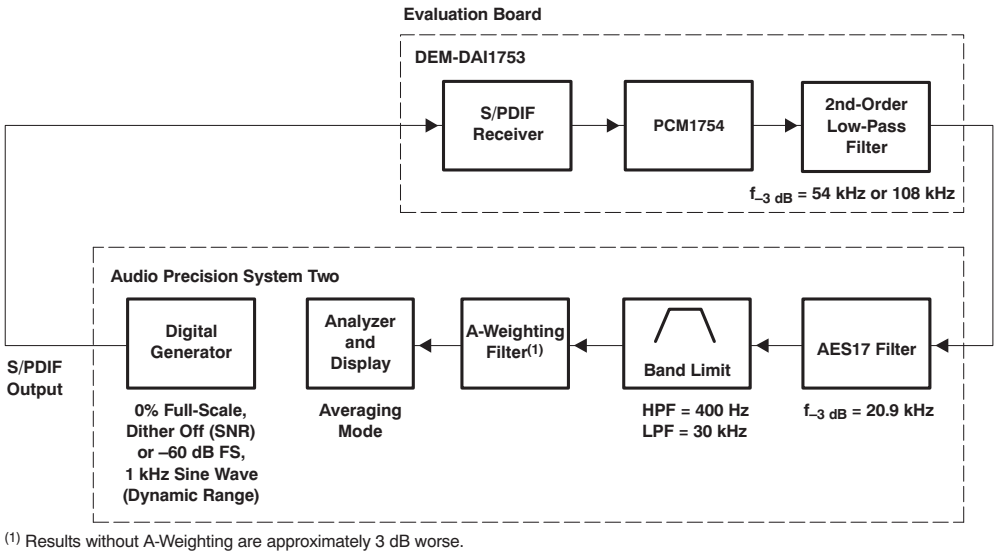
Figure 33. Test Setup for THD+N Measurement

9.2.2.3 Idle Channel Signal-to-Noise Ratio (SNR)

The SNR test provides a measure of the noise floor of the D/A converter. The input to the D/A is all-0s data, and the dither function of the digital generator must be disabled to ensure an all-0s data stream at the input of the D/A converter.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level.

(See the note provided in Figure 34).



(1) Results without A-Weighting are approximately 3 dB worse.

Figure 34. Test Setup for Dynamic Range and SNR Measurement

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9.2.3 Application Curves

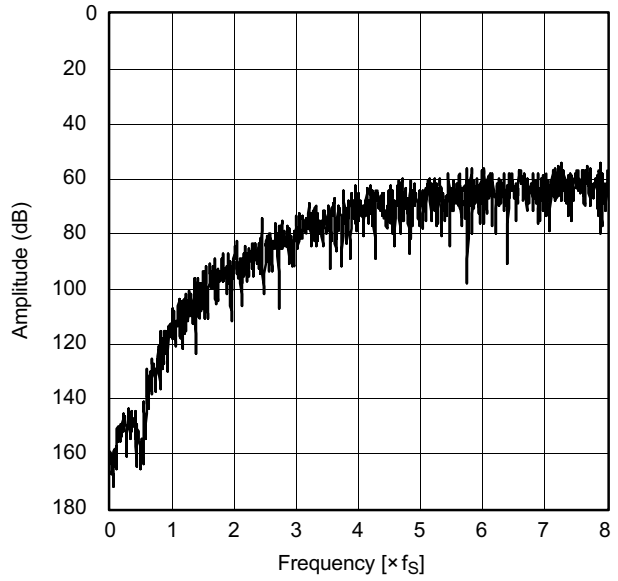

Figure 35. Quantization Noise Spectrum (×64 Oversampling)

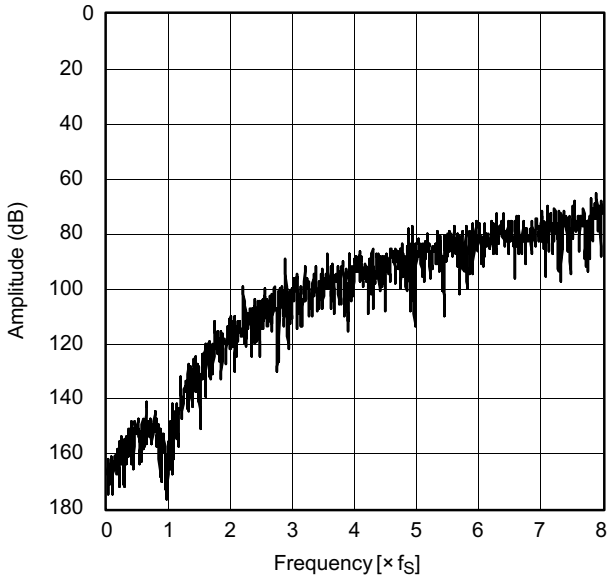

Figure 36. Quantization Noise Spectrum (×128 Oversampling)

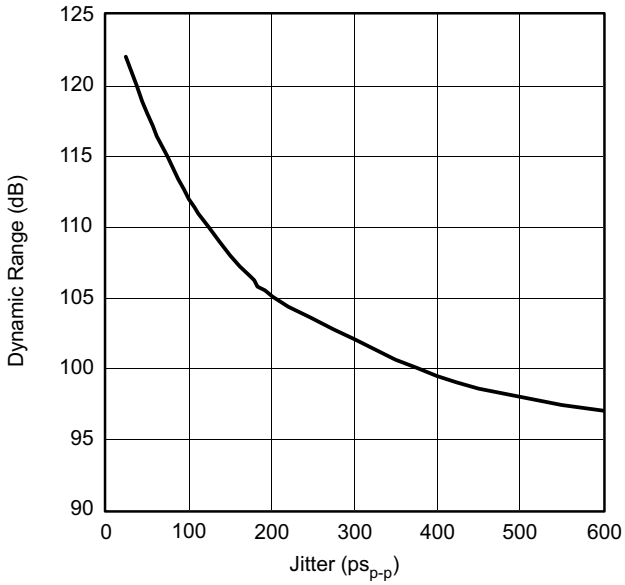

Figure 37. Jitter Dependence (×64 Oversampling)

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10 Power Supply Recommendations

The PCM175x devices are designed to operate from a 4.5-V to 5.5-V power supply. Ensure that the power supply is clean and use high-quality decoupling capacitors to reduce noise. The bulk capacitances can be from either tantalum or aluminum capacitors.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM175x devices. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 39 shows the recommended approach for single-supply applications.

11 Layout

11.1 Layout Guidelines

Figure 38 shows a typical PCB floor plan for the PCM175x devices. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM175x should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM175x. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 39 shows the recommended approach for single-supply applications.

11.2 Layout Example

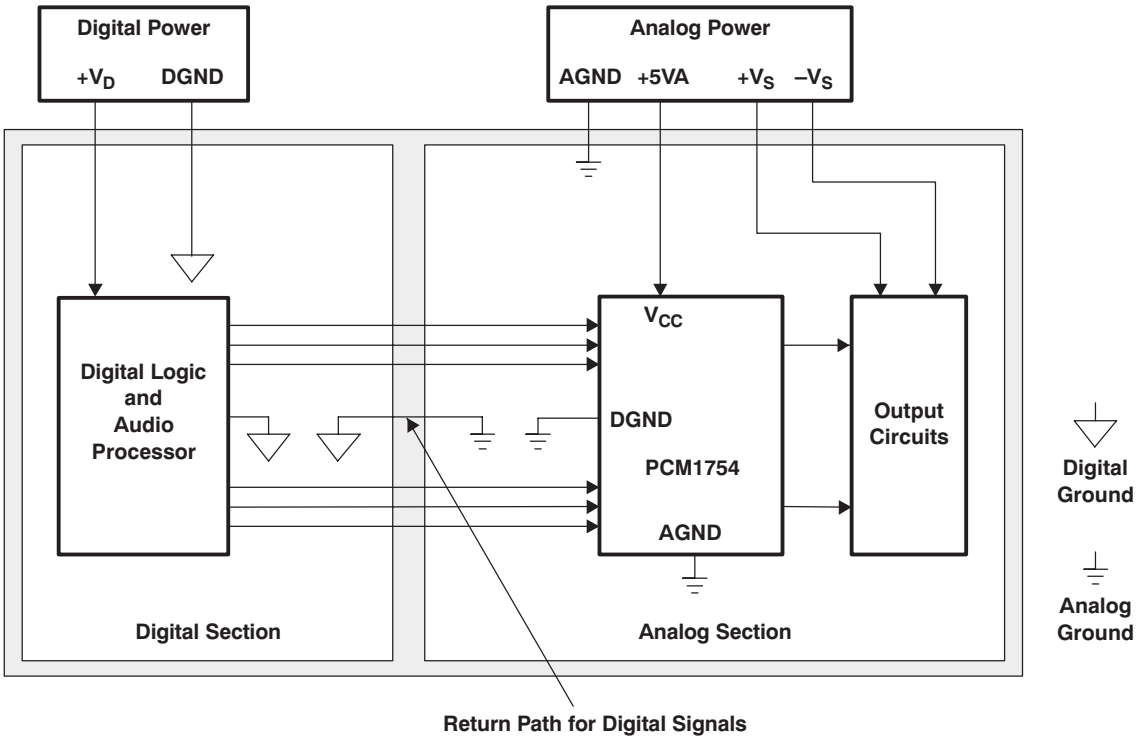

Figure 38. Recommended PCB Layout

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Layout Example (continued)

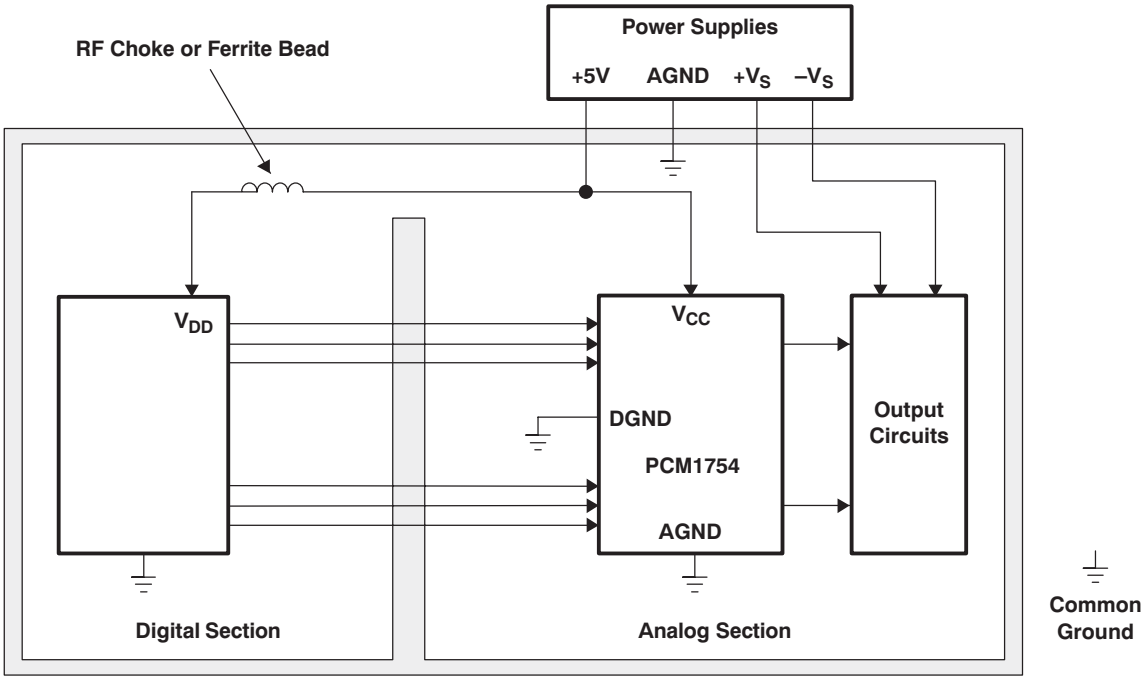

Figure 39. Single-Supply PCB Layout

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12 デバイスおよびドキュメントのサポート

12.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『Dynamic Performance Testing of Digital Audio D/A Converters』アプリケーション広報 (英語)
- テキサス・インスツルメンツ、『OPAx353 High-Speed, Single-Supply, Rail-to-Rail OPERATIONAL AMPLIFIERS MicroAmplifier™ Series』データシート (英語)
- テキサス・インスツルメンツ、『OPAx134 SoundPlus™ High Performance Audio Operational Amplifiers』データシート (英語)
- テキサス・インスツルメンツ、『PLL170x 3.3-V DUAL PLL MULTICLOCK GENERATOR』データシート (英語)
- テキサス・インスツルメンツ、『PCM175x-Q1 24-Bit 192-kHz Sampling Enhanced Multi-Level Delta-Sigma Audio Digital-to-Analog Converter』データシート (英語)

12.2 関連リンク

表 8 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8. 関連リンク

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ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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12.4 コミュニティ・リソース

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM1753DBQ	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1753
PCM1753DBQ.B	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1753
PCM1753DBQR	Active	Production	SSOP (DBQ) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1753
PCM1753DBQR.B	Active	Production	SSOP (DBQ) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1753
PCM1754DBQ	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1754
PCM1754DBQ.B	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1754
PCM1754DBQG4	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1754
PCM1754DBQR	Active	Production	SSOP (DBQ) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1754
PCM1754DBQR.B	Active	Production	SSOP (DBQ) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1754
PCM1754DBQRG4	Active	Production	SSOP (DBQ) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1754
PCM1755DBQ	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1755
PCM1755DBQ.B	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1755
PCM1755DBQR	Active	Production	SSOP (DBQ) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1755
PCM1755DBQR.B	Active	Production	SSOP (DBQ) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1755

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF PCM1753, PCM1754 :

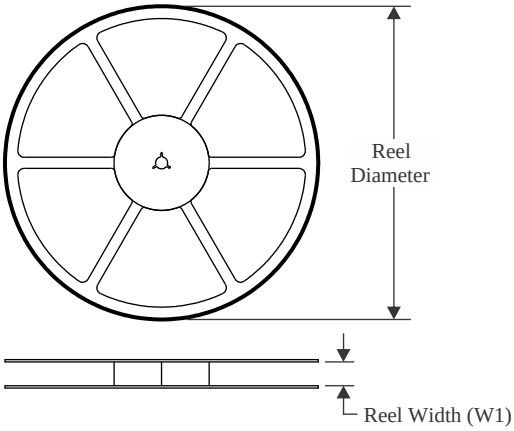
- Automotive : PCM1753-Q1, PCM1754-Q1

NOTE: Qualified Version Definitions:

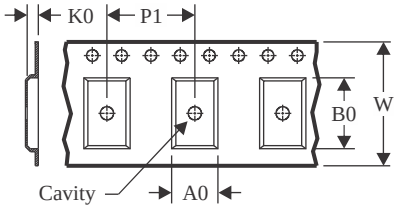
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

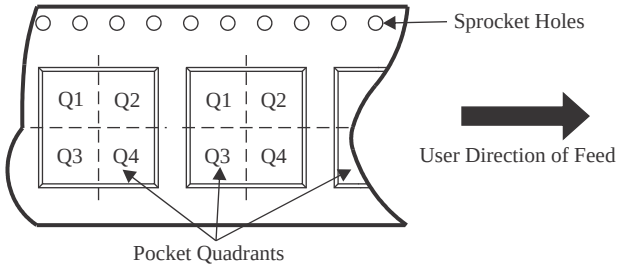


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

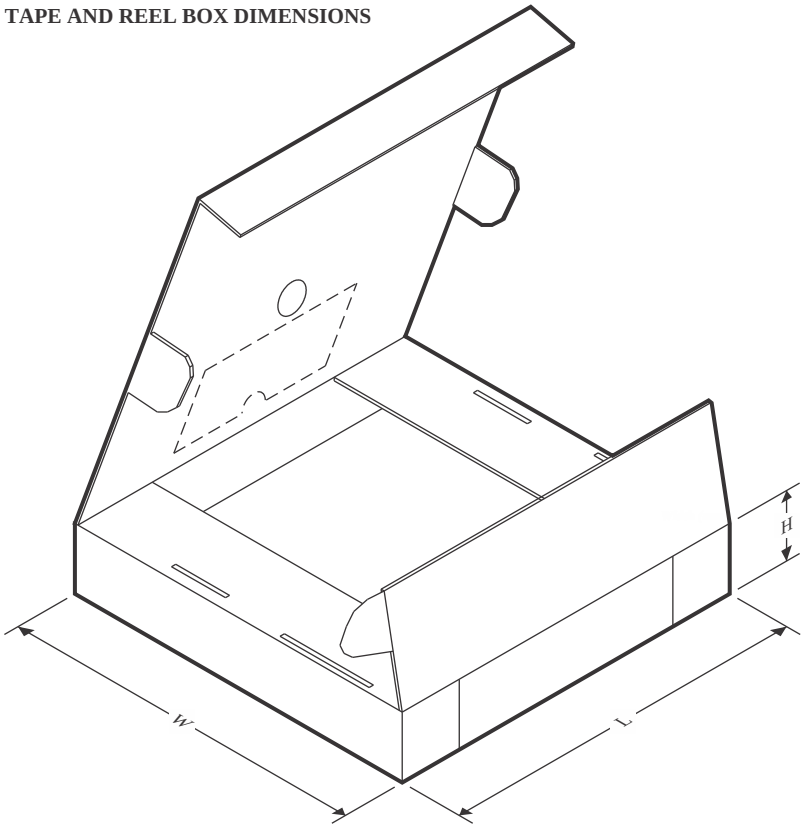
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1753DBQR	SSOP	DBQ	16	2000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
PCM1754DBQR	SSOP	DBQ	16	2000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
PCM1755DBQR	SSOP	DBQ	16	2000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

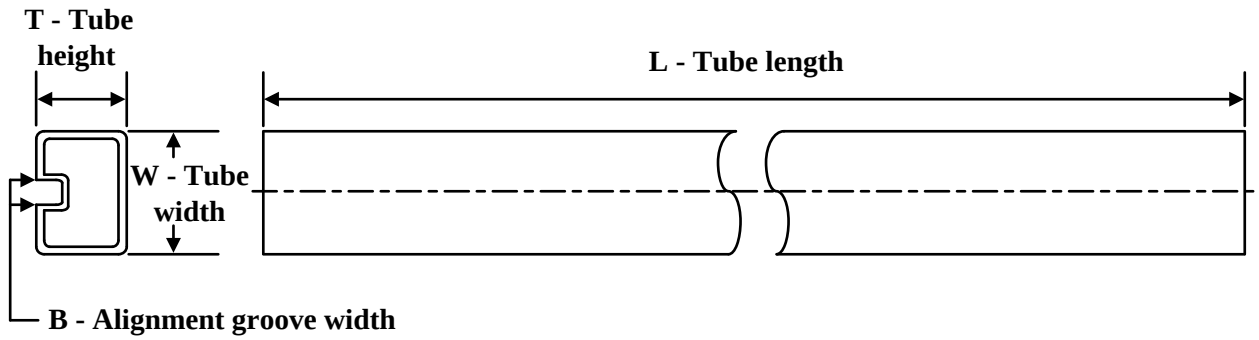
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

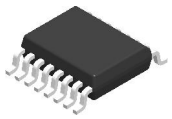
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1753DBQR	SSOP	DBQ	16	2000	356.0	356.0	35.0
PCM1754DBQR	SSOP	DBQ	16	2000	356.0	356.0	35.0
PCM1755DBQR	SSOP	DBQ	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM1753DBQ	DBQ	SSOP	16	75	506.6	8	3940	4.32
PCM1753DBQ.B	DBQ	SSOP	16	75	506.6	8	3940	4.32
PCM1754DBQ	DBQ	SSOP	16	75	506.6	8	3940	4.32
PCM1754DBQ.B	DBQ	SSOP	16	75	506.6	8	3940	4.32
PCM1754DBQG4	DBQ	SSOP	16	75	506.6	8	3940	4.32
PCM1755DBQ	DBQ	SSOP	16	75	506.6	8	3940	4.32
PCM1755DBQ.B	DBQ	SSOP	16	75	506.6	8	3940	4.32

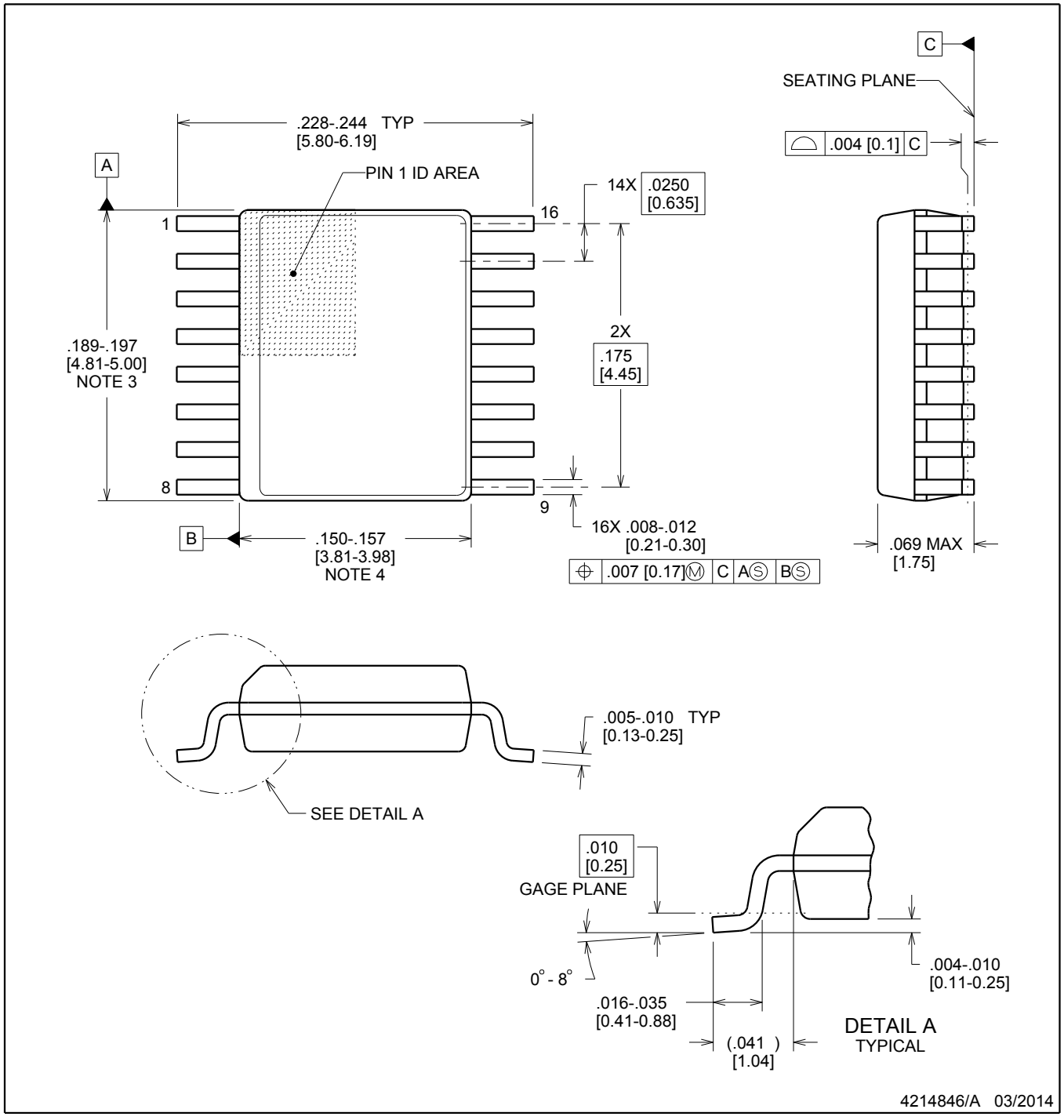


PACKAGE OUTLINE

DBQ0016A

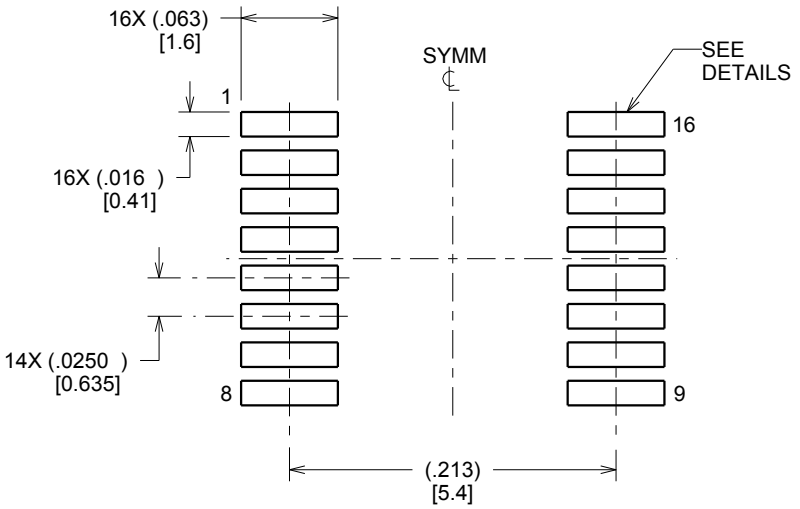
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

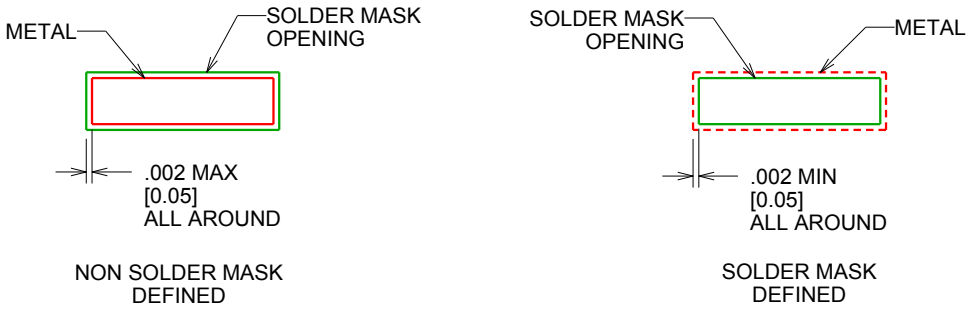


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

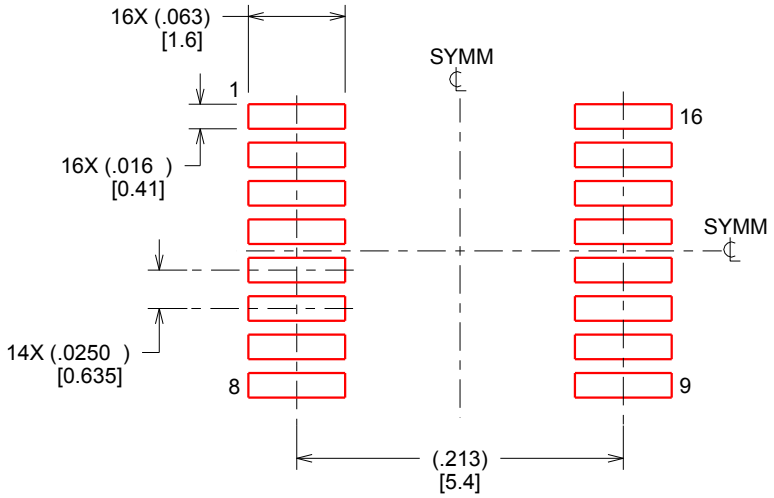
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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