

PCF8575 割り込み出力付き、リモート 16 ビット、I²C および SMBus I/O エクスパンダ

1 特長

- I²C からパラレルポートへのエクスパンダ
- オープンドレイン割り込み出力
- 低いスタンバイ消費電流: 10 μ A 以下
- ほとんどのマイクロコントローラと互換
- 400kHz の Fast I²C バス
- 3 本のハードウェア アドレスピンにより、8 つまでのデバイスをアドレス指定可能
- 大電流の駆動能力を持つラッチ付き出力により、LED を直接駆動
- V_{CC} への電流ソースにより出力をアクティブに High に駆動
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
 - 人体モデルで 2000V
 - マシンモデルで 200V
 - 荷電デバイスモデルで 1000V

2 アプリケーション

- テレコム シェルター: フィルタ ユニット
- サーバー
- ルーター (テレコム スイッチング機器)
- パーソナルコンピュータ
- パーソナルエレクトロニクス
- 産業用オートメーション
- 限定された GPIO を利用した製品

3 概要

この 2 線式双方向バス (I²C) 用 16 ビット I/O エクスパンダは、2.5V~5.5V の V_{CC} で動作するように設計されています。

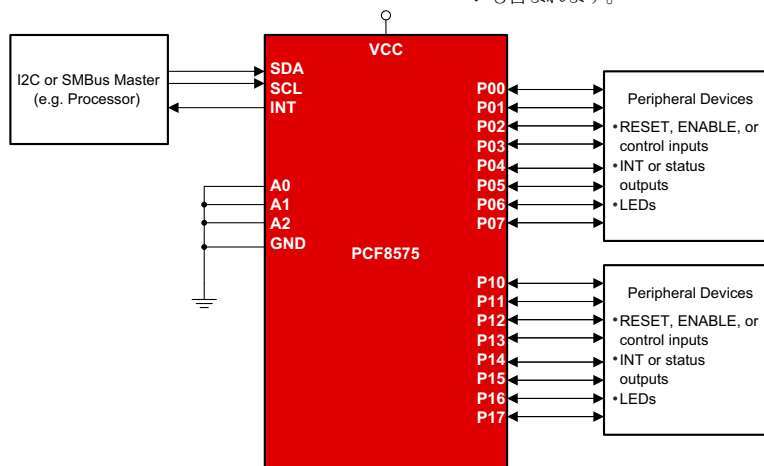
PCF8575 デバイスは、I²C インターフェイス [シリアル クロック (SCL)、シリアル データ (SDA)] により、ほとんどのマイクロコントローラ ファミリの汎用リモート I/O 拡張に使用できます。

このデバイスには 16 ビット、疑似双方向の入力/出力 (I/O) ポート (P07~P00、P17~P10) があり、大電流駆動能力を持つラッチ付き出力により LED を直接駆動できます。それぞれの疑似双方向 I/O は、データ方向制御信号を使用せずに、入力または出力として使用できます。電源投入時、I/O は HIGH になります。このモードでは、V_{CC} への電流源のみがアクティブになります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
PCF8575	SSOP (DB, 24)	8.2mm × 7.8mm
	SSOP (DBQ) (24)	8.65mm × 6mm
	TVSOP (DGV) (24)	5mm × 6.4mm
	SOIC (DW, 24)	15.5mm × 10.3mm
	TSSOP (PW, 24)	7.8mm × 6.4mm
	VQFN (RGV, 24)	4mm × 4mm

- (1) 利用可能なパッケージについては、[セクション 12](#) を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



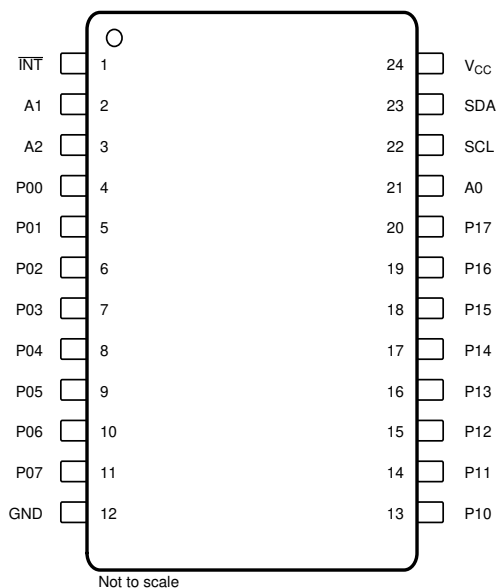
概略回路図



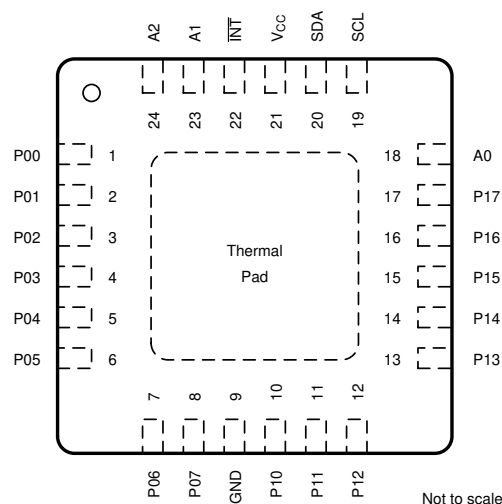
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4 Pin Configuration and Functions



4-1. DB, DBQ, DGV, DW, or PW Package SSOP, TVSOP, SOIC, TSSOP (Top View)



4-2. RGE Package VQFN (Top View)

PIN			TYPE	DESCRIPTION
NAME	DB, DBQ, DGV, DW, AND PW	RGE		
A0	21	18	I	Address input 0. Connect directly to V _{CC} or ground. Pull-up resistors are not needed.
A1	2	23	I	Address input 1. Connect directly to V _{CC} or ground. Pull-up resistors are not needed.
A2	3	24	I	Address input 2. Connect directly to V _{CC} or ground. Pull-up resistors are not needed.
INT	1	22	O	Interrupt output. Connect to V _{CC} through a pull-up resistor.
P00	4	1	I/O	P-port input/output. Push-pull design structure.
P01	5	2	I/O	P-port input/output. Push-pull design structure.
P02	6	3	I/O	P-port input/output. Push-pull design structure.
P03	7	4	I/O	P-port input/output. Push-pull design structure.
P04	8	5	I/O	P-port input/output. Push-pull design structure.
P05	9	6	I/O	P-port input/output. Push-pull design structure.
P06	10	7	I/O	P-port input/output. Push-pull design structure.
P07	11	8	I/O	P-port input/output. Push-pull design structure.
GND	12	9	—	Ground
P10	13	10	I/O	P-port input/output. Push-pull design structure.
P11	14	11	I/O	P-port input/output. Push-pull design structure.
P12	15	12	I/O	P-port input/output. Push-pull design structure.
P13	16	13	I/O	P-port input/output. Push-pull design structure.
P14	17	14	I/O	P-port input/output. Push-pull design structure.
P15	18	15	I/O	P-port input/output. Push-pull design structure.
P16	19	16	I/O	P-port input/output. Push-pull design structure.
P17	20	17	I/O	P-port input/output. Push-pull design structure.
SCL	22	19	I	Serial clock line. Connect to V _{CC} through a pull-up resistor
SDA	23	20	I/O	Serial data line. Connect to V _{CC} through a pull-up resistor.
V _{CC}	24	21	—	Supply voltage

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.5	6.5	V
V _I	Input voltage range ⁽²⁾	−0.5	V _{CC} + 0.5	V
V _O	Output voltage range ⁽²⁾	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		−20 mA
I _{OK}	Output clamp current	V _O < 0		−20 mA
I _{OK}	Input/output clamp current	V _O < 0 or V _O > V _{CC}		−20 mA
I _{OL}	Continuous output low current	V _O = 0 to V _{CC}		50 mA
I _{OH}	Continuous output high current	V _O = 0 to V _{CC}		−4 mA
	Continuous current through V _{CC} or GND			±100 mA
T _{stg}	Storage temperature range			150 °C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under セクション 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	1000

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.5	5.5	V
V _{IH}	High-level input voltage	0.7 × V _{CC}	V _{CC} + 0.5	V
V _{IL}	Low-level input voltage	−0.5	0.3 × V _{CC}	V
I _{OH}	P-port high-level output current		−1	mA
I _{OHT}	P-port transient pullup current		−10	mA
I _{OL}	P-port low-level output current		25	mA
T _A	Operating free-air temperature	−40	85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		PCF8575						UNIT
		DB	DBQ	DGV	DW	PW	RGE	
		24 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	87.8	61	86	75.6	99.7	53.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.9			47.9	42.5	50.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.8			50.1	66.1	31.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	14.3			21.1	2.7	3.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	56.2			49.7	65.5	31.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	-			-	-	14.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input diode clamp voltage	I _I = –18 mA	2.5 V to 5.5 V	–1.2			V
V _{POR}	Power-on reset voltage	V _I = V _{CC} or GND, I _O = 0	V _{POR}		1.2	1.8	V
I _{OH}	P port	V _O = GND	2.5 V to 5.5 V	–30		–300	μA
I _{OHT}	P-port transient pullup current	High during ACK, V _{OHT} = GND	2.5 V	–0.5	–1		mA
I _{OL}	SDA	V _{OL} = 0.4 V	2.5 V to 5.5 V	3			mA
	P port	V _{OL} = 0.4 V		5	15		
		V _{OL} = 1 V		10	25		
	INT	V _{OL} = 0.4 V		1.6			
I _I	SCL, SDA	V _I = V _{CC} or GND	2.5 V to 5.5 V			±5	μA
	A0, A1, A2					±1	
I _{IHL}	P port	–250mV < V _I < GND	2.5 V to 5.5 V			±400	μA
I _{CC}	Operating mode	V _I = V _{CC} or GND, I _O = 0, f _{scl} = 400 kHz	5.5 V		100	200	μA
			3.6 V		30	75	
			2.7 V		20	50	
	Standby mode	V _I = V _{CC} or GND, I _O = 0, f _{scl} = 0 kHz	5.5 V		2.5	10	
			3.6 V		2.5	10	
			2.7 V		2.5	10	
ΔI _{CC}	Supply current increase	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.5 V to 5.5 V			200	μA
C _I	SCL	V _I = V _{CC} or GND	2.5 V to 5.5 V		3	7	pF
C _{IO}	SDA	V _{IO} = V _{CC} or GND	2.5 V to 5.5 V		3	7	pF
	P port				4	10	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.

5.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

			MIN	MAX	UNIT
f _{scl}	I ² C clock frequency			400	kHz
t _{sch}	I ² C clock high time		0.6		μs
t _{scl}	I ² C clock low time		1.3		μs
t _{sp}	I ² C spike time			50	ns
t _{sds}	I ² C serial data setup time		100		ns
t _{sdh}	I ² C serial data hold time		0		ns
t _{icr}	I ² C input rise time		20 + 0.1C _b ⁽¹⁾	300	ns
t _{icf}	I ² C input fall time		20 + 0.1C _b ⁽¹⁾	300	ns
t _{ocf}	I ² C output fall time	10-pF to 400-pF bus		300	ns
t _{buf}	I ² C bus free time between Stop and Start		1.3		μs
t _{sts}	I ² C start or repeated Start condition setup		0.6		μs
t _{sth}	I ² C start or repeated Start condition hold		0.6		μs
t _{sps}	I ² C Stop condition setup		0.6		μs
t _{vd}	Valid-data time	SCL low to SDA output valid		1.2	μs
C _b	I ² C bus capacitive load			400	pF

(1) C_b = total bus capacitance of one bus line in pF

5.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 6-2 and Figure 6-3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	INT		4	μ s
t_{ir}	Interrupt reset delay time	SCL	INT		4	μ s
t_{pv}	Output data valid	SCL	P port		4	μ s
t_{su}	Input data setup time	P port	SCL	0		μ s
t_h	Input data hold time	P port	SCL	4		μ s

6 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

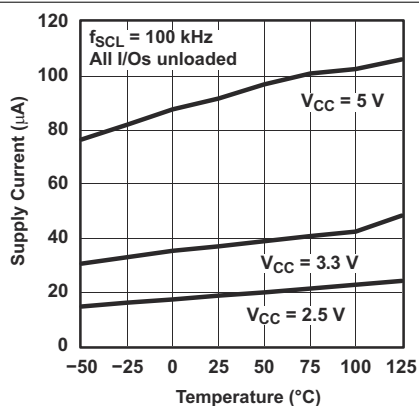


図 6-1. Supply Current vs Temperature

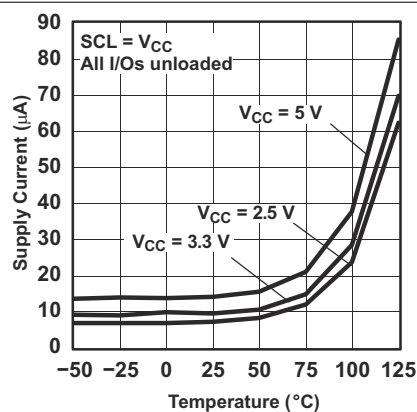


図 6-2. Standby Supply Current vs Temperature

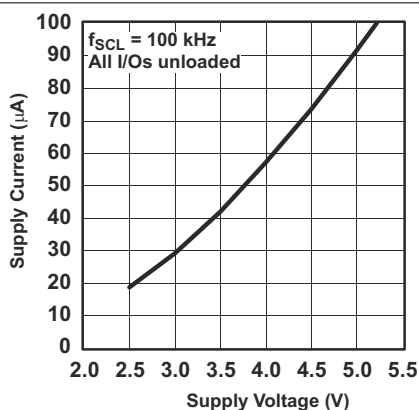


図 6-3. Supply Current vs Supply Voltage

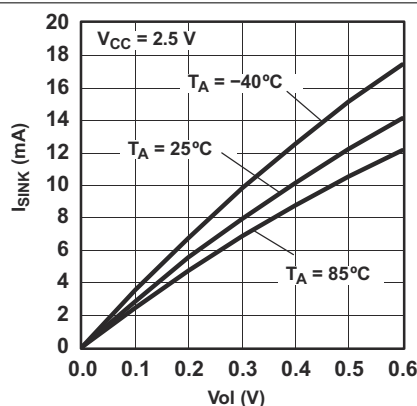


図 6-4. I/O Sink Current vs Output Low Voltage

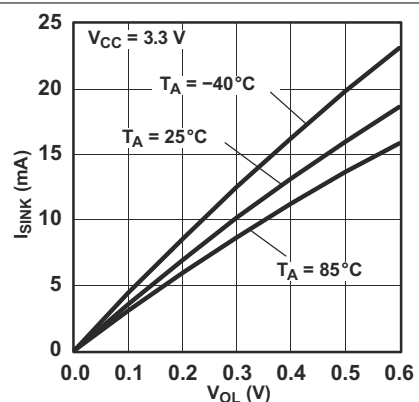


図 6-5. I/O Sink Current vs Output Low Voltage

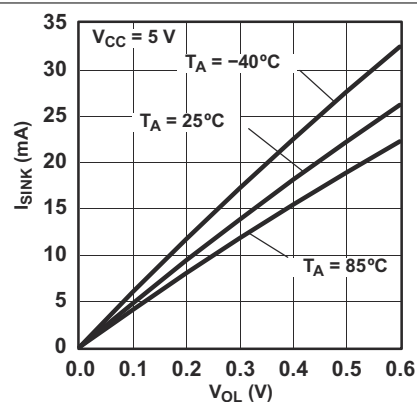


図 6-6. I/O Sink Current vs Output Low Voltage

6 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

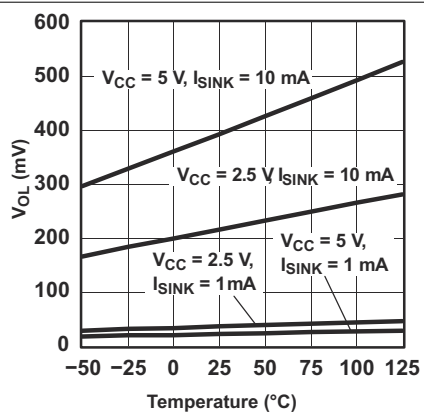


Figure 6-7. I/O Output Low Voltage vs Temperature

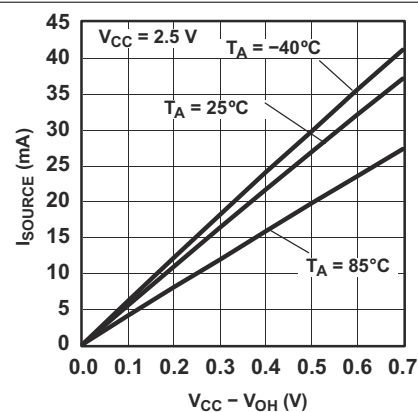


Figure 6-8. I/O Source Current vs Output High Voltage

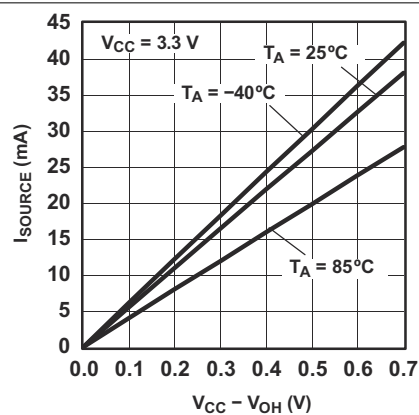


Figure 6-9. I/O Source Current vs Output High Voltage

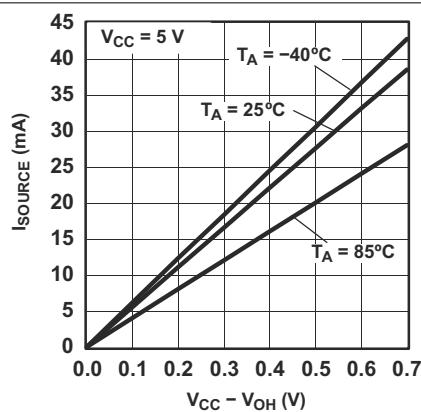


Figure 6-10. I/O Source Current vs Output High Voltage

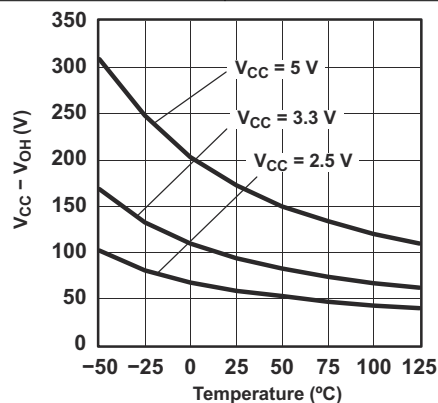
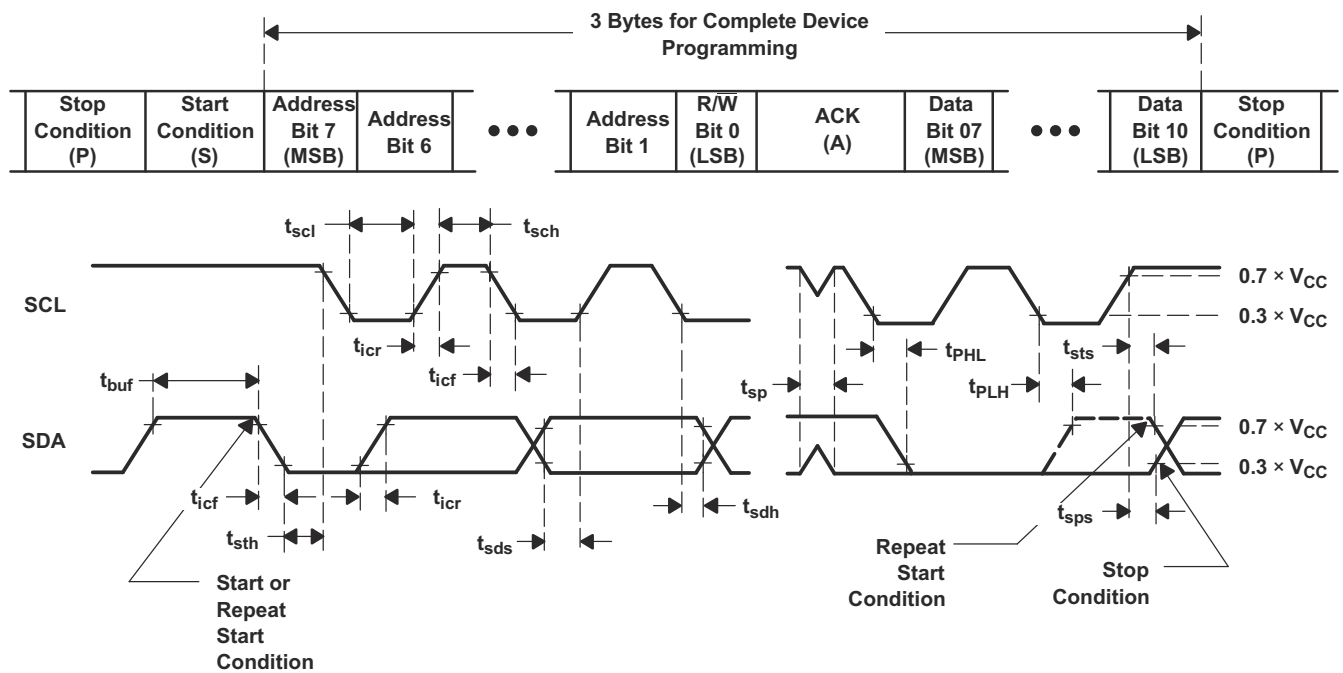
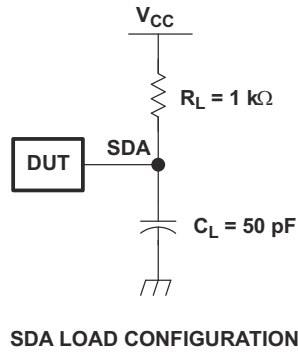


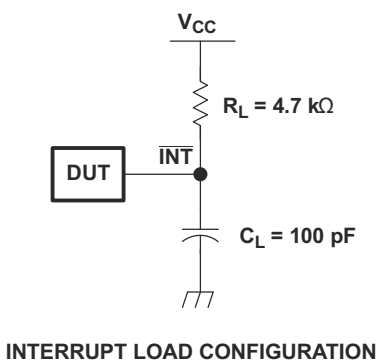
Figure 6-11. I/O High Voltage vs Temperature

7 Parameter Measurement Information



BYTE	DESCRIPTION
1	I ² C address
2, 3	P-port data

図 7-1. I²C Interface Load Circuit and Voltage Waveforms



INTERRUPT LOAD CONFIGURATION

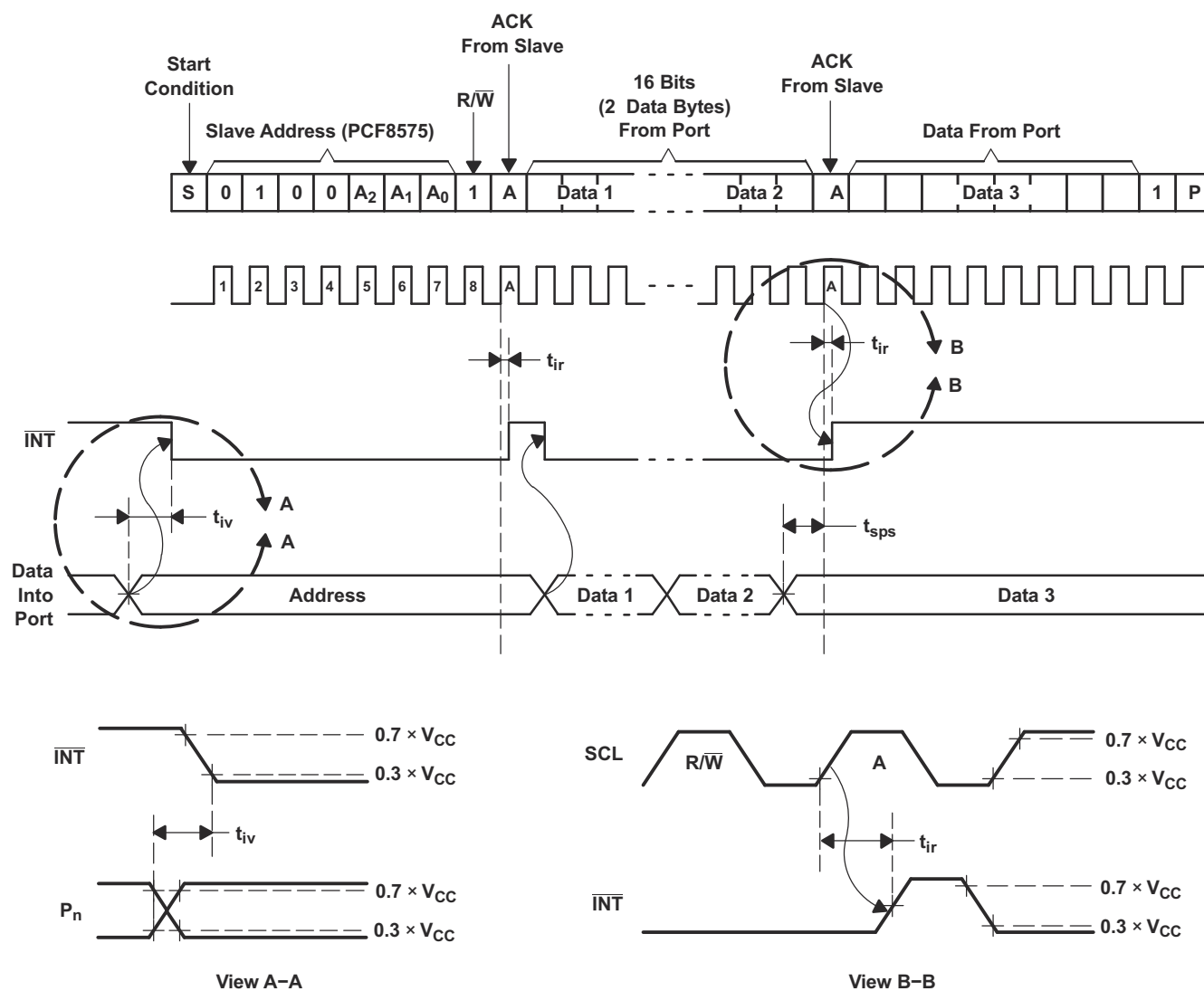


図 7-2. Interrupt Load Circuit and Voltage Waveforms

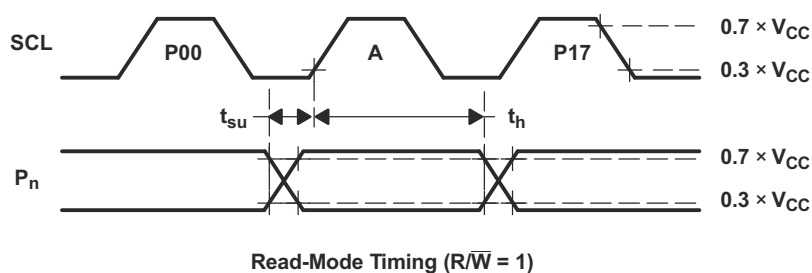
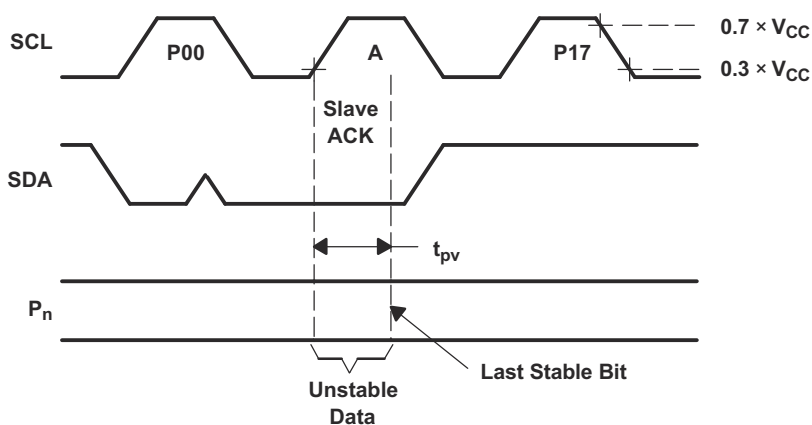
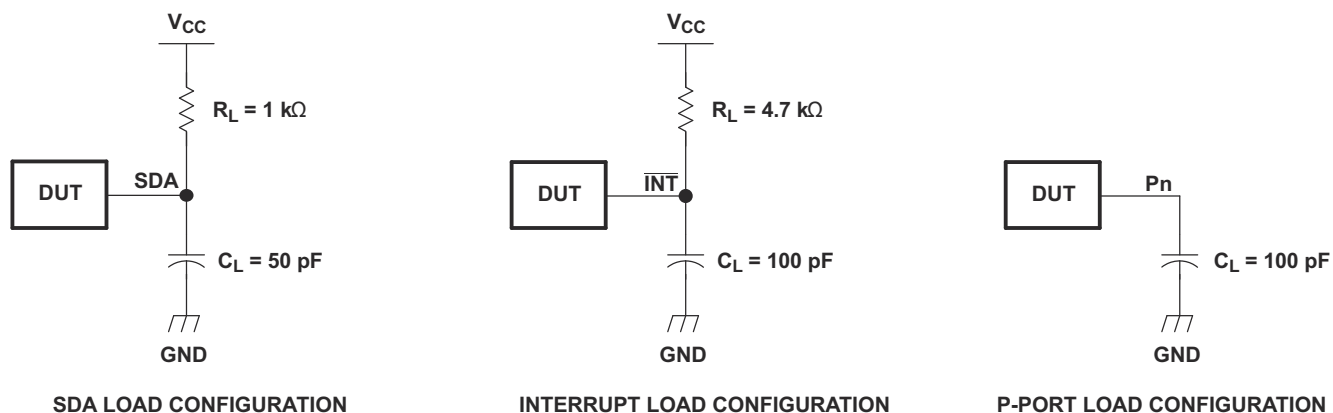


図 7-3. P-Port Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The PCF8575 provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface serial clock (SCL) and serial data (SDA).

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07–P00, P17–P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source (I_{OH}) to V_{CC} is active. An additional strong pullup to V_{CC} (I_{OHT}) allows fast-rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs. After power on, as all the I/Os are set high, all of them can be used as inputs. Any change in setting of the I/Os as either input or outputs can be done with the write mode. If a high is applied externally to an I/O that has been written earlier to low, a large current (I_{OL}) will flow to GND.

The PCF8575 provides an open-drain interrupt ($\overline{INT}$) output, which can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv} , the signal $\overline{INT}$ is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting, or data is read from or written to the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal or in the write mode at the ACK bit after the falling edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short), due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit. This device does not have internal configuration or status registers. Instead, read or write to the device I/Os directly after sending the device address (see [Figure 8-6](#) and [Figure 8-7](#)).

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports, without having to communicate via the I²C bus. Thus, the PCF8575 can remain a simple target device.

Every data transmission to or from the PCF8575 must consist of an even number of bytes. The first data byte in every pair refers to port 0 (P07–P00), and the second data byte in every pair refers to port 1 (P17–P10). To write to the ports (output mode), the controller first addresses the target device, setting the last bit of the byte containing the target address to logic 0. The PCF8575 acknowledges, and the controller sends the first data byte for P07–P00. After the first data byte is acknowledged by the PCF8575, the second data byte (P17–P10) is sent by the controller. Once again, the PCF8575 acknowledges the receipt of the data, after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten. When the PCF8575 receives the pairs of data bytes, the first byte is referred to as P07–P00 and the second byte as P17–P10. The third byte is referred to as P07–P00, the fourth byte as P17–P10, and so on.

Before reading from the PCF8575, all ports desired as input should be set to logic 1. To read from the ports (input mode), the controller first addresses the target device, setting the last bit of the byte containing the target address to logic 1. The data bytes that follow on the SDA are the values on the ports. If the data on the input port changes faster than the controller can read, this data may be lost.

When power is applied to V_{CC} , an internal power-on reset holds the PCF8575 in a reset state until V_{CC} has reached V_{POR} . At that time, the reset condition is released, and the device I²C-bus state machine initializes the bus to its default state.

The hardware pins (A0, A1, and A2) are used to program and vary the fixed I²C address and allow up to eight devices to share the same I²C bus or SMBus. The fixed I²C address of the PCF8575 is the same as the PCF8575C, PCF8574, PCA9535, and PCA9555, allowing up to eight of these devices, in any combination, to share the same I²C bus or SMBus.

8.2 Functional Block Diagram

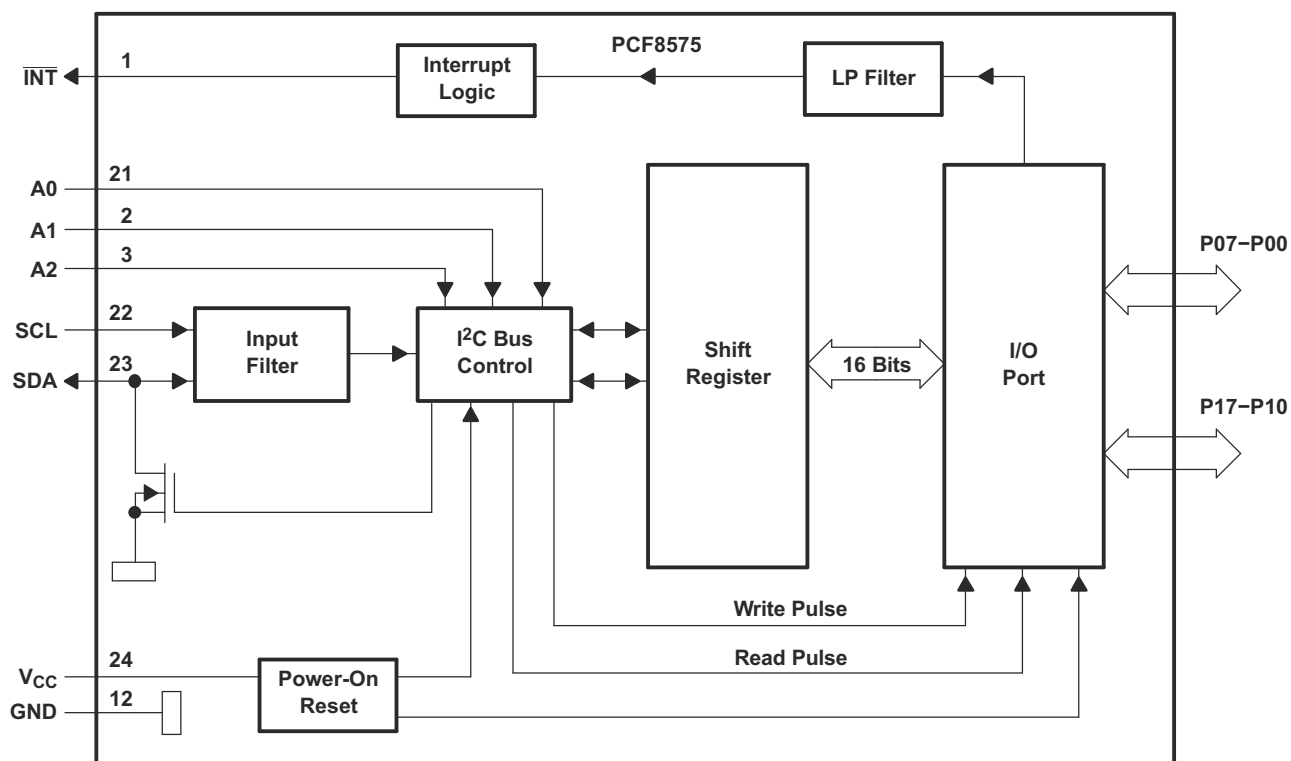


図 8-1. Logic Diagram (Positive Logic)

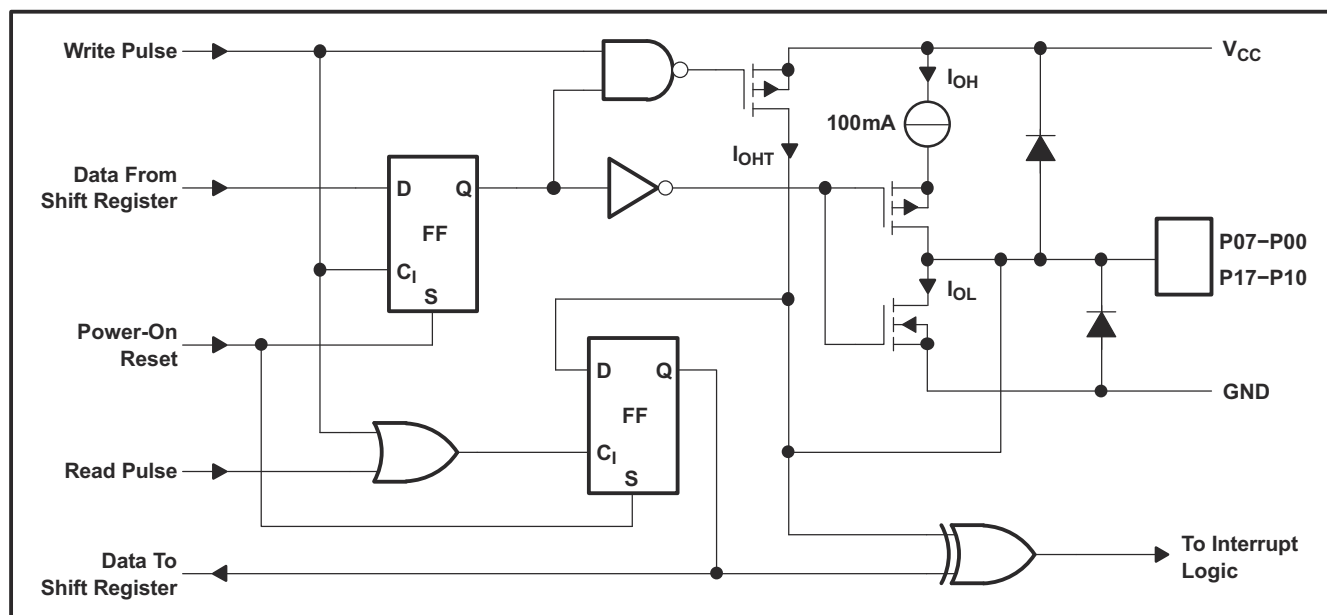


図 8-2. Simplified Schematic Diagram of Each P-Port Input or Output

8.3 Feature Description

8.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a controller sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see [Figure 8-3](#)). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/ $\overline{W}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A2–A0) of the target device must not be changed between the Start and Stop conditions.

The data byte follows the address ACK. If the R/ $\overline{W}$ bit is high, the data from this device are the values read from the P port. If the R/ $\overline{W}$ bit is low, the data are from the controller, to be output to the P port. The data byte is followed by an ACK sent from this device. If other data bytes are sent from the controller, following the ACK, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (t_{pv}) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see [Figure 8-4](#)).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the controller (see [Figure 8-3](#)).

The number of data bytes transferred between the Start and Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A target receiver that is addressed must generate an ACK after the reception of each byte. Also, a controller must generate an ACK after the reception of each byte that has been clocked out of the target transmitter. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 8-5](#)). Setup and hold times must be taken into account.

A controller receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the target. This is done by the controller receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

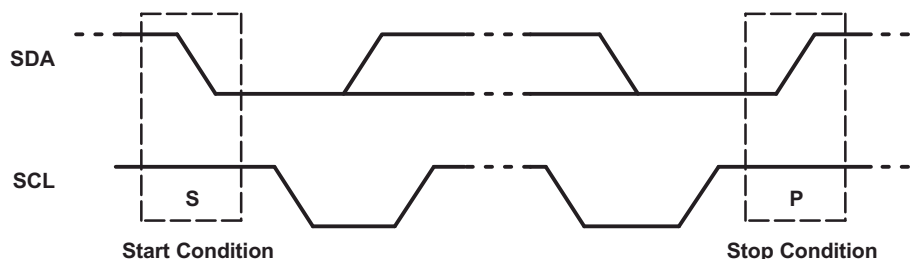


Figure 8-3. Definition of Start and Stop Conditions

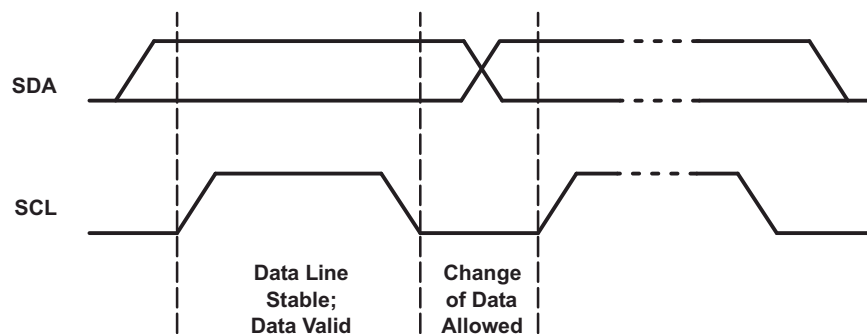


図 8-4. Bit Transfer

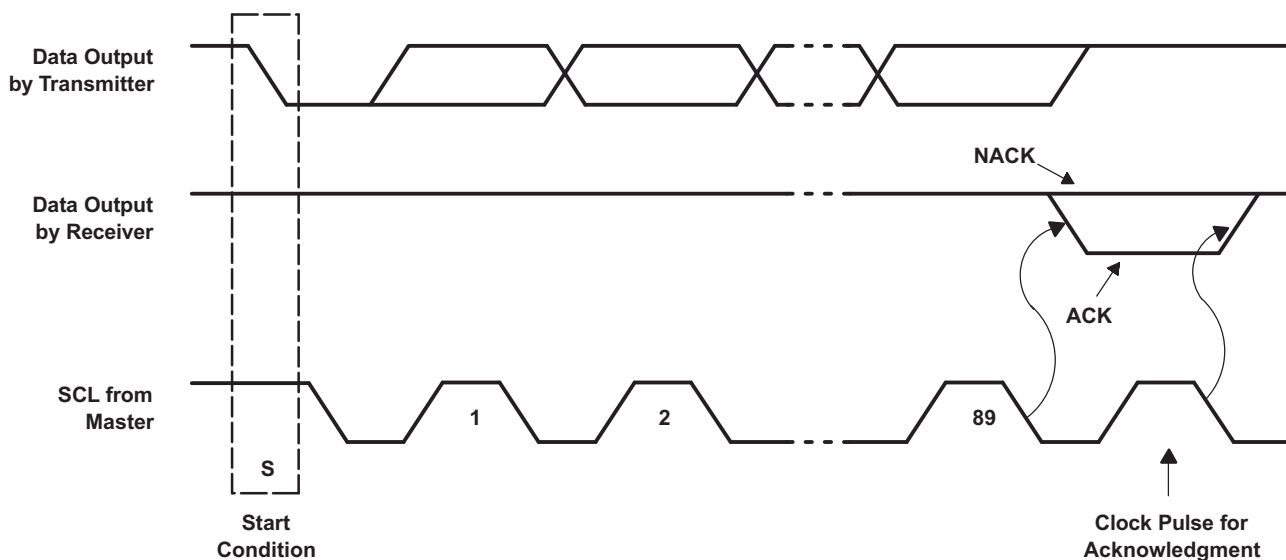


図 8-5. Acknowledgment on I²C Bus

8.3.2 Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I ² C target address	L	H	L	L	A2	A1	A0	R/ $\bar{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

8.3.3 Address Reference

INPUTS			I ² C BUS TARGET 8-BIT READ ADDRESS	I ² C BUS TARGET 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	65 (decimal), 41 (hexadecimal)	64 (decimal), 40 (hexadecimal)
L	L	H	67 (decimal), 43 (hexadecimal)	66 (decimal), 42 (hexadecimal)
L	H	L	69 (decimal), 45 (hexadecimal)	68 (decimal), 44 (hexadecimal)
L	H	H	71 (decimal), 47 (hexadecimal)	70 (decimal), 46 (hexadecimal)
H	L	L	73 (decimal), 49 (hexadecimal)	72 (decimal), 48 (hexadecimal)
H	L	H	75 (decimal), 4B (hexadecimal)	74 (decimal), 4A (hexadecimal)
H	H	L	77 (decimal), 4D (hexadecimal)	76 (decimal), 4C (hexadecimal)
H	H	H	79 (decimal), 4F (hexadecimal)	78 (decimal), 4E (hexadecimal)

8.4 Device Functional Modes

図 8-6 and 図 8-7 show the address and timing diagrams for the write and read modes, respectively.

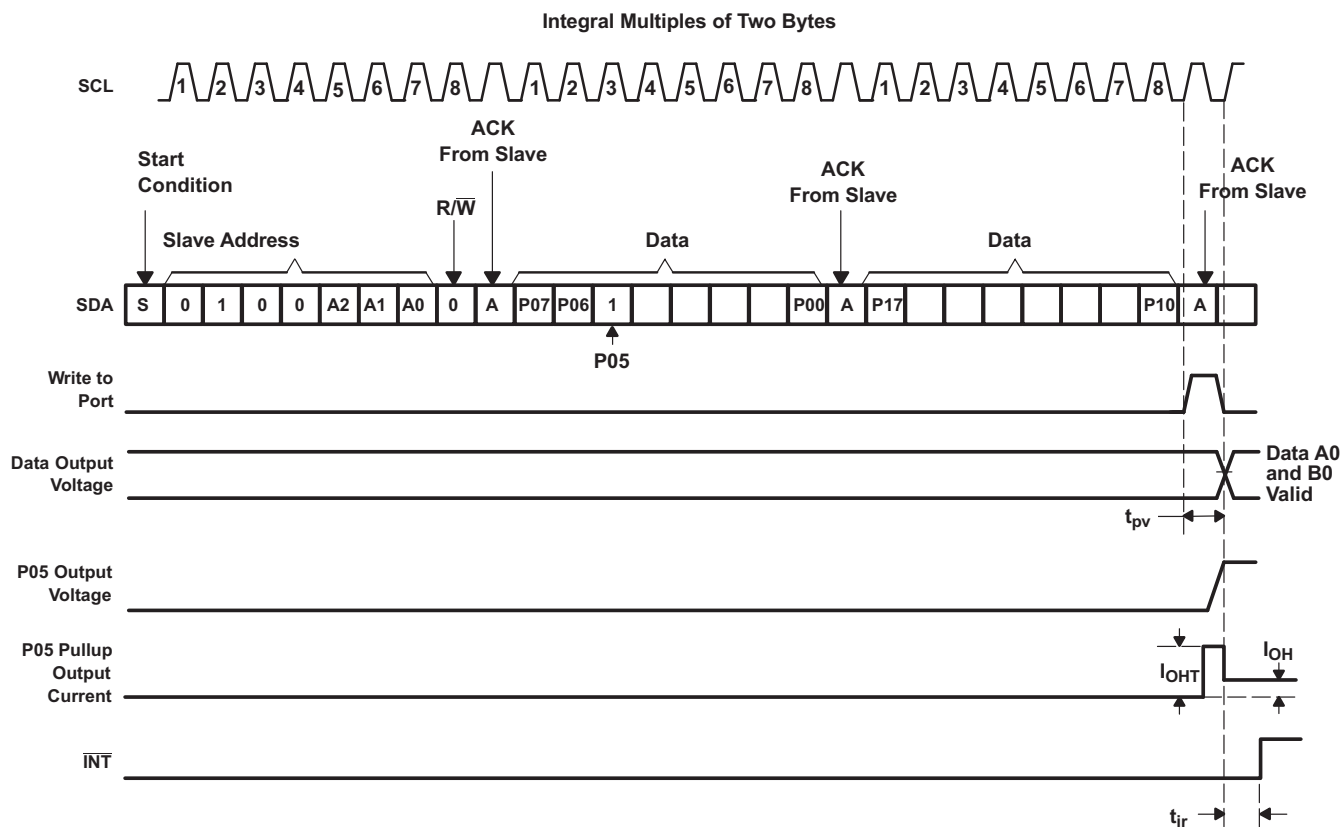
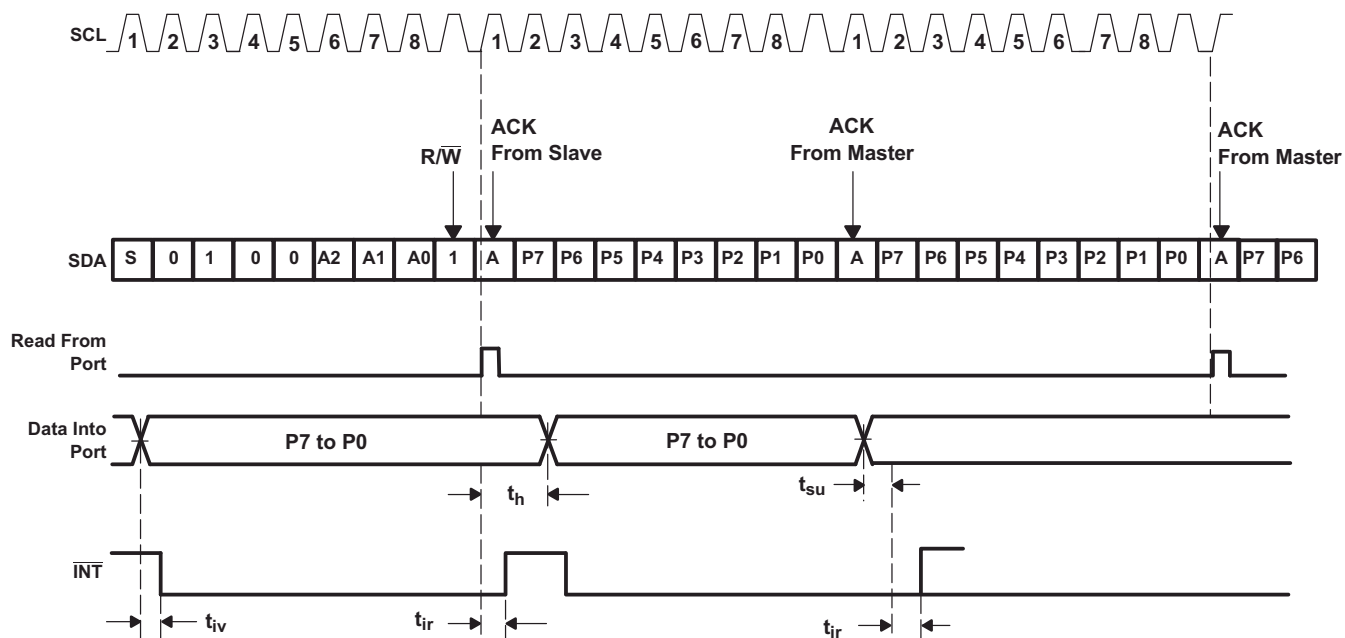


図 8-6. Write Mode (Output)



8-7. Read Mode (Input)

9 Application and Implementation

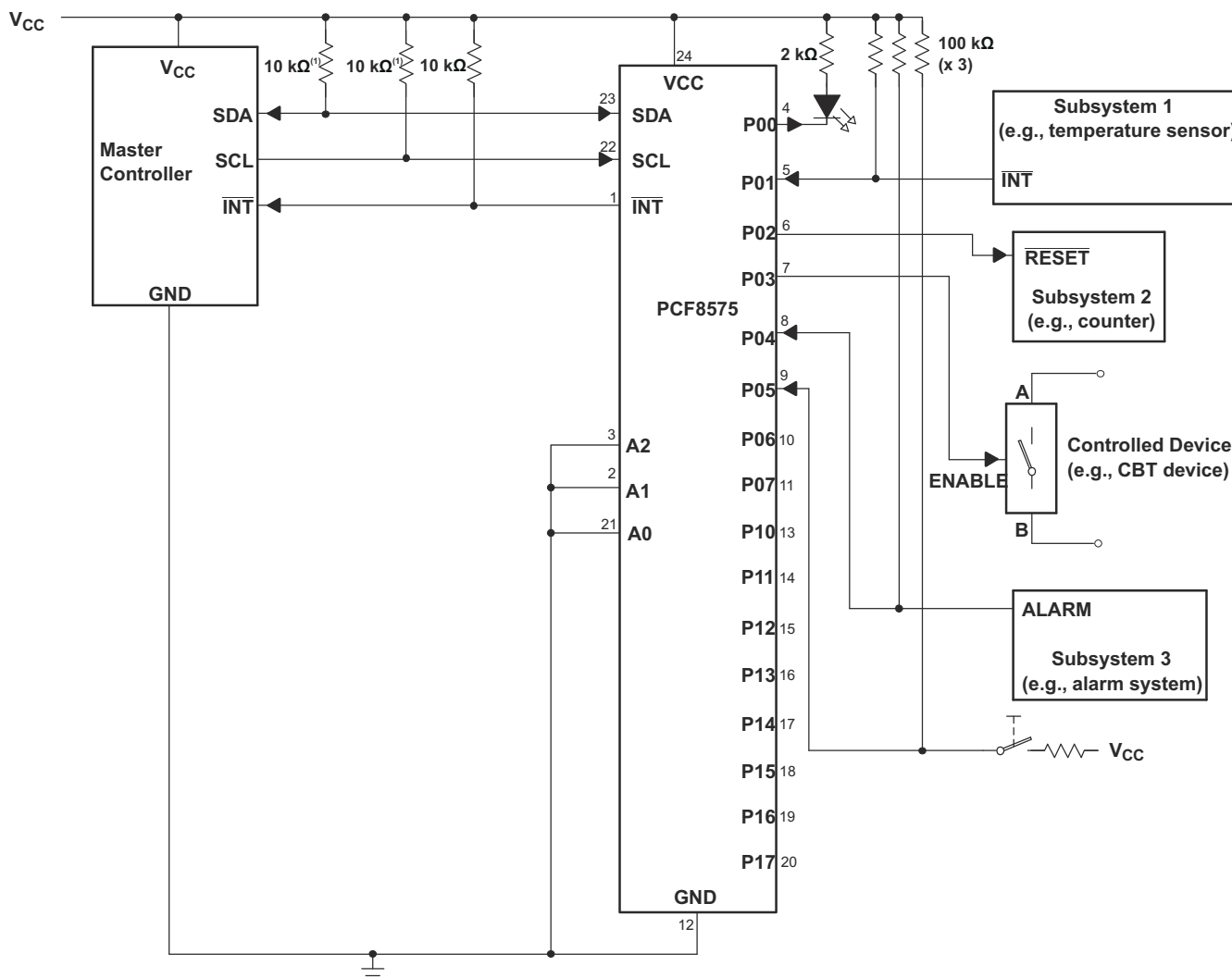
注

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9.1 Application Information

図 9-1 shows an application in which PCF8575 can be used.

9.2 Typical Application



- The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that could be powered on while VCC is powered off, then the supply current, ICC, will increase as a result.
- Device address is configured as 0100000 for this example.
- P0, P2, and P3 are configured as outputs.
- P1, P4, and P5 are configured as inputs.
- P6 and P7 are not used and must be configured as outputs.

図 9-1. Application Schematic

9.2.1 Design Requirements

9.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in [Figure 9-1](#). For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC} . The LED is a diode, with threshold voltage V_T , and when a P-port is configured as an input the LED will be off but V_I is a V_T drop below V_{CC} .

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. [Figure 9-2](#) shows a high-value resistor in parallel with the LED. [Figure 9-3](#) shows V_{CC} less than the LED supply voltage by at least V_T . Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

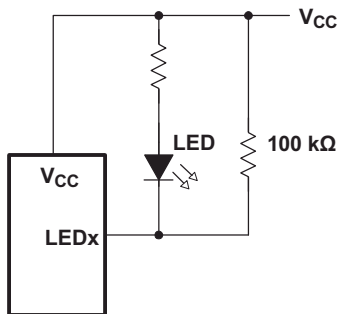


Figure 9-2. High-Value Resistor in Parallel With LED

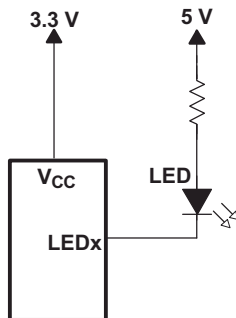


Figure 9-3. Device Supplied by a Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_p , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I²C bus. The minimum pull-up resistance is a function of V_{CC} , $V_{OL(max)}$, and I_{OL} :

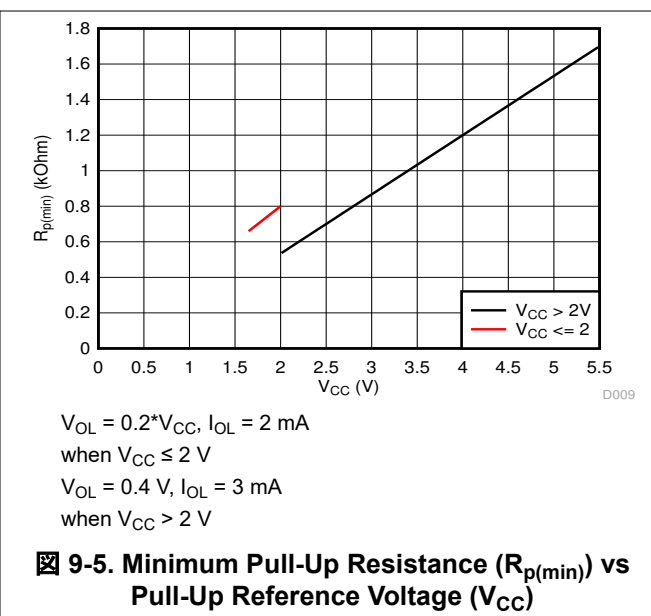
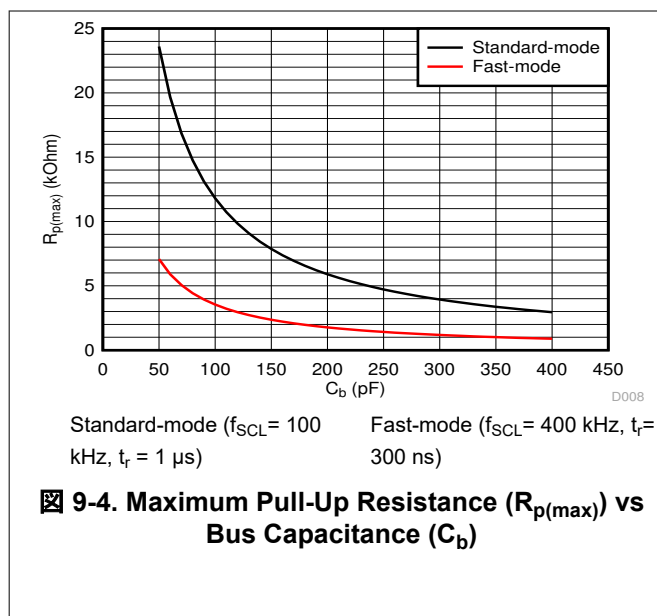
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, $f_{SCL} = 400$ kHz) and bus capacitance, C_b :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I²C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8575, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional targets on the bus.

9.2.3 Application Curves

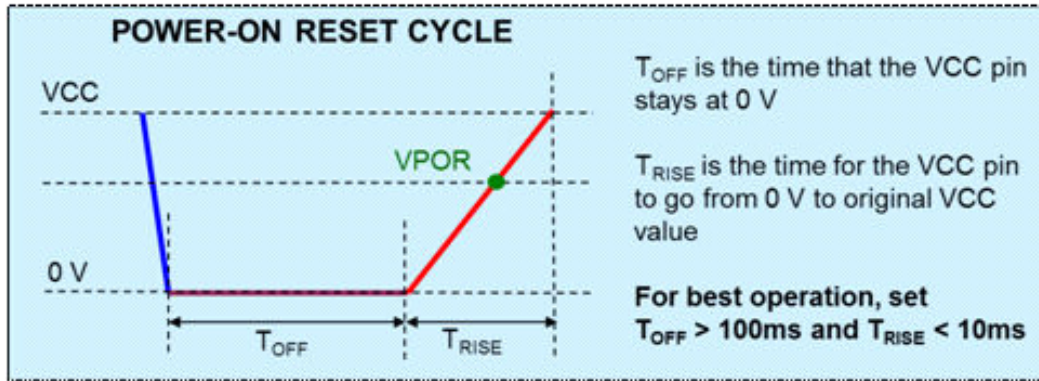


9.3 Power Supply Recommendations

The operating power-supply voltage range of the PCF8575 is 2.5 V to 5.5 V applied at the VCC pin. When the PCF8575 is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I²C bus logic is initialized properly.

9.3.1 Power-On Reset

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.



9.3.2 System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

9.4 Layout

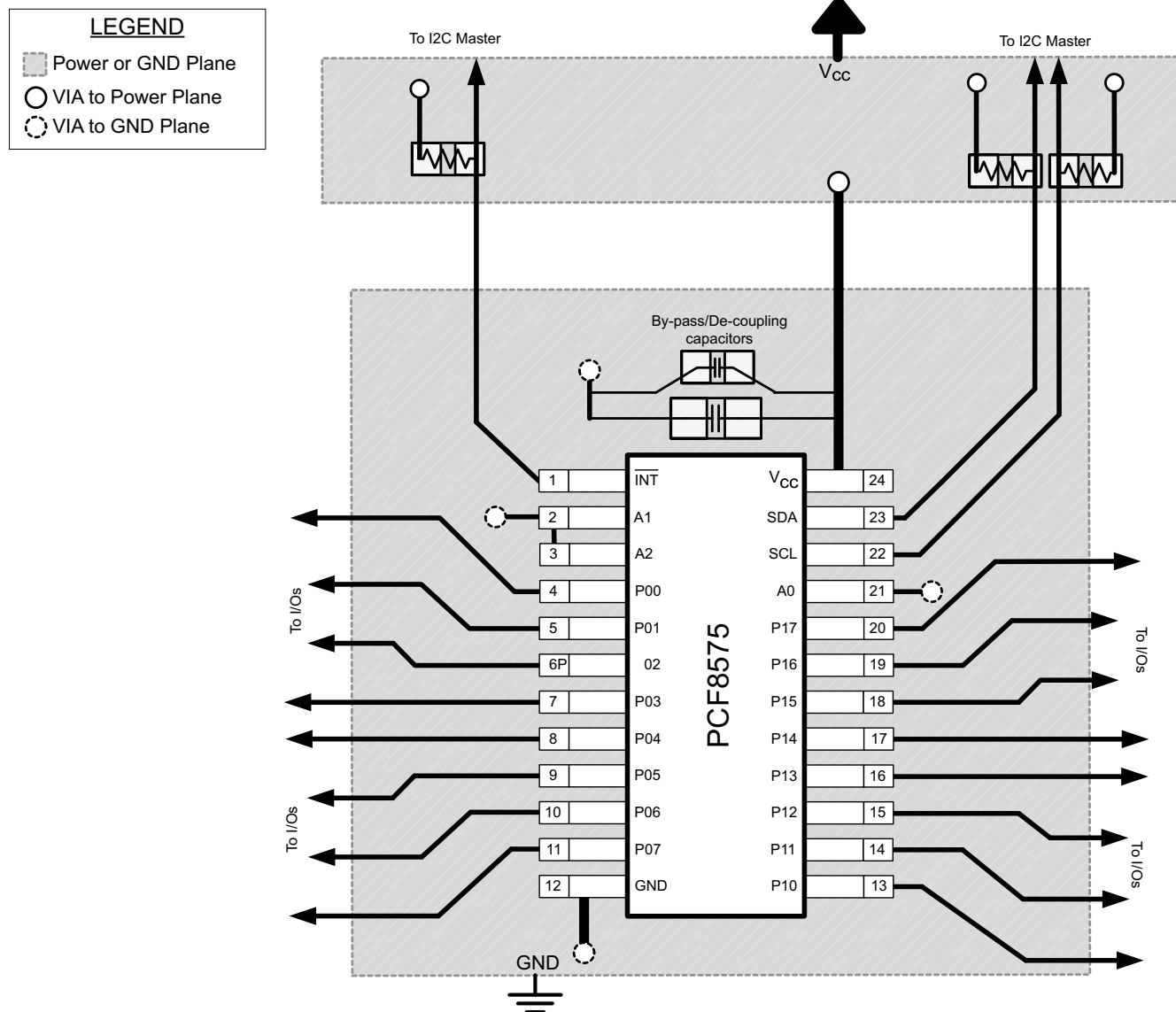
9.4.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCF8575 device, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8575 as possible. These best practices are shown in [Figure 9-6](#).

For the layout example provided in [Figure 9-6](#), it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in [Figure 9-6](#).

9.4.2 Layout Example



9-6. Layout Example for PCF8575

10 Device and Documentation Support

10.1 Device Support

10.2 Documentation Support

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (February 2020) to Revision I (August 2024)	Page
• I ² C に言及している場合、すべての旧式の用語をコントローラおよびターゲットに更新.....	1
• 「製品情報」表を「パッケージ情報」表に更新.....	1
• Updated Thermal Information.....	4
• Removed footnote #2 from Electrical Characteristics.....	5
• Updated I _{IHL} test condition.....	5

Changes from Revision G (August 2018) to Revision H (February 2020)	Page
• Updated  8-6	16

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCF8575DBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCF8575
PCF8575DBQR.A	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCF8575
PCF8575DBR	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575
PCF8575DBR.A	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575
PCF8575DGVR	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575
PCF8575DGVR.A	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575
PCF8575DW	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	-40 to 85	PCF8575
PCF8575DWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575
PCF8575DWR.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575
PCF8575PW	Obsolete	Production	TSSOP (PW) 24	-	-	Call TI	Call TI	-40 to 85	PF575
PCF8575PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575
PCF8575PWR.A	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575
PCF8575PWRE4	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575
PCF8575RGER	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF575 Q1
PCF8575RGER.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF575 Q1
PCF8575RGERG4	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF575 Q1
PCF8575RGERG4.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF575 Q1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCF8575DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCF8575DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCF8575DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCF8575DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCF8575PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCF8575RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCF8575RGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

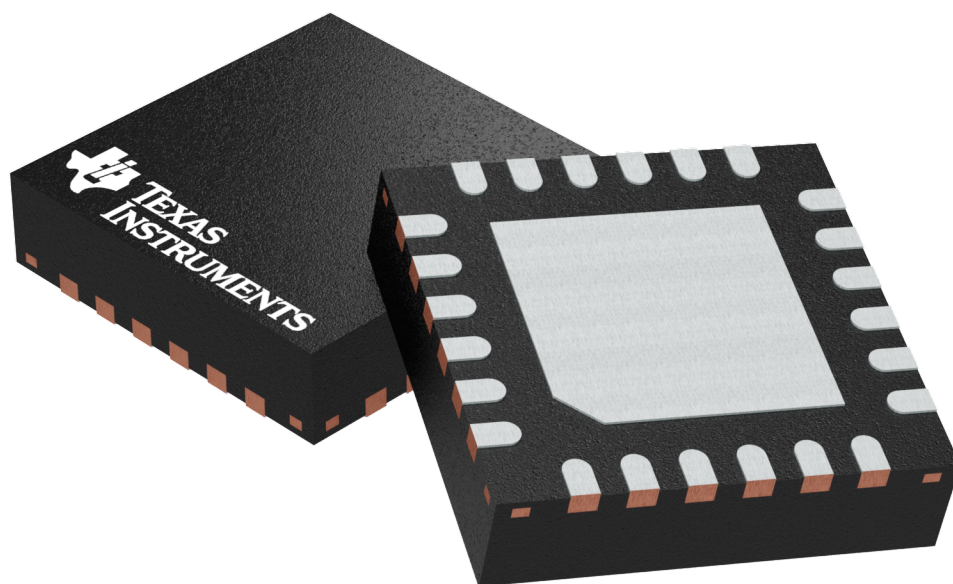
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCF8575DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
PCF8575DBR	SSOP	DB	24	2000	353.0	353.0	32.0
PCF8575DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
PCF8575DWR	SOIC	DW	24	2000	350.0	350.0	43.0
PCF8575PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
PCF8575RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
PCF8575RGERG4	VQFN	RGE	24	3000	367.0	367.0	35.0

RGE 24

GENERIC PACKAGE VIEW

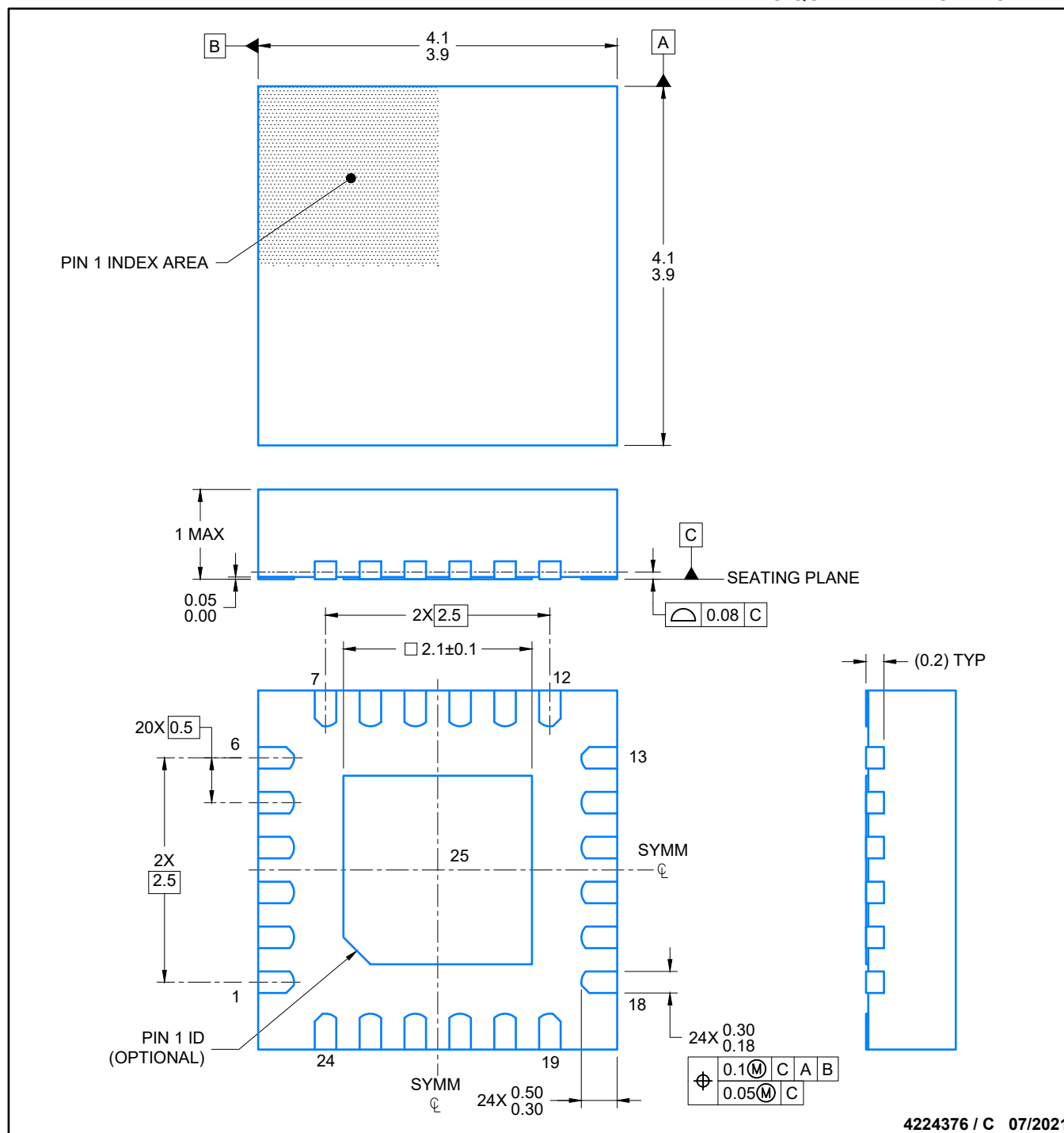
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



4224376 / C 07/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

VQFN - 1 mm max height

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

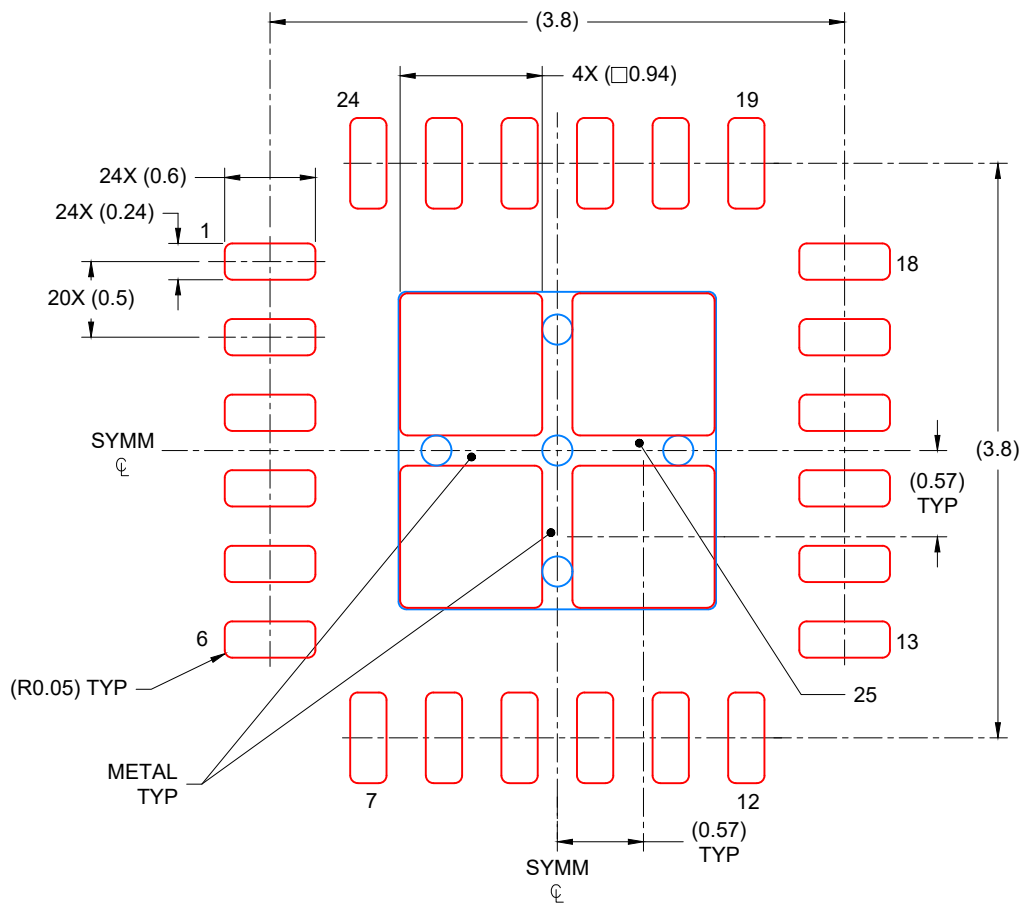
SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 80% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224376 / C 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

VQFN - 1 mm max height

Figure 1: Top view of the PCB layout showing dimensions and component locations. The layout is symmetrical about a central vertical axis (SYM) and a central horizontal axis (CL). Dimensions include 2X (3.8), 2X (3.45), 2X (2.5), SQ (2.1), 24X (0.6), 24X (0.24), 20X (0.5), 2X (0.8), 2X (2.5), 2X (3.45), 2X (3.8), 4X SQ (0.25) TYP, 2X (0.8), and 6X (0.2) VIA TYP. Component locations are marked with A1, A2, A3, A4, 1, 6, 7, 12, 13, 18, 19, 24, 25, and 26. A central square area is highlighted with a dashed line.

0.07 MAX ALL AROUND

METAL

EXPOSED METAL

SOLDER MASK OPENING

NON SOLDER MASK DEFINED (PREFERRED)

0.07 MIN ALL AROUND

METAL UNDER SOLDER MASK

EXPOSED METAL

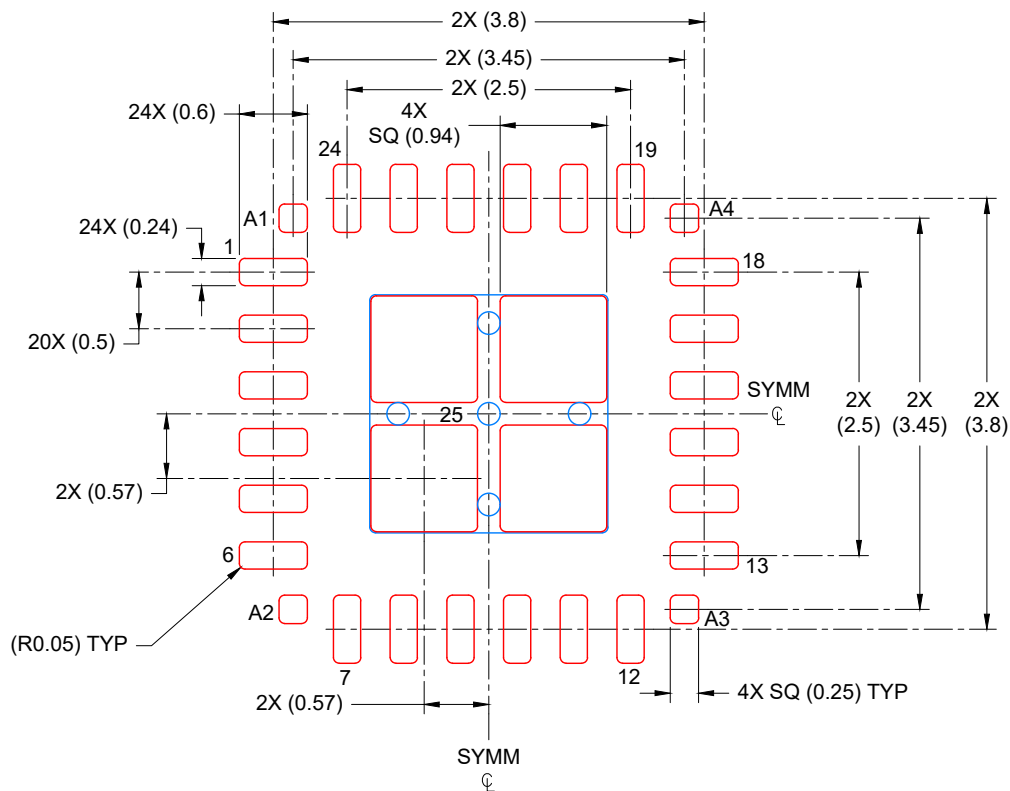
SOLDER MASK OPENING

SOLDER MASK DEFINED

SOLDER MASK DETAILS



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SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 80% PRINTED COVERAGE BY AREA
 SCALE: 15X

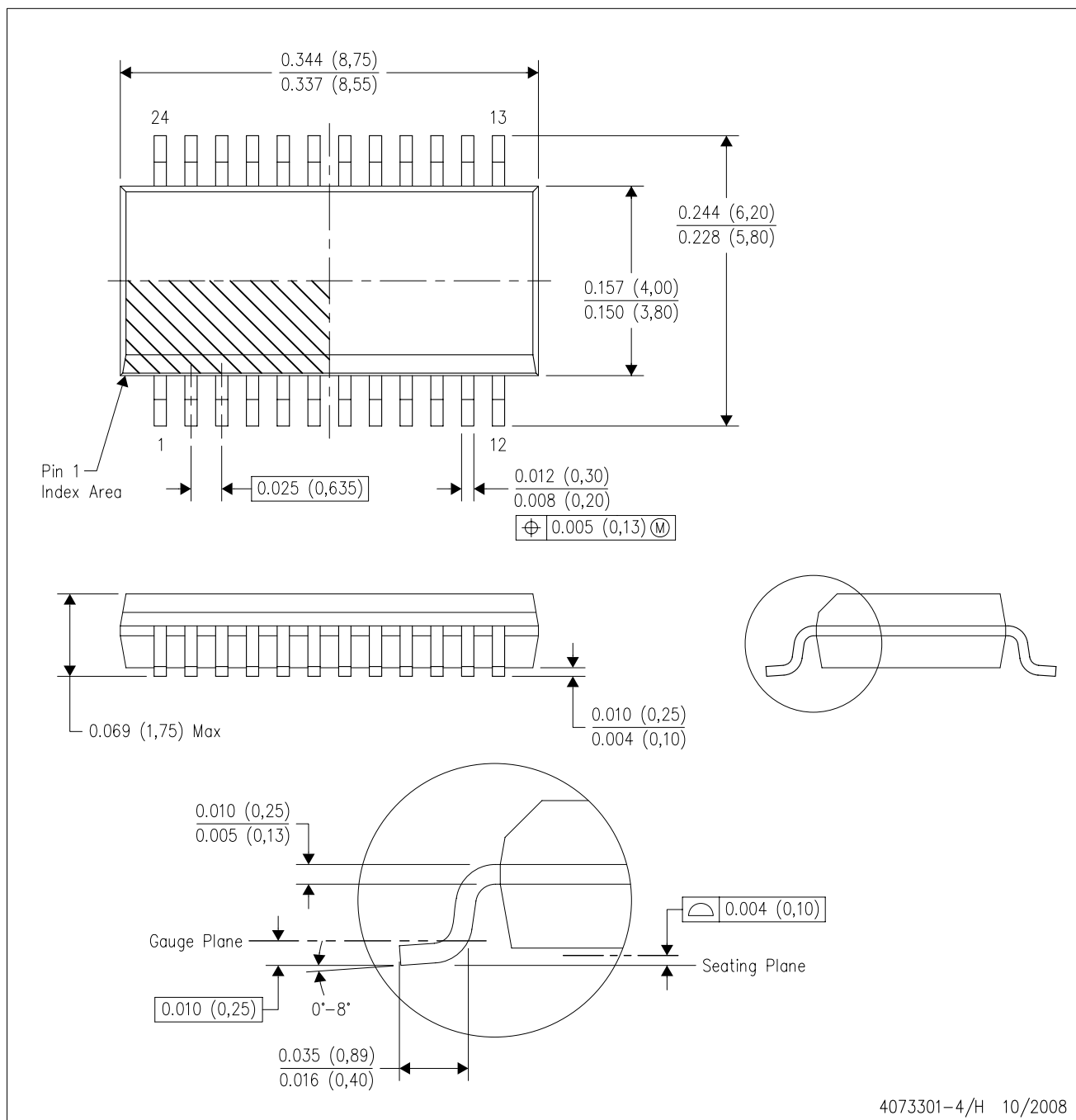
4225246/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



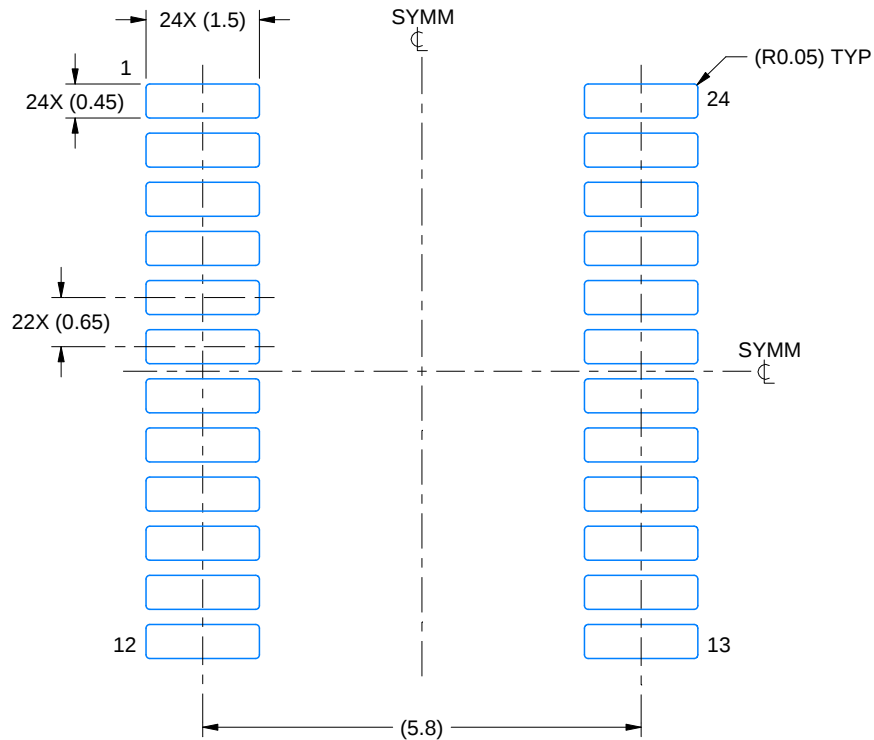
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

EXAMPLE BOARD LAYOUT

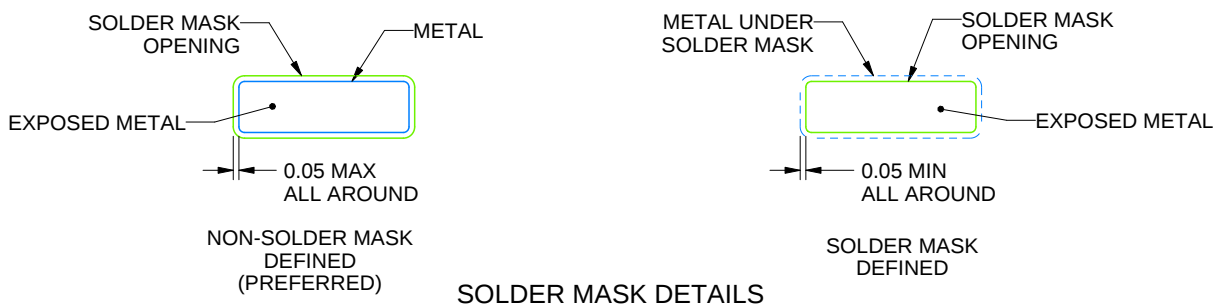
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

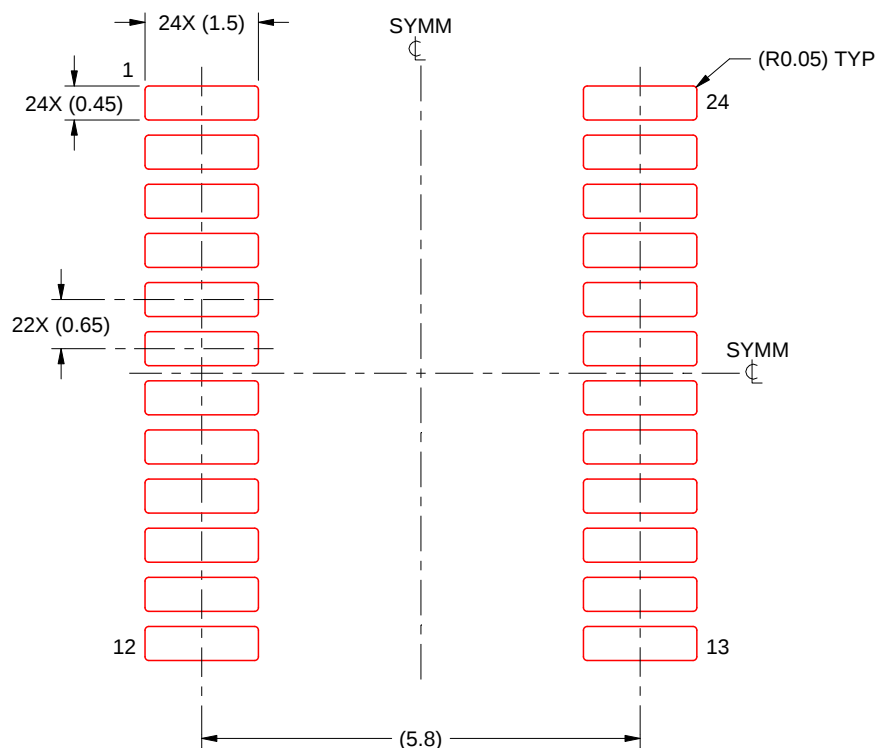
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

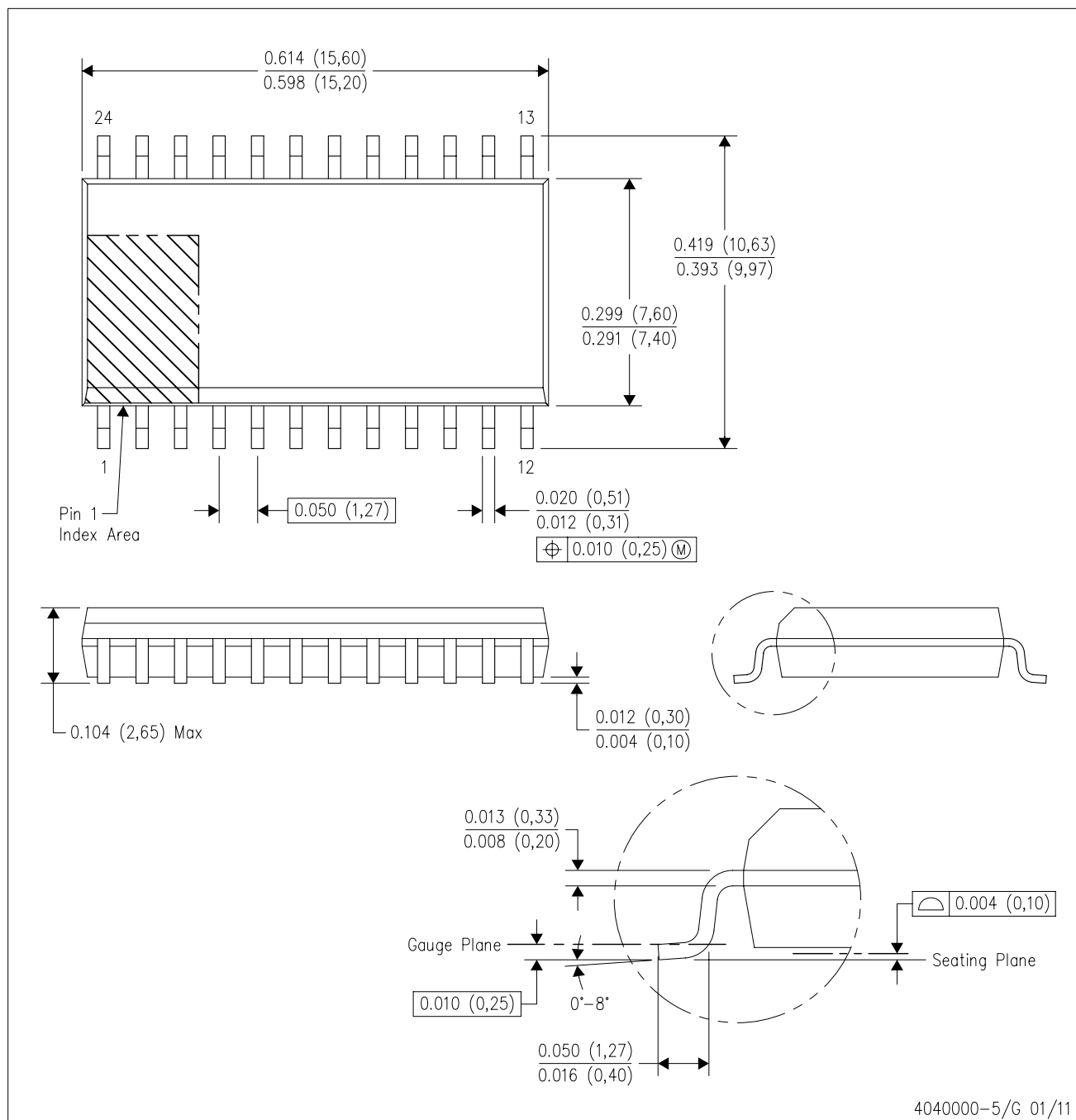
4220208/A 02/2017

NOTES: (continued)

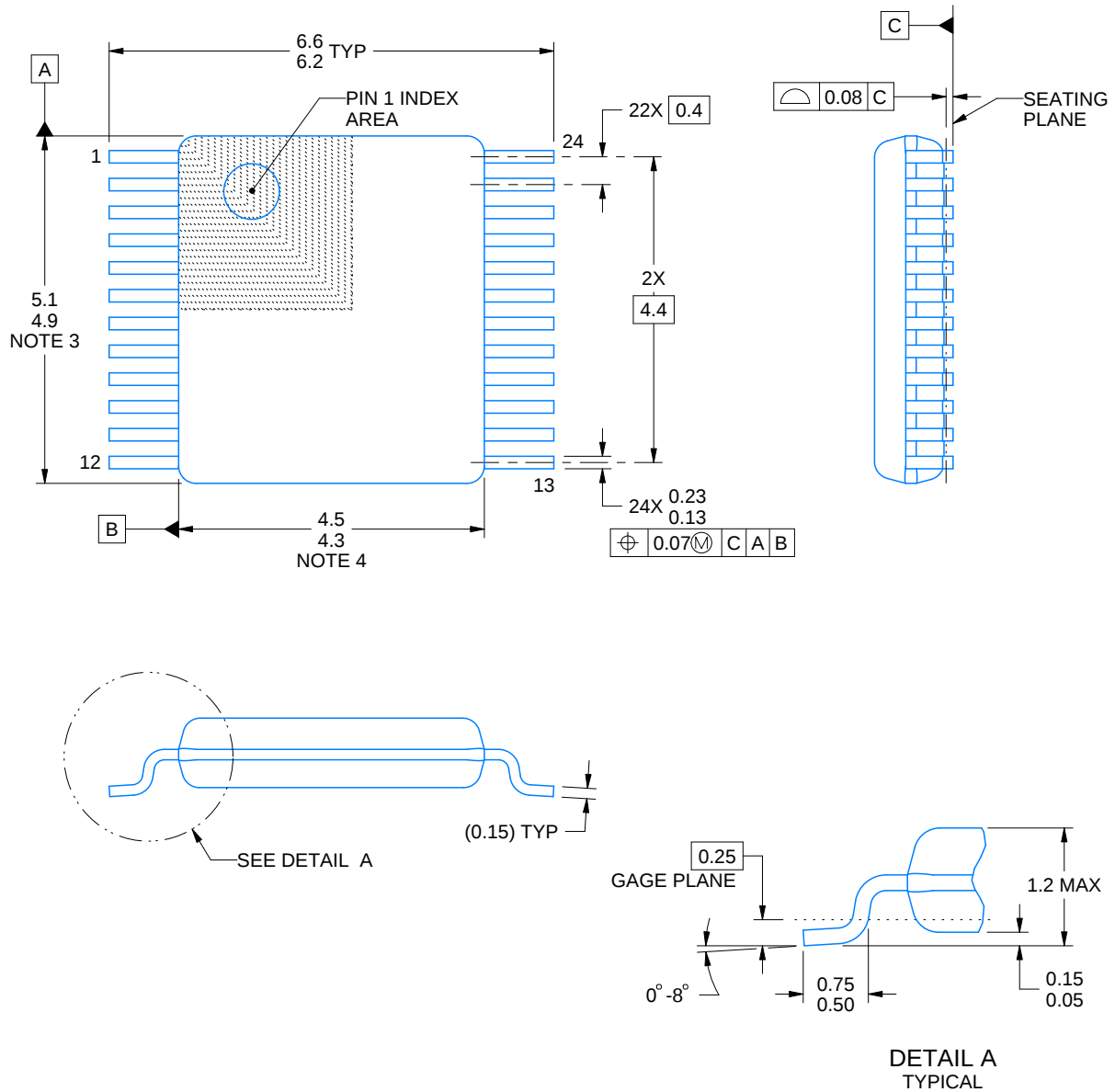
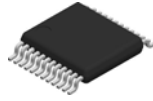
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.



4229221/A 12/2022

NOTES:

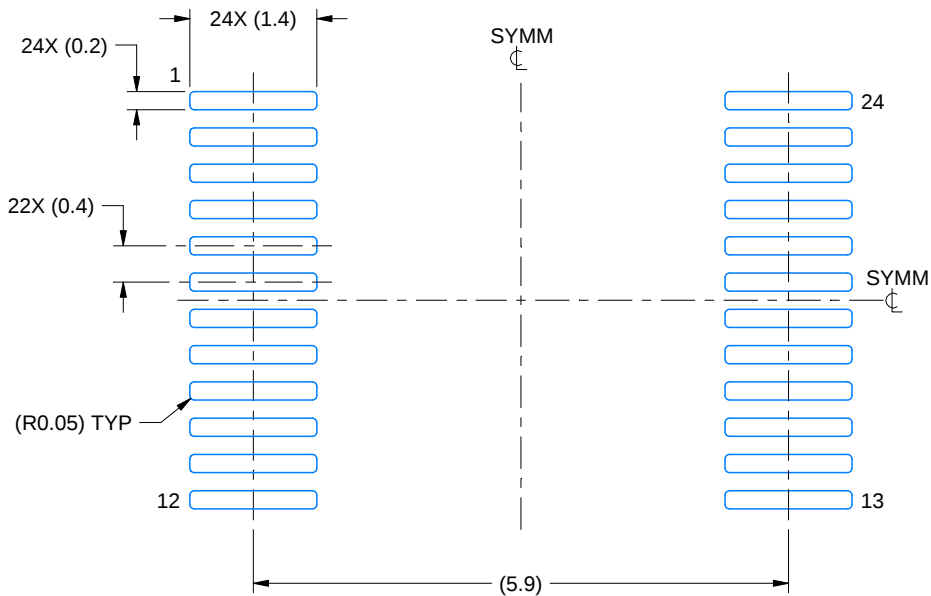
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

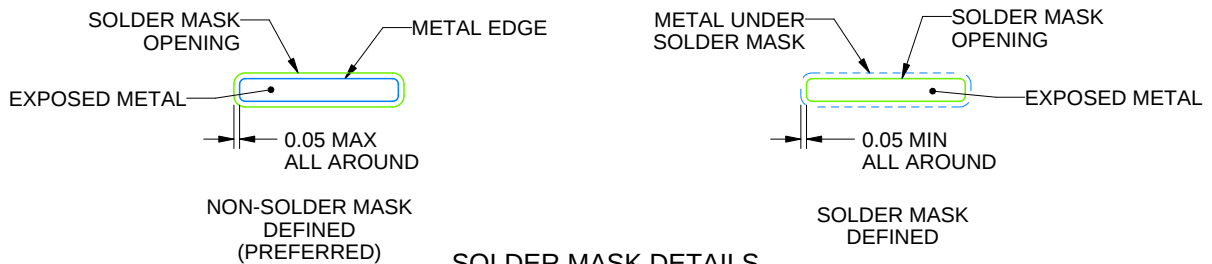
DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

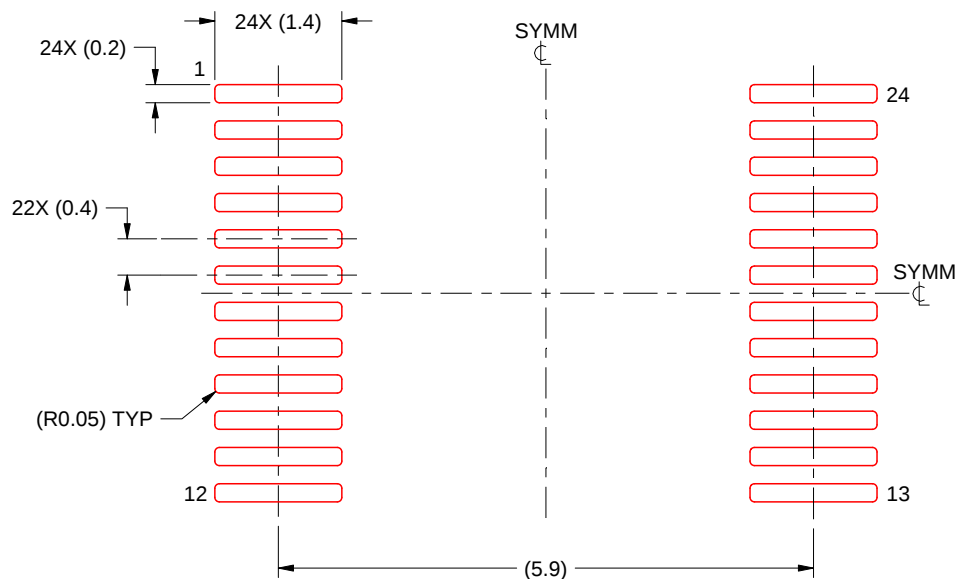
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

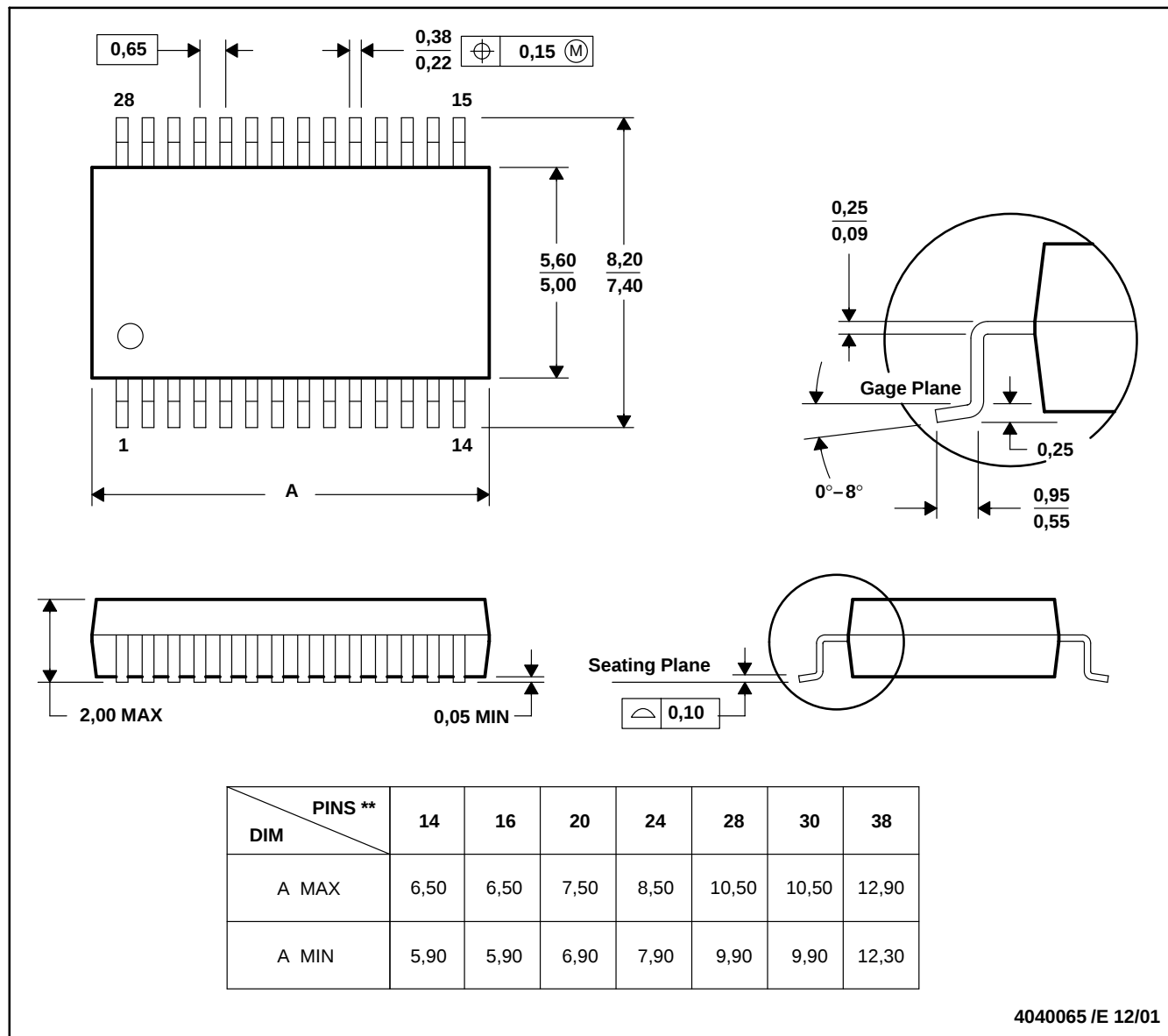
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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