OPT3001-Q1 環境光センサ(ALS)

1 特長

- 車載デバイス用に AEC-Q100 認定済み
  - 温度グレード 2 (USON、SOT-5X3 パッケージ):-40℃～105℃、T_A
  - 温度グレード 3 (USON パッケージのみ):-40℃～85℃、T_A
- 高精度の光フィルタリングにより人間の目に適合
  - 99% 超 (標準値) の IR を除去 (USON パッケージ)
  - ±85° の入射角にわたって 99% 超 (標準値) の IR を除去 (SOT-5X3 パッケージ)
- 自動フルスケール設定機能により、ソフトウェアが簡素化され、適切な構成を実現
- 測定範囲:0.01lux～83klux
- 自動ゲイン範囲設定により、
  23 ビットの実効ダイナミック レンジを実現
- 12 個のバイナリ重み付けフルスケール レンジ設定:
  レンジ間のマッチング < 0.2% (標準値)
- 小さい動作電流:1.8μA (標準値)
- 広い電源電圧範囲:1.6V～3.6V
- 5.5V 許容の I/O
- 柔軟な割り込みシステム
- 小さなフォームファクタ
  - 2mm × 2mm × 0.65mm の USON パッケージ
  - 2.1mm x 1.9mm x 0.6mm の SOT-5X3 パッケージ

2 アプリケーション

- 車載用車内および車外照明
- インフォテインメントおよびクラスタ ディスプレイ
- エレクトロクロマティック ミラーとスマート ミラー
- ワイパー モジュール
- ヘッド アップ ディスプレイ (HUD) システム
- 車載用カメラ システム

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
OPT3001-Q1	DNP (USON、6)	2.00mm × 2.00mm
	DTS (SOT-5X3、8)	2.10 mm × 1.90mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

3 概要

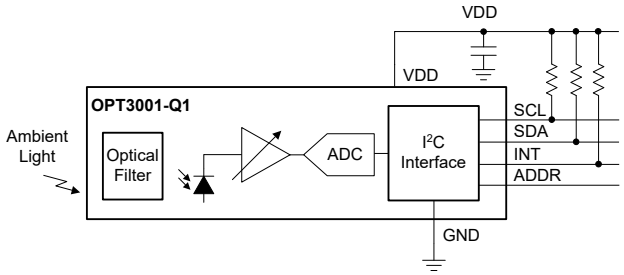
OPT3001-Q1 は、可視光の強度を測定する光センサです。このセンサのスペクトル応答は、人間の目の明所視応答によく合致し、強力な赤外線除去も備えており、SOT-5X3 パッケージ バリアントについては、その赤外線除去が広い入射角にわたって有効です。

OPT3001-Q1 は、人間の目と同じように光の強度を測定するシングル チップのルクス メーターです。OPT3001-Q1 デバイスは、高精度のスペクトル応答と強力な IR 除去により、光源にかかわらず人間の目の感覚に一致する照度を正確に測定できます。また、強力な IR 除去機能があるため、産業用のデザインで美観上の理由から暗色のガラス下にセンサを設置する必要がある場合でも、高い精度を維持できます。OPT3001-Q1 デバイスは、人間の目が感じる光環境を実現するシステム向けに開発された製品です。人間の目との一致度が低く、IR 除去も弱いフォトダイオード、フォトレジスタ、その他の環境光センサの代替品として理想的です。

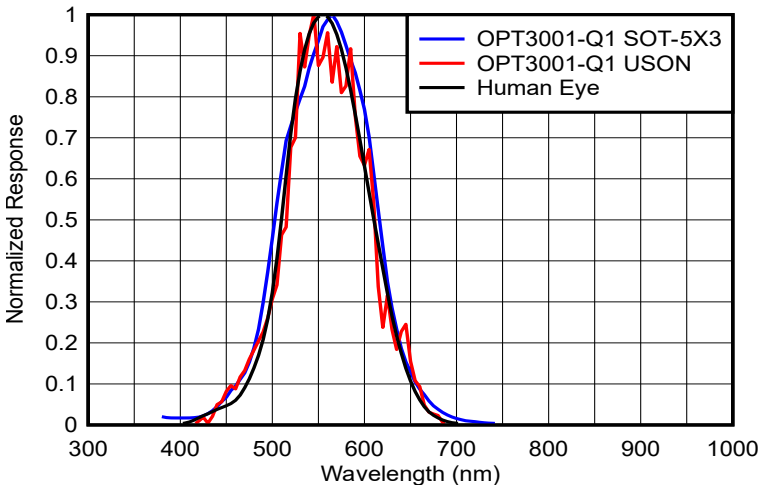
柔軟なデジタル動作により、システムの統合が可能です。連続的な測定も、1 回のみの測定も実行できます。制御および割り込みシステムは自律的に動作するため、プロセッサがスリープ中でもセンサが適切なウェイクアップ イベントを調べ、割り込みピンで通知します。デジタル出力は、I²C および SMBus 互換の 2 線式シリアル インターフェイスで通知されます。

OPT3001-Q1 デバイスは消費電力が低く、電源電圧も低いため、バッテリ駆動のシステムで長時間動作可能です。

内蔵のフルスケール設定機能により、手動でフルスケール範囲を選択することなく、0.01 ルクスから 83k ルクスの測定に対応できます。この機能により、23 ビットの実効ダイナミック レンジにわたって光の測定が可能です。



ブロック図



スペクトル応答：OPT3001-Q1 と人間の目の比較

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4 Pin Configuration and Functions

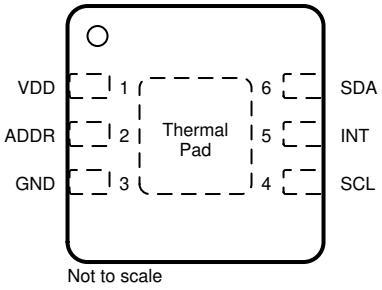


図 4-1. DNP Package 6-Pin USON Top View

表 4-1. Pin Functions

PIN		Type(1)	DESCRIPTION
NO.	NAME		
1	V_{DD}	I	Device power. Connect to a 1.6-V to 3.6-V supply.
2	ADDR	I	Address pin. This pin sets the LSBs of the I^2C address.
3	GND	P	Ground
4	SCL	I	I^2C clock. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
5	INT	O	Interrupt output, open-drain. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
6	SDA	I/O	I^2C data. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.

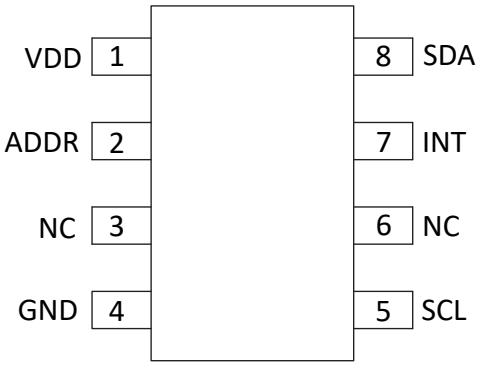


図 4-2. DTS Package 8-Pin SOT-5X3 Top View

表 4-2. Pin Functions

PIN		Type(1)	DESCRIPTION
NO.	NAME		
1	V_{DD}	P	Device power. Connect to a 1.6-V to 3.6-V supply.
2	ADDR	I	Address pin. This pin sets the LSBs of the I^2C address.
3	NC	No Connection	No Connection
4	GND	P	Ground
5	SCL	I	I^2C clock. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
6	NC	No Connection	No Connection
7	INT	O	Interrupt output, open-drain. Connect with a 10kΩ resistor to a 1.6-V to 5.5-V supply.
8	SDA	I/O	I^2C data. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.

(1) I = Input; O = Output; I/O = Input or Output; P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD to GND	–0.5	6	V
	SDA, SCL, INT, and ADDR to GND	–0.5	6	V
Current in to any pin			10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150(2)	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Long exposure to temperatures higher than 105°C can cause package discoloration, spectral distortion, and measurement inaccuracy.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	1.6		3.6	V
Operating temperature (Grade 2: OPT3001DNPQ1, OPT3001DTSQ1)	–40		105	°C
Operating temperature (Grade 3: OPT3001IDNPQ1)	–40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		OPT3001-Q1		UNIT
		DNP (USON)	DTS (SOT)	
		6 pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.2	171.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	83.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.2	66.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.4	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.8	65.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.0	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

All specifications at TA = 25°C, VDD = 3.3 V, 800-ms conversion-time (CT=1)(1), automatic full-scale range (RN[3:0] = 1100b)(1), white LED and normal-angle incidence of light, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Optical						
SOT-5X3 Variant						
	Peak irradiance spectral responsivity			560		nm
	Measurement output result	0.64 lux per ADC code, 2620.8 lux full-scale (RN[3:0] = 0110)(1), 2000 lux input(2)	2500	3125	3750	ADC codes
			1600	2000	2400	lux
	Measurement drift across temperature	Input illuminance = 2000 lux		0.035		%/°C
	Half-power-angle	50% of full-power reading		60		degrees
USON Variant						
	Peak irradiance spectral responsivity			550		nm
	Measurement output result	0.64 lux per ADC code, 2620.8 lux full-scale (RN[3:0] = 0110)(1), 2000 lux input(2)	2812	3125	3437	ADC codes
			1800	2000	2200	lux
	Measurement drift across temperature	Input illuminance = 2000 lux		0.02		%/°C
	Half-power-angle	50% of full-power reading		57		degrees
Common Specifications						
	Resolution (LSB)	Lowest full-scale range, RN[3:0]=0000b(1) at 800 ms conversion time		0.01		lux
		Lowest full-scale range, RN[3:0]=0000b(1) at 100 ms conversion time		0.08		
	Full-scale illuminance			83865.6		lux
	Relative accuracy between gain ranges (3)			0.2		%
	Infrared response (850nm)(2)	From -85° to +85° angle of incidence (SOT-5X3 only)		0.2		%
	Light Source Variation (incandescent, halogen, fluorescent)	Bare device, no cover glass		4		%
	Linearity	Input illuminance > 40 lux		2		%
		Input illuminance < 40 lux		5		%
	Dark Condition ADC output	0.01 lux per ADC Code		0	3	ADC codes
PSRR	Power-supply rejection ratio(4)	VDD at 3.6 V and 1.6 V		0.1		%/V(3)
POWER SUPPLY						
V_{DD}	Operating Range		1.6		3.6	V
V_{I2C}	Operating range for I2C pull up resistor	I^2C pullup resistor, $V_{DD} \leq V_{I2C}$	1.6		5.5	V

All specifications at TA = 25°C, VDD = 3.3 V, 800-ms conversion-time (CT=1)(1), automatic full-scale range (RN[3:0] = 1100b)(1), white LED and normal-angle incidence of light, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent current	Dark	Active, Vdd=3.6V		1.8	2.5	µA
			Shutdown (M[1:0]=00)(1), VDD=3.6V		0.3	0.47	µA
		Full-scale lux	Active, Vdd=3.6V		3.7		
			Shutdown (M[1:0]=00)(1)		0.4		
POR	Power-on-reset threshold				0.8		V
DIGITAL							
C_{IO}	I/O Pin Capacitance				3		pF
	Total Integration-time(5)	(CT = 1)(1) , 800-ms mode, fixed lux range		720	800	880	ms
		(CT = 0)(1) , 100-ms mode, fixed lux range		90	100	110	ms
V_{IL}	Low-level input voltage (SDA, SCL, and ADDR)			0		0.3 X V_{DD}	V
V_{IH}	High-level input voltage (SDA, SCL, and ADDR)			0.7 X V_{DD}		5.5	V
I_{IL}	Low-level input current (SDA, SCL, and ADDR)				0.01	0.25(6)	µA
V_{OL}	Low-level output voltage (SDA and INT)	I_{OL}=3mA				0.32	V
I_{ZH}	Output logic high, high-Z leakage current (SDA, INT)	Measured with V_{DD} at pin			0.01	0.25(6)	µA
TEMPERATURE							
Specified temperature range		Grade 2 (SOT-5X3, USON variant)		–40		105	°C
		Grade 3 (USON variant)		–40		85	

(1) Refers to a control field within the configuration register
(2) Tested with the white LED calibrated to 2k lux and an 850-nm LED
(3) Characterized by measuring fixed near-full-scale light levels on the higher adjacent full-scale range setting.
(4) PSRR is the percent change of the measured lux output from the current value, divided by the change in power supply voltage, as characterized by results from 3.6-V and 1.6-V power supplies.
(5) The conversion-time, from start of conversion until the data are ready to be read, is the integration-time plus 3 ms.
(6) The specified leakage current is dominated by the production test equipment limitations. Typical values are much smaller

5.6 Timing Requirements (1)

		MIN	TYP	MAX	UNIT
I²C FAST MODE					
f_{SCL}	SCL operating frequency	0.01		0.4	MHz
t_{BUF}	Bus free time between stop and start	1300			ns
t_{HDSTA}	Hold time after repeated start	600			ns
t_{SUSTA}	Setup time for repeated start	600			ns
t_{SUSTO}	Setup time for stop	600			ns
t_{HDDAT}	Data hold time	20		900	ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_{RC} and t_{FC}	Clock rise and fall time			300	ns
t_{RD} and t_{FD}	Data rise and fall time			300	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms

		MIN	TYP	MAX	UNIT
I²C HIGH-SPEED MODE					
f_{SCL}	SCL operating frequency	0.01		2.6	MHz
t_{BUF}	Bus free time between stop and start	160			ns
t_{HDSTA}	Hold time after repeated start	160			ns
t_{SUSTA}	Setup time for repeated start	160			ns
t_{SUSTO}	Setup time for stop	160			ns
t_{HDDAT}	Data hold time	20		140	ns
t_{SUDAT}	Data setup time	20			ns
t_{LOW}	SCL clock low period	240			ns
t_{HIGH}	SCL clock high period	60			ns
t_{RC} and t_{FC}	Clock rise and fall time			40	ns
t_{RD} and t_{FD}	Data rise and fall time			80	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms

(1) All timing parameters are referenced to low and high voltage thresholds of 30% and 70%, respectively, of final settled value.

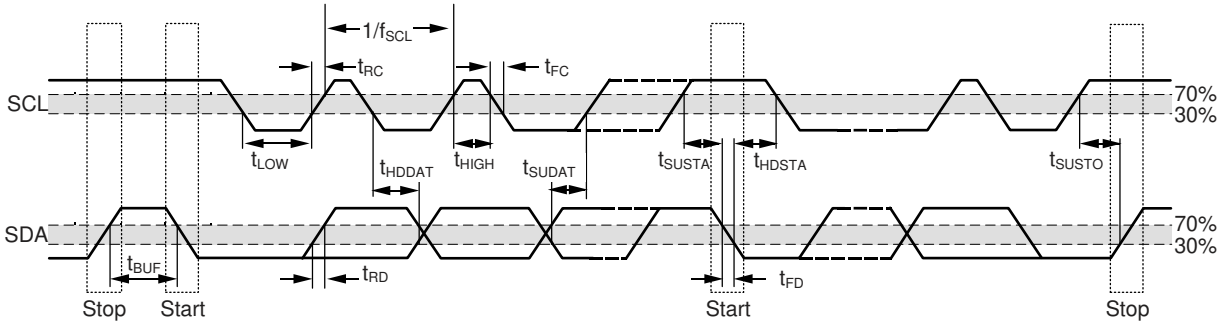


図 5-1. I²C Detailed Timing Diagram

5.7 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3V, 800ms conversion time (CT = 1), automatic full-scale range (RN[3:0] = 1100b), white LED, and normal-angle incidence of light, unless otherwise specified.

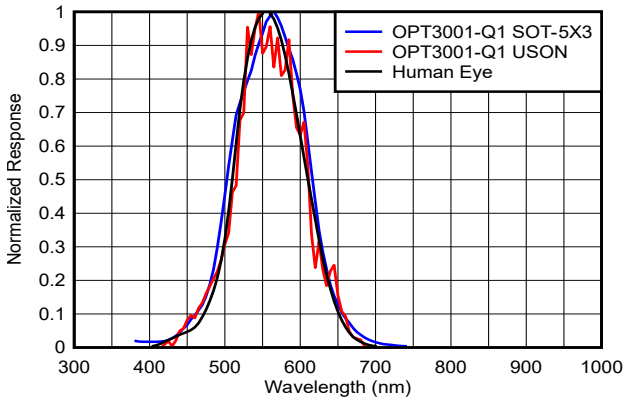


図 5-2. Spectral Response vs Wavelength

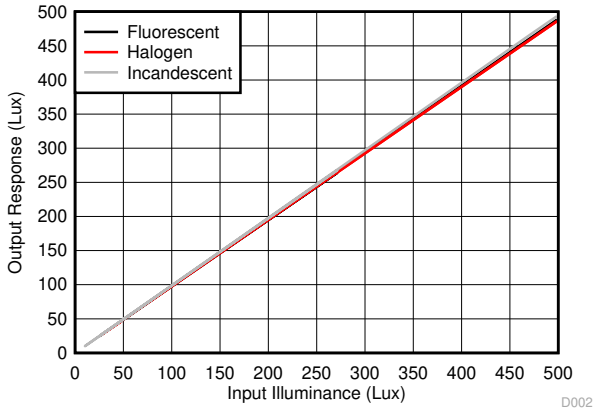


図 5-3. Output Response vs Input Illuminance, Multiple Light Sources: Fluorescent, Halogen, Incandescent

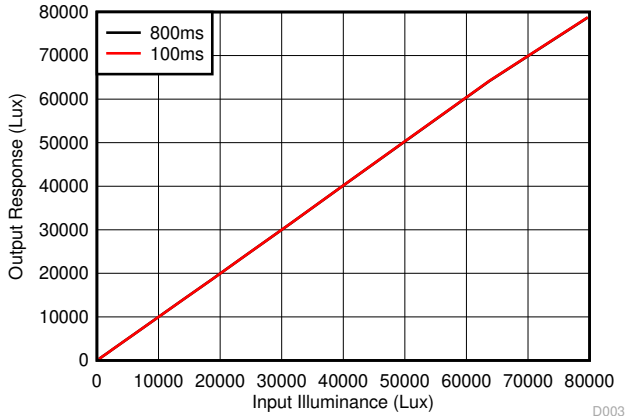


図 5-4. Output Response vs Input Illuminance: Entire Range = 0lux to 83klux

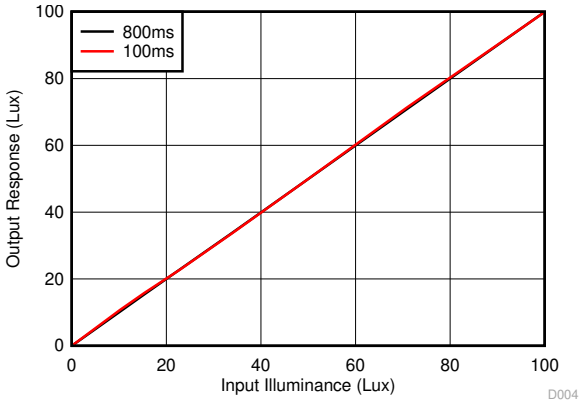


図 5-5. Output Response vs Input Illuminance: Mid Range = 0lux to 100lux

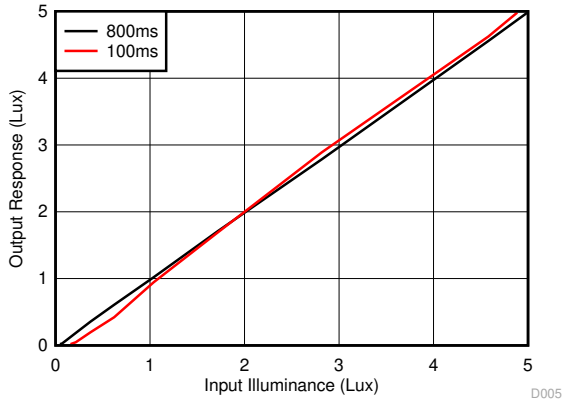
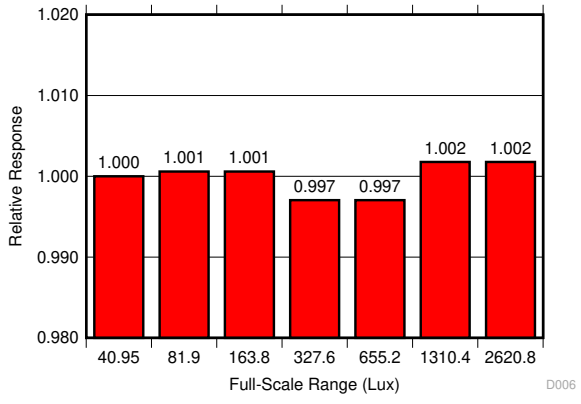
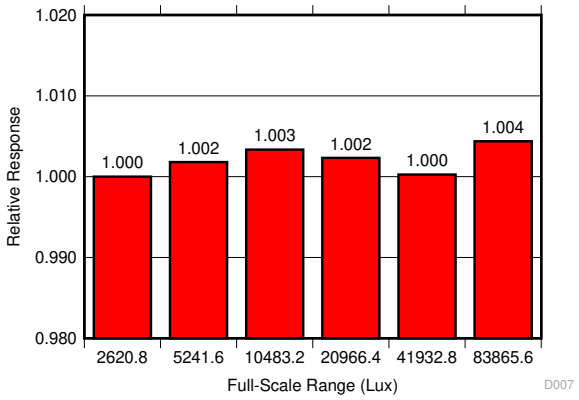


図 5-6. Output Response vs Input Illuminance: Low Range = 0lux to 5lux



Input illuminance = 33lux, normalized to response of 40.95lux full-scale

図 5-7. Full-Scale-Range Matching: Lowest 7 Ranges



Input illuminance = 2490lux, normalized to response of 2560lux full-scale

図 5-8. Full-Scale-Range Matching (Highest 6 Ranges)

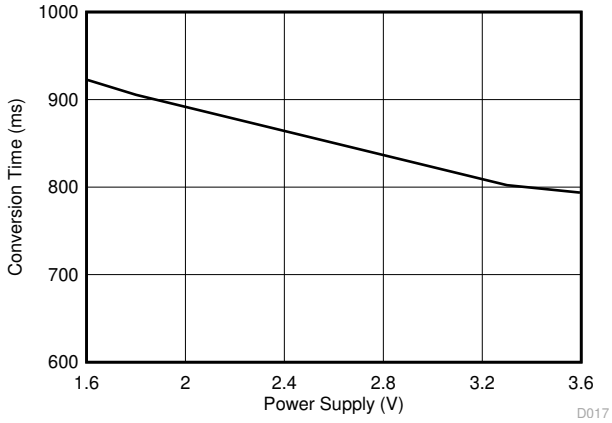
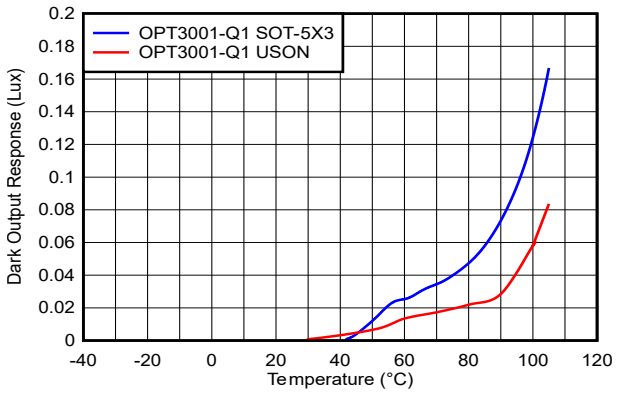
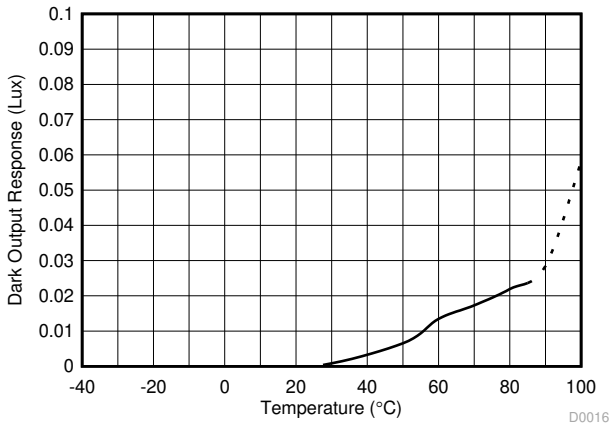


図 5-9. Conversion Time vs Power Supply



Average of 30 devices

図 5-10. Dark Response vs Temperature (Grade 2)



Average of 30 devices

図 5-11. Dark Response vs Temperature (Grade 3)

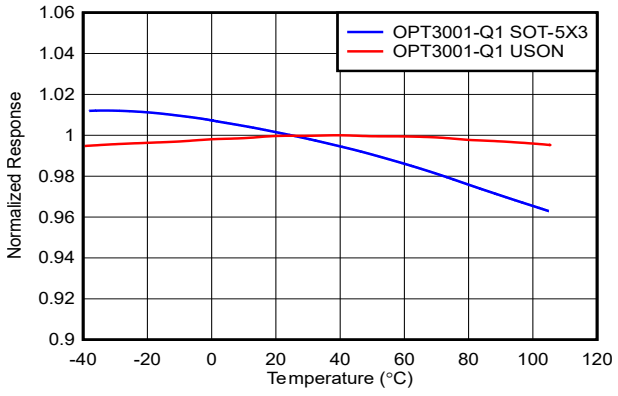


図 5-12. Normalized Response vs Temperature (Grade 2)

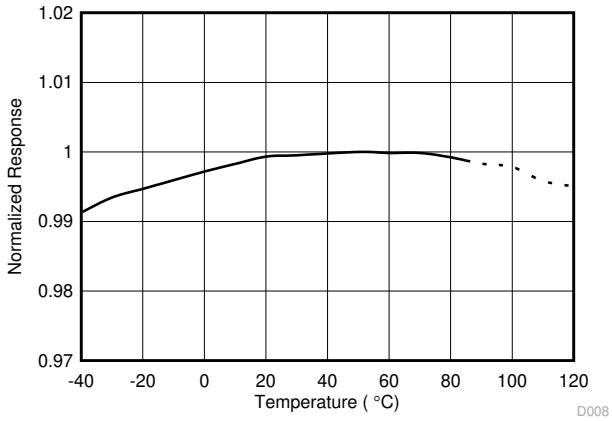


図 5-13. Normalized Response vs Temperature (Grade 3)

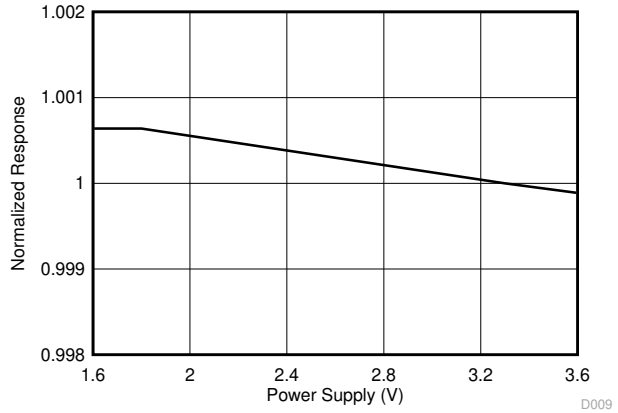


図 5-14. Normalized Response vs Power-Supply Voltage

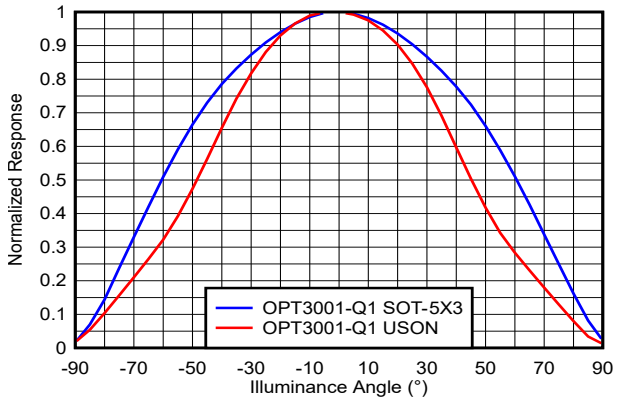
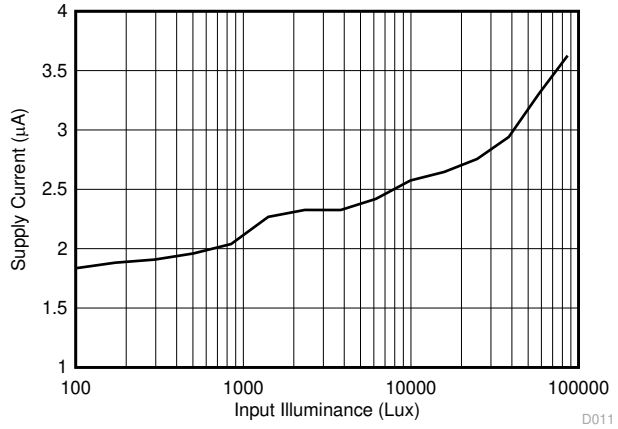
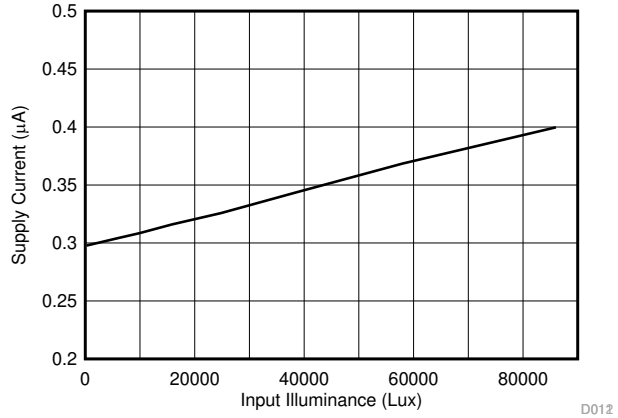


図 5-15. Normalized Response vs Illuminance Angle



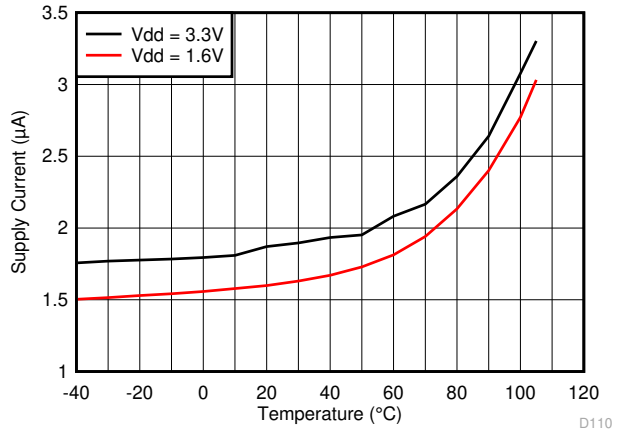
M[1:0] = 10b

図 5-16. Supply Current vs Input Illuminance



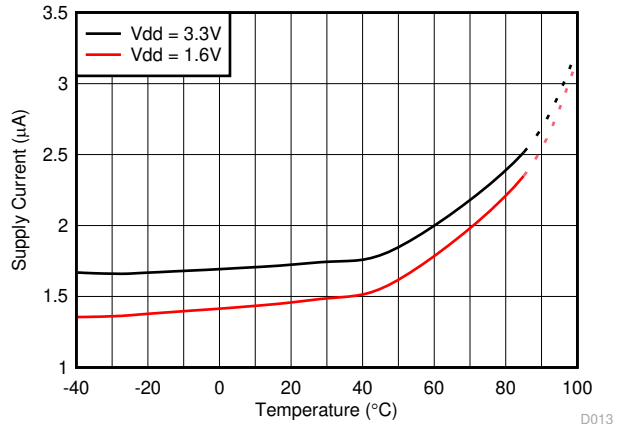
M[1:0] = 00b

図 5-17. Shutdown Current vs Input Illuminance



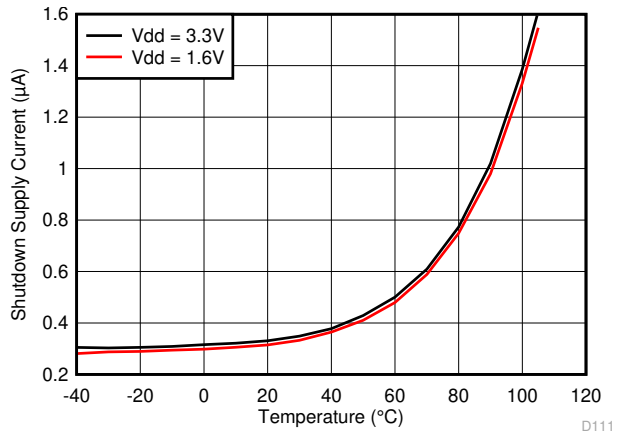
M[1:0] = 10b

図 5-18. Supply Current vs Temperature (Grade 2)



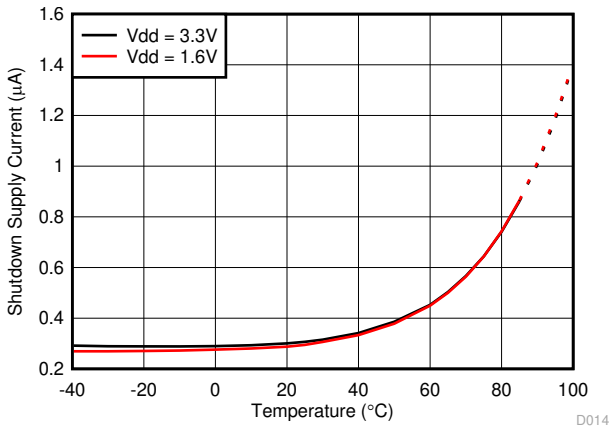
M[1:0] = 10b

図 5-19. Supply Current vs Temperature (Grade 3)



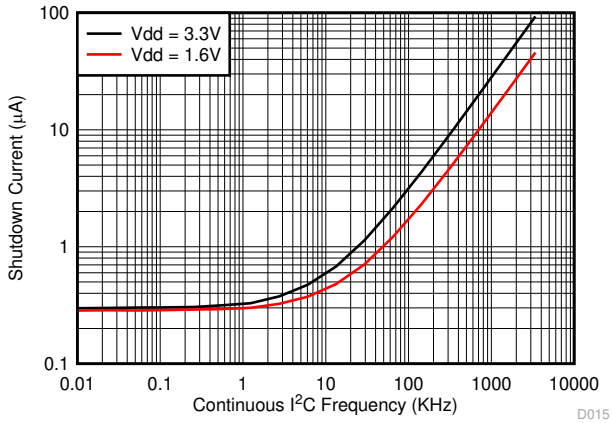
M[1:0] = 00b, input illuminance = 0 lux

図 5-20. Shutdown Current vs Temperature (Grade 2)



M[1:0] = 00b, input illuminance = 0lux

図 5-21. Shutdown Current vs Temperature (Grade 3)



Input illuminance = 80lux, SCL = SDA, continuously toggled at I^2C frequency Note: A typical application runs at a lower duty cycle and thus consumes a lower current.

図 5-22. Supply Current vs Continuous I^2C Frequency

6 Detailed Description

6.1 Overview

The OPT3001-Q1 device measures the ambient light that illuminates the device. This device measures light with a spectral response very closely matched to the human eye, and with very good infrared rejection.

Matching the sensor spectral response to that of the human eye response is vital because ambient light sensors are used to measure and help create ideal human lighting experiences. Strong rejection of infrared light, which a human does not see, is a crucial component of this matching. This matching makes the OPT3001-Q1 device especially good for operation underneath windows that are visibly dark, but infrared transmissive.

The OPT3001-Q1 device is fully self-contained to measure the ambient light and report the result in lux digitally over the I^2C bus. The result can also be used to alert a system and interrupt a processor with the INT pin. The result can also be summarized with a programmable window comparison and communicated with the INT pin.

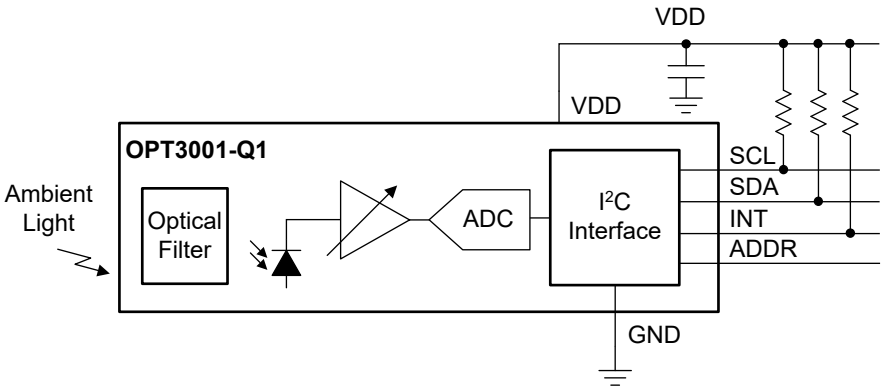
The OPT3001-Q1 device can be configured into an automatic full-scale, range-setting mode that always selects the optimal full-scale range setting for the lighting conditions. This mode frees the user from having to program the software for potential iterative cycles of measurement and readjustment of the full-scale range until optimal for any given measurement. The device can be commanded to operate continuously or in single-shot measurement modes.

The device integrates the result over either 100 ms or 800 ms, so the effects of 50-Hz and 60-Hz noise sources from typical light bulbs are nominally reduced to a minimum.

The device starts up in a low-power shutdown state, such that the OPT3001-Q1 device only consumes active-operation power after being programmed into an active state.

The OPT3001-Q1 optical filtering system is not excessively sensitive to non-ideal particles and micro-shadows on the optical surface. This reduced sensitivity is a result of the relatively minor device dependency on uniform-density optical illumination of the sensor area for infrared rejection. Proper optical surface cleanliness is always recommended for best results on all optical devices.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Human Eye Matching

The OPT3001-Q1 spectral response closely matches that of the human eye. If the ambient light sensor measurement is used to help create a good human experience, or create optical conditions that are optimal for a human, the sensor must measure the same spectrum of light that a human sees.

The device also has excellent infrared light (IR) rejection. This IR rejection is especially important because many real-world lighting sources have significant infrared content that humans do not see. If the sensor measures infrared light that the human eye does not see, then a true human experience is not accurately represented.

Furthermore, if the ambient light sensor is hidden underneath a dark window (such that the end-product user cannot see the sensor) the infrared rejection of the OPT3001-Q1 device becomes significantly more important because many dark windows attenuate visible light but transmit infrared light. This attenuation of visible light and lack of attenuation of IR light amplifies the ratio of the infrared light to visible light that illuminates the sensor. Results can still be well matched to the human eye under this condition because of the high infrared rejection of the OPT3001-Q1 device.

6.3.2 Automatic Full-Scale Range Setting

The OPT3001-Q1 device has an automatic full-scale range setting feature that eliminates the need to predict and set the optimal range for the device. In this mode, the OPT3001-Q1 device automatically selects the optimal full-scale range for the given lighting condition. The OPT3001-Q1 device has a high degree of result matching between the full-scale range settings. This matching eliminates the problem of varying results or the need for range-specific, user-calibrated gain factors when different full-scale ranges are chosen. For further details, see the セクション 6.4.1 section.

6.3.3 Interrupt Operation, INT Pin, and Interrupt Reporting Mechanisms

The device has an interrupt reporting system that allows the processor connected to the I^2C bus to go to sleep, or otherwise ignore the device results, until a user-defined event occurs that requires possible action. Alternatively, this same mechanism can also be used with any system that can take advantage of a single digital signal that indicates whether the light is above or below levels of interest.

The interrupt event conditions are controlled by the high-limit and low-limit registers, as well as the configuration register latch and fault count fields. The results of comparing the result register with the high-limit register and low-limit register are referred to as *fault events*. The fault count register dictates how many consecutive same-result fault events are required to trigger an interrupt event and subsequently change the state of the interrupt reporting mechanisms, which are the INT pin, the flag high field, and the flag low field. The latch field allows a choice between a latched window-style comparison and a transparent hysteresis-style comparison.

The INT pin has an open-drain output, which requires the use of a pull-up resistor. This open-drain output allows multiple devices with open-drain INT pins to be connected to the same line, thus creating a logical *NOR* or *AND* function between the devices. The polarity of the INT pin can be controlled with the polarity of interrupt field in the configuration register. When the POL field is set to 0, the pin operates in an active low behavior that pulls the pin low when the INT pin becomes active. When the POL field is set to 1, the pin operates in an active high behavior and becomes high impedance, thus allowing the pin to go high when the INT pin becomes active.

Additional details of the interrupt reporting registers are described in the セクション 6.4.2 and セクション 7.1 sections.

6.3.4 I²C Bus Overview

The OPT3001-Q1 device offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another. The I²C interface is used throughout this document as the primary example with the SMBus protocol specified only when a difference between the two protocols is discussed.

The OPT3001-Q1 device is connected to the bus with two pins: an SCL clock input pin and an SDA open-drain bidirectional data pin. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates start and stop conditions. To address a specific device, the controller initiates a start condition by pulling the data signal line (SDA) from a high logic level to a low logic level while SCL is high. All targets on the bus shift in the target address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an acknowledge bit by pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition. When all data are transferred, the controller generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The OPT3001-Q1 device includes a 28ms timeout on the I²C interface to prevent locking up the bus. If the SCL line is held low for this duration of time, the bus state machine is reset.

6.3.4.1 Serial Bus Address

To communicate with the OPT3001-Q1 device, the controller must first initiate an I²C start command. Then, the controller must address target devices via a target address byte. The target address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

Four I²C addresses are possible by connecting the ADDR pin to one of four pins: GND, VDD, SDA, or SCL. 表 6-1 summarizes the possible addresses with the corresponding ADDR pin configuration. The state of the ADDR pin is sampled on every bus communication and must be driven or connected to the desired level before any activity on the interface occurs.

表 6-1. Possible I²C Addresses with Corresponding ADDR Configuration

DEVICE I²C ADDRESS	ADDR PIN
1000 100	GND
1000 101	VDD
1000 110	SDA
1000 111	SCL

6.3.4.2 Serial Interface

The OPT3001-Q1 device operates as a target device on both the I²C bus and SMBus. Connections to the bus are made using the SCL clock input line and the SDA open-drain I/O line. The OPT3001-Q1 device supports the transmission protocol for standard mode (up to 100kHz), fast mode (up to 400kHz), and high-speed mode (up to 2.6MHz). All data bytes are transmitted most-significant bits first.

The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. See the *セクション 8.1.1* section for further details of the I²C bus noise immunity.

6.4 Device Functional Modes

6.4.1 Automatic Full-Scale Setting Mode

The OPT3001-Q1 device has an automatic full-scale-range setting mode that eliminates the need for a user to predict and set the optimal range for the device. This mode is entered when the configuration register range number field (RN[3:0]) is set to 1100b.

The first measurement that the device takes in auto-range mode is a 10 ms range assessment measurement. The device then determines the appropriate full-scale range to take the first full measurement.

For subsequent measurements, the full-scale range is set by the result of the previous measurement. If a measurement is towards the low side of full-scale, the full-scale range is decreased by one or two settings for the next measurement. If a measurement is towards the upper side of full-scale, the full-scale range is increased by one setting for the next measurement.

If the measurement exceeds the full-scale range, resulting from a fast increasing optical transient event, the current measurement is terminated. This invalid measurement is not reported. A 10 ms measurement is taken to assess and properly reset the full-scale range. Then, a new measurement is taken with this proper full-scale range. Therefore, during a fast increasing optical transient in this mode, a measurement can possibly take longer to complete and report than indicated by the configuration register conversion time field (CT).

6.4.2 Interrupt Reporting Mechanism Modes

There are two major types of interrupt reporting mechanism modes: latched window-style comparison mode and transparent hysteresis-style comparison mode. The configuration register latch field (L) (see the configuration register, bit 4) controls which of these two modes is used. An end-of-conversion mode is also associated with each major mode type. The end-of-conversion mode is active when the two most significant bits of the threshold low register are set to 11b. The mechanisms report via the flag high and flag low fields, the conversion ready field, and the INT pin.

6.4.2.1 Latched Window-Style Comparison Mode

The latched window-style comparison mode is typically selected when using the OPT3001-Q1 device to interrupt an external processor. In this mode, a fault is recognized when the input signal is above the high-limit register or below the low-limit register. When the consecutive fault events trigger the interrupt reporting mechanisms, these mechanisms are latched, thus reporting whether the fault is the result of a high or low comparison. These mechanisms remain latched until the configuration register is read, which clears the INT pin and flag high and flag low fields. The SMBus alert response protocol, described in detail in the *セクション 6.5.1.3* section, clears the pin but does not clear the flag high and flag low fields. The behavior of this mode, along with the conversion ready flag, is summarized in 表 6-2. Note that 表 6-2 does not apply when the two threshold low register MSBs (see the *セクション 6.4.2.2* section for clarification on the MSBs) are set to 11b.

表 6-2. Latched Window-Style Comparison Mode: Flag Setting and Clearing Summary

OPERATION	FLAG HIGH FIELD (2) (4)	FLAG LOW FIELD	INT PIN(1)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	X	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	X	1	Active	1
The conversion is complete with fault count criterion not met	X	X	X	1
Configuration register read(3)	0	0	Inactive	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	X	0
SMBus alert response protocol	X	X	Inactive	X

(1) The INT pin depends on the setting of the polarity field (POL). The INT pin is low when the pin state is active and POL = 0 (active low) or when the pin state is inactive and POL = 1 (active high).
(2) X = no change from the previous state.
(3) Immediately after the configuration register is read, the device automatically resets the conversion ready field to the 0 state. Thus, if two configuration register reads are performed immediately after a conversion completion, the first reads 1 and the second reads 0.
(4) The high-limit register is assumed to be greater than the low-limit register. If this assumption is incorrect, the flag high field and flag low field can take on different behaviors.

6.4.2.2 Transparent Hysteresis-Style Comparison Mode

The transparent hysteresis-style comparison mode is typically used when a single digital signal is desired that indicates whether the input light is higher than or lower than a light level of interest. If the result register is higher than the high-limit register for a consecutive number of events set by the fault count field, the INT line is set to active, the flag high field is set to 1, and the flag low field is set to 0. If the result register is lower than the low-limit register for a consecutive number of events set by the fault count field, the INT line is set to inactive, the flag low field is set to 1, and the flag high field is set to 0. The INT pin and flag high and flag low fields do not change state with configuration reads and writes. The INT pin and flag fields continually report the appropriate comparison of the light to the low-limit and high-limit registers. The device does not respond to the SMBus alert response protocol while in either of the two transparent comparison modes (configuration register, latch field = 0). The behavior of this mode, along with the conversion ready is summarized in 表 6-3. Note that 表 6-3 does not apply when the two threshold low register MSBs (LE[3:2] from 表 7-6) are set to 11.

表 6-3. Transparent Hysteresis-Style Comparison Mode: Flag Setting and Clearing Summary (2) (4)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(1)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	0	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	0	1	Inactive	1
The conversion is complete with fault count criterion not met	X	X	X	1
Configuration register read(3)	X	X	X	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	X	0
SMBus alert response protocol	X	X	X	X

6.4.2.3 End-of-Conversion Mode

An end-of-conversion indicator mode can be used when every measurement is desired to be read by the processor, prompted by the INT pin going active on every measurement completion. This mode is entered by setting the most significant two bits of the low-limit register (LE[3:2] from the Low-Limit Register) to 11b. This end-of-conversion mode is typically used in conjunction with the latched window-style comparison mode. The INT pin becomes inactive when the configuration register is read or the configuration register is written with a non-shutdown parameter or in response to an SMBus alert response. 表 6-4 summarizes the interrupt reporting mechanisms as a result of various operations.

表 6-4. End-of-Conversion Mode while in Latched Window-Style Comparison Mode: Flag Setting and Clearing Summary (2)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(1)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	X	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	X	1	Active	1
The conversion is complete with fault count criterion not met	X	X	Active	1
Configuration register read(3)	0	0	Inactive	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	X	0
SMBus alert response protocol	X	X	Inactive	X

Note that when transitioning from end-of-conversion mode to the standard comparison modes (that is, programming LE[3:2] from 11b to 00b) while the configuration register latch field (L) is 1, a subsequent write to the configuration register latch field (L) to 0 is necessary to properly clear the INT pin. The latch field can then be set back to 1 if desired.

6.4.2.4 End-of-Conversion and Transparent Hysteresis-Style Comparison Mode

The combination of end-of-conversion mode and transparent hysteresis-style comparison mode can also be programmed simultaneously. The behavior of this combination is shown in 表 6-5.

表 6-5. End-Of-Conversion Mode while in Transparent Hysteresis-Style Comparison Mode: Flag Setting and Clearing Summary (2)

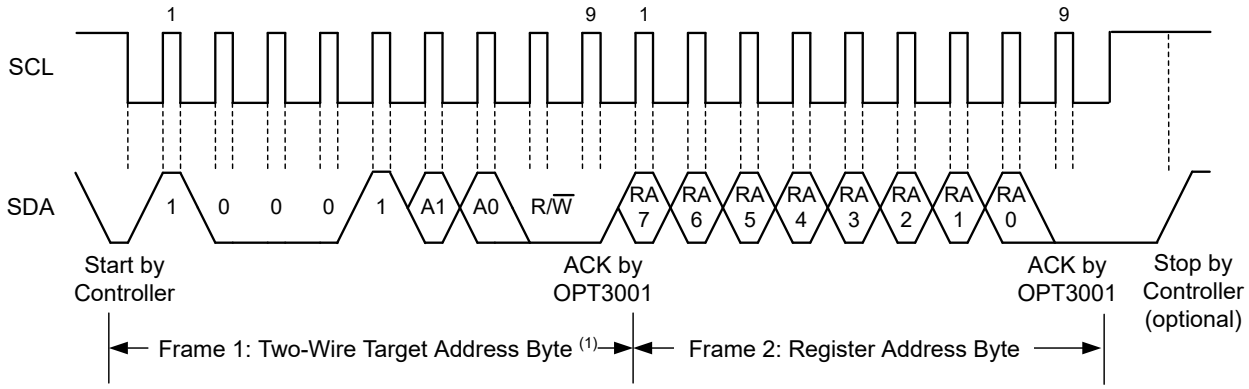
OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(1)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	0	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	0	1	Active	1
The conversion is complete with fault count criterion not met	X	X	Active	1
Configuration register read(3)	X	X	Inactive	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	Inactive	0
SMBus alert response protocol	X	X	X	X

6.5 Programming

The OPT3001-Q1 device supports the transmission protocol for standard mode (up to 100kHz), fast mode (up to 400kHz), and high-speed mode (up to 2.6MHz). Fast and standard modes are described as the default protocol, referred to as *F/S*. High-speed mode is described in the *セクション 6.5.1.1* section.

6.5.1 Writing and Reading

Accessing a specific register on the OPT3001-Q1 device is accomplished by writing the appropriate register address during the I²C transaction sequence. Refer to 表 7-1 for a complete list of registers and the corresponding register addresses. The value for the register address (as shown in 図 6-1) is the first byte transferred after the target address byte with the R/W bit low.



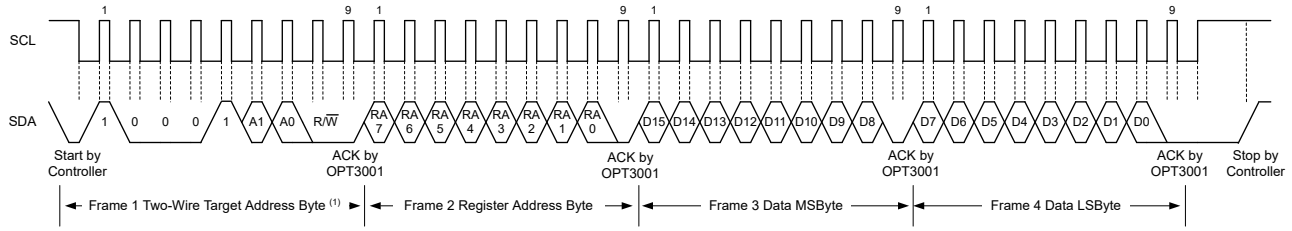
A. The value of the target address byte is determined by the ADDR pin setting; see 表 6-1.

図 6-1. Setting the I²C Register Address

Writing to a register begins with the first byte transmitted by the controller. This byte is the target address with the R/W bit low. The OPT3001-Q1 device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register that data are to be written to. The next two bytes are written to the register addressed by the register address. The OPT3001-Q1 device acknowledges receipt of each data byte. The controller can terminate the data transfer by generating a start or stop condition.

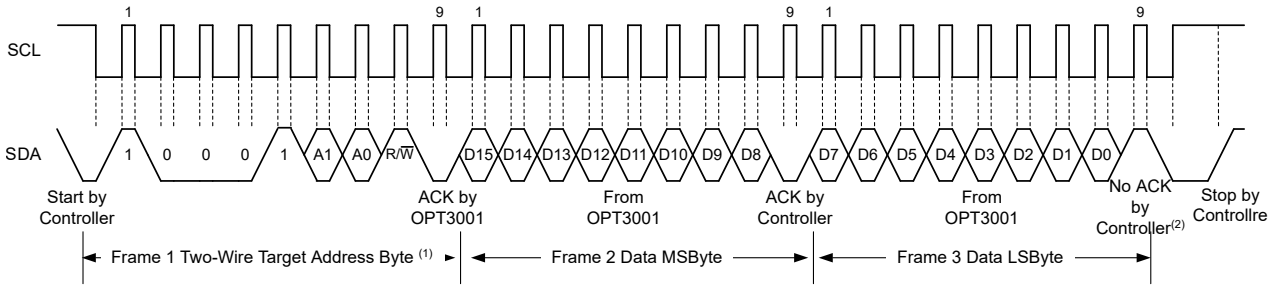
When reading from the OPT3001-Q1 device, the last value stored in the register address by a write operation determines which register is read during a read operation. To change the register address for a read operation, a new partial I²C write transaction must be initiated. This partial write is accomplished by issuing a target address byte with the R/W bit low, followed by the register address byte and a stop command. The controller then generates a start condition and sends the target address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register address. This byte is followed by an acknowledge from the controller; then the target transmits the least significant byte. The controller acknowledges receipt of the data byte. The controller can terminate the data transfer by generating a not-acknowledge after receiving any data byte, or by generating a start or stop condition. If repeated reads from the same register are desired, continually sending the register address bytes is not necessary; the OPT3001-Q1 device retains the register address until that number is changed by the next write operation.

図 6-2 and 図 6-3 show the write and read operation timing diagrams, respectively. Note that register bytes are sent most significant byte first, followed by the least significant byte.



A. The value of the target address byte is determined by the setting of the ADDR pin; see 表 6-1.

図 6-2. I²C Write Example



A. The value of the target address byte is determined by the ADDR pin setting; see 表 6-1.
B. An ACK by the controller can also be sent.

図 6-3. I²C Read Example

6.5.1.1 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up resistors or active pull-up devices. The master generates a start condition followed by a valid serial byte containing the high-speed (HS) master code 0000 1XXXb. This transmission is made in either standard mode or fast mode (up to 400kHz). The OPT3001-Q1 device does not acknowledge the HS master code but does recognize the code and switches the internal filters to support a 2.6MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.6MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS mode. A stop condition ends the HS mode and switches all internal filters of the OPT3001-Q1 device to support the F/S mode.

6.5.1.2 General-Call Reset Command

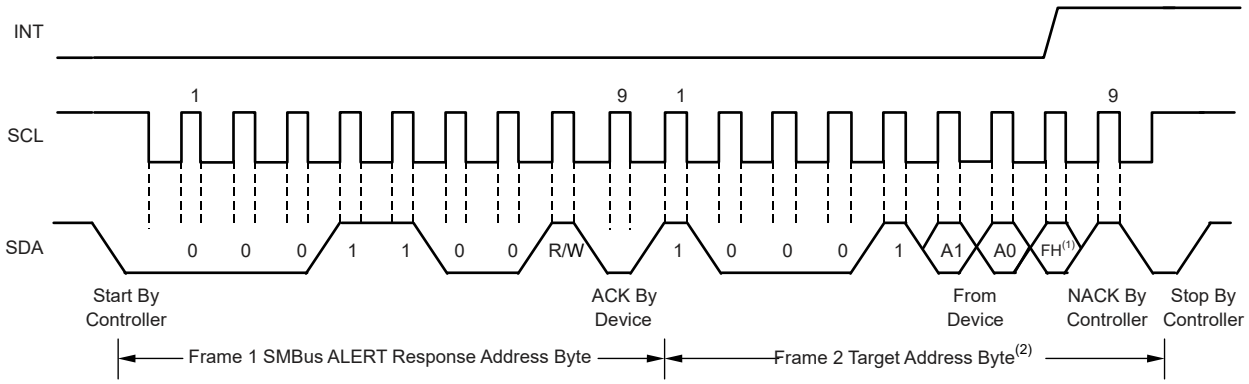
The I²C general-call reset allows the host controller in one command to reset all devices on the bus that respond to the general-call reset command. The general call is initiated by writing to the I²C address 0 (0000 0000b). The reset command is initiated when the subsequent second address byte is 06h (0000 0110b). With this transaction, the device issues an acknowledge bit and sets all of the registers to the power-on-reset default condition.

6.5.1.3 SMBus Alert Response

The SMBus alert response provides a quick identification for which device issued the interrupt. Without this alert response capability, the processor does not know which device pulled the interrupt line when there are multiple target devices connected.

The OPT3001-Q1 device is designed to respond to the SMBus alert response address, when in the latched window-style comparison mode (configuration register, latch field = 1). The OPT3001-Q1 device does not respond to the SMBus alert response when in transparent mode (configuration register, latch field = 0).

The response behavior of the OPT3001-Q1 device to the SMBus alert response is shown in 図 6-4. When the interrupt line to the processor is pulled to active, the controller can broadcast the alert response target address (0001 1001b). Following this alert response, any target devices that generated an alert can identify themselves by acknowledging the alert response and sending the respective I^2C address on the bus. The alert response can activate several different target devices simultaneously. If more than one target attempts to respond, bus arbitration rules apply. The device with the lowest address wins the arbitration. If the OPT3001-Q1 device loses the arbitration, the device does not acknowledge the I^2C transaction and the INT pin remains in an active state, prompting the I^2C controller processor to issue a subsequent SMBus alert response. When the OPT3001-Q1 device wins the arbitration, the device acknowledges the transaction and sets the INT pin to inactive. The controller can issue that same command again, as many times as necessary to clear the INT pin. See the *セクション 6.4.2* section for additional details of how the flags and INT pin are controlled. The controller can obtain information about the source of the OPT3001-Q1 interrupt from the address broadcast in the above process. The flag high field (configuration register, bit 6) is sent as the final LSB of the address to provide the controller additional information about the cause of the OPT3001-Q1 interrupt. If the controller requires additional information, the result register or the configuration register can be queried. The flag high and flag low fields are not cleared upon an SMBus alert response.



A. FH is the flag high field (FH) in the configuration register (see 表 7-5).

B. A1 and A0 are determined by the ADDR pin; see 表 6-1.

図 6-4. Timing Diagram for SMBus Alert Response

7 Register Maps

7.1 Internal Registers

The device is operated over the I^{2}C bus with registers that contain configuration, status, and result information. All registers are 16 bits long.

There are four main registers: result, configuration, low-limit, and high-limit. There are also two ID registers: manufacturer ID and device ID. 表 7-1 lists these registers.

表 7-1. Register Map

REGISTER	ADDRESS (Hex) (1)	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Result	00h	E3	E2	E1	E0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
Configuration	01h	RN3	RN2	RN1	RN0	CT	M1	M0	OVF	CRF	FH	FL	L	POL	ME	FC1	FC0
Low Limit	02h	LE3	LE2	LE1	LE0	TL11	TL10	TL9	TL8	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
High Limit	03h	HE3	HE2	HE1	HE0	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
Manufacturer ID	7Eh	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Device ID	7Fh	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0

(1) Register offset and register address are used interchangeably.

7.1.1 Register Descriptions

注

Register offset and register address are used interchangeably.

7.1.1.1 Result Register (offset = 00h)

This register contains the result of the most recent light to digital conversion. This 16-bit register has two fields: a 4-bit exponent and a 12-bit mantissa.

図 7-1. Result Register (Read-Only)

15	14	13	12	11	10	9	8
E3	E2	E1	E0	R11	R10	R9	R8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	R1	R0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

表 7-2. Result Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	E[3:0]	R	0h	**Exponent.** These bits are the exponent bits. 表 7-3 provides further details.
11:0	R[11:0]	R	000h	**Fractional result.** These bits are the result in straight binary coding (zero to full-scale).

表 7-3. Full-Scale Range and LSB Size as a Function of Exponent Level

E3	E2	E1	E0	FULL-SCALE RANGE (lux)	LSB SIZE (lux per LSB)
0	0	0	0	40.95	0.01

表 7-3. Full-Scale Range and LSB Size as a Function of Exponent Level (続き)

E3	E2	E1	E0	FULL-SCALE RANGE (lux)	LSB SIZE (lux per LSB)
0	0	0	1	81.90	0.02
0	0	1	0	163.80	0.04
0	0	1	1	327.60	0.08
0	1	0	0	655.20	0.16
0	1	0	1	1310.40	0.32
0	1	1	0	2620.80	0.64
0	1	1	1	5241.60	1.28
1	0	0	0	10483.20	2.56
1	0	0	1	20966.40	5.12
1	0	1	0	41932.80	10.24
1	0	1	1	83865.60	20.48

The formula to translate this register into lux is given in 式 1:

$$\text{lux} = \text{LSB\_Size} \times \text{R[11:0]} \quad (1)$$

where:

$$\text{LSB\_Size} = 0.01 \times 2^{\text{E[3:0]}} \quad (2)$$

LSB_Size can also be taken from 表 7-3. The complete lux equation is shown in 式 3:

$$\text{lux} = 0.01 \times (2^{\text{E[3:0]}}) \times \text{R[11:0]} \quad (3)$$

A series of result register output examples with the corresponding LSB weight and resulting lux are given in 表 7-4. Note that many combinations of exponents (E[3:0]) and fractional results (R[11:0]) can map onto the same lux result, as shown in the examples of 表 7-4.

表 7-4. Examples of Decoding the Result Register into lux

RESULT REGISTER (Bits 15:0, Binary)	EXPONENT (E[3:0], Hex)	FRACTIONAL RESULT (R[11:0], Hex)	LSB WEIGHT (lux, Decimal)	RESULTING LUX (Decimal)
0000 0000 0000 0001b	00h	001h	0.01	0.01
0000 1111 1111 1111b	00h	FFFh	0.01	40.95
0011 0100 0101 0110b	03h	456h	0.08	88.80
0111 1000 1001 1010b	07h	89Ah	1.28	2818.56
1000 1000 0000 0000b	08h	800h	2.56	5242.88
1001 0100 0000 0000b	09h	400h	5.12	5242.88
1010 0010 0000 0000b	0Ah	200h	10.24	5242.88
1011 0001 0000 0000b	0Bh	100h	20.48	5242.88
1011 0000 0000 0001b	0Bh	001h	20.48	20.48
1011 1111 1111 1111b	0Bh	FFFh	20.48	83865.60

Note that the exponent field can be disabled (set to zero) by enabling the exponent mask (configuration register, ME field = 1) and manually programming the full-scale range (configuration register, RN[3:0] < 1100b (0Ch)), allowing for simpler operation in a manually-programmed, full-scale mode. Calculating lux from the result register contents only requires multiplying the result register by the LSB weight (in lux) associated with the specific programmed full-scale range (see 表 7-3). See the Low-Limit Register for details.

See the configuration register conversion time field (CT, bit 11) description for more information on lux resolution as a function of conversion time.

7.1.1.2 Configuration Register (offset = 01h) [reset = C810h]

This register controls the major operational modes of the device. This register has 11 fields, which are documented below. If a measurement conversion is in progress when the configuration register is written, the active measurement conversion immediately aborts. If the new configuration register directs a new conversion, that conversion is subsequently started.

図 7-2. Configuration Register

15	14	13	12	11	10	9	8
RN3	RN2	RN1	RN0	CT	M1	M0	OVF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
7	6	5	4	3	2	1	0
CRF	FH	FL	L	POL	ME	FC1	FC0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only

表 7-5. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RN[3:0]	R/W	1100b	**Range number field (read or write).** The range number field selects the full-scale lux range of the device. The format of this field is the same as the result register exponent field (E[3:0]); see 表 7-3. When RN[3:0] is set to 1100b (0Ch), the device operates in automatic full-scale setting mode, as described in the *セクション 6.4.1* section. In this mode, the automatically chosen range is reported in the result exponent (register 00h, E[3:0]). The device powers up as 1100 in automatic full-scale setting mode. Codes 1101b, 1110b, and 1111b (0Dh, 0Eh, and 0Fh) are reserved for future use.
11	CT	R/W	1b	**Conversion time field (read or write).** The conversion time field determines the length of the light to digital conversion process. The choices are 100ms and 800ms. A longer integration time allows for a lower noise measurement. The conversion time also relates to the effective resolution of the data conversion process. The 800ms conversion time allows for the fully specified lux resolution. The 100ms conversion time with full-scale ranges above 0101b for E[3:0] in the result and configuration registers also allows for the fully specified lux resolution. The 100ms conversion time with full-scale ranges below and including 0101b for E[3:0] can reduce the effective result resolution by up to three bits, as a function of the selected full-scale range. Range 0101b reduces by one bit. Ranges 0100b, 0011b, 0010b, and 0001b reduces by two bits. Range 0000b reduces by three bits. The result register format and associated LSB weight does not change as a function of the conversion time. 0 = 100ms 1 = 800ms
10:9	M[1:0]	R/W	00b	**Mode of conversion operation field (read or write).** The mode of conversion operation field controls whether the device is operating in continuous conversion, single-shot, or low-power shutdown mode. The default is 00b (shutdown mode), such that upon power-up, the device only consumes operational level power after appropriately programming the device. When single-shot mode is selected by writing 01b to this field, the field continues to read 01b while the device is actively converting. When the single-shot conversion is complete, the mode of conversion operation field is automatically set to 00b and the device is shut down. When the device enters shutdown mode, either by completing a single-shot conversion or by a manual write to the configuration register, there is no change to the state of the reporting flags (conversion ready, flag high, flag low) or the INT pin. These signals are retained for subsequent read operations while the device is in shutdown mode. 00 = Shutdown (default) 01 = Single-shot 10, 11 = Continuous conversions

表 7-5. Configuration Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
8	OVF	R	0b	**Overflow flag field (read-only).** The overflow flag field indicates when an overflow condition occurs in the data conversion process, typically because the light illuminating the device exceeds the programmed full-scale range of the device. Under this condition OVF is set to 1, otherwise OVF remains at 0. The field is reevaluated on every measurement. If the full-scale range is manually set (RN[3:0] field < 1100b), the overflow flag field can be set while the result register reports a value less than full-scale. This result occurs if the input light has a temporary high spike level that temporarily overloads the integrating ADC converter circuitry but returns to a level within range before the conversion is complete. Thus, the overflow flag reports a possible error in the conversion process. This behavior is common to integrating-style converters. If the full-scale range is automatically set (RN[3:0] field = 1100b), the only condition that sets the overflow flag field is if the input light is beyond the full-scale level of the entire device. When there is an overflow condition and the full-scale range is not at maximum, the OPT3001-Q1 device aborts the current conversion, sets the full-scale range to a higher level, and starts a new conversion. The flag is set at the end of the process. This process repeats until there is either no overflow condition or until the full-scale range is set to the maximum range.
7	CRF	R	0b	**Conversion ready field (read-only).** The conversion ready field indicates when a conversion completes. The field is set to 1 at the end of a conversion and is cleared (set to 0) when the configuration register is subsequently read or written with any value except one containing the shutdown mode (mode of operation field, M[1:0] = 00b). Writing a shutdown mode does not affect the state of this field; see the *セクション 6.4.2* section for more details.
6	FH	R	0b	**Flag high field (read-only).** The flag high field (FH) identifies that the result of a conversion is larger than a specified level of interest. FH is set to 1 when the result is larger than the level in the high-limit register (register address 03h) for a consecutive number of measurements defined by the fault count field (FC[1:0]). See the *セクション 6.4.2* section for more details on clearing and other behaviors of this field.
5	FL	R	0b	**Flag low field (read-only).** The flag low field (FL) identifies that the result of a conversion is smaller than a specified level of interest. FL is set to 1 when the result is smaller than the level in the low-limit register (register address 02h) for a consecutive number of measurements defined by the fault count field (FC[1:0]). See the *セクション 6.4.2* section for more details on clearing and other behaviors of this field.
4	L	R/W	1b	**Latch field (read or write).** The latch field controls the functionality of the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL). This bit selects the reporting style between a latched window-style comparison and a transparent hysteresis-style comparison. 0 = The device functions in transparent hysteresis-style comparison operation, where the three interrupt reporting mechanisms directly reflect the comparison of the result register with the high- and low-limit registers with no user-controlled clearing event. See the *セクション 6.3.3* section for further details. 1 = The device functions in latched window-style comparison operation, latching the interrupt reporting mechanisms until a user-controlled clearing event.
3	POL	R/W	0b	**Polarity field (read or write).** The polarity field controls the polarity or active state of the INT pin. 0 = The INT pin reports active low, pulling the pin low upon an interrupt event. 1 = Operation of the INT pin is inverted, where the INT pin reports active high, becoming high impedance and allowing the INT pin to be pulled high upon an interrupt event.
2	ME	R/W	0b	**Mask exponent field (read or write).** The mask exponent field forces the result register exponent field (register 00h, bits E[3:0]) to 0000b when the full-scale range is manually set, which can simplify the processing of the result register when the full-scale range is manually programmed. This behavior occurs when the mask exponent field is set to 1 and the range number field (RN[3:0]) is set to less than 1100b. Note that the masking is only performed to the result register. When using the interrupt reporting mechanisms, the result comparison with the low-limit and high-limit registers is unaffected by the ME field.

表 7-5. Configuration Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1:0	FC[1:0]	R/W	00b	**Fault count field (read or write).** The fault count field instructs the device as to how many consecutive fault events are required to trigger the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL). The fault events are described in the latch field (L), flag high field (FH), and flag low field (FL) descriptions. 00 = One fault count (default) 01 = Two fault counts 10 = Four fault counts 11 = Eight fault counts

7.1.1.3 Low-Limit Register (offset = 02h) [reset = C0000h]

This register sets the lower comparison limit for the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL), as described in the *セクション 6.4.2* section.

図 7-3. Low-Limit Register

15	14	13	12	11	10	9	8
LE3	LE2	LE1	LE0	TL11	TL10	TL9	TL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 7-6. Low-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	LE[3:0]	R/W	0h	**Exponent.** These bits are the exponent bits. 表 7-7 provides further details.
11:0	TL[11:0]	R/W	000h	**Result.** These bits are the result in straight binary coding (zero to full-scale).

The format of this register is nearly identical to the format of the result register described in the Result Register. The low-limit register exponent (LE[3:0]) is similar to the result register exponent (E[3:0]). The low-limit register result (TL[11:0]) is similar to result register result (R[11:0]).

The equation to translate this register into the lux threshold is given in 式 4, which is similar to the equation for the result register, 式 3.

$$\text{lux} = 0.01 \times (2^{\text{LE}[3:0]}) \times \text{TL}[11:0] \quad (4)$$

表 7-7 gives the full-scale range and LSB size as the range and size applies to the low-limit register. The detailed discussion and examples given in for the Result Register apply to the low-limit register as well.

表 7-7. Full-Scale Range and LSB Size as a Function of Exponent Level

LE3	LE2	LE1	LE0	FULL-SCALE RANGE (lux)	LSB SIZE (lux per LSB)
0	0	0	0	40.95	0.01
0	0	0	1	81.90	0.02
0	0	1	0	163.80	0.04
0	0	1	1	327.60	0.08
0	1	0	0	655.20	0.16
0	1	0	1	1310.40	0.32

表 7-7. Full-Scale Range and LSB Size as a Function of Exponent Level (続き)

LE3	LE2	LE1	LE0	FULL-SCALE RANGE (lux)	LSB SIZE (lux per LSB)
0	1	1	0	2620.80	0.64
0	1	1	1	5241.60	1.28
1	0	0	0	10483.20	2.56
1	0	0	1	20966.40	5.12
1	0	1	0	41932.80	10.24
1	0	1	1	83865.60	20.48

注

The result and limit registers are all converted into lux values internally for comparison. These registers can have different exponent fields. However, when using a manually-set full-scale range (configuration register, RN < 0Ch, with mask enable (ME) active), programming the manually-set full-scale range into the LE[3:0] and HE[3:0] fields can simplify the choice of programming the register. This simplification results in the user only having to think about the fractional result and not the exponent part of the result.

7.1.1.4 High-Limit Register (offset = 03h) [reset = BFFFh]

The high-limit register sets the upper comparison limit for the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL), as described in the *セクション 6.3.3* section. The format of this register is almost identical to the format of the low-limit register (described in the Low-Limit Register) and the result register (described in the Result Register). To explain the similarity in more detail, the high-limit register exponent (HE[3:0]) is similar to the low-limit register exponent (LE[3:0]) and the result register exponent (E[3:0]). The high-limit register result (TH[11:0]) is similar to the low-limit result (TH[11:0]) and the result register result (R[11:0]). Note that the comparison of the high-limit register with the result register is unaffected by the ME bit.

When using a manually-set, full-scale range with the mask enable (ME) active, programming the manually-set, full-scale range into the HE[3:0] bits can simplify the choice of values required to program into this register. The formula to translate this register into lux is similar to 式 4. The full-scale values are similar to 表 7-3.

図 7-4. High-Limit Register

15	14	13	12	11	10	9	8
HE3	HE2	HE1	HE0	TH11	TH10	TH9	TH8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 7-8. High-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	HE[3:0]	R/W	Bh	**Exponent.** These bits are the exponent bits.
11:0	TH[11:0]	R/W	FFFh	**Result.** These bits are the result in straight binary coding (zero to full-scale).

7.1.1.5 Manufacturer ID Register (offset = 7Eh) [reset = 5449h]

This register is intended to help uniquely identify the device.

図 7-5. Manufacturer ID Register

15	14	13	12	11	10	9	8
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

表 7-9. Manufacturer ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ID[15:0]	R	5449h	**Manufacturer ID.** The manufacturer ID reads 5449h. In ASCII code, this register reads *TI*.

7.1.1.6 Device ID Register (offset = 7Fh) [reset = 3001h]

This register is also intended to help uniquely identify the device.

図 7-6. Device ID Register

15	14	13	12	11	10	9	8
DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

表 7-10. Device ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DID[15:0]	R	3001h	**Device ID.** The device ID reads 3001h.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

Ambient light sensors are used in a wide variety of applications that require control as a function of ambient light. Because ambient light sensors nominally match the human eye spectral response, these sensors are better than photodiodes when the goal is to create an experience for human beings. Very common applications include display optical-intensity control and industrial or home lighting control.

There are two categories of interface to the OPT3001-Q1 device: electrical and optical.

8.1.1 Electrical Interface

The electrical interface is quite simple, as illustrated in 図 8-1. Connect the OPT3001-Q1 I^2C SDA and SCL pins to the same pins of an applications processor, microcontroller, or other digital processor. If that digital processor requires an interrupt resulting from an event of interest from the OPT3001-Q1 device, then connect the INT pin to either an interrupt or general-purpose I/O pin of the processor. There are multiple uses for this interrupt, including signaling the system to wake up from low-power mode, processing other tasks while waiting for an ambient light event of interest, or alerting the processor that a sample is ready to be read. Connect pullup resistors between a power supply appropriate for digital communication and the SDA and SCL pins (because the resistors have open-drain output structures). If the INT pin is used, connect a pullup resistor to the INT pin. A typical value for these pullup resistors is 10kΩ. The resistor choice can be optimized in conjunction to the bus capacitance to balance the system speed, power, noise immunity, and other requirements.

The power supply and grounding considerations are discussed in the *セクション 8.4* section.

Although spike suppression is integrated in the SDA and SCL pin circuits, use proper layout practices to minimize the amount of coupling into the communication lines. One possible introduction of noise occurs from capacitively coupling signal edges between the two communication lines themselves. Another possible noise introduction comes from other switching noise sources present in the system, especially for long communication lines. In noisy environments, shield communication lines to reduce the possibility of unintended noise coupling into the digital I/O lines that can be incorrectly interpreted.

8.1.2 Optical Interface

The optical interface is physically located within the package, facing away from the PCB, as specified by the *Sensor Area* in セクション 11.

Physical components, such as a plastic housing and a window that allows light from outside of the design to illuminate the sensor (see 図 8-2), can help protect the OPT3001-Q1 device and neighboring circuitry. Sometimes, a dark or opaque window is used to further enhance the visual appeal of the design by hiding the sensor from view. This window material is typically transparent plastic or glass.

Any physical component that affects the light that illuminates the sensing area of a light sensor also affects the performance of that light sensor. Therefore, for optimal performance, make sure to understand and control the effect of these components. Design a window width and height to permit light from a sufficient field of view to illuminate the sensor. For best performance, use a field of view of at least ±35°, or ideally ±45° or more. Understanding and designing the field of view is discussed further in the *OPT3001: Ambient Light Sensor Application Guide* application note.

The visible-spectrum transmission for dark windows typically ranges between 5% to 30%, but can be less than 1%. Specify a visible-spectrum transmission as low as, but no more than, necessary to achieve sufficient visual appeal because decreased transmission decreases the available light for the sensor to measure. The windows

are made dark by either applying an ink to a transparent window material, or including a dye or other optical substance within the window material. This attenuating transmission in the visible spectrum of the window creates a ratio between the light on the outside of the design and the light that is measured by the OPT3001-Q1 device. To accurately measure the light outside of the design, compensate the OPT3001-Q1 measurement for this ratio; an example is given in *セクション 8.2.2.2*.

Ambient light sensors are used to help create ideal lighting experiences for humans; therefore, the matching of the sensor spectral response to that of the human eye response is vital. Infrared light is not visible to the human eye, and can interfere with the measurement of visible light when sensors lack infrared rejection. Therefore, the ratio of visible light to interfering infrared light affects the accuracy of any practical system that represents the human eye. The strong rejection of infrared light by the OPT3001-Q1 device allows measurements consistent with human perception under high-infrared lighting conditions, such as from incandescent, halogen, or sunlight sources.

Although the inks and dyes of dark windows serve the primary purpose of being minimally transmissive to visible light, some inks and dyes can also be very transmissive to infrared light. The use of these inks and dyes further decreases the ratio of visible to infrared light, and thus decreases sensor measurement accuracy. However, because of the excellent infrared rejection of the OPT3001-Q1 device, this effect is minimized, and good results are achieved under a dark window with similar spectral responses to those shown in 図 8-3.

For best accuracy, avoid grill-like window structures, unless the designer understands the optical effects sufficiently. These grill-like window structures create a nonuniform illumination pattern at the sensor that make light measurement results vary with placement tolerances and angle of incidence of the light. If a grill-like structure is desired, the OPT3001-Q1 device is an excellent sensor choice because the device is minimally sensitive to illumination uniformity issues disrupting the measurement process.

Light pipes can appear attractive for aiding in the optomechanical design that brings light to the sensor; however, do not use light pipes with any ambient light sensor unless the system designer fully understands the ramifications of the optical physics of light pipes within the full context of his design and objectives.

8.2 Typical Application

Measuring the ambient light with the OPT3001-Q1 device in a product case and under a dark window is described in this section. The schematic for this design is shown in 図 8-1.

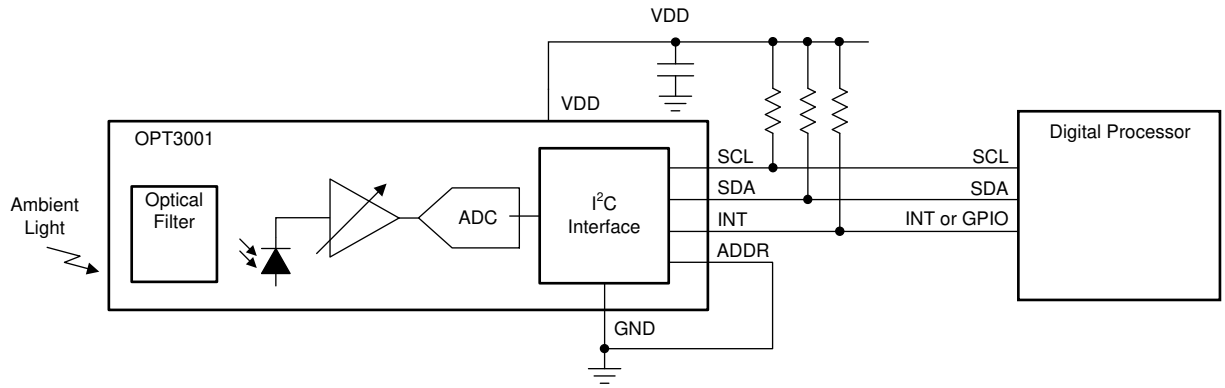


図 8-1. Measuring Ambient Light in a Product Case Behind a Dark Window

8.2.1 Design Requirements

The basic requirements of this design are:

- Sensor is hidden under dark glass so that sensor is not obviously visible. Note that this requirement is subjective to designer preference.
- Accuracy of measurement of fluorescent light is 15%
- Variation in measurement between fluorescent, halogen, and incandescent bulbs (also known as light source variation) is as small as possible.

8.2.2 Detailed Design Procedure

8.2.2.1 Optomechanical Design

After completing the electrical design, the next task is the optomechanical design. Design a product case that includes a window to transmit the light from outside the product to the sensor, as shown in 図 8-2. Design the window width and window height to give a ±45° field of view. A rigorous design of the field of view takes into account the location of the sensor area, as shown in セクション 11. The OPT3001-Q1 active sensor area is centered along one axis of the package top view, but has a minor offset on the other axis of the top view. Window sizing and placement is discussed in more rigorous detail in the *OPT3001: Ambient Light Sensor Application Guide* application note.

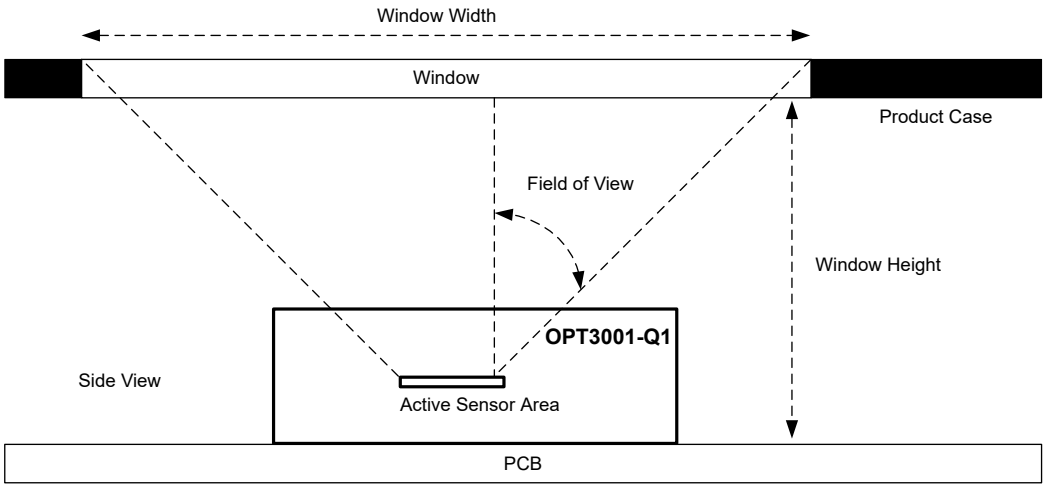


図 8-2. Product Case and Window Over the OPT3001-Q1 Device

8.2.2.2 Dark Window Selection and Compensation

There are several approaches to selecting and compensating for a dark window. One of many approaches is the method described in this section.

Sample several different windows with various levels of darkness. Choose a window that is dark enough to optimize the balance between the aesthetics of the device and sensor performance. Note that the aesthetic evaluation is the subjective opinion of the designer; observing the window on the physical design is preferred over referring to the window transmission specifications. Verify that the selected window is not darker than absolutely necessary because a darker window allows less light to illuminate the sensor and therefore impedes sensor accuracy.

The window chosen for this application example is dark and has less than 7% transmission at 550nm. 図 8-3 shows the normalized response of the spectrum. Note that the equipment used to measure the transmission spectrum is not capable of measuring the absolute accuracy (non-normalized) of the dark window sample, but only the relative normalized spectrum. Also note that the window is much more transmissive to infrared

wavelengths longer than 700nm than to visible wavelengths between 400nm and 650nm. This imbalance between infrared and visible light decreases the ratio of visible light to infrared light at the sensor. Although having the window decrease this ratio as little as possible (by having a window with a close ratio of visible transmission to infrared transmission) is preferred, the OPT3001-Q1 device still performs well as shown in 図 8-6.

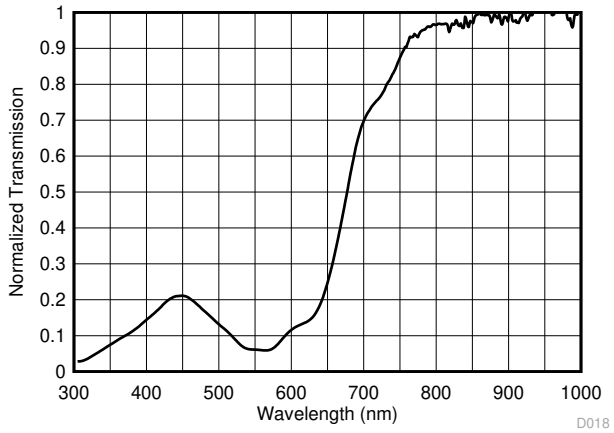


図 8-3. Normalized Transmission Spectral Response of the Chosen Dark Window

After choosing the dark window, measure the attenuating effect of the dark window for later compensation. To measure this attenuation, measure a fluorescent light source with a lux meter, then measure that same light with the OPT3001-Q1 device under the dark window. To measure accurately, use a fixture that can accommodate either the lux meter or the design containing the OPT3001-Q1 device and dark window, with the center of each of the sensing areas being in exactly the same *X, Y, Z* location, as shown in 図 8-4. The *Z* placement of the design (distance from the light source) is the top of the window, and not the OPT3001-Q1 device.

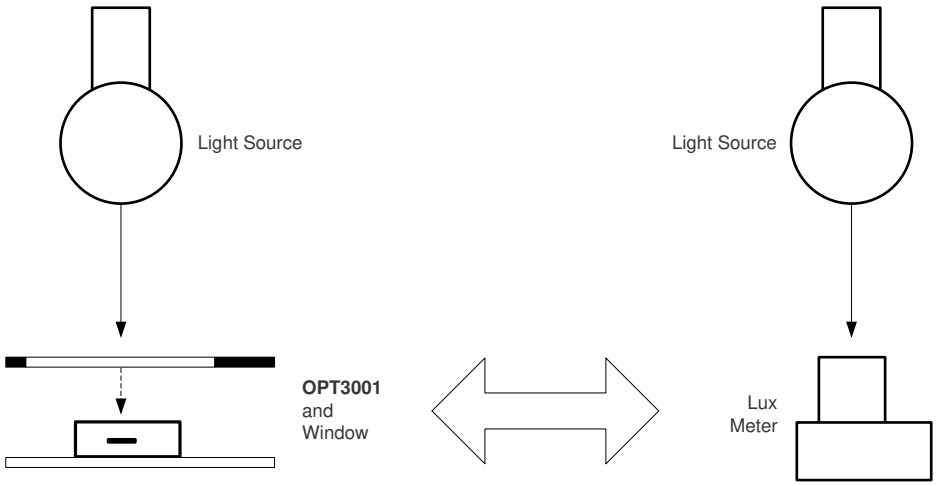


図 8-4. Fixture With One Light Source Accommodating Either a Lux Meter or the Design (Window and OPT3001-Q1 Device) in the Exact Same X,Y,Z Position

The fluorescent light in this location measures 1000lux with the lux meter, and 73lux with the OPT3001-Q1 device under the dark window within the application. Therefore, the window has an effective transmission of 7.3% for the fluorescent light. This 7.3% is the weighted average attenuation across the entire spectrum, weighted by the spectral response of the lux meter (or photopic response).

For all subsequent OPT3001-Q1 measurements under this dark window, the following formula is applied.

Compensated Measurement = Uncompensated Measurement / (7.3%) (5)

8.2.3 Application Curves

To validate that the design example now measures correctly, create a sequential number of different light intensities with the fluorescent light by using neutral density filters to attenuate the light. Different light intensities can also be created by changing the distance between the light source, and the measurement devices. However, these two methods for changing the light level have minor accuracy tradeoffs that are beyond the scope of this discussion. Measure each intensity with both the lux meter and the OPT3001-Q1 device under the window, and compensate using 式 5. The results are displayed in 図 8-5, and show that the application accurately reports results very similar to the lux meter.

To validate that the design measures a variety of light sources correctly, despite the large ratio of infrared transmission to visible light transmission of the window, measure the application with a halogen bulb and an incandescent bulb. Use the physical location and light attenuation procedures that were used for the fluorescent light. The results are shown in 図 8-6.

The addition of the dark window changes the results as seen by comparing the results of the same measurement with a window (図 8-6) and without a window (図 5-3). Even after the expected change, the performance is still good. All data are both within 15% of the correct answer, and within 15% of the other bulb measurements.

Results can vary at different angles of light because the OPT3001-Q1 device does not match the lux meter at all angles of light.

If the measurement variation between the light sources is not acceptable, choose a different window that has a closer ratio of visible light transmission to infrared light transmission.

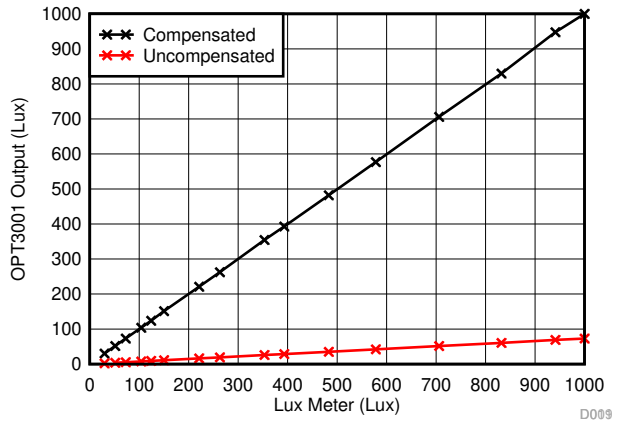


図 8-5. Uncompensated and Compensated Output of the OPT3001-Q1 Grade 3 Device Under a Dark Window Illuminated by Fluorescent Light Source

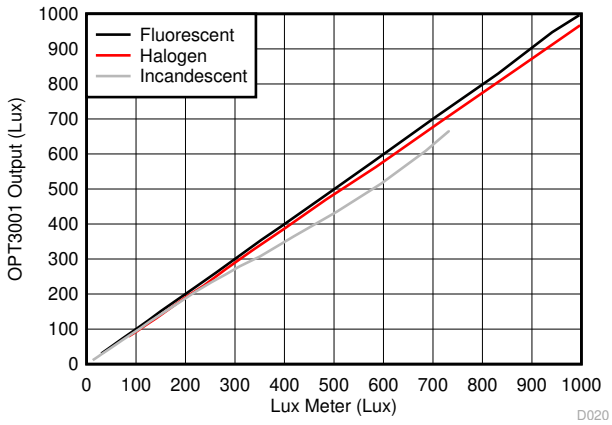


図 8-6. Compensated Output of the OPT3001-Q1 Grade 3 Device Under a Dark Window Illuminated by Fluorescent, Halogen, and Incandescent Light Sources

8.3 Best Design Practices

As with any optical product, special care must be taken into consideration when handling the OPT3001-Q1 device. Although the OPT3001-Q1 device has low sensitivity to dust and scratches, proper optical device handling procedures are still recommended.

The optical surface of the device must be kept clean for optimal performance in both prototyping with the device and mass production manufacturing procedures. Tweezers with plastic or rubber contact surfaces are recommended to avoid scratches on the optical surface. Avoid manipulation with metal tools when possible. The optical surface must be kept clean of fingerprints, dust, and other optical-inhibiting contaminants.

If the device optical surface requires cleaning, the use of de-ionized water or isopropyl alcohol is recommended. A few gentile brushes with a soft swab are appropriate. Avoid potentially abrasive cleaning and manipulating tools and excessive force that can scratch the optical surface.

If the OPT3001-Q1 device performs less than optimally, inspect the optical surface for dirt, scratches, or other optical artifacts.

8.4 Power Supply Recommendations

Although the OPT3001-Q1 device has low sensitivity to power-supply issues, good practices are always recommended. For best performance, the OPT3001-Q1 V_{DD} pin must have a stable, low-noise power supply with a 100nF bypass capacitor close to the device and solid grounding. There are many options for powering the OPT3001-Q1 device, because the device current consumption levels are very low.

8.5 Layout

8.5.1 Layout Guidelines

The PCB layout design for the OPT3001-Q1 device requires a couple of considerations. Bypass the power supply with a capacitor placed close to the OPT3001-Q1 device. Note that optically reflective surfaces of components also affect the performance of the design. The three-dimensional geometry of all components and structures around the sensor must be taken into consideration to prevent unexpected results from secondary optical reflections. Placing capacitors and components at a distance of at least twice the height of the component is typically sufficient. The most optimal optical layout is to place all close components on the opposite side of the PCB from the OPT3001-Q1 device. However, this approach is not practical for the constraints of every design.

Electrically connecting the thermal pad to ground is recommended. This connection can be created either with a PCB trace or with vias to ground directly on the thermal pad. If the thermal pad contains vias, the vias are recommended to be of a small diameter (< 0.2mm) to prevent the vias from wicking the solder away from the appropriate surfaces.

An example PCB layout with the OPT3001-Q1 device is shown in 図 8-7.

8.5.2 Layout Example

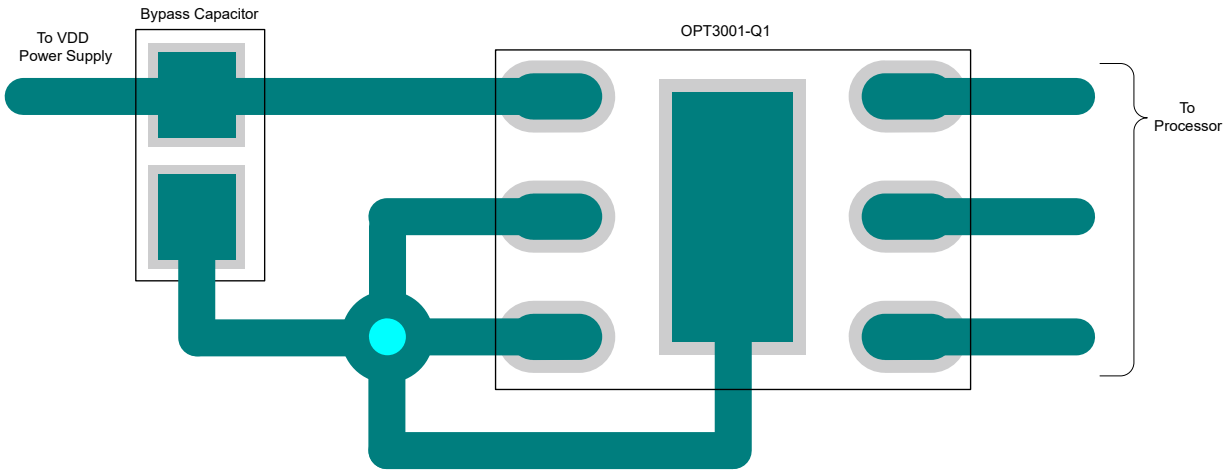


図 8-7. OPT3001-Q1 USON Layout Example

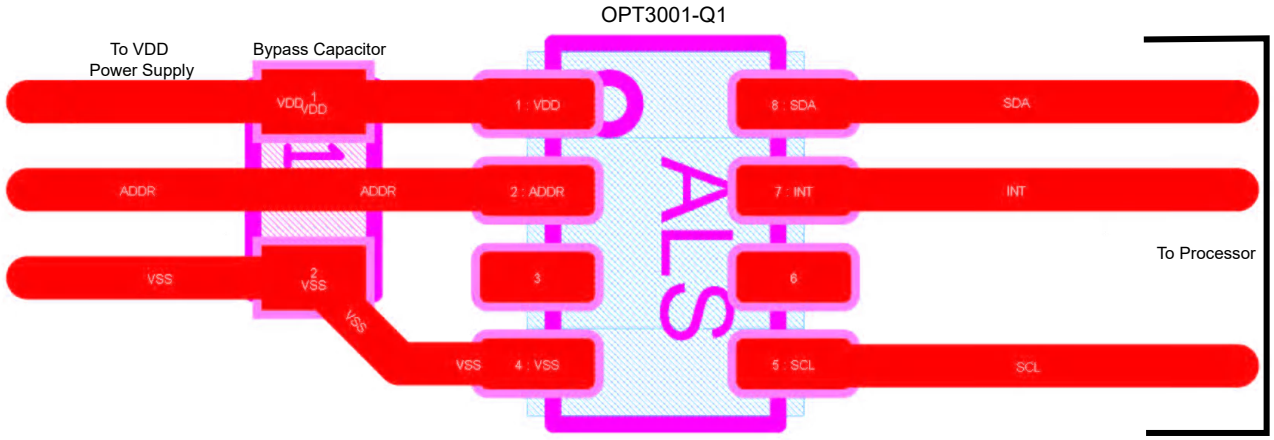


図 8-8. OPT3001-Q1 SOT-5X3 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPT3001: Ambient Light Sensor Application Guide*, application note
- Texas Instruments, *OPT3001EVM User's Guide*
- Texas Instruments, *QFN/SON PCB Attachment*, application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2018) to Revision B (December 2024)	Page
• SOT-5X3 バリアントの動作温度とパッケージ サイズを追加	1
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	2
• Added missing link to *Electrical Interface* section in *Serial Interface* section	15
• Added application information to *セクション 8* section	29

Changes from Revision * (March 2017) to Revision A (December 2018)	Page
• 以下を追加。デバイス温度グレード 2：-40℃～105℃の動作時周囲温度範囲	1
• 以下を追加。デバイス温度グレード 3：-40℃～85℃の動作時周囲温度範囲	1
• 以下を追加。動作時温度範囲 (グレード 2)：-40℃～105℃	1
• Added *Dark Response vs Temperature (Grade 2)*	9
• Added *Normalized Response vs Temperature (Grade 2)*	9
• Added *Supply Current vs Temperature (Grade 2)*	9
• Added *Shutdown Current vs Temperature (Grade 2)*	9

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

11.1 Soldering and Handling Recommendations

The OPT3001-Q1 device has been qualified for three soldering reflow operations per JEDEC JSTD-020.

Note that excessive heat can discolor the device and affect optical performance.

See application report *QFN/SON PCB Attachment* (SLUA271), for details on soldering thermal profile and other information. If the OPT3001-Q1 device must be removed from a PCB, discard the device and do not reattach.

As with most optical devices, handle the OPT3001-Q1 device with special care to verify that optical surfaces stay clean and free from damage. See the *Do's and Don'ts* section for more detailed recommendations. For best optical performance, solder flux and any other possible debris must be cleaned after soldering processes.

11.2 DNP (S-PDSO-N6) Mechanical Drawings

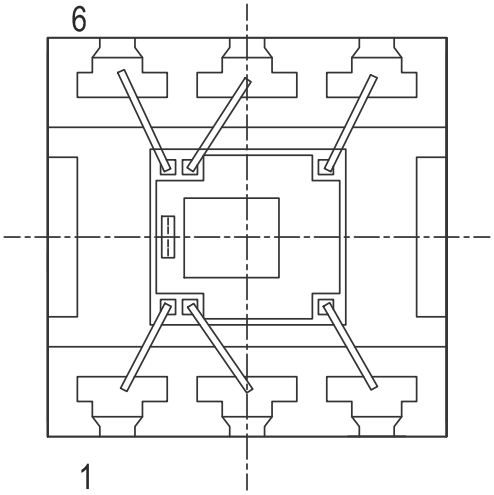


図 11-1. Package Orientation Visual Reference of Pin 1 (Top View)

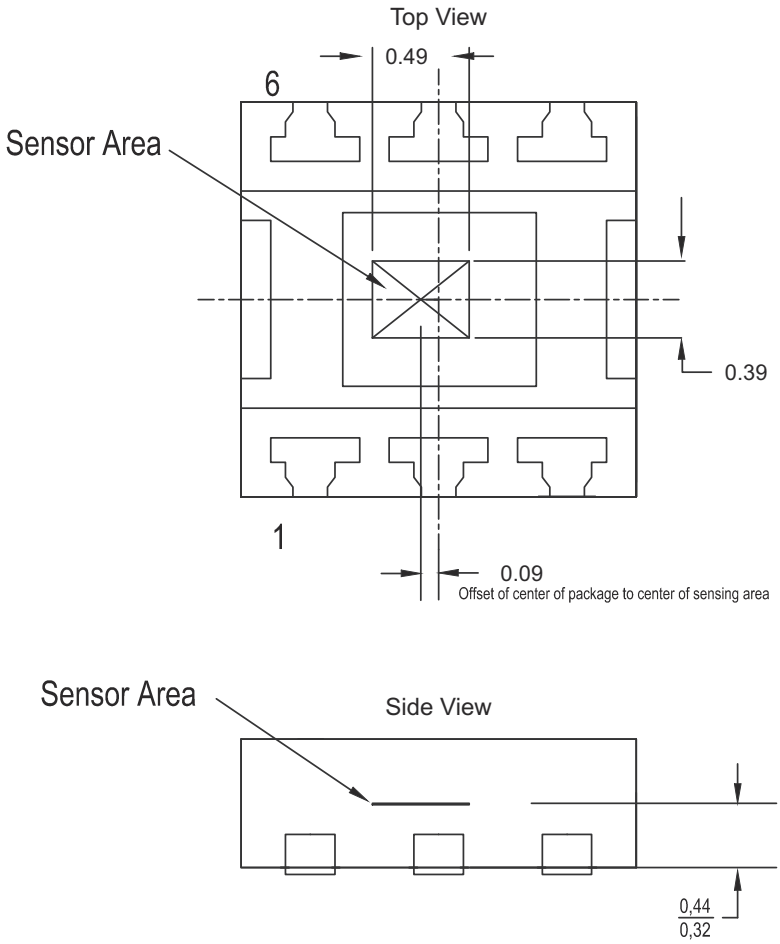


図 11-2. Mechanical Outline Showing Sensing Area Location (Top and Side Views)

11.3 DTS (SOT-5X3) Mechanical Drawings

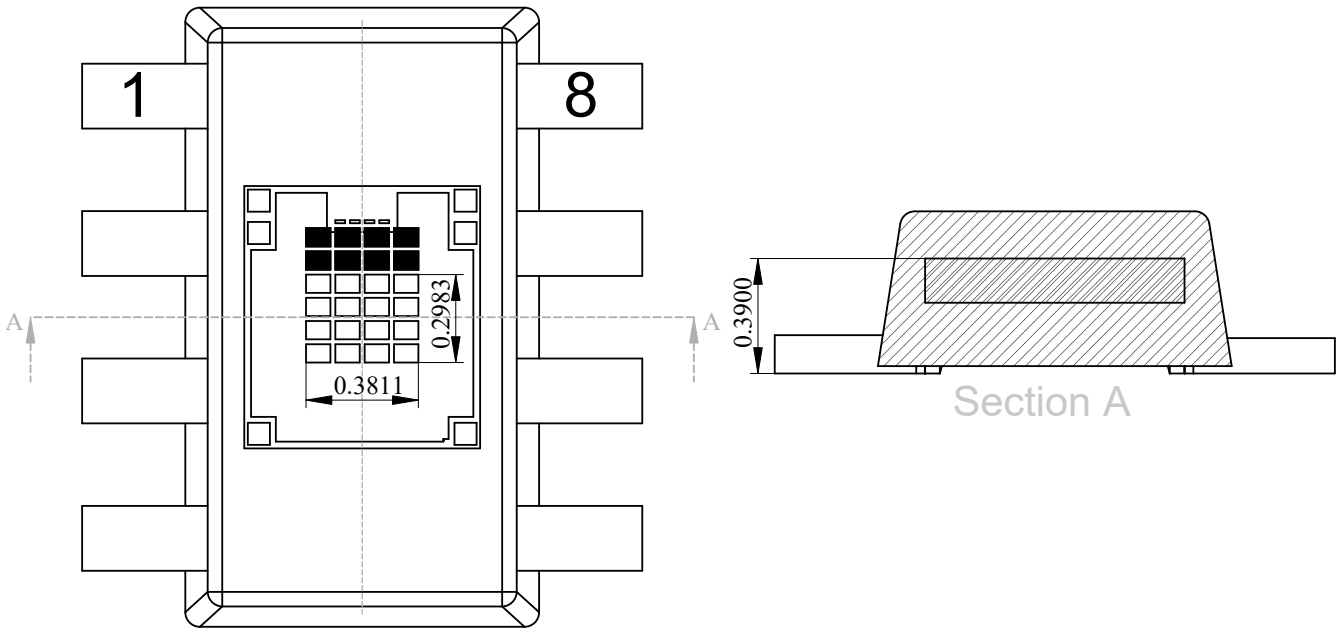


図 11-3. Package Orientation Visual Reference of Pin 1 (Top View) & Sectional View

Identifying DTS Package Orientation Using Automated Optical Inspection (AOI) Systems

Automated optical inspection (AOI) systems are used in the PCB assembly process to identify the device orientation during device placement. Typically, on non-optical packages, the pin 1 marker is a white dot or indentation on the black package. This is used by the AOI system to orient the package. Light sensor ICs such as the OPT3001-Q1 use a transparent package to allow light to enter the package and reach the sensor. This section provides instruction for determining orientation on the DTS package. The same approach can also be applied to the DNP package. The following figures show how the package can be oriented from the bottom and top side. On the bottom side the DTS package has a pin 1 chamfer. On the top side there are four features that can be used to orient the device.

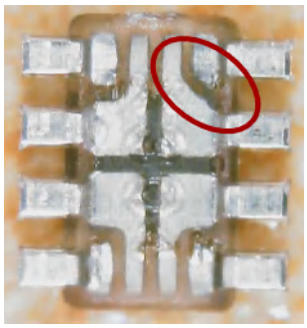
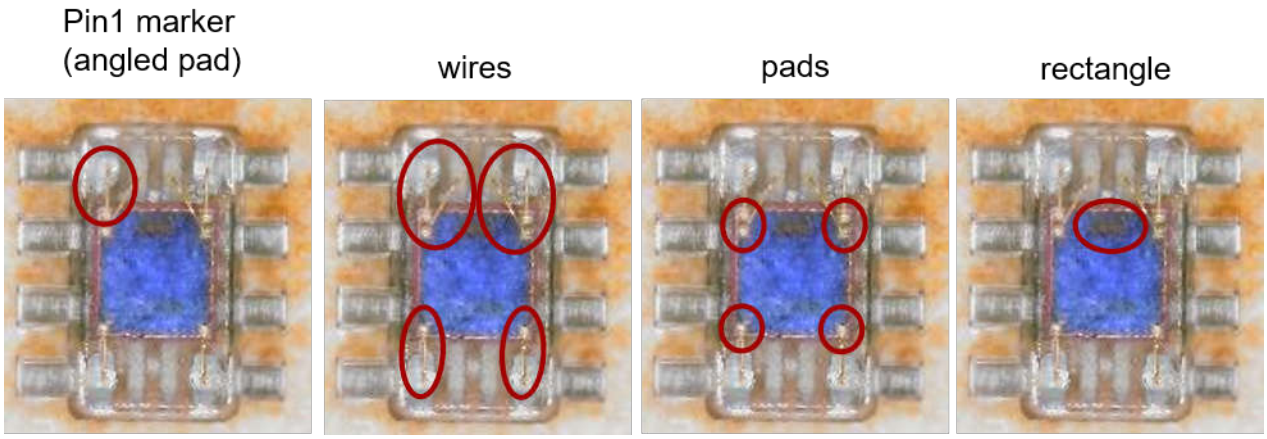


図 11-4. Identifying DTS Package Orientation - Backside



1. The pin 1 chamfer can be seen through the package.
2. The bond wires and bond pads on the die can also be used.
3. The asymmetry in either wires or pads (4 at the top and 2 at the bottom) can be used to orient the device.
4. The rectangular feature on the die indicates orientation.

図 11-5. Identifying DTS Package Orientation - Topside

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPT3001DNPRQ1	Active	Production	USON (DNP) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	ED
OPT3001DNPRQ1.A	Active	Production	USON (DNP) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	ED
OPT3001DNPRQ1.B	Active	Production	USON (DNP) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	ED
OPT3001IDNPRQ1	Active	Production	USON (DNP) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	ED
OPT3001IDNPRQ1.A	Active	Production	USON (DNP) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	ED
OPT3001IDNPRQ1.B	Active	Production	USON (DNP) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	ED
OPT3001IDNPTQ1	Obsolete	Production	USON (DNP) | 6	-	-	Call TI	Call TI	-40 to 85	ED

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPT3001-Q1 :

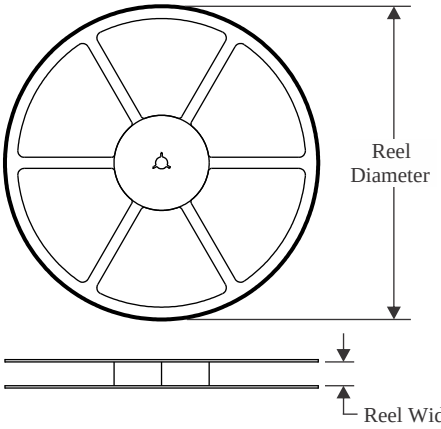
- Catalog : OPT3001

NOTE: Qualified Version Definitions:

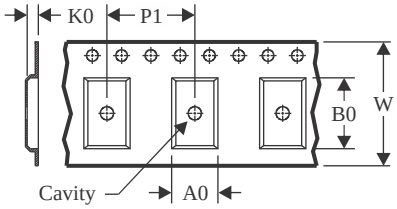
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

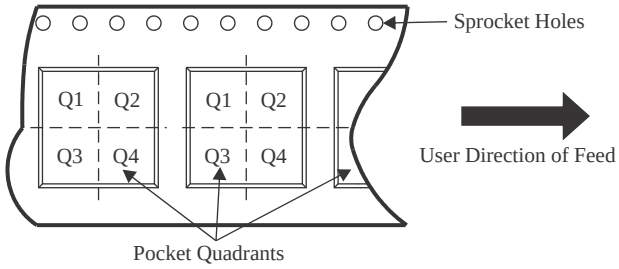


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

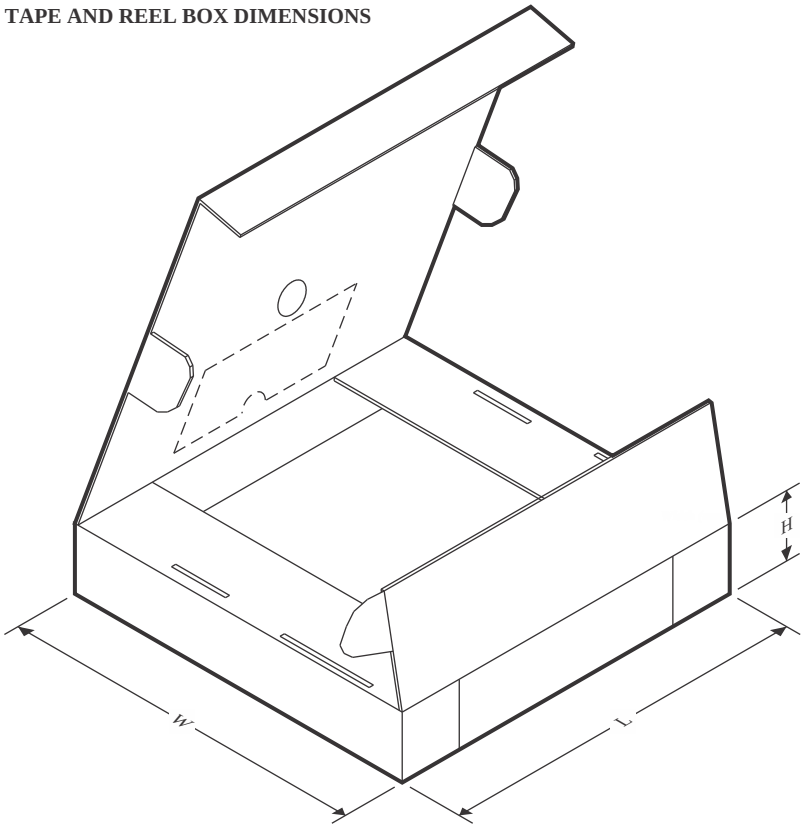
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPT3001DNPRQ1	USON	DNP	6	3000	330.0	12.4	2.3	2.3	0.9	8.0	12.0	Q1
OPT3001IDNPRQ1	USON	DNP	6	3000	330.0	12.4	2.3	2.3	0.9	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

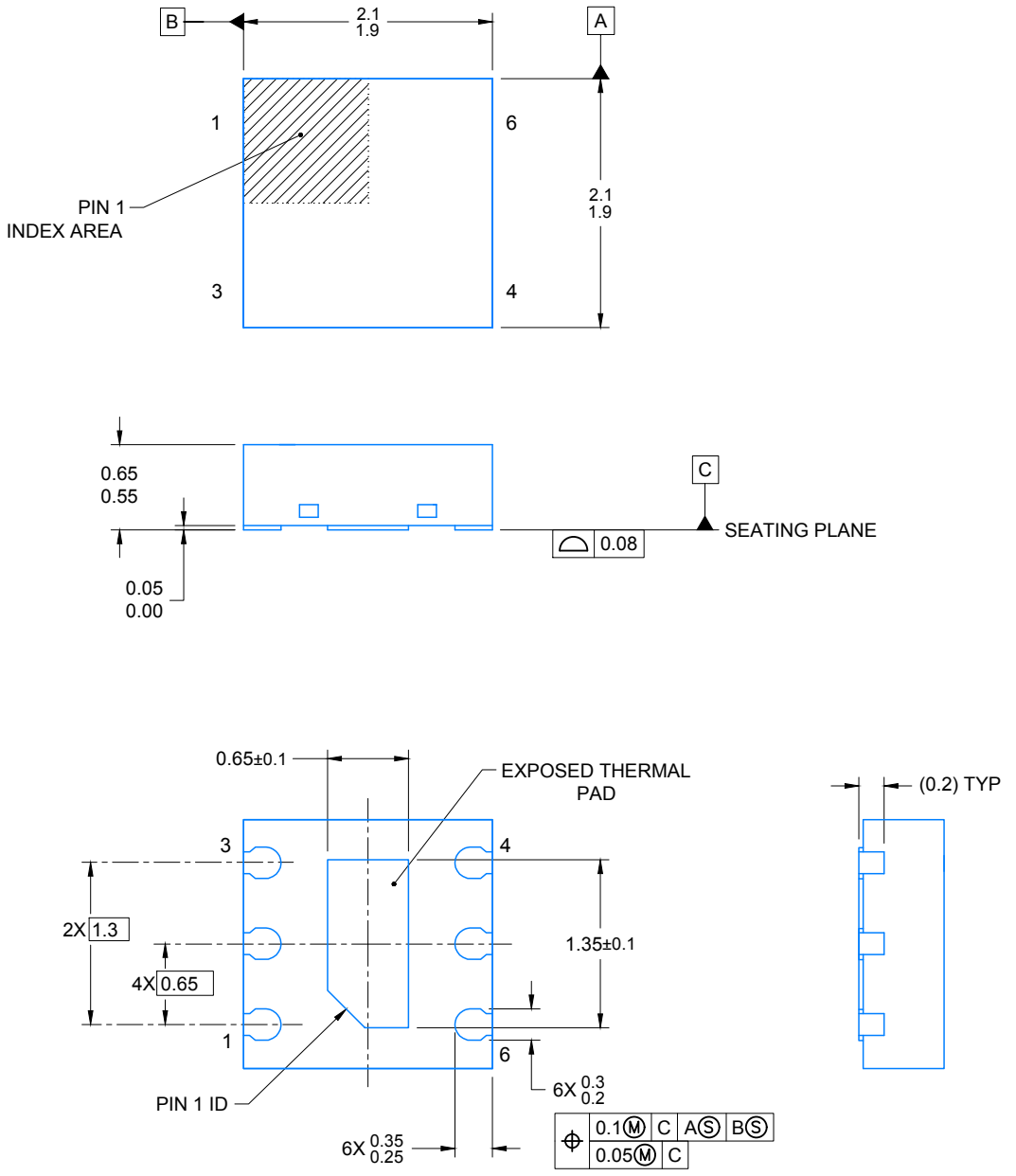
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPT3001DNPRQ1	USON	DNP	6	3000	356.0	338.0	48.0
OPT3001IDNPRQ1	USON	DNP	6	3000	356.0	338.0	48.0

PACKAGE OUTLINE

DNP0006A

USON - 0.65 mm mm max height

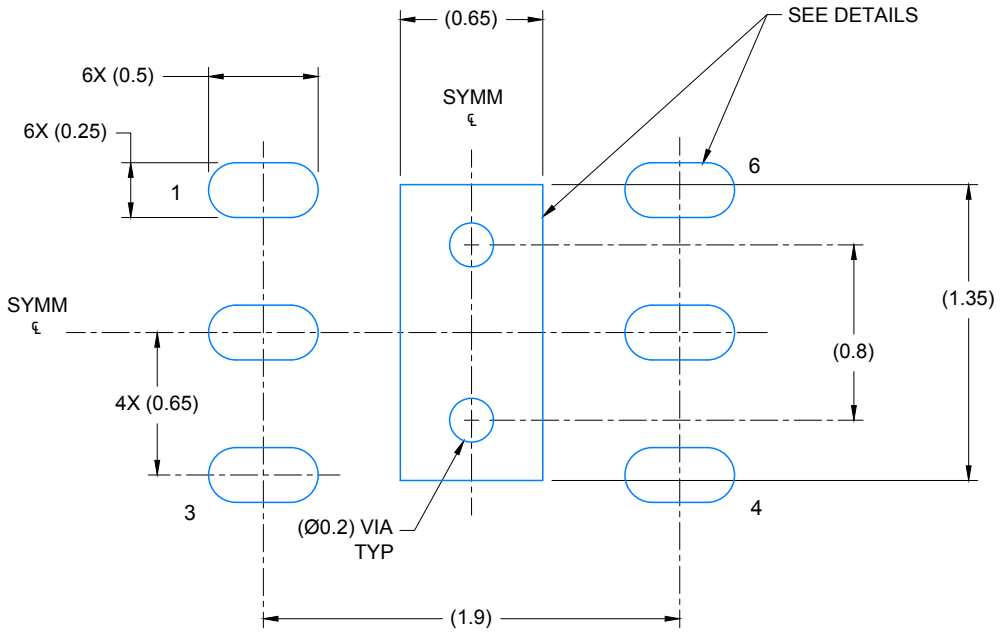
PLASTIC SMALL OUTLINE NO-LEAD



4221434/C 01/2018

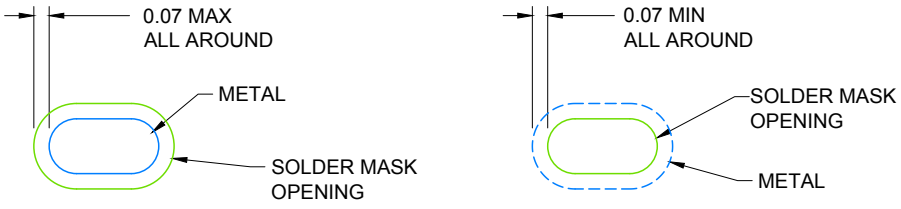
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Optical package with clear mold compound.



LAND PATTERN EXAMPLE

SCALE: 30X



NON SOLDER MASK DEFINED (PREFERRED)

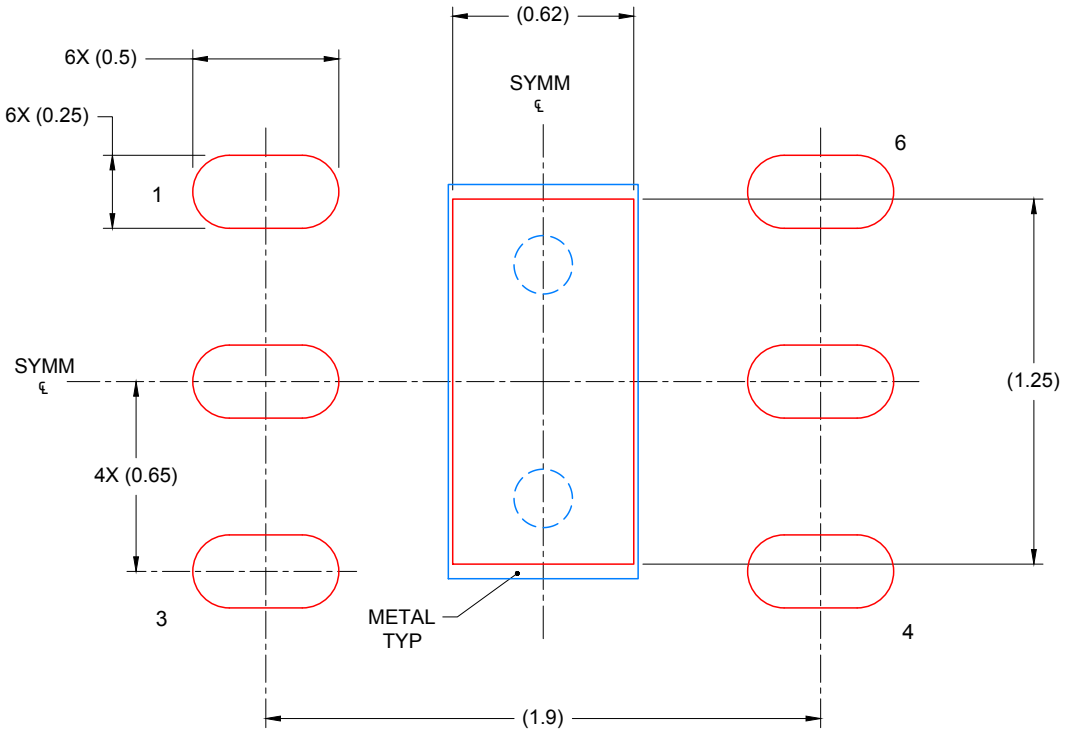
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221434/C 01/2018

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 40X

4221434/C 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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