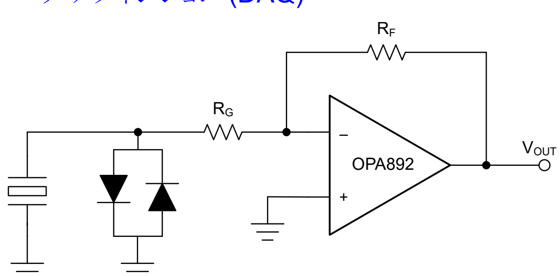
OPAx892 2GHz、10V/V ゲイン安定、0.95nV/√Hz、超低 THD オペアンプ

1 特長

- 0.95nV/√Hz の非常に低い電圧ノイズ
- 高速度:
  - ゲイン帯域幅積:2GHz
  - スルー レート:700V/µs
  - 30ns のセトリング タイム (0.1%)
- 10V/V 以上のゲインで安定
- 出力駆動、I_O = 200mA (標準値)
- 非常に低い歪み:
  - THD = -78dBc (f = 1MHz、R_L = 150Ω)
  - THD+N = –114dBc (f = 1kHz、BW = 80kHz)
- 広範な電源:
  - V_{CC} = ±4.5V～±18V
- OPA892 のオフセット ヌル ピン

2 アプリケーション

- 超音波スキャナ
- ソース メジャー ユニット (SMU)
- 電力品質メータ
- 超音波スキャナ
- ベクトル信号トランシーバ (VST)
- 業務用オーディオ ミキサまたは制御卓
- 業務用マイク / ワイヤレス システム
- 業務用スピーカ システム
- 業務用オーディオ アンプ
- サウンドバー
- ターンテーブル
- 業務用ビデオ カメラ
- ギターおよびその他楽器用アンプ
- データ アクイジション (DAQ)



低歪み圧電センサ アンプ

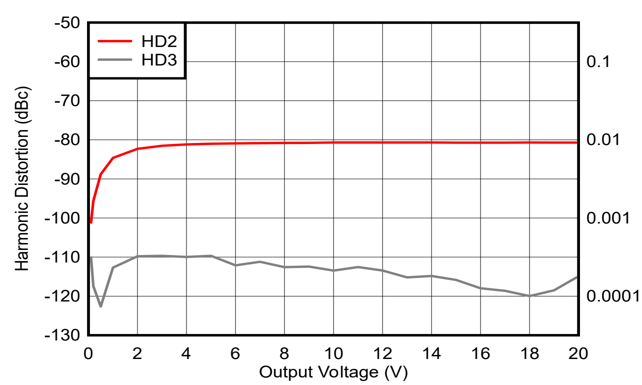
3 概要

OPA892 および OPA2892 (OPAx892) は電圧ノイズが非常に低い高速電圧帰還アンプで、通信やイメージングなど低い電圧ノイズが要求されるアプリケーションに最適です。シングルアンプの OPA892 とデュアルアンプの OPA2892 は AC 性能が非常に優れており、10V/V のゲインで 290MHz の帯域幅、700V/µs のスルーレート、30ns のセトリング タイム (0.1%) を実現します。OPAx892 は、10 以上および –9 以下のゲインで安定しています。これらのアンプには、200mA の大きな駆動能力があり、アンプごとに 7.5mA の電流しか消費しません。f = 1MHz において全高調波歪み (THD) が -68dBc である OPAx892 は、低歪みを必要とするアプリケーション用に設計されています。広い出力電圧範囲にわたって低歪みを維持するため、OPAx892 はイメージング、ソナー、オーディオなどの広いダイナミック レンジのアプリケーションに有用です。

製品情報

部品番号	アンプ	パッケージ (1)	パッケージ サイズ (2)
OPA892	1	D (SOIC、8)	4.9mm × 6mm
OPA2892	2	DGN (HVSSOP、8)	3mm × 4.9mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



V_{CC} = ±15V、R_L = 150Ω、f = 1MHz

高調波歪みと ピーク ツー ピークの出力電圧との関係

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4 Pin Configuration and Functions

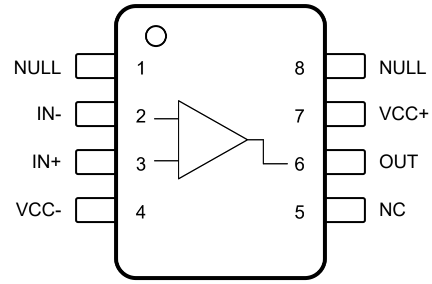


図 4-1. OPA892: D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions: OPA892

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN–	2	Input	Inverting input
IN+	3	Input	Noninverting input
NC	5	—	No connection
NULL	1, 8	Input	Voltage offset adjust
OUT	6	Output	Output of amplifier
VCC–	4	—	Negative power supply
VCC+	7	—	Positive power supply

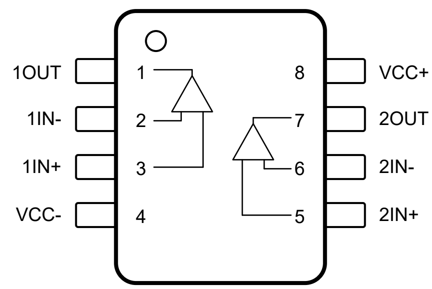


図 4-2. OPA2892: DGN Package, 8-pin HVSSOP (Top View)

表 4-2. Pin Functions: OPA2892

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	2	Input	Channel 1 inverting input
1IN+	3	Input	Channel 1 noninverting input
1OUT	1	Output	Channel 1 output
2IN–	6	Input	Channel 2 inverting input
2IN+	5	Input	Channel 2 noninverting input
2OUT	7	Output	Channel 2 output
VCC–	4	—	Negative power supply
VCC+	8	—	Positive power supply
Thermal pad		—	Thermal pad. DGN (HVSSOP) package only. For best thermal performance, connect pad to large copper plane. Thermal pad can be connected to any pin on the device, or any other potential on the board if voltage on thermal pad remains between VCC+ and VCC–.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage, $V_{CC+} - V_{CC-}$			37	V
V_I	Input voltage			$\pm V_{CC}$	V
I_O	Output current[2]			240	mA
V_{IO}	Differential input voltage			±1.5	V
I_{IN}	Continuous input current			10	mA
T_J	Junction temperature	Any condition		150	°C
		Continuous operation, long-term reliability[3]		125	
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) When continuously operating at any output current, do not exceed the maximum junction temperature. Keep the output current less than the absolute maximum rating regardless of time interval.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation greater than this temperature can result in reduced reliability, lifetime of the device, or both.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Dual-supply	±4.5	±15	±18	V
		Single-supply	9	30	36	
T_A	Operating free-air temperature		–40	25	85	°C

5.4 Thermal Information

THERMAL METRIC[1]		OPA892	OPA2892	UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	52	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.0	75.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	24.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.6	4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.4	24.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.1	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C, V_{CC} = ±15 V, and R_L = 150 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB)	Gain = 10	V_{CC} = ±15 V		290		MHz
			V_{CC} = ±5 V		250		
		Gain = 20	V_{CC} = ±15 V		110		
			V_{CC} = ±5 V		100		
	Bandwidth for 0.1-dB flatness	Gain = 10	V_{CC} = ±15 V		17		
			V_{CC} = ±5 V		17		
	Full power bandwidth[(1)]	$V_{O(PP)}$ = 20 V, V_{CC} = ±15 V			11.1		
		$V_{O(PP)}$ = 5 V, V_{CC} = ±5 V			31.8		
SR	Slew rate[(2)]	Gain = 10	V_{CC} = ±15 V, 20-V step		700		V/µs
			V_{CC} = ±5 V, 5-V step		500		
t_s	Settling time to 0.1%	Gain = –10	V_{CC} = ±15 V, 5-V step		22		ns
			V_{CC} = ±5 V, 2-V step		22		
	Settling time to 0.01%	Gain = –10	V_{CC} = ±15 V, 5-V step		160		
			V_{CC} = ±5 V, 2-V step		160		
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	Gain = 10, f = 1 kHz, BW = 80 kHz	V_{CC} = ±15 V, R_L = 600 Ω, V_O = 3 V_{RMS}		–114		dB
					0.0002		%
			V_{CC} = ±15 V, R_L = 2 kΩ, V_O = 3 V_{RMS}		–114		dB
					0.0002		%
			V_{CC} = ±5 V, R_L = 600 Ω, V_O = 1 V_{RMS}		–106		dB
					0.0005		%
			V_{CC} = ±5 V, R_L = 2 kΩ, V_O = 1 V_{RMS}		–106		dB
					0.0005		%
IMD	Intermodulation distortion	Gain = 10, SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)	V_{CC} = ±15 V, V_O = 3 V_{RMS}, R_L = 600 Ω		–109		dB
					0.00036		%
			V_{CC} = ±15 V, V_O = 3 V_{RMS}, R_L = 2 kΩ		–109		dB
					0.00036		%
			V_{CC} = ±5 V, V_O = 1 V_{RMS}, R_L = 600 Ω		–105		dB
					0.00056		%
			V_{CC} = ±5 V, V_O = 1 V_{RMS}, R_L = 2 kΩ		–105		dB
					0.00056		%
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, gain = 10, V_{CC} = ±15 V			–78		dBc
			R_L = 1 kΩ		–86		
		$V_{O(pp)}$ = 2 V, f = 1 MHz, gain = 10, V_{CC} = ±5 V			–77		
			R_L = 1 kΩ		–85		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V, f > 10 kHz			0.95		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V, f > 10 kHz			2.3		pA/√Hz
X_T	Channel-to-channel crosstalk (OPA2892 only)	V_{CC} = ±5 V or ±15 V, f = 1 MHz			–54		dBc

5.5 Electrical Characteristics (続き)

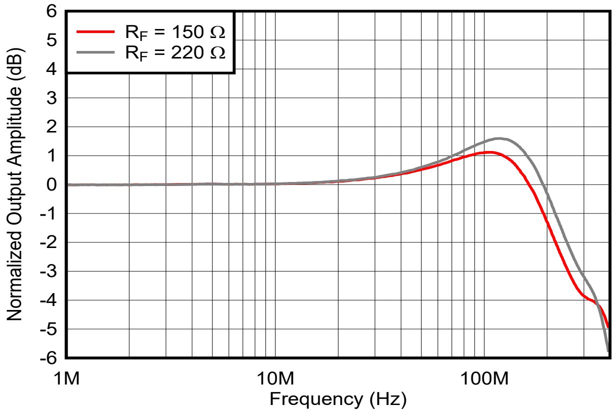
at T_A = 25°C, V_{CC} = ±15 V, and R_L = 150 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC PERFORMANCE							
	Open-loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	93	100		dB
			T_A = full range	92			dB
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ	T_A = 25°C	92	98		dB
			T_A = full range	91			dB
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V, T_A = 25°C			0.2	1	mV
	Offset voltage drift	V_{CC} = ±5 V or ±15 V, T_A = full range			1		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		9	20	µA
			T_A = full range			33	µA
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	250	nA
			T_A = full range			400	nA
	Input offset current drift	V_{CC} = ±5 V or ±15 V, T_A = full range			0.2		nA/°C
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage	V_{CC} = ±15 V		±13.8	±14.3		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15 V, V_{ICR} = ±12 V	T_A = 25 °C	85	104		dB
			T_A = full range	80			
		V_{CC} = ±5 V, V_{ICR} = ±2.5 V	T_A = 25 °C	90	106		
			T_A = full range	85			
	Input impedance	Common-mode			10 || 1.2		MΩ || pF
		Differential-mode			6 ||1.8		kΩ || pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±15 V, R_L = 250 Ω		±12	±12.9		V
		V_{CC} = ±5 V, R_L = 150 Ω		±3	±3.5		
		V_{CC} = ±15 V, R_L = 1 kΩ		±13	±13.6		
		V_{CC} = ±5 V, R_L = 1 kΩ		±3.4	±3.8		
I_O	Output current	R_L = 10 Ω	V_{CC} = ±15 V	160	200		mA
			V_{CC} = ±5 V	120	160		
R_O	Output resistance(3)	Open-loop			8		Ω
POWER SUPPLY							
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		7.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C			9	
			T_A = full range		6.5	10	
PSRR	Power-supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25 °C	90	105		dB
			T_A = full range	85			

(1) Full-power bandwidth = slew rate / [π $V_{O(P-P)}$].
(2) Slew rate is measured from an output level range of 25% to 75%.
(3) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also セクション 5.1.

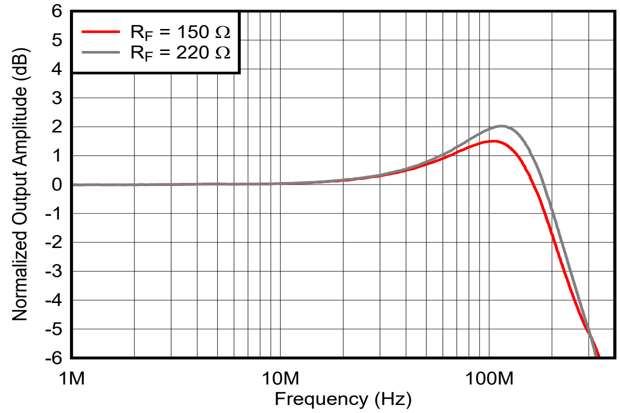
5.6 Typical Characteristics

at T_A = 25°C, V_{CC} = ± 15 V, gain = +10 V/V, R_L = 150 Ω, and R_F = 220 Ω (unless otherwise noted)



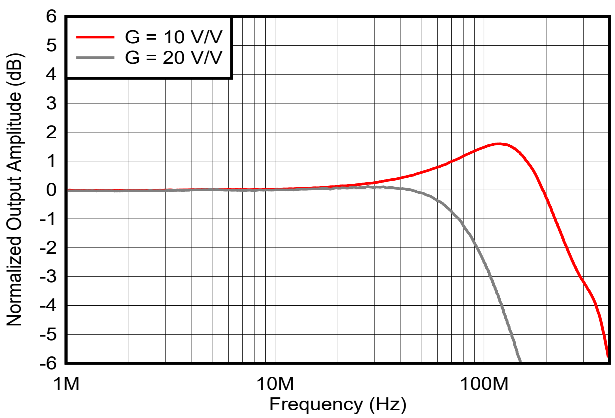
V_{CC} = ±15 V, V_{OUT} = 100 mV_{PP}

図 5-1. Frequency Response vs Feedback Resistance



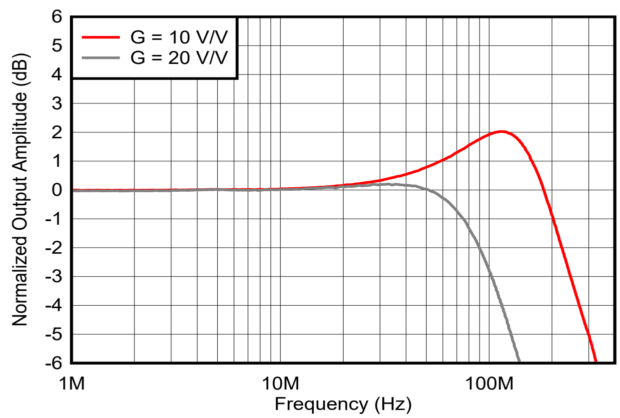
V_{CC} = ±5 V, V_{OUT} = 100 mV_{PP}

図 5-2. Frequency Response vs Feedback Resistance



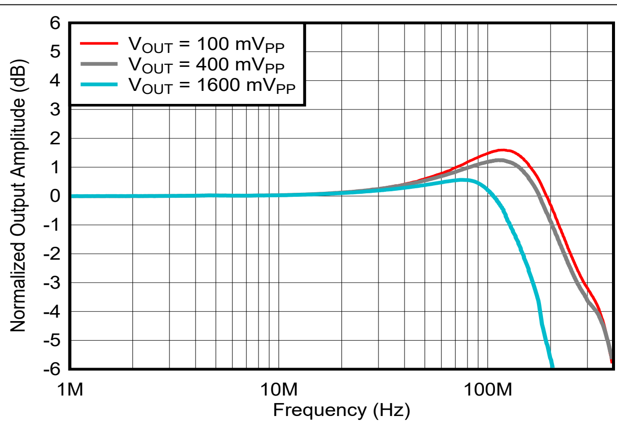
V_{CC} = ±15 V, V_{OUT} = 100 mV_{PP}

図 5-3. Frequency Response vs Gain



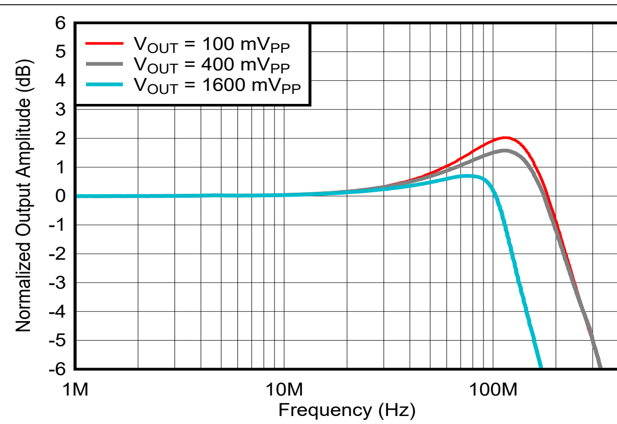
V_{CC} = ±5 V, V_{OUT} = 100 mV_{PP}

図 5-4. Frequency Response vs Gain



V_{CC} = ±15 V

図 5-5. Large-signal Frequency Response



V_{CC} = ±5 V

図 5-6. Large-signal Frequency Response

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +10 V/V, R_L = 150 Ω, and R_F = 220 Ω (unless otherwise noted)

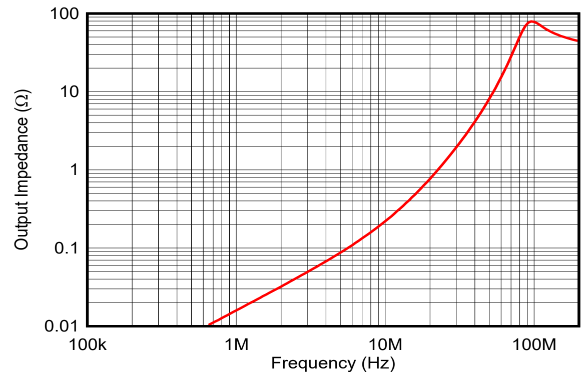


図 5-7. Closed-loop Output Impedance

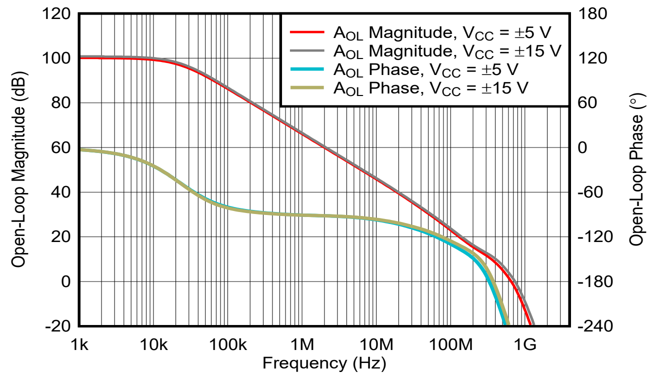


図 5-8. Open-loop Gain and Phase Response

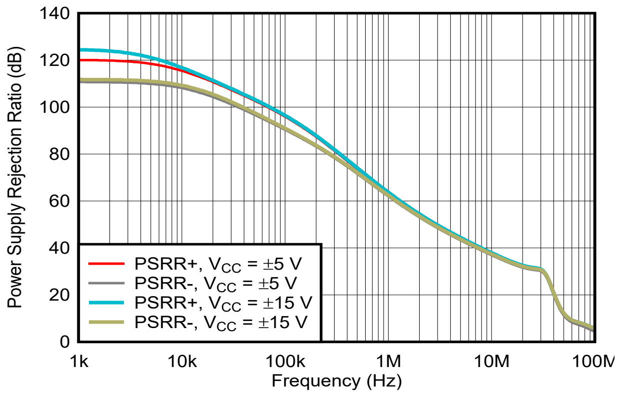


図 5-9. Power-Supply Rejection Ratio vs Frequency

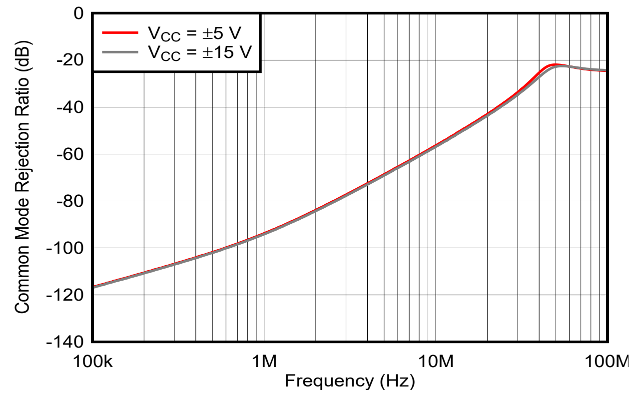
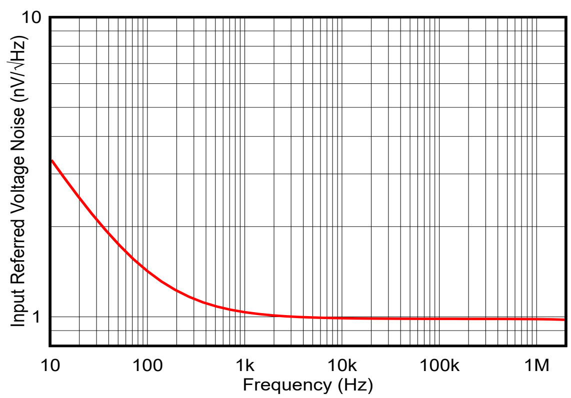
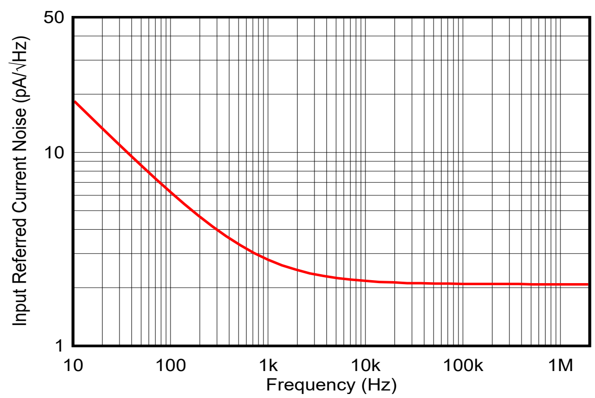


図 5-10. Common-mode Rejection Ratio vs Frequency



V_{CC} = ±15 V

図 5-11. Input-referred Voltage Noise vs Frequency

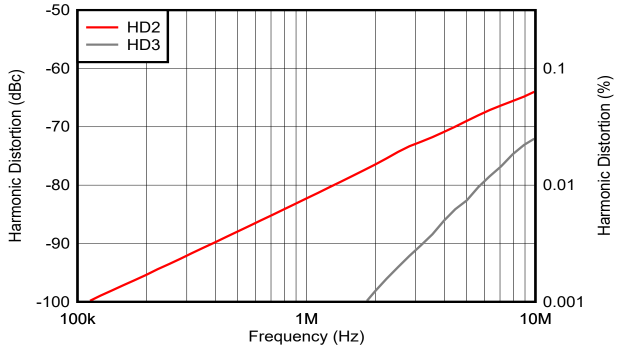


V_{CC} = ±15 V, R_L = 150 Ω, V_{OUT} = 2 V_{PP}

図 5-12. Input-referred Current Noise vs Frequency

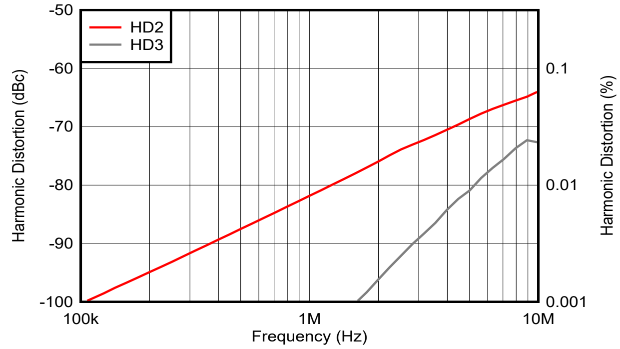
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +10 V/V, R_L = 150 Ω, and R_F = 220 Ω (unless otherwise noted)



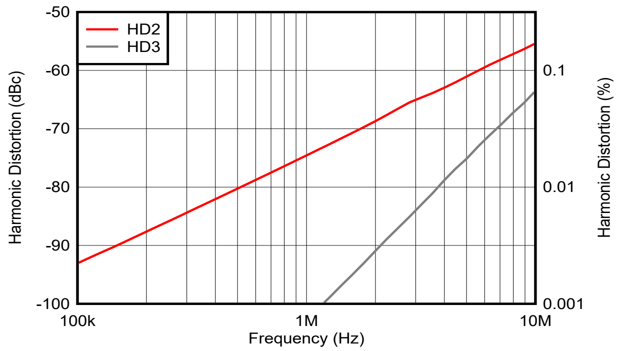
V_{CC} = ±15 V, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}

図 5-13. Harmonic Distortion vs Frequency



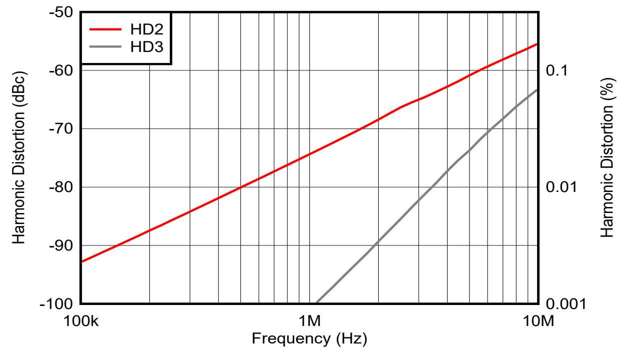
V_{CC} = ±5 V, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}

図 5-14. Harmonic Distortion vs Frequency



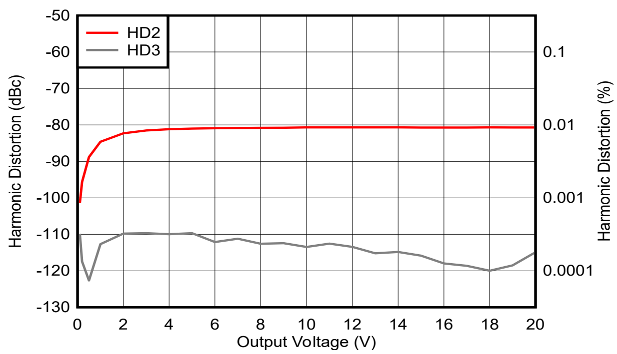
V_{CC} = ±15 V, R_L = 150 Ω, V_{OUT} = 2 V_{PP}

図 5-15. Harmonic Distortion vs Frequency



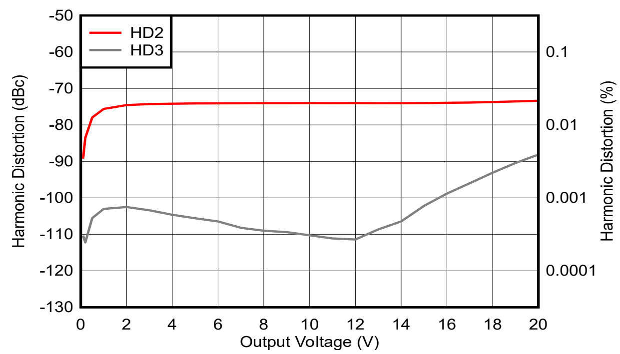
V_{CC} = ±5 V, R_L = 150 Ω, V_{OUT} = 2 V_{PP}

図 5-16. Harmonic Distortion vs Frequency



V_{CC} = ±15 V, R_L = 1 kΩ, f = 1 MHz

図 5-17. Harmonic Distortion vs Peak-to-Peak Output Voltage

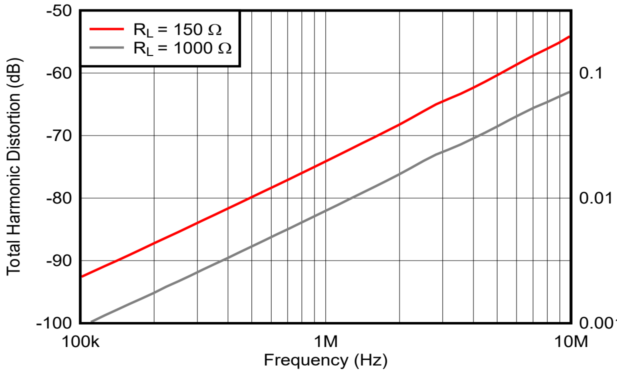


V_{CC} = ±15 V, R_L = 150 Ω, f = 1 MHz

図 5-18. Harmonic Distortion vs Peak-to-Peak Output Voltage

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +10 V/V, R_L = 150 Ω, and R_F = 220 Ω (unless otherwise noted)



V_{CC} = ±15 V, V_{OUT} = 2 V_{PP}

図 5-19. Total Harmonic Distortion vs Frequency

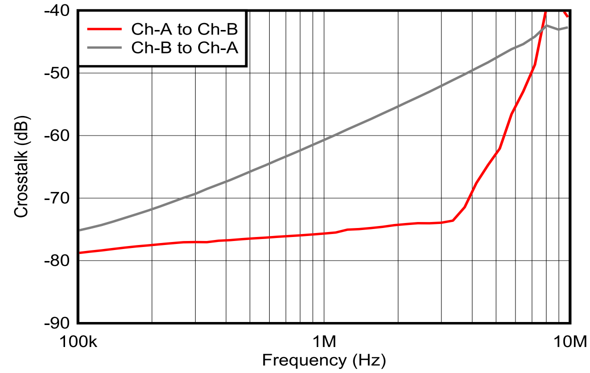


図 5-20. OPA2892 Crosstalk vs Frequency

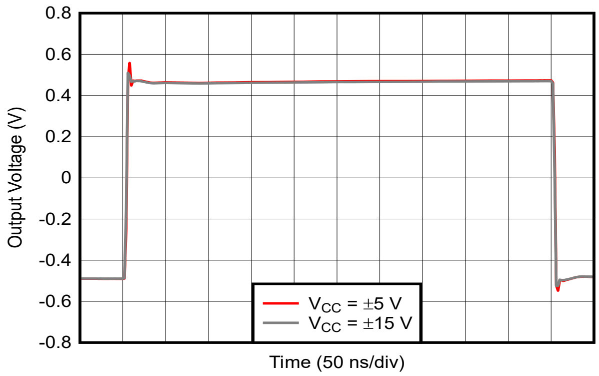
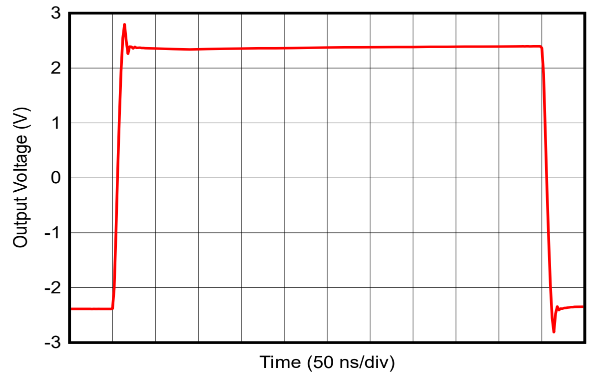
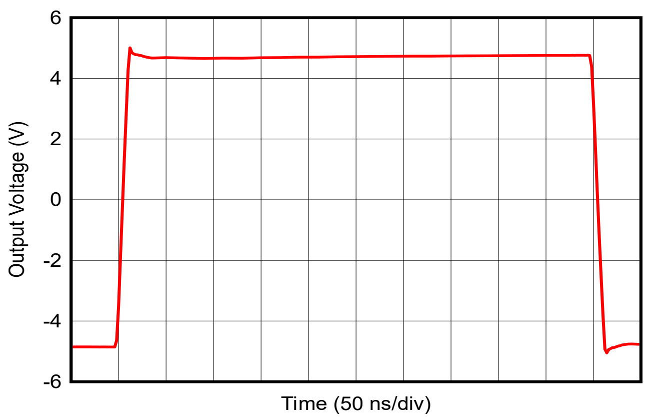


図 5-21. 1-V Step Response



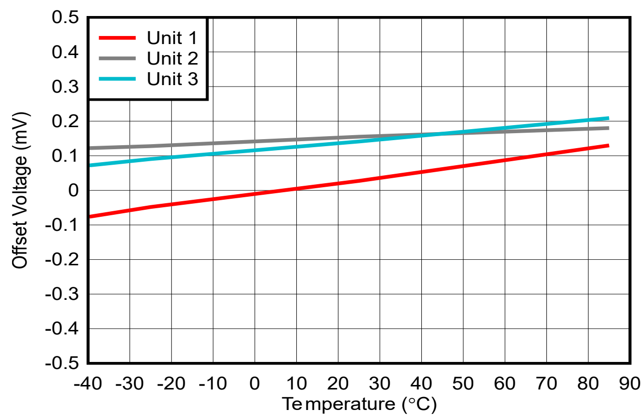
V_{CC} = ±5 V

図 5-22. 5-V Step Response



V_{CC} = ±15 V

図 5-23. 10-V Step Response

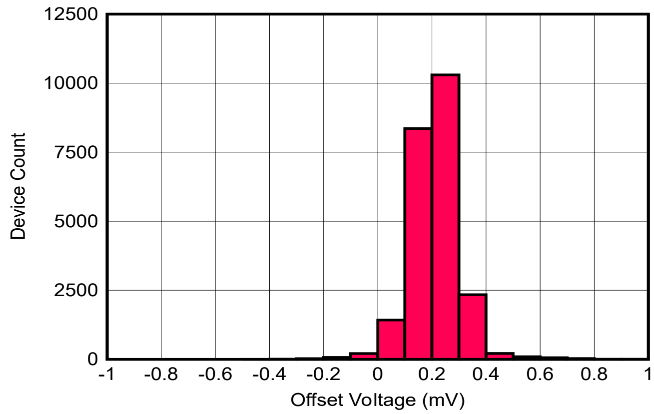


3 typical units

図 5-24. Input Offset Voltage vs Ambient Temperature

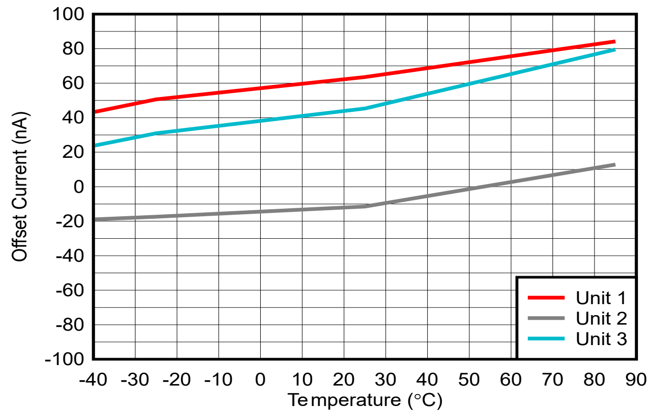
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +10 V/V, R_L = 150 Ω, and R_F = 220 Ω (unless otherwise noted)



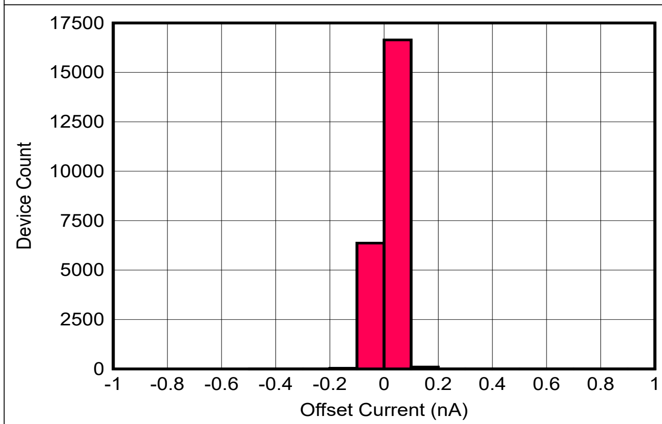
μ = 0.212 mV, σ = 0.0903 mV

図 5-25. Voltage Offset Distribution



3 typical units

図 5-26. Input Offset Current vs Ambient Temperature



μ = 0.164 nA, σ = 0.0395 nA

図 5-27. Input Offset Current vs Ambient Temperature

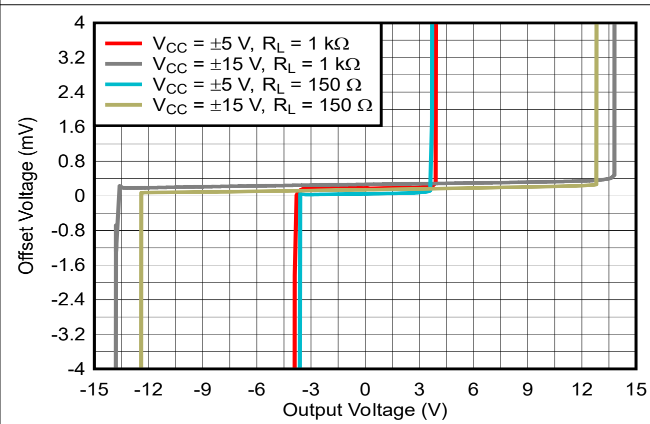


図 5-28. Offset Voltage vs Output Voltage

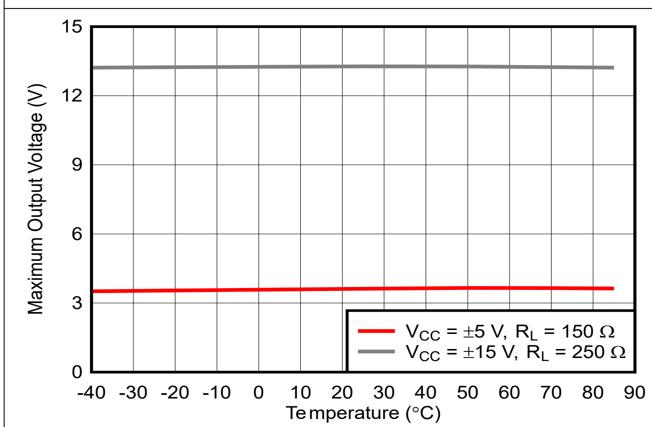


図 5-29. Maximum Output Voltage Swing vs Ambient Temperature

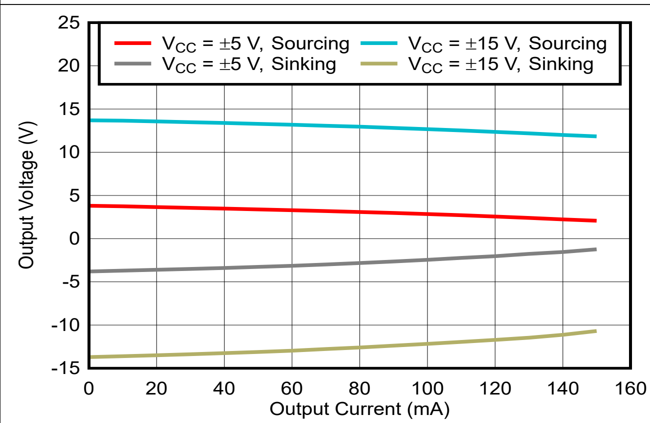


図 5-30. Output Swing vs Load Current

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +10 V/V, R_L = 150 Ω, and R_F = 220 Ω (unless otherwise noted)

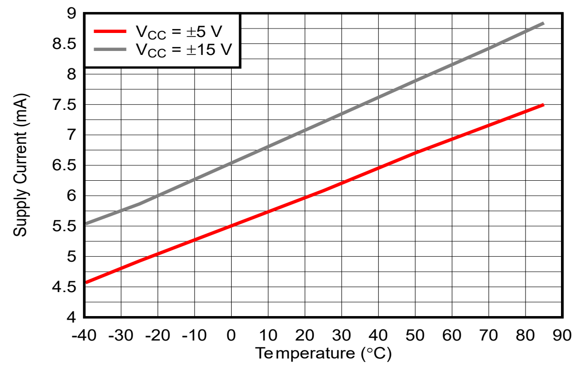
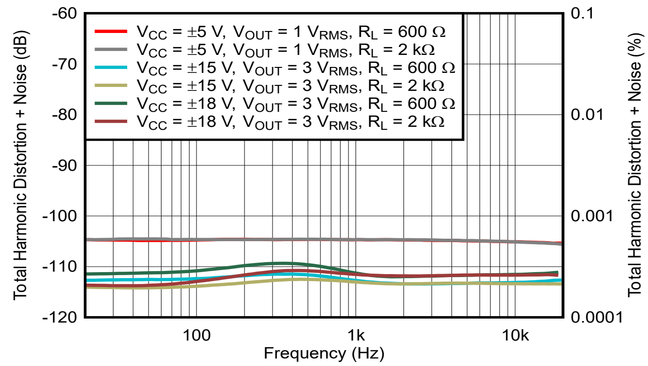
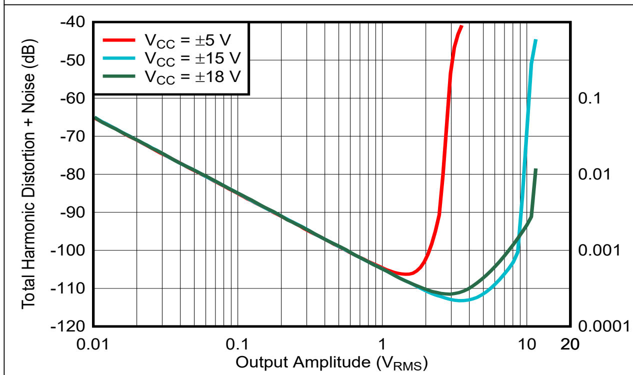


図 5-31. Supply Current vs Ambient Temperature



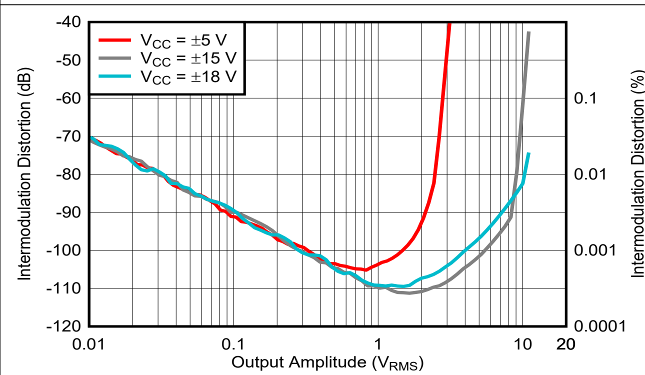
BW = 80 kHz

図 5-32. THD+N vs Frequency



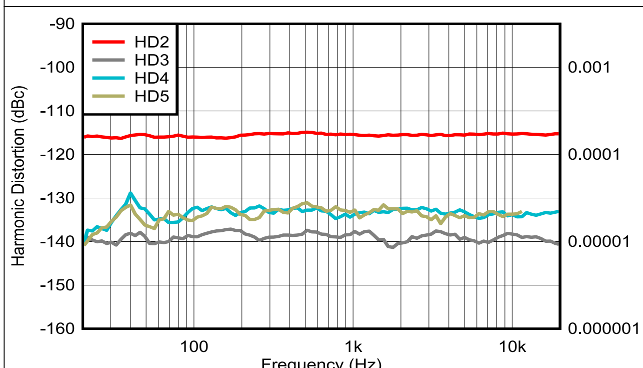
R_L = 2 kΩ, f = 1 kHz, BW = 80 kHz

図 5-33. THD+N Ratio vs Output Amplitude



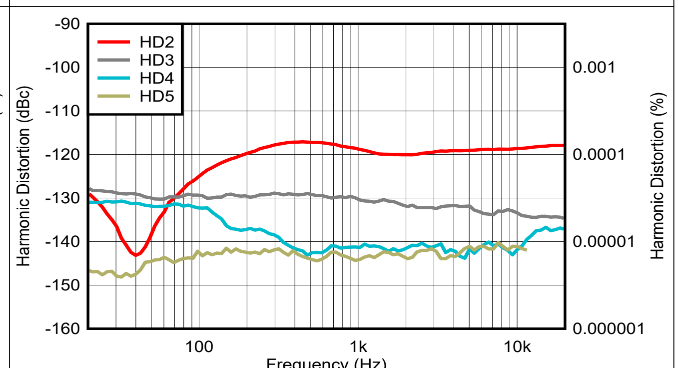
Gain = +10 V/V, SMPTE/DIN two-tone 4:1 (60 Hz and 7 kHz), R_L = 2 kΩ, BW = 80 kHz

図 5-34. Intermodulation Distortion vs Amplitude



V_{CC} = ±5 V, V_{OUT} = 1 V_{RMS}, R_L = 2 kΩ, BW = 80 kHz

図 5-35. Distortion Harmonics vs Frequency

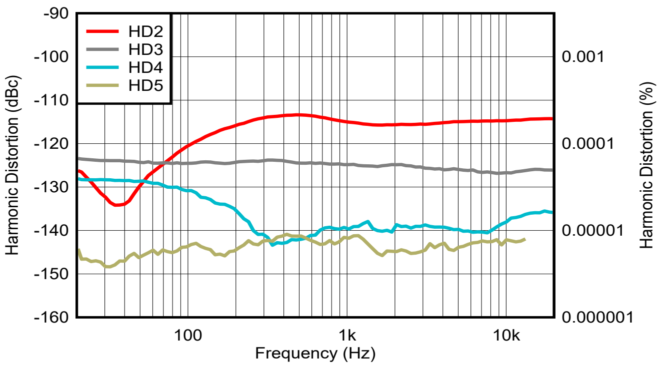


V_{CC} = ±15 V, V_{OUT} = 3 V_{RMS}, R_L = 2 kΩ, BW = 80 kHz

図 5-36. Distortion Harmonics vs Frequency

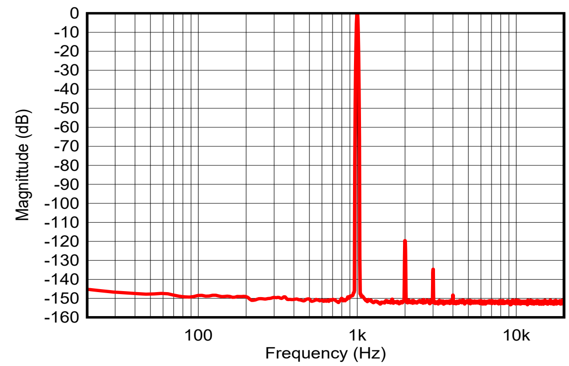
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +10 V/V, R_L = 150 Ω, and R_F = 220 Ω (unless otherwise noted)



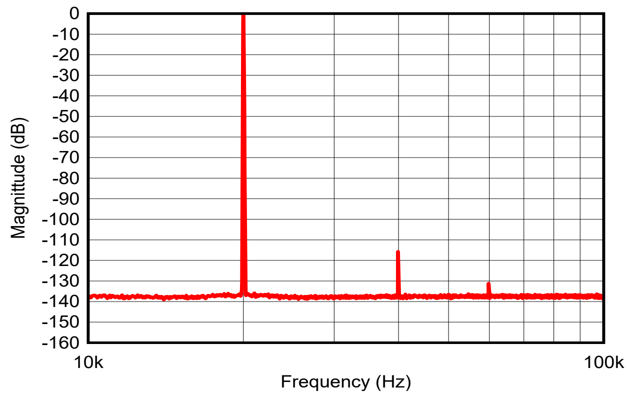
V_{CC} = ±18 V, V_{OUT} = 3 V_{RMS},
R_L = 2 kΩ, BW = 80 kHz

図 5-37. Distortion Harmonics vs Frequency



V_{CC} = ±15 V, V_{OUT} = 3 V_{RMS}, R_L = 2 kΩ

図 5-38. 1-kHz Output Spectrum



V_{CC} = ±5 V, V_{OUT} = 1 V_{RMS}, R_L = 2 kΩ

図 5-39. 20-kHz Output Spectrum

6 Detailed Description

6.1 Overview

The OPAx892 are high-speed operational amplifiers configured in a decompensated voltage-feedback architecture. The OPAx892 are stable with gain configurations of 10 V/V or greater. These amplifiers are built using a greater than 30-V, complementary, bipolar process with NPN and PNP transistors possessing an f_T of several GHz. This configuration results in exceptionally high-performance amplifiers with wide bandwidth, high slew rate, fast settling time, and low distortion.

6.2 Functional Block Diagram

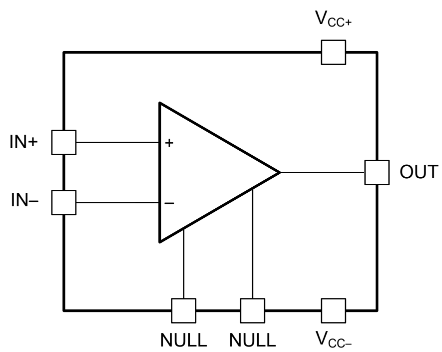


図 6-1. OPA892: Single Channel

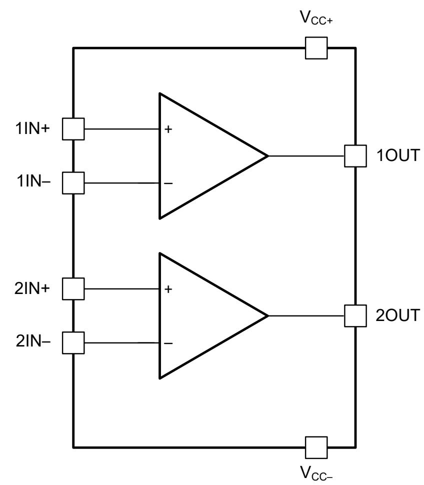


図 6-2. OPA2892: Dual Channel

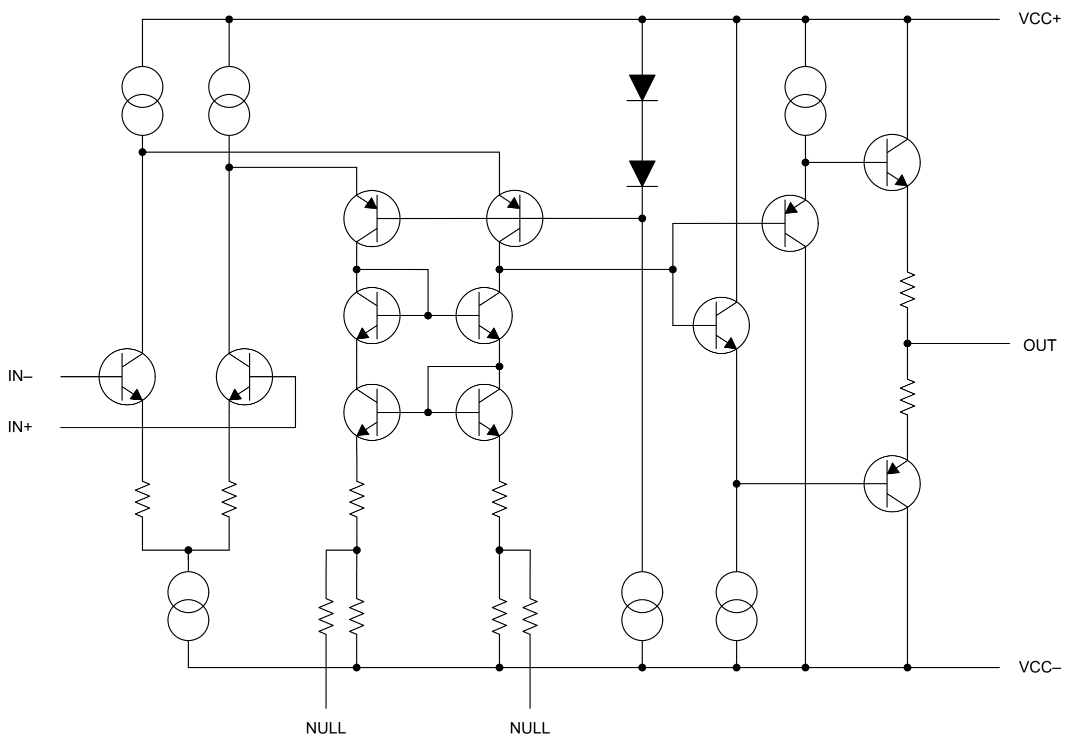


図 6-3. OPA892 Simplified Schematic

6.3 Feature Description

6.3.1 Offset Nulling

The OPAx892 have a very low input offset voltage for high-speed amplifiers. However, if additional correction is required, an offset nulling function is provided on the OPA892. To adjust the input offset voltage, place a potentiometer between pin 1 and pin 8 of the device, and tie the wiper to the negative supply. 図 6-4 shows this feature.

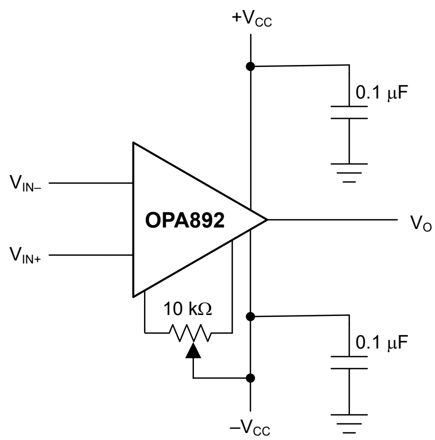


図 6-4. Offset Nulling Schematic

6.4 Device Functional Modes

The OPAx892 family has a single functional mode and can be used with both single-supply or split power-supply configurations. The power-supply voltage must be greater than 9 V (±4.5 V) and less than 36 V (±18 V).

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Driving a Capacitive Load

The OPAx892 are internally compensated to maximize bandwidth and slew-rate performance. To maintain stability, take additional precautions when driving capacitive loads with a high-performance amplifier. As a result of the internal compensation, significant capacitive loading directly on the output node decreases the device phase margin, and potentially lead to high-frequency ringing or oscillations. Therefore, for capacitive loads greater than 10 pF, place an isolation resistor in series with the output of the amplifier. 図 7-1 shows this configuration. For most applications, a minimum resistance of 20 Ω is recommended. In 75-Ω transmission systems, setting the series resistor value to 75 Ω is a beneficial choice because this value isolates any capacitance loading and provides source impedance matching.

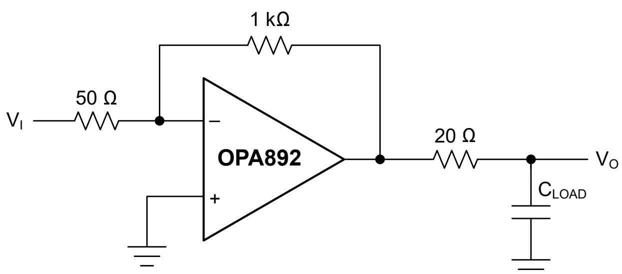


図 7-1. Driving a Capacitive Load

7.1.2 General Configuration

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. 図 7-2 shows how the simplest way to accomplish this limiting is to place an RC filter at the noninverting pin of the amplifier.

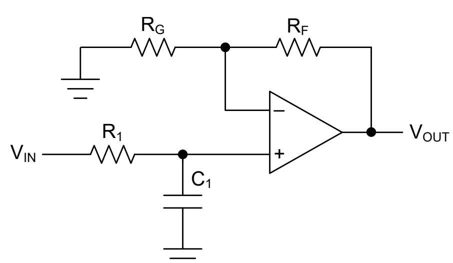


図 7-2. Single-Pole Low-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + sR_1C_1}\right) \quad (1)$$

7.2 Typical Application

One important characteristic of the OPAx892 amplifier is the decompensated architecture. By pushing out the dominate pole to a higher frequency using this common technique, the amplifier is no longer stable in lower gain configurations. The minimum stable gain for the OPAx892 is specified to be 10 V/V. When a lower gain is needed in a preamp or buffer application, a related product to be considered is the OPA891. Because the OPA891 is not decompensated, the gain-bandwidth product is approximately an order of magnitude lower than the OPAx892. Both of these amplifiers have similar noise performance, but the best bandwidth and distortion performance comes from using the correct amplifier depending on the gain needs of the application.

When applications require gain of 10 V/V or larger, choose the OPAx892 to obtain a low value of harmonic distortion and THD+N. 図 7-3 shows a where in the analog signal chain this type of amplification can be required. Often found in applications such as ultrasound, audio, and sonar, a preamp is used near the input sensor to boost the signal to a more practical level with an emphasis on keeping noise and distortion as small as possible. Later in the signal chain, significantly more gain can be required to provide for other required functions such analog filtering, mixing, splitting, or just the need to match the signal level to a following device. An amplifier such as the OPAx892 maintains the fidelity of the signal by providing the needed gain with significantly impacting distortion over a wide bandwidth and output swing. 図 7-4 shows the amplifier design example. The amplification stage provides an additional 10 V/V of gain to the analog signal chain.

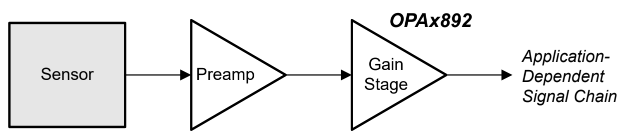


図 7-3. Gain Stage in an Analog-Front-End Block Diagram

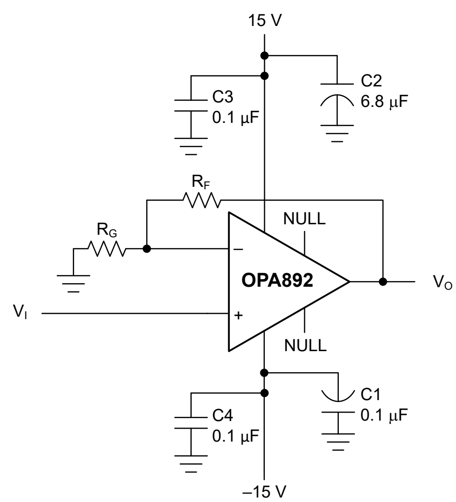


図 7-4. Noninverting Gain Configuration

7.2.1 Design Requirements

The objective is to design a 10 V/V amplifier to be for a mid-stage amplifier that minimizes the THD of the signal over the output range shown in 表 7-1.

表 7-1. Design Parameters

PARAMETER	VALUE
Supply voltage	±15 V
Voltage gain	+10 V/V
Small-signal peaking	< 2 dB
Load resistance	1 kΩ

7.2.2 Detailed Design Procedure

As detailed by 図 7-4, the example design is a common non-inverting op-amp configuration. In this design example, the spit ±15 V supplies are bypassed by a pair of capacitors as discussed in セクション 7.4.1. Although not explicitly shown, a optional resistor equal to R_F || R_G can be added from the noninverting input to ground to keep the inputs balanced to help mitigate input bias current impact.

Set the gain to 10 V/V by the proper selection of the two resistors using equation 式 2. In this example, set the ratio of the resistance to 9 to obtain the design goal of a gain of 10. There exists a second degree of freedom that allows the absolute value to be somewhat arbitrary while maintaining the specified ratio of resistor values. Increasing feedback resistance leads to an increase in the amount of overshoot in the small-signal frequency response (see 図 5-1). In the time domain, the impact shows up as and increase in ringing and settling time for step-function input signals. If the resistances are very small, power dissipation effects increase.

$$\text{gain} = \frac{V_O}{V_I} = 1 + \frac{R_F}{R_G} \tag{2}$$

The best practice is to chose the resistors to be in of moderate values to avoid the detrimental effects at both extremes. Choosing R_F = 220 Ω is a good compromise in between these two extremes. Using 式 2, the corresponding gain resistor is found to be 24 Ω. The amount of small-signal peaking is a modest 1.5 dB (see 図 5-1), which meets the design goal.

A unique feature of this amplifier family is the output stage has been designed to drive a substantial amount of output current. This choice allows for the OPAx892 to maintain significant bandwidth even with very large input signals. 図 7-5 shows the modest reduction of bandwidth, even for output signals as large as 20 V_{PP}. The time domain impact of this feature is a more precise amplification (that is, lower distortion) even for large dynamic range input signals.

Using the amplifier designed in this section, 図 7-6 shows the measured components of THD down to the 5th harmonic. The figure shows that the 2nd harmonic dictates the THD performance, with the 4th harmonic being the next highest component. Other amplifiers can produce low distortion at lower input levels but distortion rapidly rises as the output amplitude rises. 図 5-17 shows the harmonic distortion stays approximately constant, even at large values of output amplitude, making the OPAx892 a solid choice for large amplitude applications where distortion and noise are critical considerations.

7.2.3 Application Curves

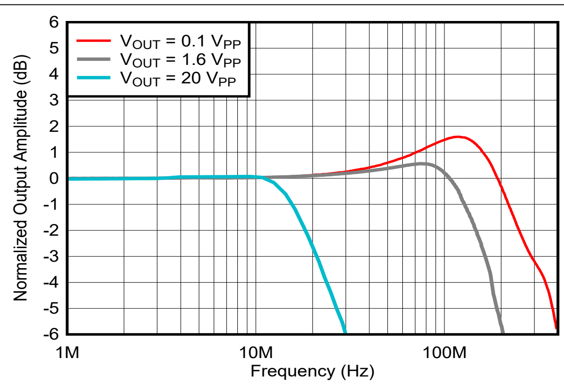
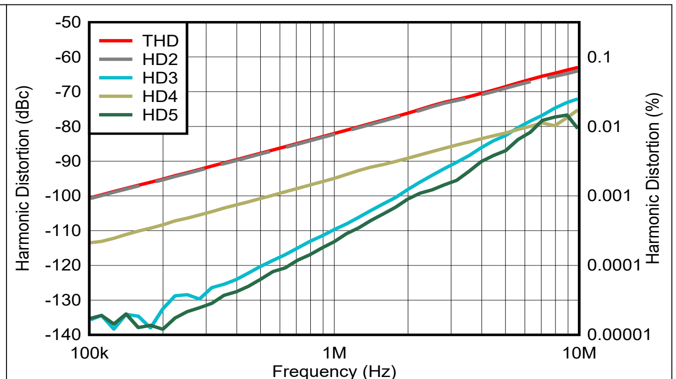


図 7-5. Very Large-Signal Frequency Response



V_{OUT} = 2 V_{PP}

図 7-6. Harmonic Distortion Components vs Frequency

7.3 Power Supply Recommendations

The OPAx892 devices are designed to operate on power supplies ranging from ±4.5 V to ±16 V (single-ended supplies of 9 V to 32 V). Use a power-supply accuracy of 5% or better. When operated on a board with high-speed digital signals, provide isolation between digital signal noise and the analog input pins. The OPAx892 are connected to the positive power supply (V_{CC+}) through pin 7 and pin 8, respectively. Both devices use pin 4 for the negative power supply (V_{CC-}). Decouple each supply pin to GND as close to the device as possible.

7.4 Layout

7.4.1 Layout Guidelines

To achieve the levels of high-frequency performance of the OPAx892, follow proper printed-circuit board (PCB), high-frequency design techniques. The following is a general set of guidelines. In addition, a OPAx892 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- **Ground planes**—ensure that the ground plane used on the board provides all components with a low-inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize stray capacitance.
- **Proper power-supply decoupling**—use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply pin. Sharing the tantalum capacitor among several amplifiers is possible depending on the application, but always use a 0.1-µF ceramic capacitor on the supply pin of every amplifier. In addition, place the 0.1-µF capacitor as close as possible to the supply pin. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. Strive for distances of less than 0.1 inch (2.54 mm) between the device power pins and the ceramic capacitors.
- **Short trace runs or compact part placements**—optimized high-frequency performance is achieved when stray series inductance has been minimized. To realize this, make the circuit layout as compact as possible, thereby minimizing the length of all trace runs. Pay particular attention to the inputs of the amplifier, keeping the trace lengths as short as possible. This layout helps to minimize stray capacitance at the input of the amplifier.

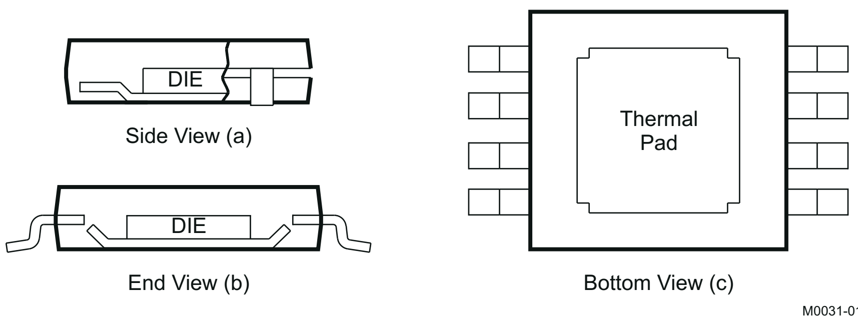
7.4.1.1 General PowerPAD™ Integrated Circuit Package Design Considerations

The OPAx892 is available in a thermally-enhanced DGN package, which is a member of the PowerPAD™ integrated circuit package family. 図 7-7 **a** and 図 7-7 **b** show that this package is constructed using a downset leadframe upon which the die is mounted. 図 7-7 **c** that this arrangement results in the leadframe being exposed as a thermal pad on the underside of the package. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD integrated circuit package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the previously awkward mechanical methods of heat sinking.

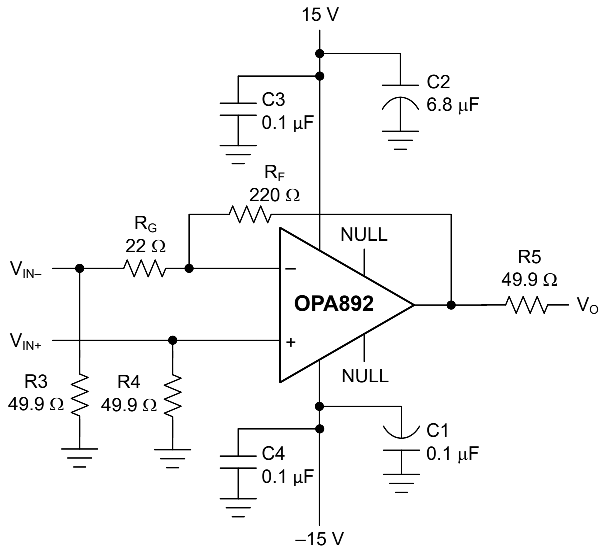
More complete details of the PowerPAD integrated circuit package installation process and thermal management techniques are found in *PowerPAD Thermally-Enhanced Package* . This document is found on the TI website (www.ti.com) by searching on the keyword PowerPAD. The document can also be ordered through your local TI sales office; refer to SLMA002 when ordering.



NOTE: The thermal pad (PowerPAD integrated circuit package) is electrically isolated from all other pins and can be connected to any potential from V_{CC-} to V_{CC+}. Typically, the thermal pad is connected to the ground plane because this plane tends to physically be the largest and is able to dissipate the most amount of heat.

図 7-7. Views of Thermally-Enhanced DGN Package

7.4.2 Layout Example



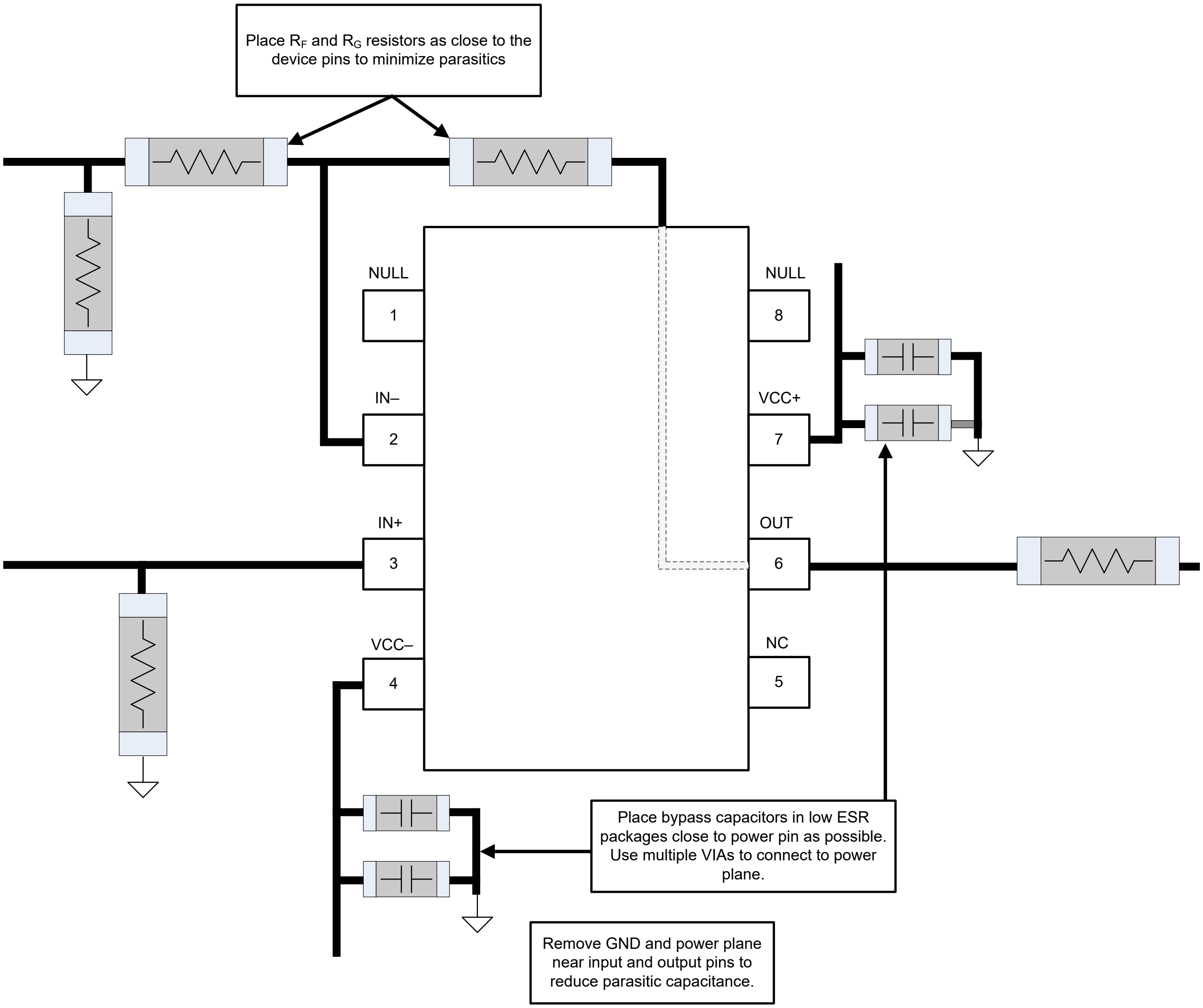


図 7-8. Layout Recommendations

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Noise Analysis in Operational Amplifier Circuits* application report
- Texas Instruments, *PowerPAD Thermally Enhanced Package* application report
- Texas Instruments, *Single op-amp evaluation module for SO-8 package*users guide
- Texas Instruments, *Dual op-amp evaluation module for SO-8 package* users guide
- Texas Instruments, *Dual op amp evaluation module for MSOP-8 package* users guide

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2023) to Revision A (July 2024) **Page**

- OPA2892 のステータスを「事前情報」から「量産データ」(アクティブ) に変更 1
- Added thermal pad information to Table 4-2, *Pin Functions: OPA2892* 3
- Added missing unit for Supply current in *Electrical Characteristics* 5
- Added Figure 5-20, *OPA2892 Crosstalk vs Frequency* 7

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2892DGNR	Active	Production	HVSSOP (DGN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2892
OPA2892DGNR.B	Active	Production	HVSSOP (DGN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2892
OPA892DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	O892
OPA892DR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	O892

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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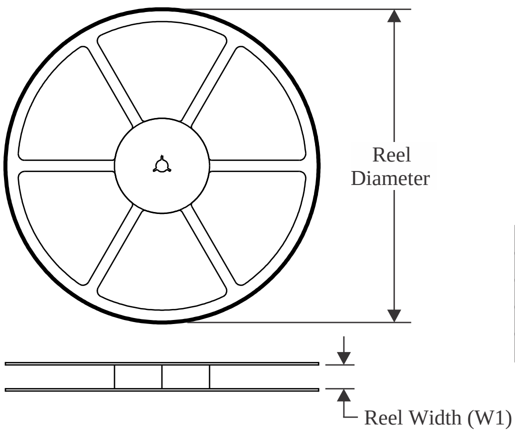
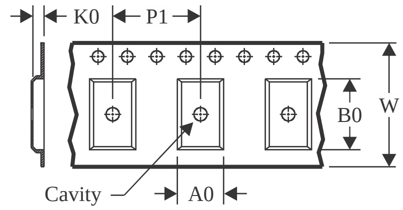
TAPE AND REEL INFORMATION

REEL DIMENSIONS

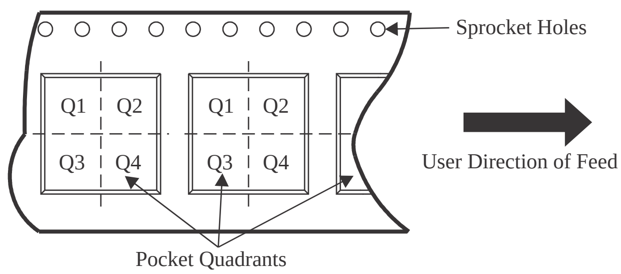


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

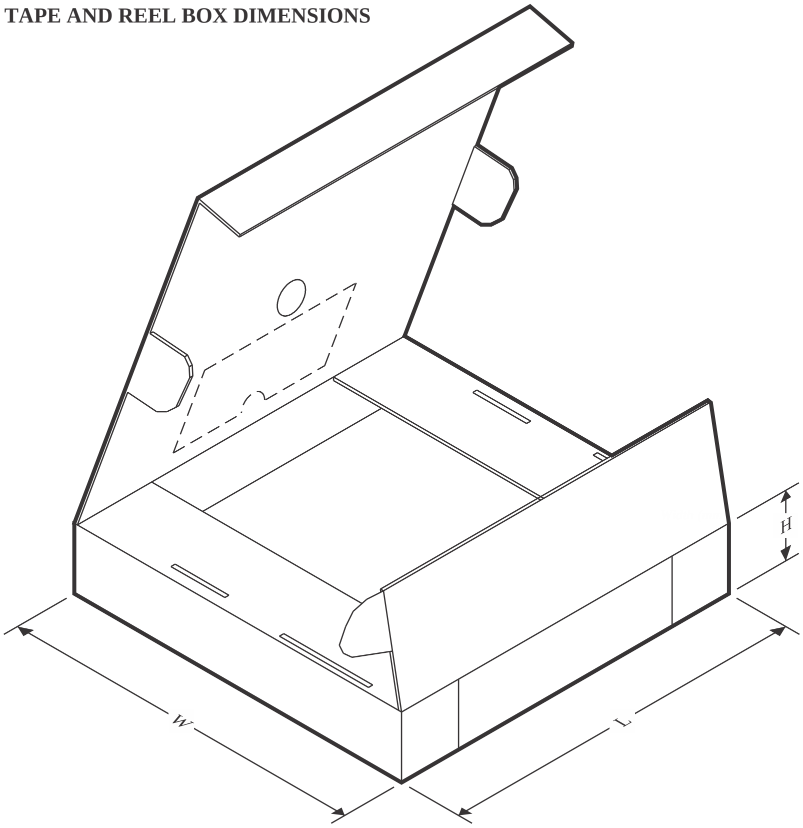
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2892DGNR	HVSSOP	DGN	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA892DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2892DGNR	HVSSOP	DGN	8	3000	353.0	353.0	32.0
OPA892DR	SOIC	D	8	3000	353.0	353.0	32.0

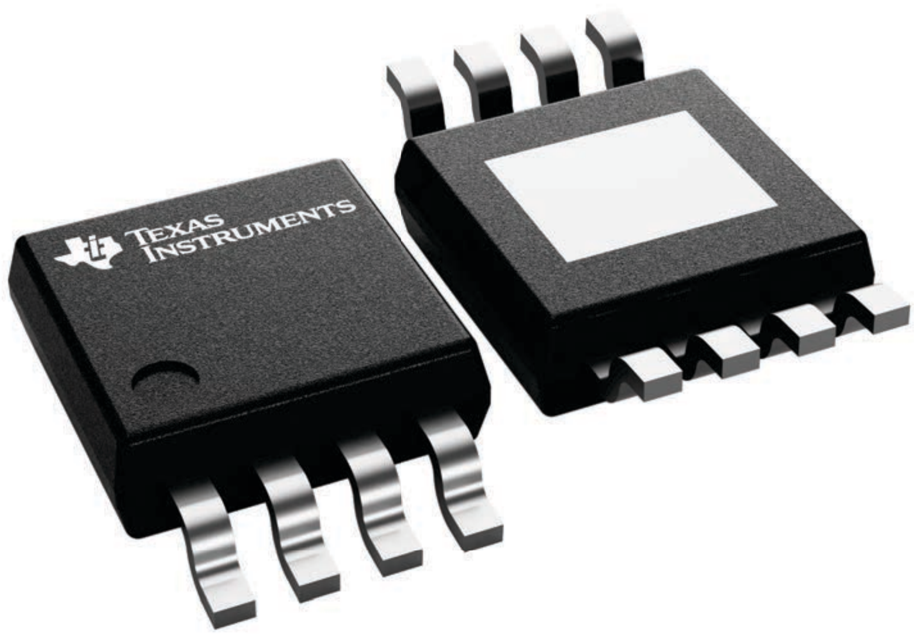
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

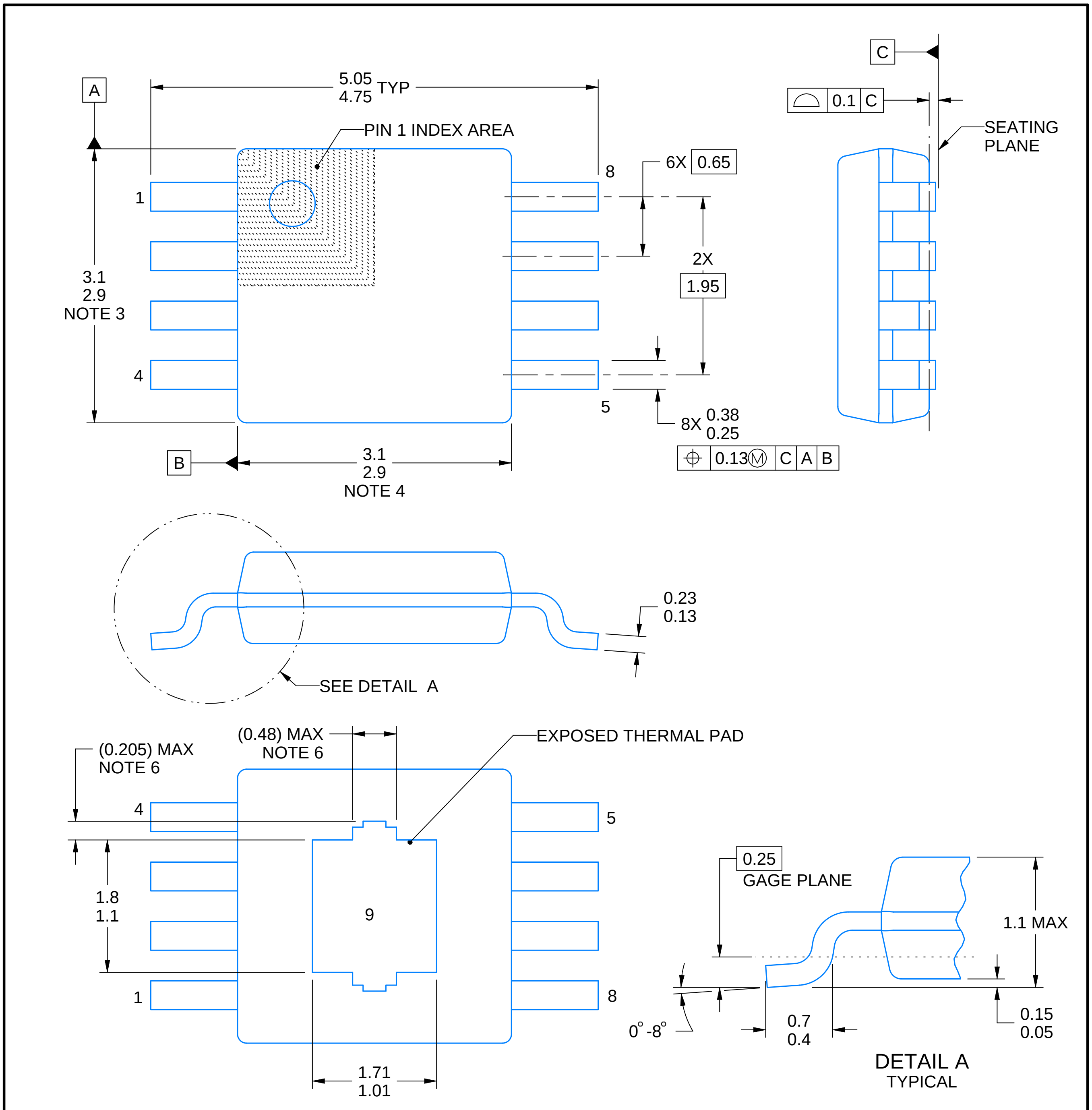
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

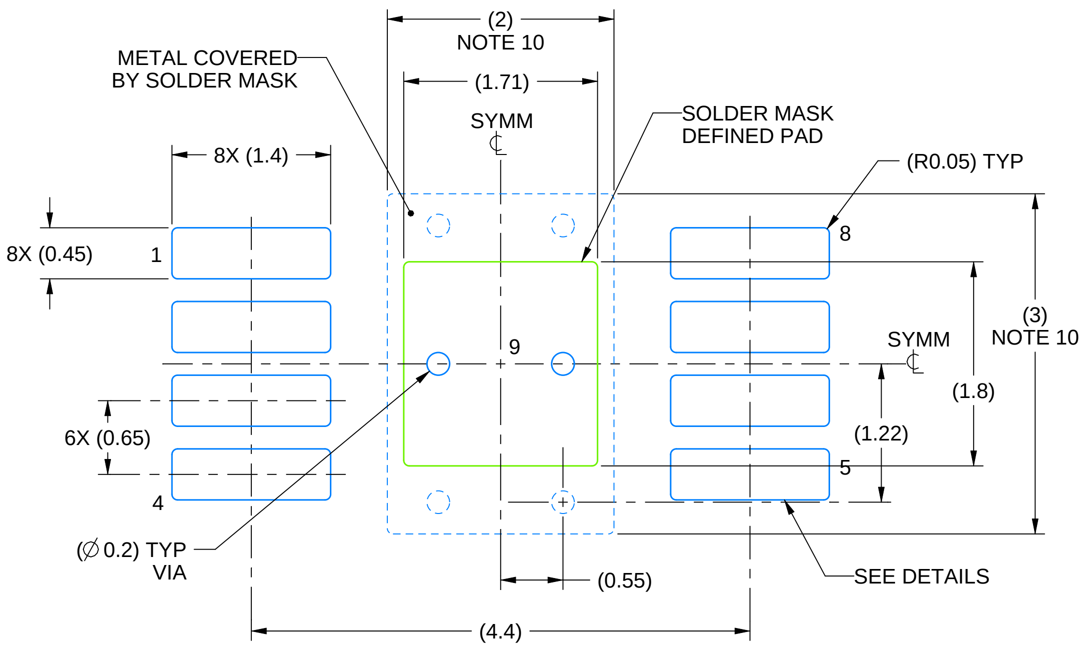


4229130/B 05/2024

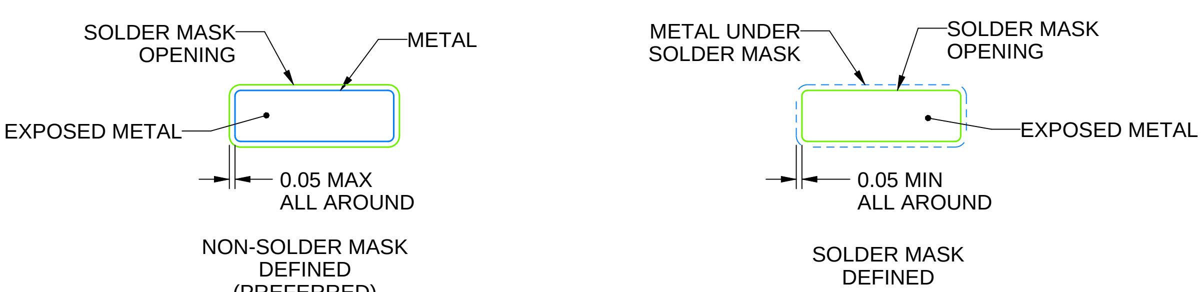
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

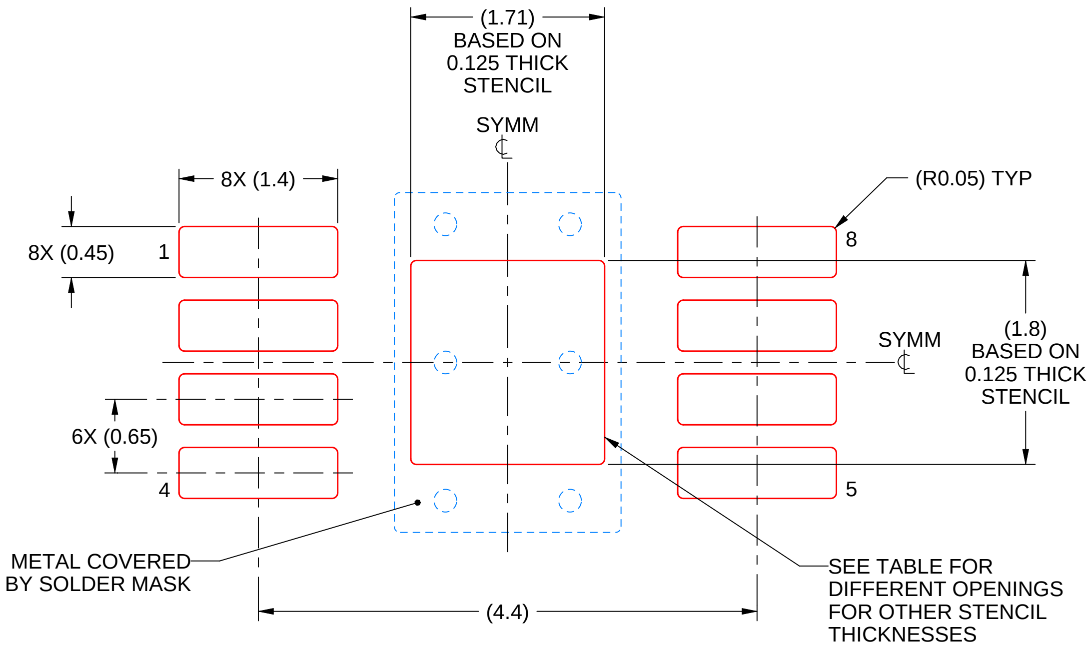


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



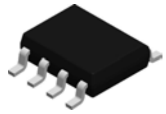
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

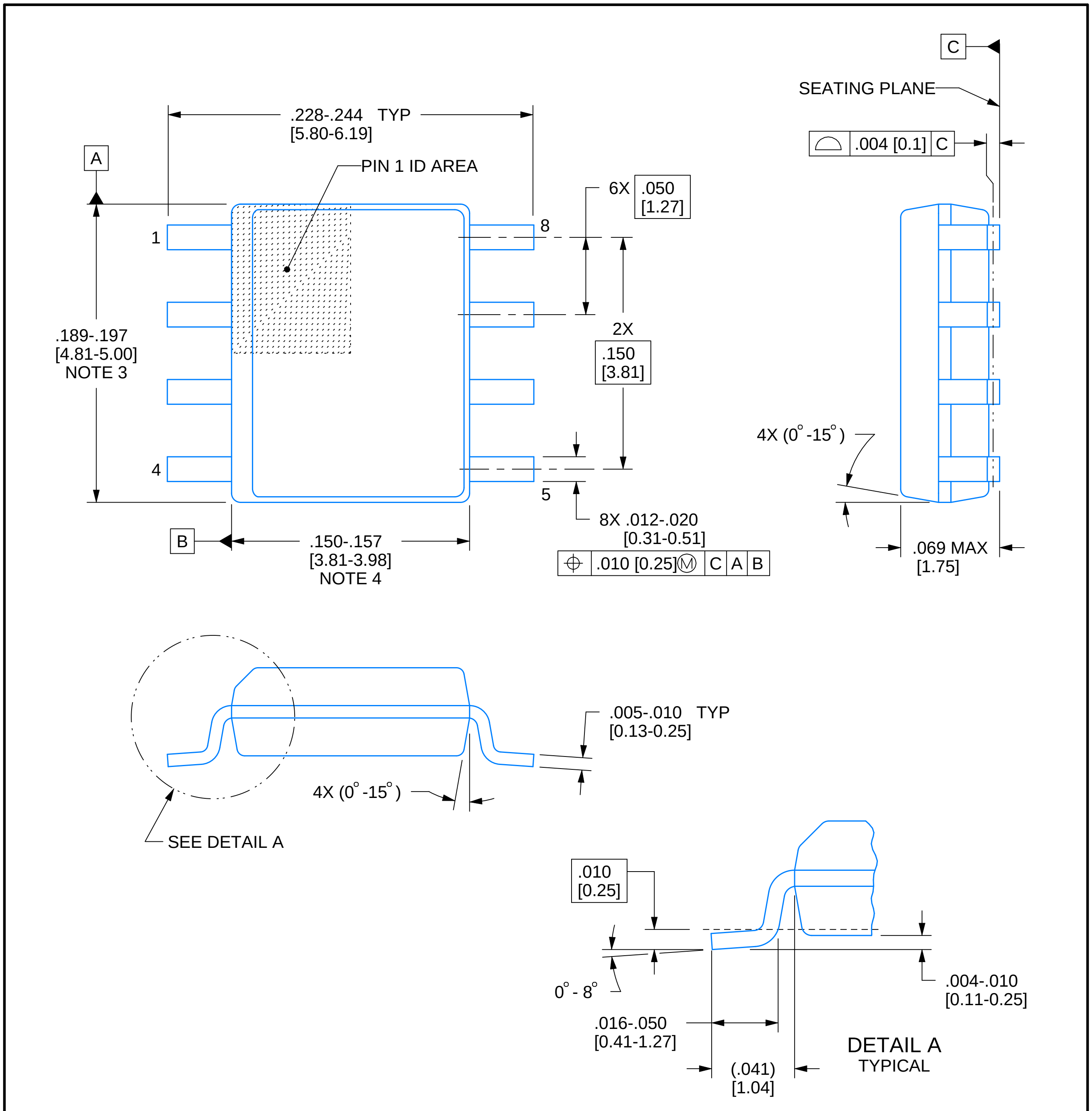
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



SOIC - 1.75 mm max height

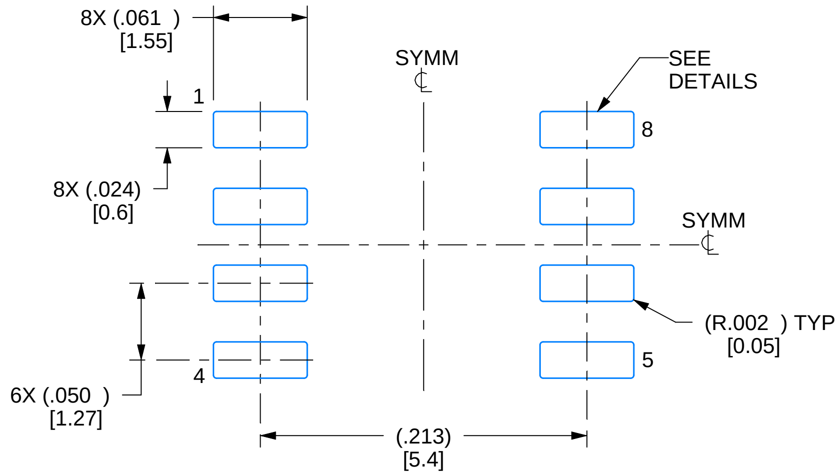
SMALL OUTLINE INTEGRATED CIRCUIT



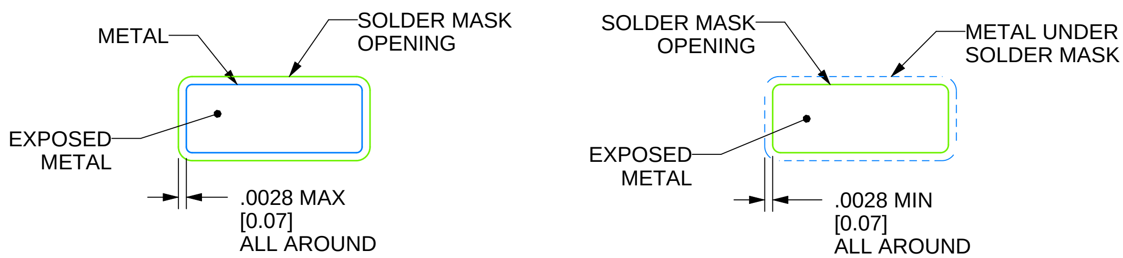
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

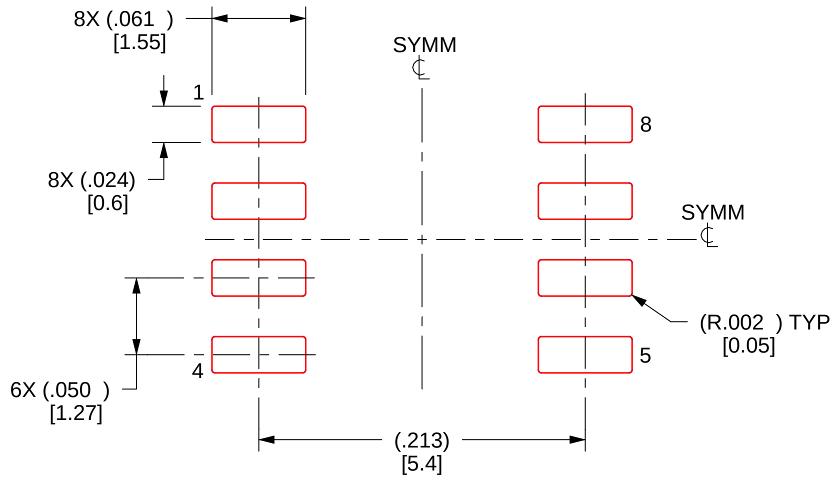
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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