

OPAx891 180MHz、0.95nV/√Hz、超低 THD オペアンプ

1 特長

- 0.95nV/√Hz の非常に低い電圧ノイズ
- 高速度:
 - 180MHz のユニティ ゲイン帯域幅
 - 2V/V (–1V/V) のゲインで 140MHz の帯域幅
 - スルー レート: 105V/μs
- 非常に低い歪み
 - THD = –91dBc (f = 1MHz, R_L = 150Ω)
 - THD = –100dBc (f = 1MHz, R_L = 1kΩ)
 - THD+N = –137dBc (f = 1kHz, BW = 80kHz)
- 25°C で 0.2mV (標準値) および 1mV (最大値) の低い入力オフセット電圧
- 200mA の出力電流ドライブ (標準値)
- ±4.5V ~ ±18V の標準動作範囲
- OPA891 のオフセット ノル ピン

2 アプリケーション

- 産業アプリケーション向けの低ノイズ、広帯域アンプ
- 電圧制御の発振器
- アクティブ フィルタ
- ビデオ アンプ
- ケーブルドライバ
- 超音波スキャナ
- ベクトル信号トランシーバ (VST)
- 業務用オーディオ ミキサまたは制御卓
- 業務用マイク / ワイヤレス システム
- 業務用スピーカ システム
- 業務用オーディオ アンプ
- サウンドバー
- ターンテーブル
- 業務用ビデオ カメラ
- ギターおよびその他楽器用アンプ
- データ アクイジション (DAQ)

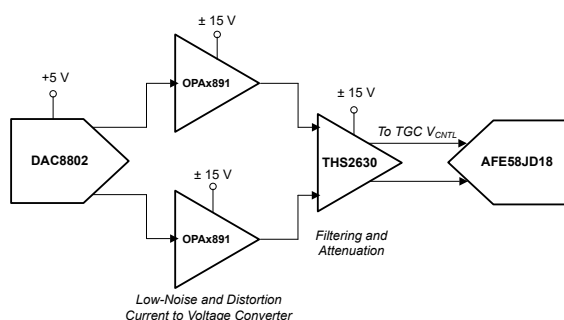
3 概要

OPA891 および OPA2891(OPAx891) は電圧ノイズが非常に低い高速電圧帰還アンプで、通信やイメージングなど低い電圧ノイズが要求されるアプリケーションに最適です。シングル アンプの OPA891 とデュアル アンプの OPA2891 は AC 特性が非常に優れており、140MHz の帯域幅、ゲイン (G) = 2V/V、105V/μs のスルーレート、70ns のセトリング タイム (0.1%) を実現しています。OPAx891 は、180MHz の帯域幅でユニティ ゲイン安定です。これらのアンプには、200mA の大きい駆動能力があり、チャンネルごとに 7.5mA の電流しか消費しません。OPAx891 は、f = 1MHz において総高調波歪 (THD) が –100dBc で、ノイズが 0.95nV/√Hz と非常に低く、A/D コンバータのバッファなど、低い歪みと低ノイズが要求されるアプリケーション向けに設計されています。

製品情報

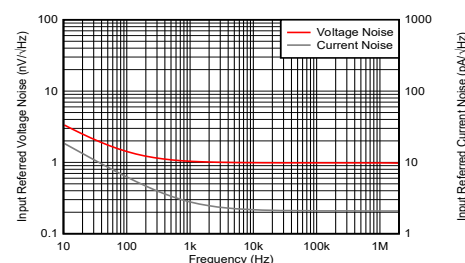
部品番号	アンプ	パッケージ (1)	パッケージ サイズ (2)
OPA891	1	D (SOIC, 8)	4.9mm × 6mm
		DGN (HVSSOP, 8)	3mm × 4.9mm
OPA2891	2	D (SOIC, 8)	4.9mm × 6mm
		DGN (HVSSOP, 8)	3mm × 4.9mm

- 詳細については、[セクション 10](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



Low-Noise and Distortion
Current to Voltage Converter

超音波時間ゲイン制御回路



電圧ノイズおよび電流ノイズと周波数との関係



Table of Contents

1 特長	1	6.4 Device Functional Modes.....	21
2 アプリケーション	1	7 Application and Implementation	22
3 概要	1	7.1 Application Information.....	22
4 Pin Configuration and Functions	3	7.2 Typical Application.....	24
5 Specifications	5	7.3 Power Supply Recommendations.....	27
5.1 Absolute Maximum Ratings.....	5	7.4 Layout.....	27
5.2 ESD Ratings.....	5	8 Device and Documentation Support	30
5.3 Recommended Operating Conditions.....	5	8.1 Documentation Support.....	30
5.4 Thermal Information - OPA891	6	8.2 Receiving Notification of Documentation Updates....	30
5.5 Thermal Information - OPA2891	6	8.3 サポート・リソース.....	30
5.6 Electrical Characteristics - $R_L = 150\Omega$	7	8.4 Trademarks.....	30
5.7 Electrical Characteristics - $R_L = 1k\Omega$	9	8.5 静電気放電に関する注意事項.....	30
5.8 Typical Characteristics.....	11	8.6 用語集.....	30
6 Detailed Description	19	9 Revision History	30
6.1 Overview.....	19	10 Mechanical, Packaging, and Orderable Information	31
6.2 Functional Block Diagrams.....	19		
6.3 Feature Description.....	20		

4 Pin Configuration and Functions

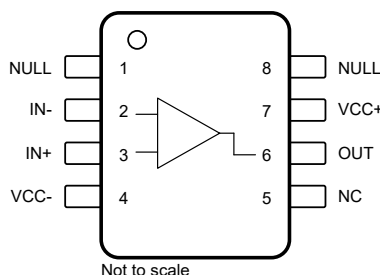


図 4-1. OPA891: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

表 4-1. Pin Functions: OPA891

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN–	2	Input	Inverting input
IN+	3	Input	Noninverting input
NC	5	—	No connection
NULL	1, 8	Input	Voltage offset adjust
OUT	6	Output	Output of amplifier
VCC–	4	—	Negative power supply
VCC+	7	—	Positive power supply
Thermal Pad	Pad	—	Thermal pad. DGN (HVSSOP) package only. For the best thermal performance, connect this pad to a large copper plane. The thermal pad can be connected to any pin on the device, or any other potential on the board, as long as the voltage on the thermal pad remains between VCC+ and VCC–.

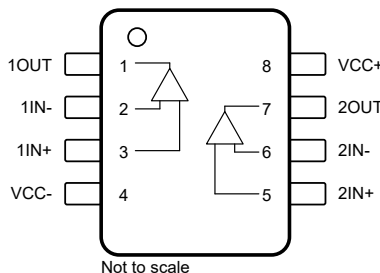


図 4-2. OPA2891: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

表 4-2. Pin Functions: OPA2891

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	2	Input	Channel 1 inverting input
1IN+	3	Input	Channel 1 noninverting input
1OUT	1	Output	Channel 1 output
2IN–	6	Input	Channel 2 inverting input
2IN+	5	Input	Channel 2 noninverting input
2OUT	7	Output	Channel 2 output
VCC–	4	—	Negative power supply
VCC+	8	—	Positive power supply

表 4-2. Pin Functions: OPA2891 (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
Thermal Pad	Pad	—	Thermal pad. DGN (HVSSOP) package only. For the best thermal performance, connect this pad to a large copper plane. The thermal pad can be connected to any pin on the device, or any other potential on the board, as long as the voltage on the thermal pad remains between VCC+ and VCC–.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage, V _{CC+} – V _{CC–}		37	V
V _I	Input voltage		±V _{CC}	V
I _O	Output current ⁽²⁾		240	mA
V _{IO}	Differential input voltage		±1.5	V
I _{IN}	Continuous input current		10	mA
T _A	Operating free-air temperature	–40	85	°C
T _J	Junction temperature	Any condition	150	°C
		Maximum junction temperature, continuous operation, long-term reliability ⁽³⁾	125	
T _{stg}	Storage temperature	–65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) When continuously operating at any output current, do not exceed the maximum junction temperature. Keep the output current less than the absolute maximum rating regardless of time interval.
- (3) The maximum junction temperature for continuous operation is limited by package constraints. Operation greater than this temperature can result in reduced reliability, lifetime of the device, or both.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±4000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	Dual-supply	±4.5	±15	±18	V
		Single-supply	9	30	36	
T _A	Operating free-air temperature		–40	25	85	°C

5.4 Thermal Information - OPA891

THERMAL METRIC ⁽¹⁾		OPA891		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	60.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.0	87.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	33	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.6	7.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.3	32.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	17.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Thermal Information - OPA2891

THERMAL METRIC ⁽¹⁾		OPA2891		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.6	52.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.7	75.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.9	24.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.2	4.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.2	24.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics - $R_L = 150\Omega$

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, and $R_L = 150\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3dB)	Gain = –1V/V or 2V/V	V _{CC} = ±15V	140		MHz	
			V _{CC} = ±5V	135			
	Bandwidth for 0.1dB flatness	Gain = –1V/V or 2V/V	V _{CC} = ±15V	9		MHz	
			V _{CC} = ±5V	9			
SR	Slew rate ⁽¹⁾	Gain = –1V/V	V _{CC} = ±15V, 20V step	105		V/μs	
			V _{CC} = ±5V, 5V step	90			
t _S	Settling time	To 0.1%, gain = –1V/V	V _{CC} = ±15V, 5V step	70		ns	
			V _{CC} = ±5V, 2.5V step	55			
		To 0.01%, gain = –1V/V	V _{CC} = ±15V, 5V step	90			
			V _{CC} = ±5V, 2.5V step	80			
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	Gain = 1V/V, R _L = 600Ω, f = 1kHz, BW = 80kHz	V _{CC} = ±15V, V _O = 3V _{RMS}	–137	dB		
				0.000014	%		
		Gain = 2V/V, R _L = 600Ω, f = 1kHz, BW = 80kHz	V _{CC} = ±5V, V _O = 1V _{RMS}	–130	dB		
				0.00003	%		
				V _{CC} = ±15V, V _O = 3V _{RMS}	–133	dB	
					0.000022	%	
IMD	Intermodulation distortion	Gain = 1V/V, R _L = 600Ω, SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)	V _{CC} = ±15V, V _O = 3V _{RMS}	–130	dB		
				0.000032	%		
		Gain = 2V/V, R _L = 600Ω, SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)	V _{CC} = ±5V, V _O = 1V _{RMS}	–126	dB		
				0.00005	%		
				–126	dB		
				0.00005	%		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	Gain = 2V/V, V _{CC} = ±5V or ±15V, f = 1MHz V _{O(pp)} = 2V		–91	dBc		
V _n	Input voltage noise	V _{CC} = ±5V or ±15V, f > 10kHz		0.95	nV/√Hz		
I _n	Input current noise	V _{CC} = ±5V or ±15V, f > 10kHz		2.3	pA/√Hz		
	Channel-to-channel crosstalk (OPA2891 only)	V _{CC} = ±5V or ±15V, f = 1MHz		–80	dBc		
DC PERFORMANCE							
V _{OS}	Input offset voltage	V _{CC} = ±5V or ±15V, T _A = 25°C		0.2	1	mV	
	Offset voltage drift	V _{CC} = ±5V or ±15V, T _A = full range		1		μV/°C	
I _{IB}	Input bias current	V _{CC} = ±5V or ±15V	T _A = 25°C	9	20	μA	
			T _A = full range		33		
I _{OS}	Input offset current	V _{CC} = ±5V or ±15V	T _A = 25°C	30	250	nA	
			T _A = full range		400		

5.6 Electrical Characteristics - $R_L = 150\Omega$ (続き)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, and $R_L = 150\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
V _{ICR}	Common-mode input voltage range	V _{CC} = ±15V		±13.8	±14.3		V
		V _{CC} = ±5V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V _{CC} = ±15V, V _{ICR} = ±12V	T _A = 25°C	85	104		dB
			T _A = full range	80			
		V _{CC} = ±5V, V _{ICR} = ±2.5V	T _A = 25°C	90	106		
			T _A = full range	85			
	Input impedance	Common-mode		10 1.2		MΩ pF	
		Differential-mode		6 1.8		kΩ pF	
OUTPUT CHARACTERISTICS							
V _O	Output voltage swing	V _{CC} = ±15V, R _L = 250Ω		±12	±12.9		V
		V _{CC} = ±5V		±3	±3.5		
I _O	Output current ⁽²⁾	R _L = 10Ω	V _{CC} = ±15V	60	200		mA
			V _{CC} = ±5V	50	160		
R _O	Output resistance	Open loop		5			Ω
POWER SUPPLY							
I _{CC}	Supply current (each amplifier)	V _{CC} = ±15V	T _A = 25°C	7.5		10	mA
			T _A = full range			11	
		V _{CC} = ±5V	T _A = 25°C	6.5		9	
			T _A = full range			10	
PSRR	Power-supply rejection ratio	V _{CC} = ±5V or ±15V, T _A = 25°C		90	105		dB
		V _{CC} = ±5V or ±15V, T _A = full range		85			

(1) Slew rate is measured from an output level range of 25% to 75%.

(2) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also [Section 5.1](#).

5.7 Electrical Characteristics - $R_L = 1k\Omega$

at T_A = full range, $V_{CC} = \pm 15V$, and $R_L = 1k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
	Unity gain bandwidth	V _{CC} = ±15V, closed loop			180		MHz
BW	Small-signal bandwidth (–3dB)	Gain = –1V/V or 2V/V	V _{CC} = ±15V		140		MHz
			V _{CC} = ±5V		135		
	Bandwidth for 0.1dB flatness	Gain = –1V/V or 2V/V	V _{CC} = ±15V		9		MHz
			V _{CC} = ±5V		9		
	Full power bandwidth ⁽¹⁾	V _{CC} = ±15V, V _{O(pp)} = 20V			1.7		MHz
		V _{CC} = ±5V, V _{O(pp)} = 5V			5.7		
SR	Slew rate				105		V/μs
t _s	Settling time	To 0.1%, gain = –1V/V	V _{CC} = ±15V, 5V step		70		ns
			V _{CC} = ±5V, 2.5V step		55		
		To 0.01%, gain = –1V/V	V _{CC} = ±15V, 5V step		90		
			V _{CC} = ±5V, 2.5V step		80		
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	Gain = 1V/V, R _L = 2kΩ, f = 1kHz, BW = 80kHz	V _{CC} = ±15V, V _O = 3V _{RMS}		–137		dB
					0.000014		%
			Gain = 2V/V, R _L = 2kΩ, f = 1kHz, BW = 80kHz	V _{CC} = ±5V, V _O = 1V _{RMS}		–130	
					0.00003		%
		Gain = 1V/V, R _L = 2kΩ, SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)		V _{CC} = ±15V, V _O = 3V _{RMS}		–133	
					0.000022		%
Gain = 2V/V, R _L = 2kΩ, SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)	V _{CC} = ±5V, V _O = 1V _{RMS}			–124		dB	
			0.00006		%		
	IMD	Intermodulation distortion	Gain = 1V/V, R _L = 2kΩ, SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)	V _{CC} = ±15V, V _O = 3V _{RMS}		–130	
					0.000032		%
Gain = 2V/V, R _L = 2kΩ, SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)				V _{CC} = ±5V, V _O = 1V _{RMS}		–126	
					0.00005		%
			Gain = 1V/V, R _L = 2kΩ, SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)	V _{CC} = ±15V, V _O = 3V _{RMS}		–126	
					0.00005		%
Gain = 2V/V, R _L = 2kΩ, SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)	V _{CC} = ±5V, V _O = 1V _{RMS}			–120		dB	
			0.0001		%		
	NOISE AND DISTORTION PERFORMANCE						
THD	Total harmonic distortion	Gain = 2V/V, V _{CC} = ±5V or ±15V, f = 1MHz V _{O(pp)} = 2V				–100	dBc
DC PERFORMANCE							
	Open-loop gain	V _{CC} = ±15V, V _O = ±10V	T _A = 25°C	93	100	dB	
			T _A = full range	92			
		V _{CC} = ±5V, V _O = ±2.5V	T _A = 25°C	92	98		
			T _A = full range	91			
V _{OS}	Input offset voltage	V _{CC} = ±5V or ±15V, T _A = 25°C			0.2	1	mV
	Offset voltage drift	V _{CC} = ±5V or ±15V, T _A = full range			1		μV/°C
I _{IB}	Input bias current	V _{CC} = ±5V or ±15V	T _A = 25°C	9	20	μA	
			T _A = full range		33		
I _{OS}	Input offset current	V _{CC} = ±5V or ±15V	T _A = 25°C	30	250	nA	
			T _A = full range		400		
	Input offset current drift	V _{CC} = ±5V or ±15V, T _A = full range			0.2		nA/°C

5.7 Electrical Characteristics - $R_L = 1\text{k}\Omega$ (続き)

at $T_A = \text{full range}$, $V_{CC} = \pm 15\text{V}$, and $R_L = 1\text{k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
V _{ICR}	Common-mode input voltage range	V _{CC} = ±15V		±13.8	±14.3		V
		V _{CC} = ±5V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V _{CC} = ±15V, V _{ICR} = ±12V	T _A = 25°C	85	104		dB
			T _A = full range	80			
		V _{CC} = ±5V, V _{ICR} = ±2.5V	T _A = 25°C	90	106		
			T _A = full range	85			
	Input impedance	Common-mode		10 1.2			MΩ pF
		Differential-mode		6 1.8			kΩ pF
OUTPUT CHARACTERISTICS							
V _O	Output voltage swing	V _{CC} = ±15V		±13	±13.6		V
		V _{CC} = ±5V		±3.4	±3.8		V
POWER SUPPLY							
PSRR	Power-supply rejection ratio	V _{CC} = ±5V or ±15V	T _A = 25°C	90	105		dB
			T _A = full range	85			

(1) Full power bandwidth = slew rate / $[\pi V_{O(pp)}]$.

5.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, gain = $+1\text{V/V}$, $R_L = 150\Omega$, and $R_F = 300\Omega$ (unless otherwise noted)

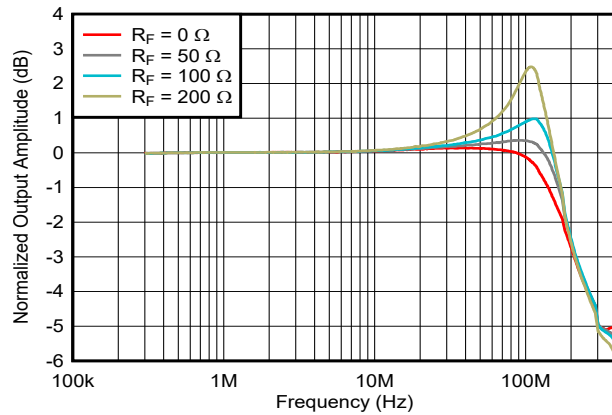


図 5-1. Frequency Response vs Feedback Resistance

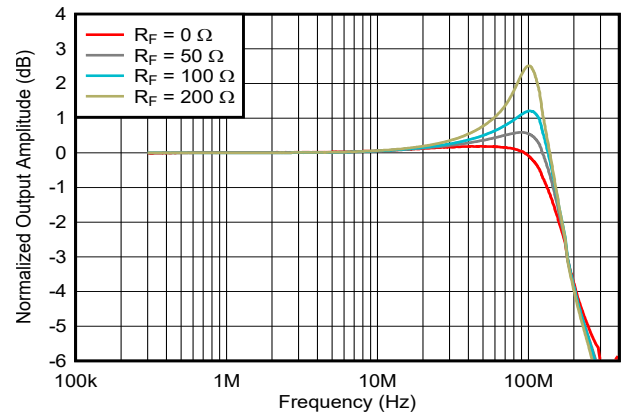


図 5-2. Frequency Response vs Feedback Resistance

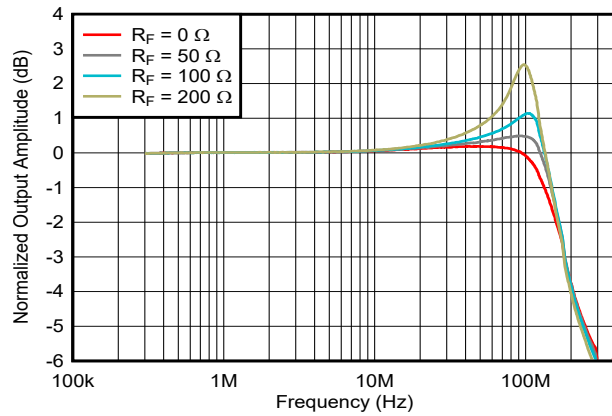


図 5-3. Frequency Response vs Feedback Resistance

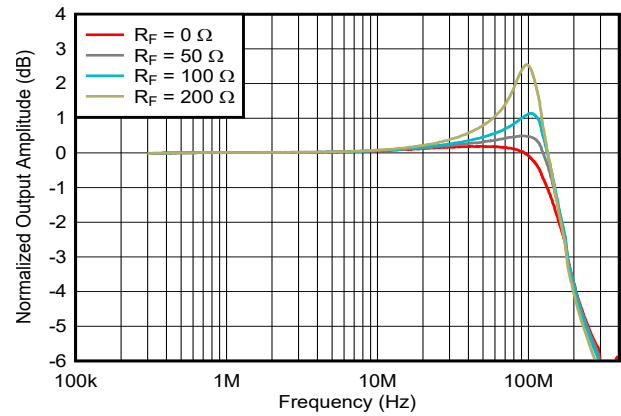


図 5-4. Frequency Response vs Feedback Resistance

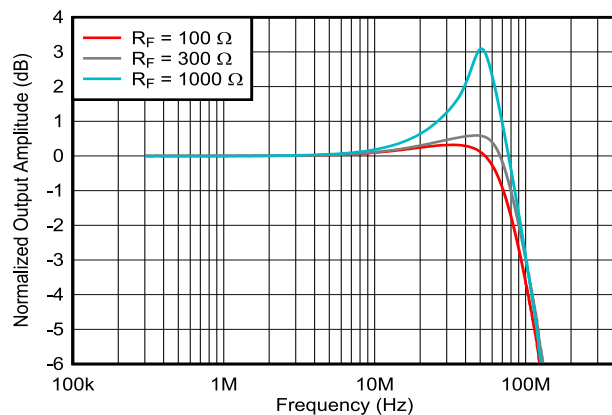


図 5-5. Frequency Response vs Feedback Resistance

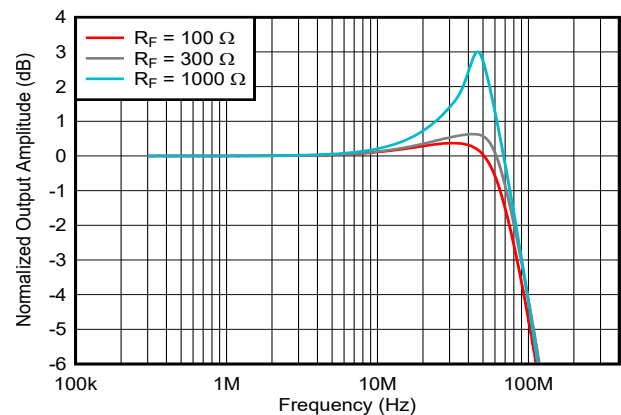


図 5-6. Frequency Response vs Feedback Resistance

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, gain = $+1\text{V/V}$, $R_L = 150\Omega$, and $R_F = 300\Omega$ (unless otherwise noted)

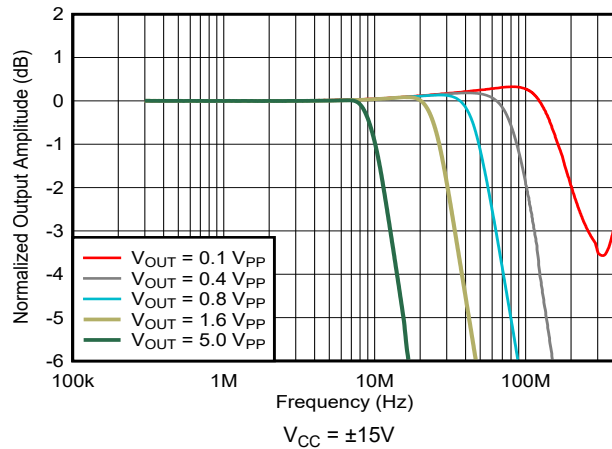


图 5-7. Large-signal Frequency Response

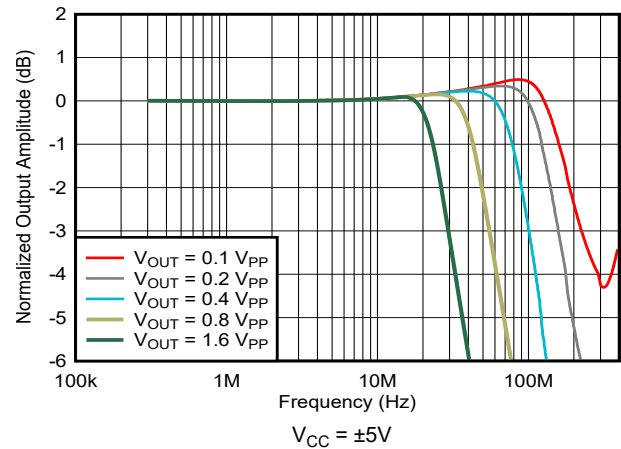


图 5-8. Large-signal Frequency Response

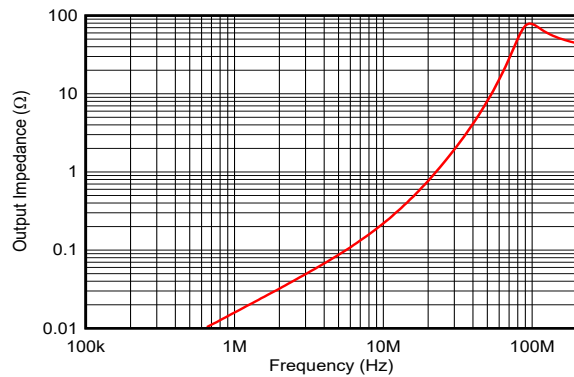


图 5-9. Closed-loop Output Impedance

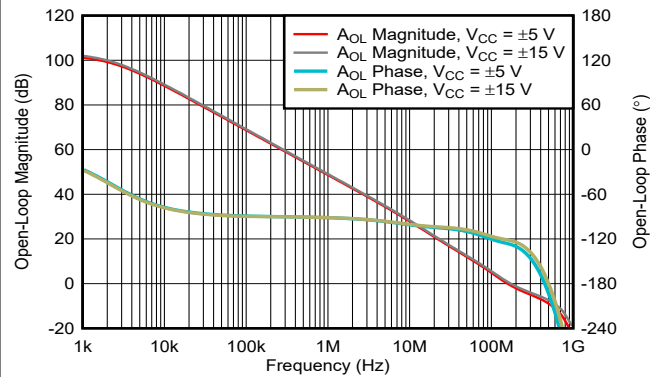


图 5-10. Open-loop Gain and Phase Response

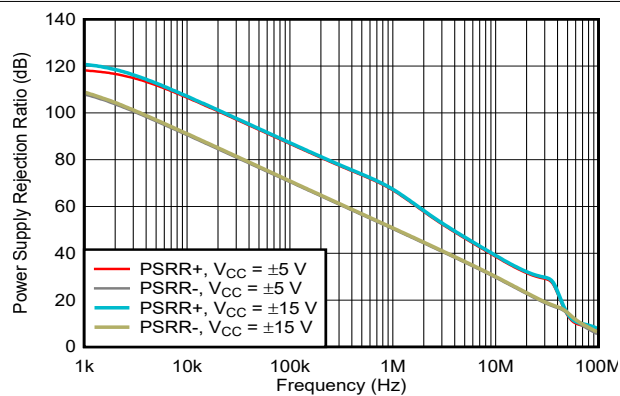


图 5-11. Power-supply Rejection Ratio vs Frequency

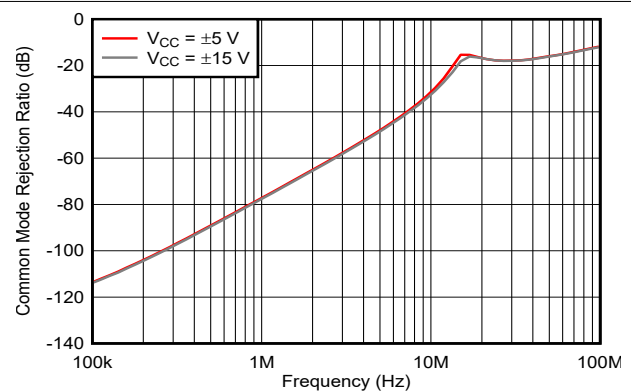


图 5-12. Common-mode Rejection Ratio vs Frequency

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, gain = $+1\text{V/V}$, $R_L = 150\Omega$, and $R_F = 300\Omega$ (unless otherwise noted)

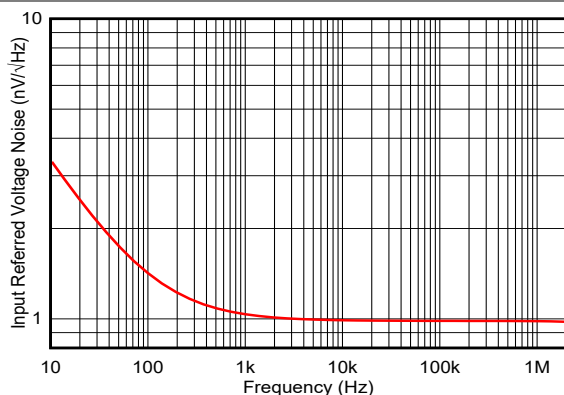


FIG 5-13. Input-Referred Voltage Noise vs Frequency

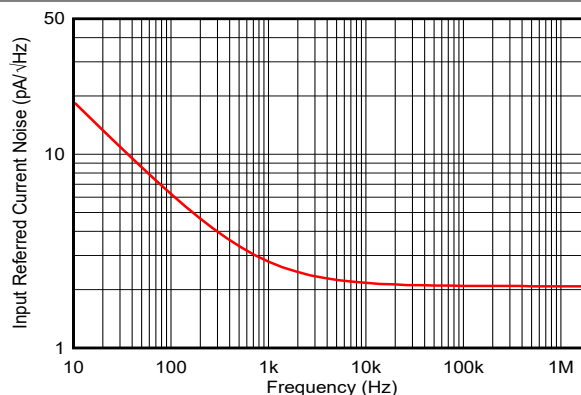
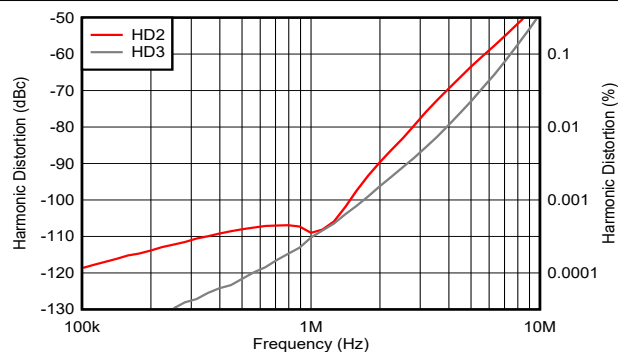
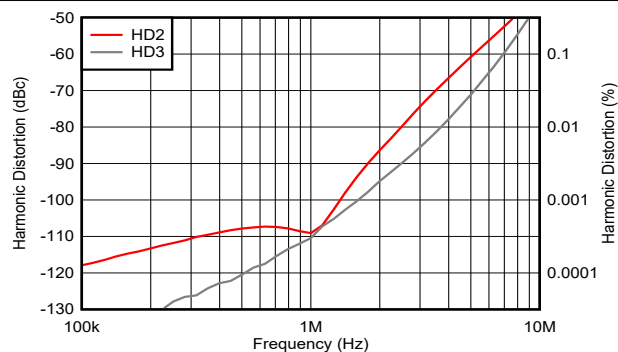


FIG 5-14. Input-Referred Current Noise vs Frequency



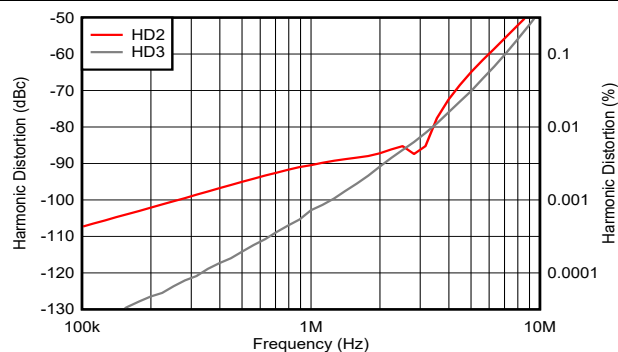
$V_{CC} = \pm 15\text{V}$, gain = $+2\text{V/V}$, $R_L = 1\text{k}\Omega$, $V_{OUT} = 2\text{V}_{PP}$

FIG 5-15. Harmonic Distortion vs Frequency



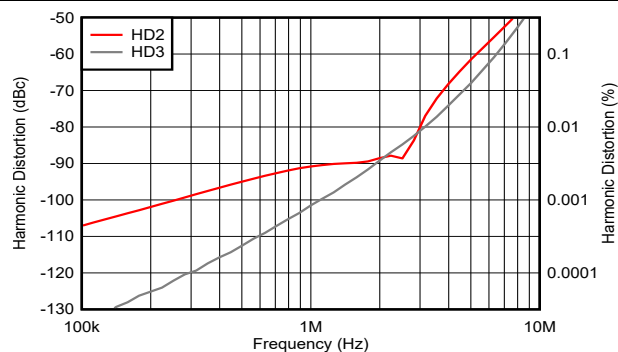
$V_{CC} = \pm 5\text{V}$, gain = $+2\text{V/V}$, $R_L = 1\text{k}\Omega$, $V_{OUT} = 2\text{V}_{PP}$

FIG 5-16. Harmonic Distortion vs Frequency



$V_{CC} = \pm 15\text{V}$, gain = $+2\text{V/V}$, $R_L = 150\Omega$, $V_{OUT} = 2\text{V}_{PP}$

FIG 5-17. Harmonic Distortion vs Frequency

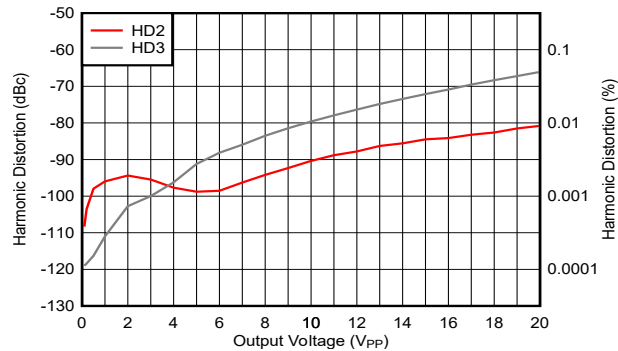


$V_{CC} = \pm 5\text{V}$, gain = $+2\text{V/V}$, $R_L = 150\Omega$, $V_{OUT} = 2\text{V}_{PP}$

FIG 5-18. Harmonic Distortion vs Frequency

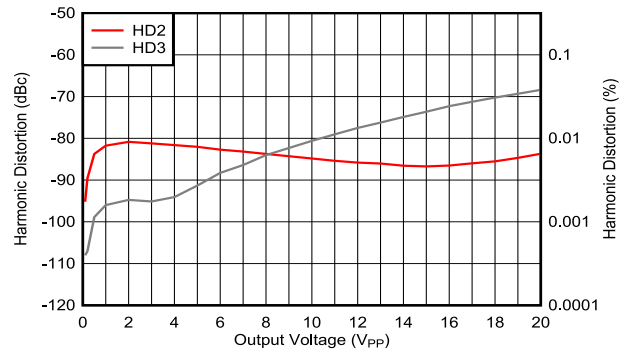
5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, gain = $+1\text{V/V}$, $R_L = 150\Omega$, and $R_F = 300\Omega$ (unless otherwise noted)



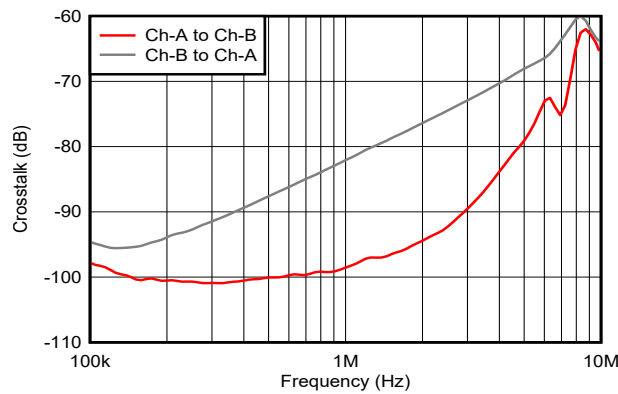
$V_{CC} = \pm 15\text{V}$, gain = $+5\text{V/V}$, $R_L = 1\text{k}\Omega$, $f = 1\text{MHz}$

图 5-19. Harmonic Distortion vs Peak-to-Peak Output Voltage



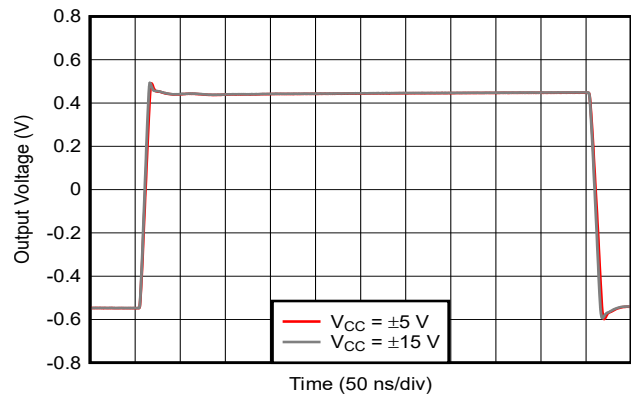
$V_{CC} = \pm 15\text{V}$, gain = $+5\text{V/V}$, $R_L = 150\Omega$, $f = 1\text{MHz}$

图 5-20. Harmonic Distortion vs Peak-to-Peak Output Voltage



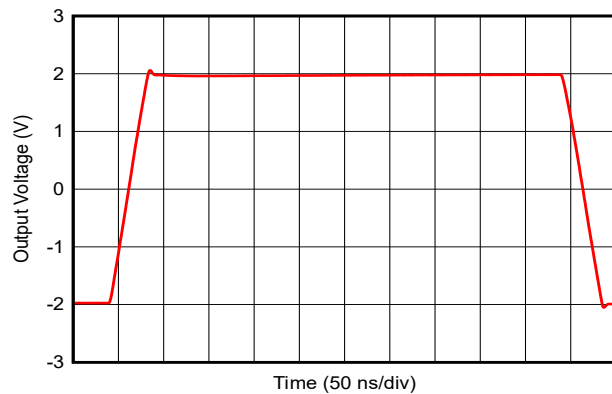
$V_{CC} = \pm 15\text{V}$, gain = $+2\text{V/V}$

图 5-21. OPA2891 Crosstalk vs Frequency



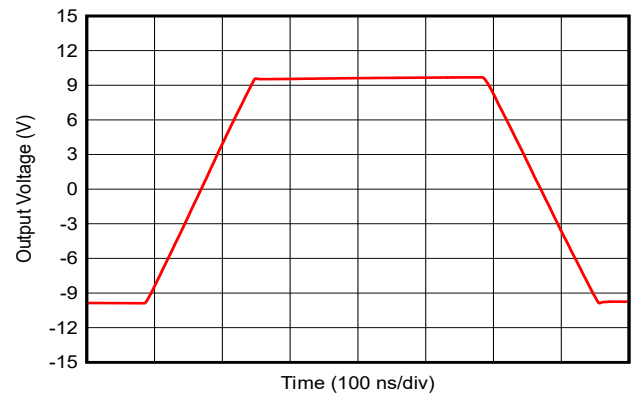
Gain = $+2\text{V/V}$

图 5-22. 1V Step Response



$V_{CC} = \pm 5\text{V}$, gain = -1V/V , $R_F = 430\Omega$

图 5-23. 4V Step Response



Gain = $+2\text{V/V}$

图 5-24. 20V Step Response

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, gain = $+1\text{V/V}$, $R_L = 150\Omega$, and $R_F = 300\Omega$ (unless otherwise noted)

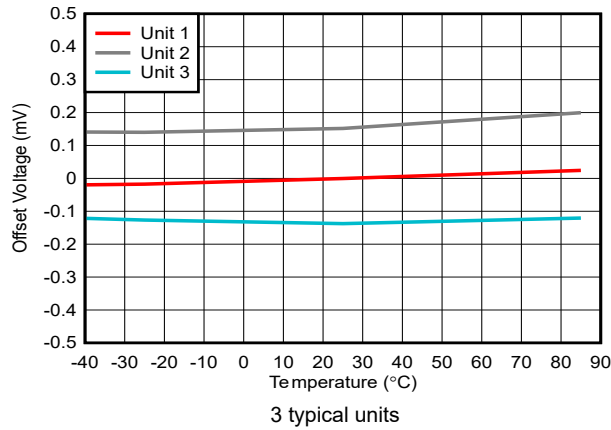


図 5-25. Input Offset Voltage vs Ambient Temperature

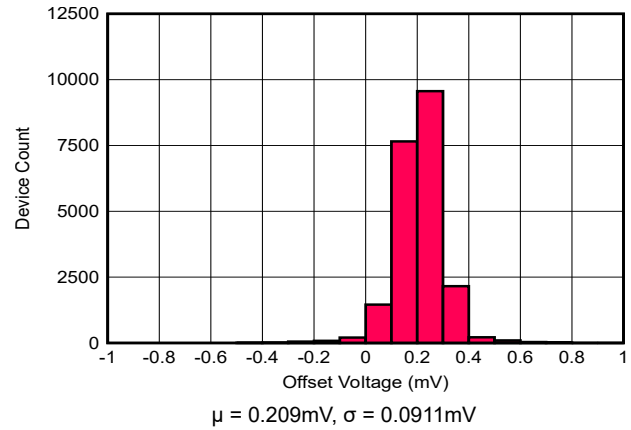


図 5-26. Voltage Offset Distribution

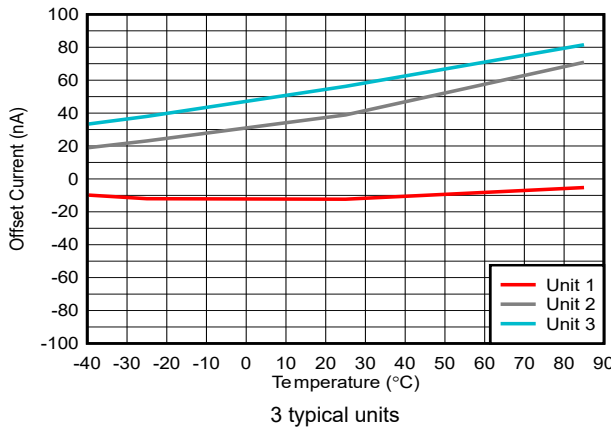


図 5-27. Input Offset Current vs Ambient Temperature

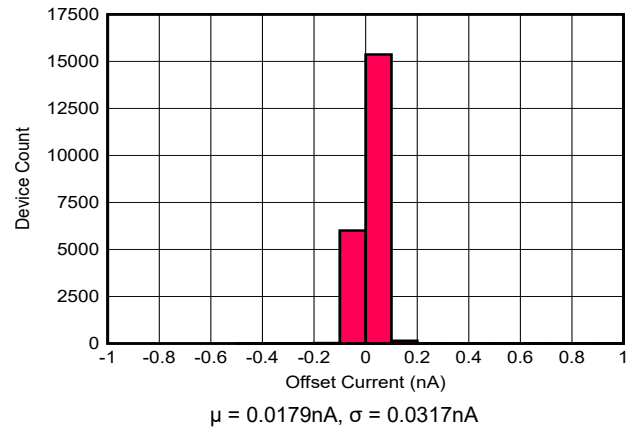


図 5-28. Input Offset Current vs Ambient Temperature

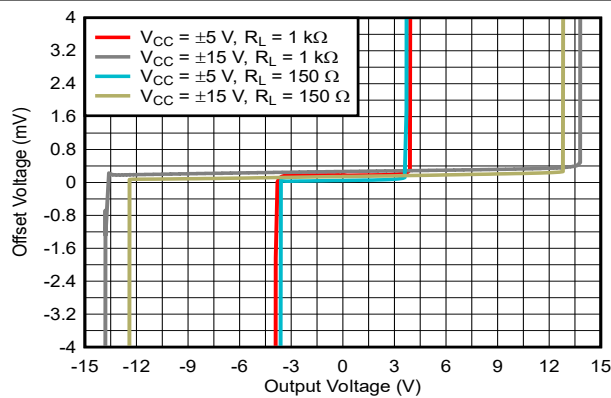


図 5-29. Offset Voltage vs Output Voltage

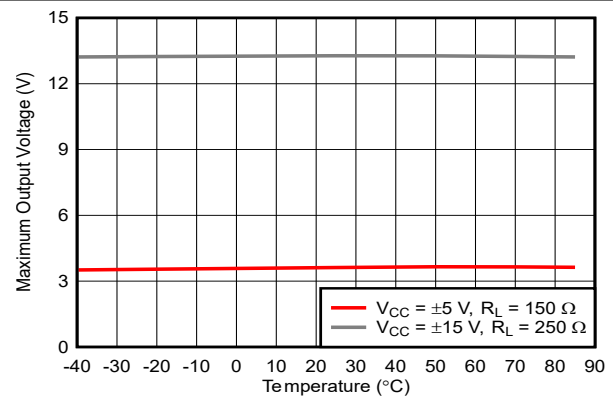


図 5-30. Maximum Output Voltage Swing vs Ambient Temperature

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, gain = $+1\text{V/V}$, $R_L = 150\Omega$, and $R_F = 300\Omega$ (unless otherwise noted)

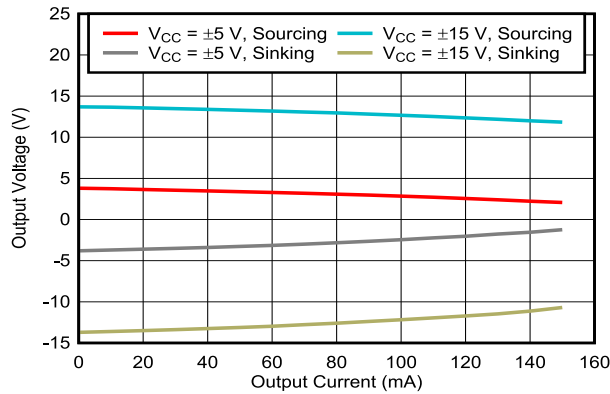


FIG 5-31. Output Swing vs Load Current

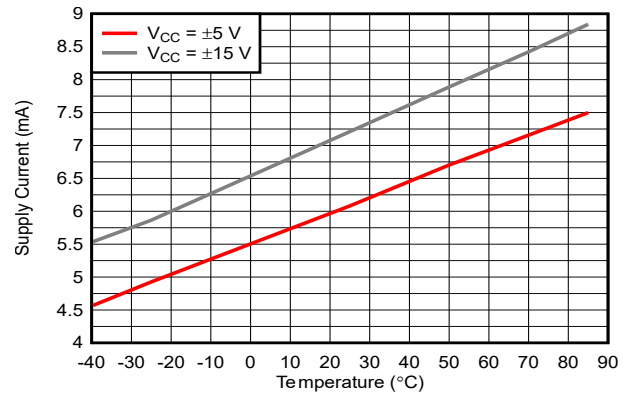


FIG 5-32. Supply Current vs Ambient Temperature

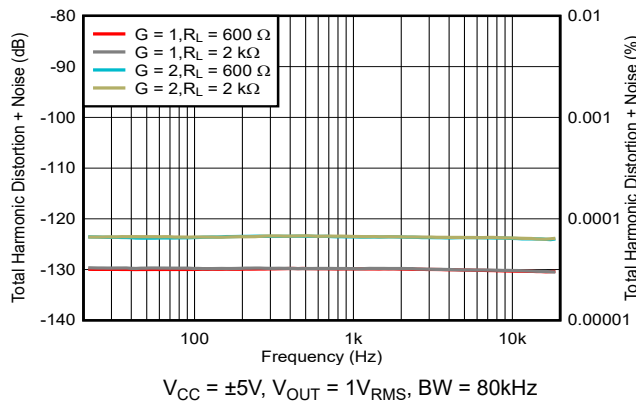


FIG 5-33. THD+N vs Frequency

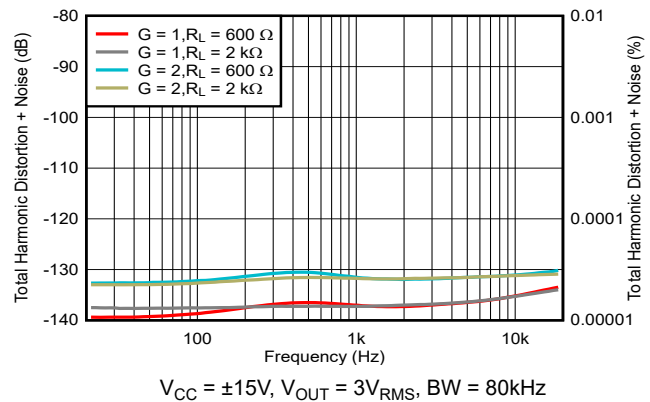


FIG 5-34. THD+N vs Frequency

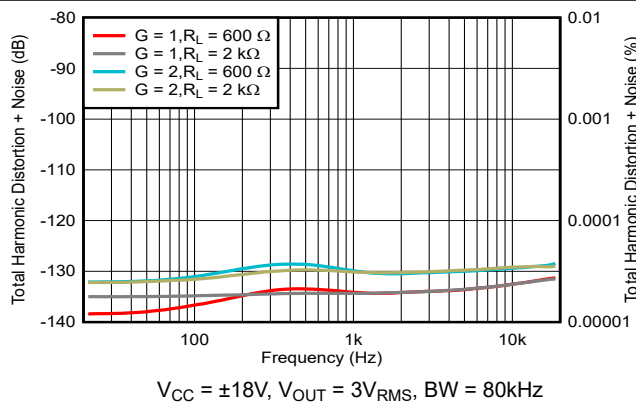


FIG 5-35. THD+N vs Frequency

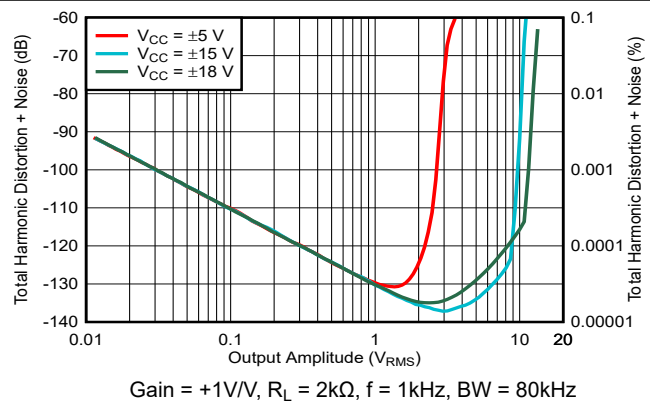


FIG 5-36. THD+N Ratio vs Output Amplitude

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, gain = $+1\text{V/V}$, $R_L = 150\Omega$, and $R_F = 300\Omega$ (unless otherwise noted)

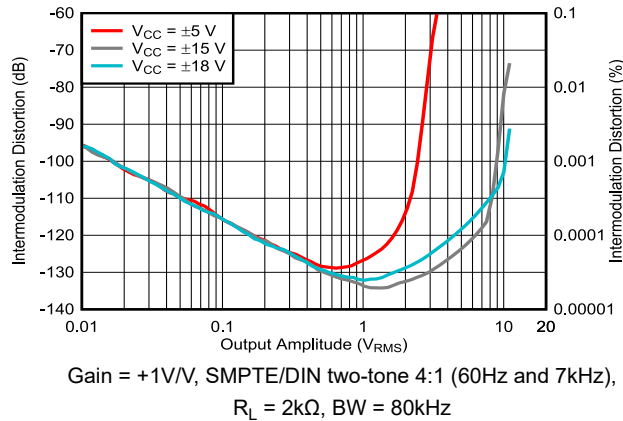


Figure 5-37. Intermodulation Distortion vs Amplitude

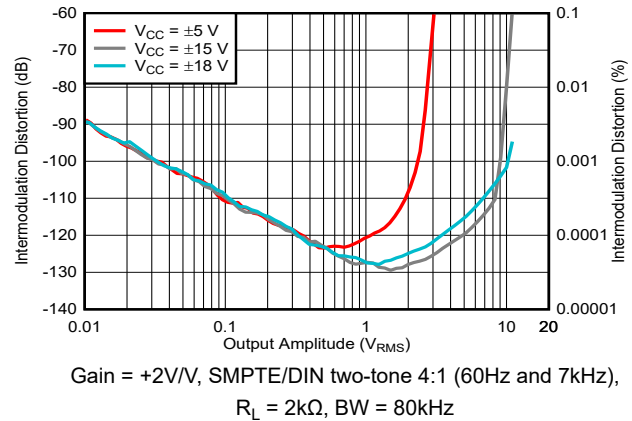


Figure 5-38. Intermodulation Distortion vs Amplitude

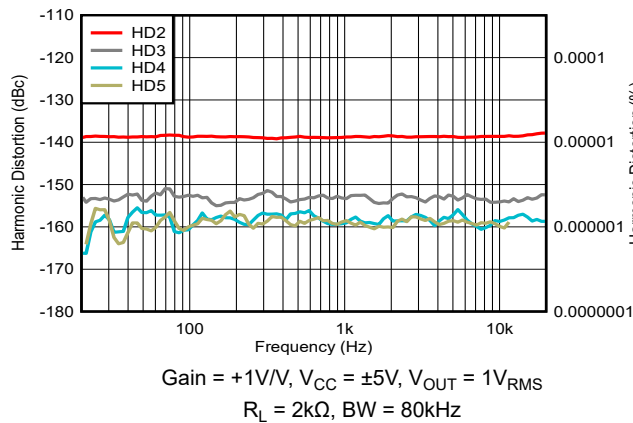


Figure 5-39. Distortion Harmonics vs Frequency

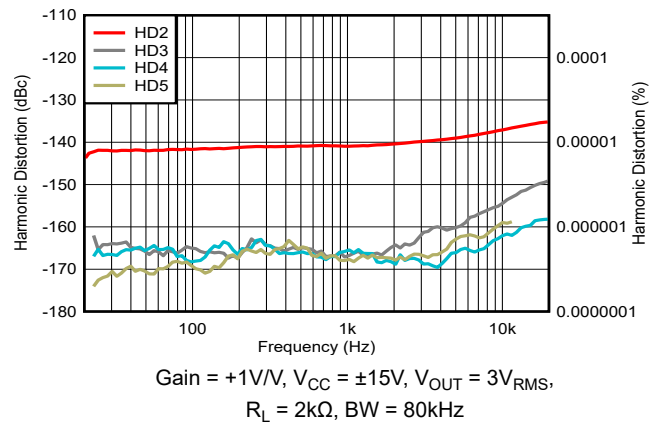


Figure 5-40. Distortion Harmonics vs Frequency

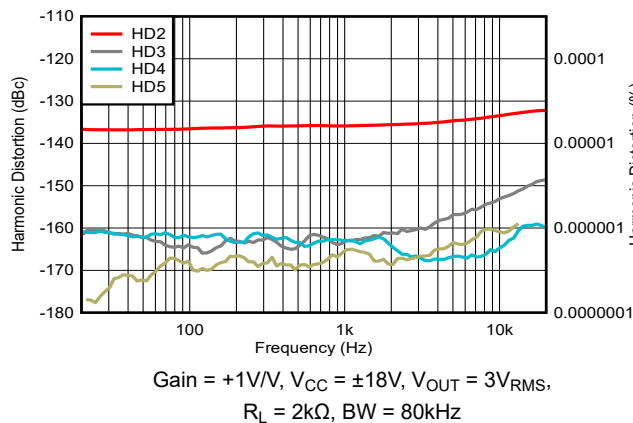


Figure 5-41. Distortion Harmonics vs Frequency

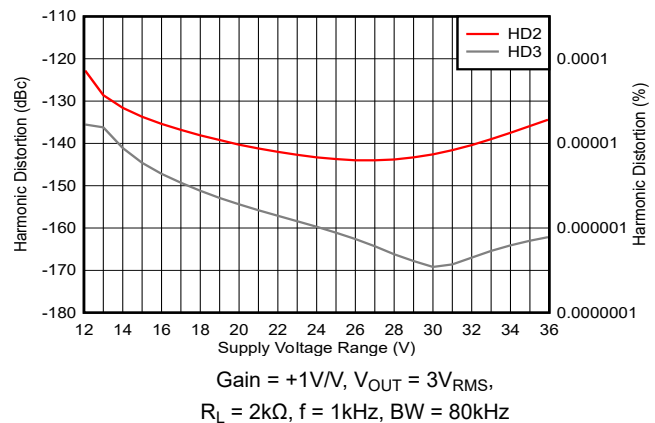


Figure 5-42. Distortion Harmonics vs Supply Voltage

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, gain = $+1\text{V/V}$, $R_L = 150\Omega$, and $R_F = 300\Omega$ (unless otherwise noted)

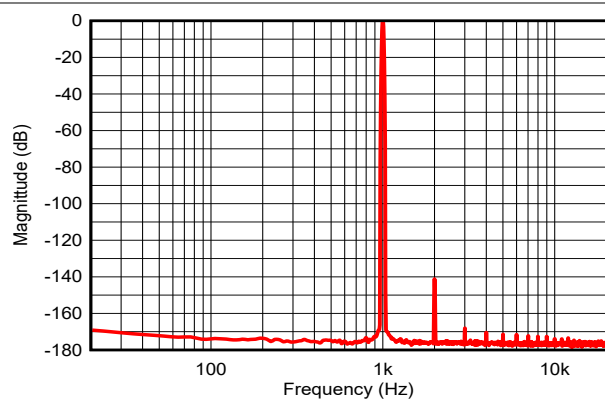


Figure 5-43. 1kHz Output Spectrum

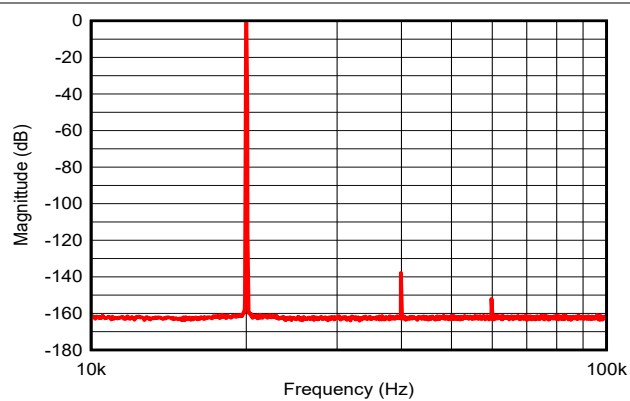


Figure 5-44. 20kHz Output Spectrum

6 Detailed Description

6.1 Overview

The OPAx891 is a high-speed operational amplifier configured in a voltage-feedback architecture. These amplifiers are built using a 36V, complementary bipolar process with NPN and PNP transistors that possess an f_T of several GHz. This configuration results in exceptionally high-performance amplifiers with wide bandwidth, high slew rate, fast settling time, and low distortion.

6.2 Functional Block Diagrams

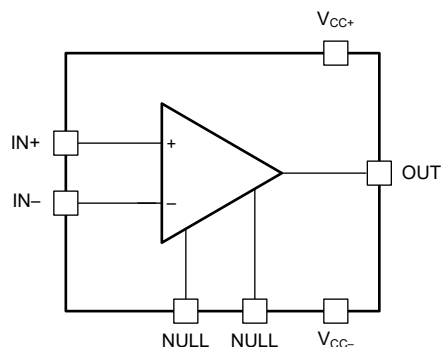


図 6-1. OPA891: Single Channel

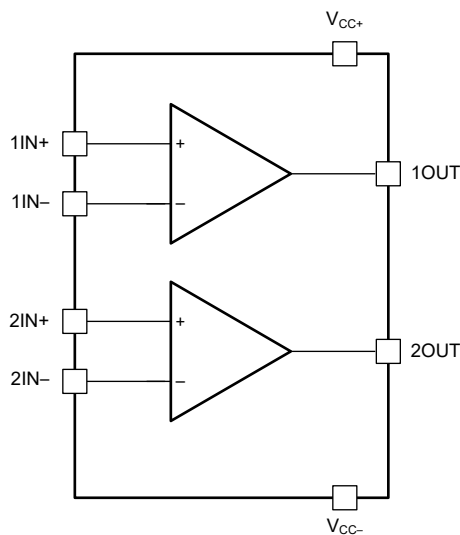


図 6-2. OPA2891: Dual Channel

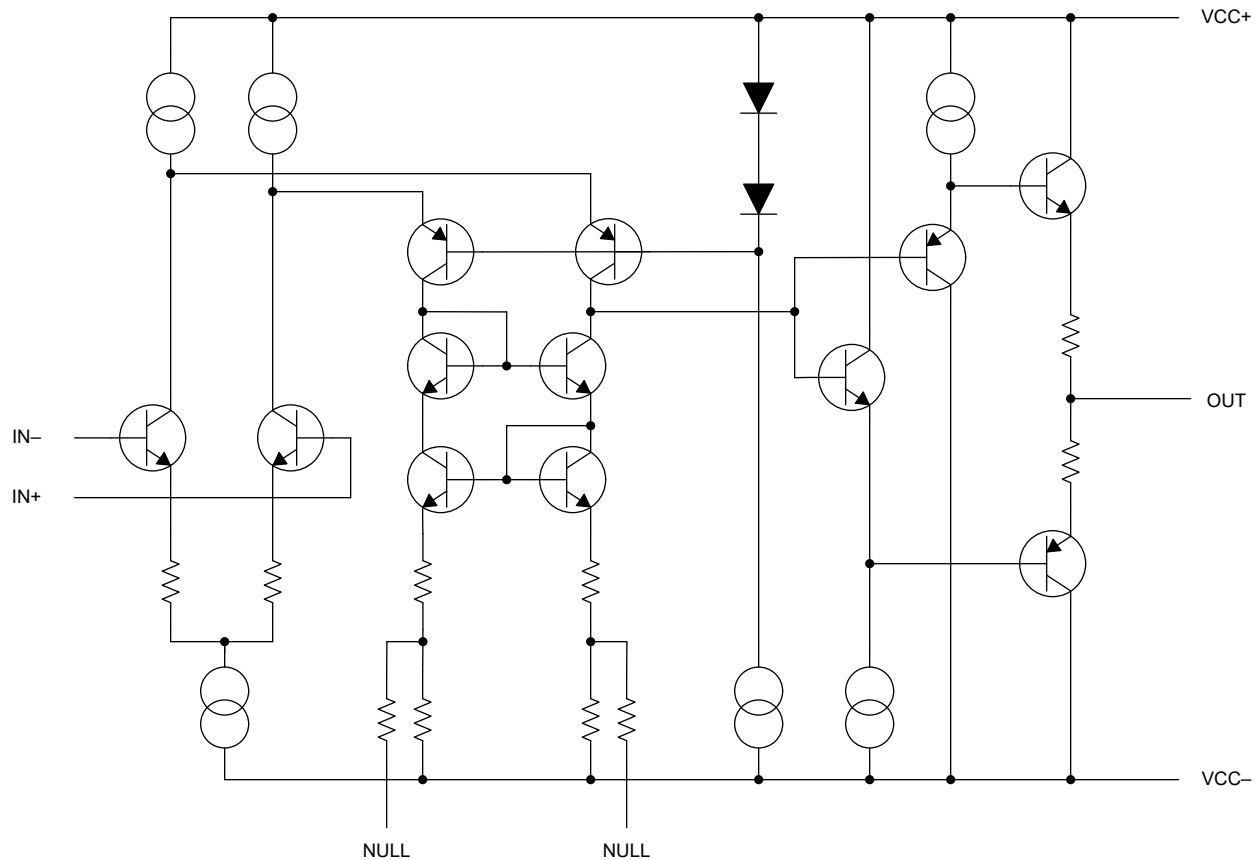


Figure 6-3. OPA891 Simplified Schematic

6.3 Feature Description

6.3.1 Offset Nulling

The OPAx891 have a very low input offset voltage for high-speed amplifiers. However, if additional correction is required, an offset nulling function is provided on the OPA891. To adjust the input offset voltage, place a potentiometer between pin 1 and pin 8 of the device, and tie the wiper to the negative supply.  6-4 shows this feature.

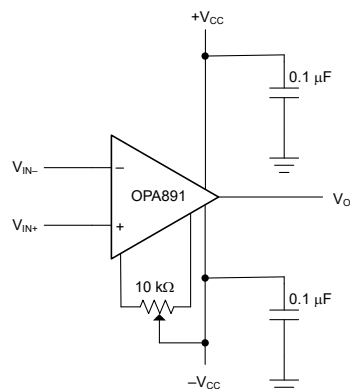


图 6-4. Offset Nulling Schematic

6.4 Device Functional Modes

The OPAx891 family has a single functional mode and can be used with both single-supply or split power-supply configurations. The power-supply voltage must be greater than 9V ($\pm 4.5V$) and less than 36V ($\pm 18V$).

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Driving a Capacitive Load

The OPAX891 are internally compensated to maximize bandwidth and slew-rate performance. To maintain stability, take additional precautions when driving capacitive loads with a high-performance amplifier. As a result of the internal compensation, significant capacitive loading directly on the output node decreases the device phase margin, and potentially lead to high-frequency ringing or oscillations. Therefore, for capacitive loads greater than 10pF, place an isolation resistor in series with the output of the amplifier. [Figure 7-1](#) shows this configuration. For most applications, a minimum resistance of 20Ω is recommended. In 75Ω transmission systems, setting the series resistor value to 75Ω is a beneficial choice because this value isolates any capacitance loading and provides source impedance matching.

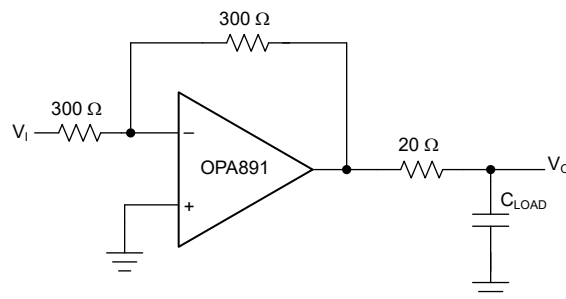


Figure 7-1. Driving a Capacitive Load

7.1.2 Low-Pass Filter Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. [Figure 7-2](#) shows how the simplest way to accomplish this limiting is to place an RC filter at the noninverting pin of the amplifier.

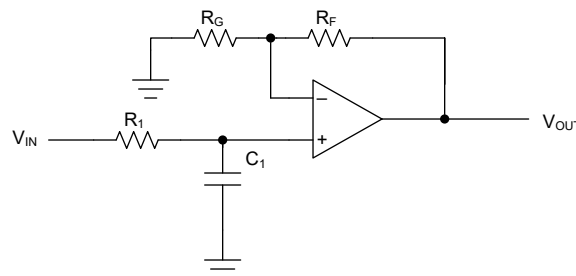


Figure 7-2. Single-Pole Low-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + sR_1C_1}\right) \quad (1)$$

If more attenuation at higher frequencies is required, a multiple-pole filter is required. [Figure 7-3](#) shows a common implementation of a second-order filter called a Sallen-Key filter. When designing this type of filter, choose an

amplifier with a bandwidth that is approximately an order of magnitude larger than the desired filter bandwidth. See [Active Low-pass Filter Design](#) for more detailed active-filter design information.

Assuming $R_1 = R_2 = R$ and $C_1 = C_2 = C$, use 式 2 to set the bandwidth of the filter.

$$f_{3dB} = \frac{1}{2\pi RC} \quad (2)$$

The Q-factor of a filter controls the amount of peaking of the small-signal frequency response and the settling time of the pulse response. Set Q to 0.707 to provide a Butterworth response with a maximally-flat pass-band. Choose the ratio of R_F and R_G to obtain the desired Q value as shown in 式 3.

$$\frac{R_F}{R_G} = 2 - \frac{1}{Q} \quad (3)$$

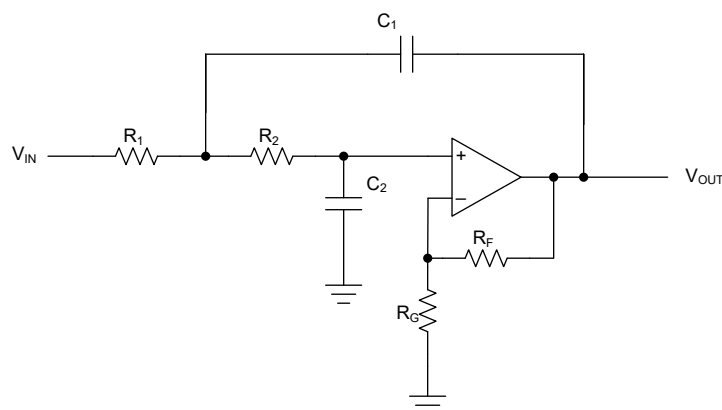


図 7-3. Two-Pole Low-Pass Sallen-Key Filter

7.2 Typical Application

This section demonstrates multiplexing several analog input signals to a high-performance driver amplifier that subsequently drives a single, high-resolution, high-speed successive-approximation-register (SAR) analog-to-digital converter (ADC). This example uses the [ADS8411](#) and the [TS5A3159](#) or [TS5A3359](#) as the ADC and the multiplexer, respectively. This application uses the OPAx891 as the operational amplifier.

図 7-4 details how the example system consists of an ADC (ADS8411), a driving operational amplifier (OPA891), a multiplexer (TS5A3159), an ac source, a dc source, and two driving operational amplifiers.

The driving amplifiers OPA1 and OPA2 are shown as two OPA891 amplifiers. Alternatively, use a single OPA2891 to save on cost and board space. The purpose of these op-amps is to make the input sources present a low impedance to rest of the circuit. Additionally, to maintain signal fidelity, these operational amplifiers must have low noise and distortion. The third OPA891, labeled OPA3 in 図 7-4, is used to maintain switching speed and drive the ADC. The passive band-pass filter before the ADC reduces unwanted noise.

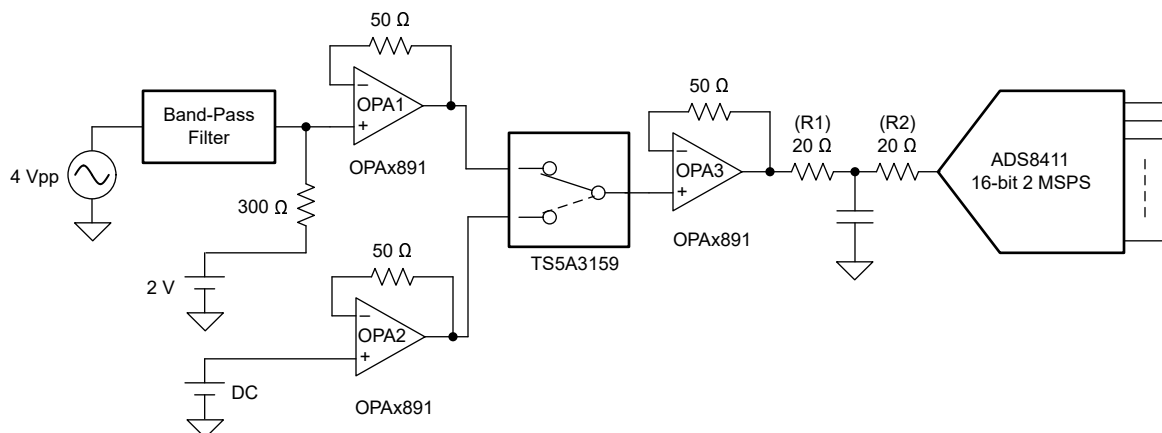


図 7-4. Multiplexing Set-Up to Drive a High-Performance ADC

7.2.1 Design Requirements

The objective is to design a multiplexed digitizer system with the dynamic performance shown in 表 7-1.

表 7-1. Design Specifications

DEVICE SPEED (MSPS)	INPUT FREQUENCY (kHz)	SNR (dB)	THD (dB)	CROSSTALK (dB)
2	20	> 84	< -90	< -110
2	100	> 84	< -90	< -96

7.2.2 Detailed Design Procedure

The ADS8411 is a 16-bit, 2MSPS analog-to-digital converter (ADC) with a 4V reference. The ADS8411 has a unipolar single-ended input and includes a 16-bit capacitor-based SAR ADC, with inherent sample and hold. The output is a 16-bit parallel interface.

The TS5A3159 is a single-pole, double-throw (SPDT) analog switch that is designed to operate from 1.65V to 5.5V. The TS5A3159 offers a low on state resistance and an excellent on resistance matching with the break-before-make feature to prevent signal distortion during the transfer of a signal from one channel to another. Additionally, the TS5A3159 provides excellent total harmonic distortion (THD) performance and consumes low power. The TS5A3359 is a single-pole, triple-throw (SP3T) version of the same switch.

7.2.2.1 Selection of Multiplexer

Figure 7-5 shows an equivalent circuit diagram of one of the channels of a multiplexer. C_S is the input capacitance of the channel; C_D is the output capacitance of the channel. R_{ON} is the resistance of the channel when the channel is turned ON. C_L and R_L are the load capacitance and resistance, respectively. V_{IN} is the input voltage of the source. R_S is the resistance of the source. V_{OUT} is the output voltage of the multiplexer.

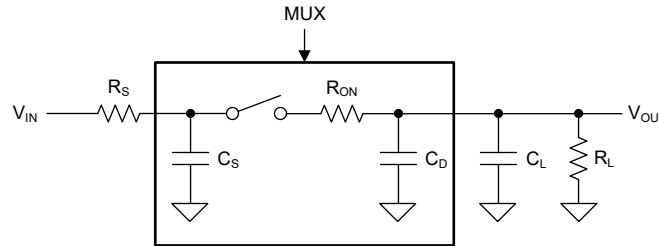


Figure 7-5. Multiplexer Equivalent Circuit

Settling time is improved when the values of R_S , R_{ON} , C_S , C_D , and C_L are small, and the value of R_L is large.

For TS5A3159:

- $R_{ON} = 1\Omega$
- $C_S = C_D = 84\text{pF}$

Typical values for the extrinsic parameters are

- $R_S = 50\Omega$
- $C_L = 5\text{pF}$
- $R_L = 10\text{k}\Omega$
- T_{RC} (time constant) = 8.65ns

For a 16-bit system, at least 18-bit settling is desired to minimize distortion from settling artifacts. For a 18-bit settling, the circuit response time required is $(18 \times \ln 2) \times T_{RC} = 108\text{ns}$, which is less than 2MSPS sampling time of 500ns. If the settling time is more than the conversion time of the ADC, the output of the multiplexer does not settle to the required accuracy resulting in distortion.

One more important parameter to consider when selecting a multiplexer is the on-state resistance variation with voltage. This variation also affects distortion because R_{ON} and R_L act like a resistor divider circuit. Any variation of R_{ON} with voltage affects the output voltage.

7.2.2.2 Signal Source

The input signal source must be a low-noise, low-distortion source with low source resistance. As discussed in the earlier section, the source resistance also must be small to avoid impacting settling time. If the source is not a low-noise and low-distortion source, a passive band-pass filter can be added to improve the signal quality as shown in Figure 7-4.

7.2.2.3 Driving Amplifier

The driving operational amplifier (OPA3 in Figure 7-4) in this application must have good slew rate, bandwidth, low noise, and distortion. The input of the operational amplifier can result in a maximum step of 4V because of MUX switching. As a result, even if the signal bandwidth is low, the driving amplifier must settle from a 4V step within one ADC sampling frame to avoid signal distortion. In this example, the settling requirement due to the ADC selection is 500ns. The OPA891 is a good choice in this application due to the high slew rate and low distortion of this operational amplifier.

7.2.2.4 Driving Amplifier Bandwidth Restriction

Restricting excess bandwidth use by including a passive RC filter before the ADC results in better SNR and THD. However, restricting the bandwidth too much results in a excessive operational amplifier settling time. If the amplifier output does not settle quick enough, some residual charges from the previous channel remain in the next sampling interval and appear as crosstalk. One approach to solve this settling issue is to reduce the throughput of the ADC. However, the high sample rate ADC is often selected to meet the need to acquire higher frequency signals, limiting the freedom to reduce the ADC throughput. Due to these tradeoffs, the choice of the filter capacitor becomes critical. [Figure 7-6](#) and [Figure 7-7](#) show SNR and crosstalk as a function of the filter capacitor.

[Figure 7-8](#) shows input settling behavior with three different filter capacitor values. The value of the capacitor changes to filter bandwidth. As the filter bandwidth increases, the settling time improves as shown in [Equation 4](#).

$$\text{Filter Bandwidth} \cong \frac{1}{2\pi R_1 C_1} \quad (4)$$

7.2.3 Application Curves

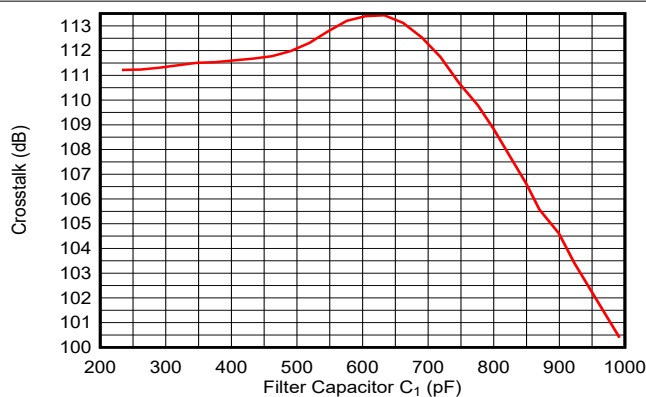


Figure 7-6. SNR vs Filter Capacitor

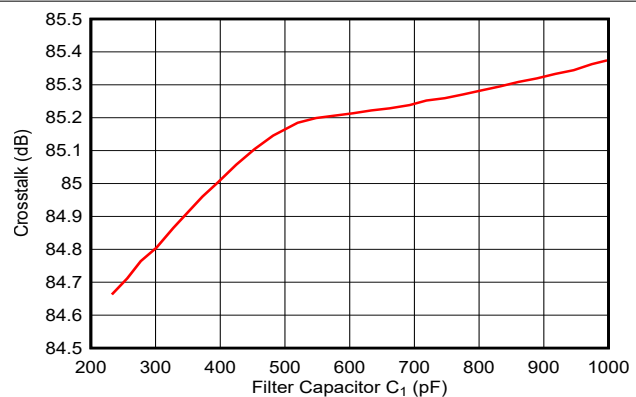


Figure 7-7. Crosstalk vs Filter Capacitor

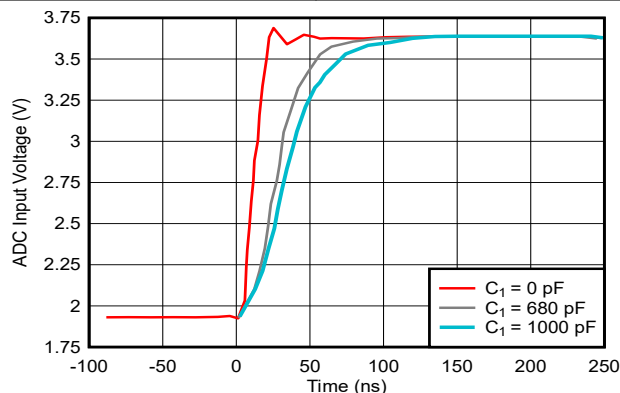


Figure 7-8. Input to ADC for Various Values of Filter Capacitors

7.3 Power Supply Recommendations

The OPAx891 family operates with a single supply or with dual supplies. Choose supplies that provide for the required headroom to supply rails as specified by the common-mode input range (CMIR). Operating from a single supply has numerous advantages. With the negative supply at ground, the dc errors due to the $-PSRR$ term are minimized. Decouple supplies as close to the amplifier as possible with low inductance capacitors decoupled to ground. When operating on a board with high-speed digital signals, provide isolation between digital signal noise and the analog input pins. When using a ground plane, remove the ground plane close to input sensitive pins to reduce stray parasitics that adversely impact device performance. For split-supply operation, an optional supply decoupling capacitor across the two power supplies improves second harmonic distortion performance.

7.4 Layout

7.4.1 Layout Guidelines

To achieve the levels of high-frequency performance of the OPAx891, follow proper printed-circuit board (PCB), high-frequency design techniques. The following is a general set of guidelines. In addition, a OPAx891 evaluation board is available to use as a guide for layout or for evaluating the device performance.

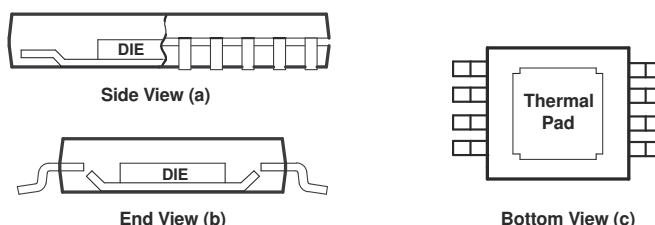
- **Ground planes**—make sure that the ground plane used on the board provides all components with a low-inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize stray capacitance.
- **Proper power-supply decoupling**—use a 6.8 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor on each supply pin. Sharing the tantalum capacitor among several amplifiers is possible depending on the application, but always use a 0.1 μ F ceramic capacitor on the supply pin of every amplifier. In addition, place the 0.1 μ F capacitor as close as possible to the supply pin. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. Strive for distances of less than 0.1 inch (2.54mm) between the device power pins and the ceramic capacitors.
- **Short trace runs or compact part placements**—optimum high-frequency performance is achieved when stray series inductance has been minimized. To reduce stray series inductance, make the circuit layout as compact as possible, thereby minimizing the length of all trace runs. Focus attention on the inputs of the amplifier, keeping the trace lengths as short as possible. This layout helps to minimize stray capacitance at the input of the amplifier.
- **Sockets**—TI does not recommend sockets for high-speed operational amplifiers. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs and compact part placements**—Improved high-frequency performance is achieved when stray series inductance is minimized. To reduce stray series inductance, the circuit layout must be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention must be provided to the inverting input of the amplifier. The length must be kept as short as possible. This design decision helps minimize stray capacitance at the input of the amplifier.

7.4.1.1 General PowerPAD™ Integrated Circuit Package Design Considerations

The OPAx891 is available in a thermally-enhanced DGN package, which is a member of the PowerPAD™ integrated circuit package family. This package is constructed using a downset lead frame upon which the die is mounted [see [Figure 7-9\(a\)](#) and [Figure 7-9\(b\)](#)]. This arrangement results in the lead frame exposed as a thermal pad on the underside of the package [see [Figure 7-9\(c\)](#)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD™ integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are soldered), the thermal pad can be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat is conducted away from the package into a ground plane or other heat-dissipating device.

The PowerPAD™ integrated circuit package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of sinking heat.



Note: The thermal pad is electrically isolated from all pins in the package.

Figure 7-9. Views of Thermally-enhanced DGN Package

Although there are many ways to properly dissipate heat in this device, the following steps show the recommended approach.

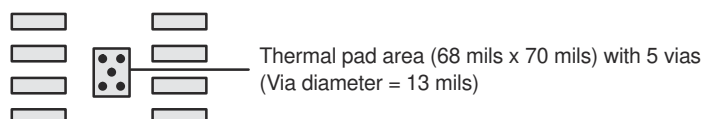


Figure 7-10. PowerPAD™ Integrated Circuit Package PCB Etch and Via Pattern

1. Prepare the PCB with a top-side etch pattern as shown in [Figure 7-10](#). There must be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes must be 13 mils (0.3302mm) in diameter. The reason to keep the holes small is to discourage solder wicking through the holes during reflow.
3. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. This action helps dissipate the heat generated by the OPAx891 device. The additional vias can be of any diameter because wicking is not a concern outside of the thermal pad area.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPAx891 package must connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask must leave the pins of the package and the thermal pad area with the five holes exposed. The bottom-side solder mask must cover the five holes of the thermal pad area, which prevents solder from pulling away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and to all the device pins.
8. With these preparatory steps in place, the OPAx891 device is placed in position and run through the solder reflow operation as any standard surface-mount component.

7.4.2 Layout Example

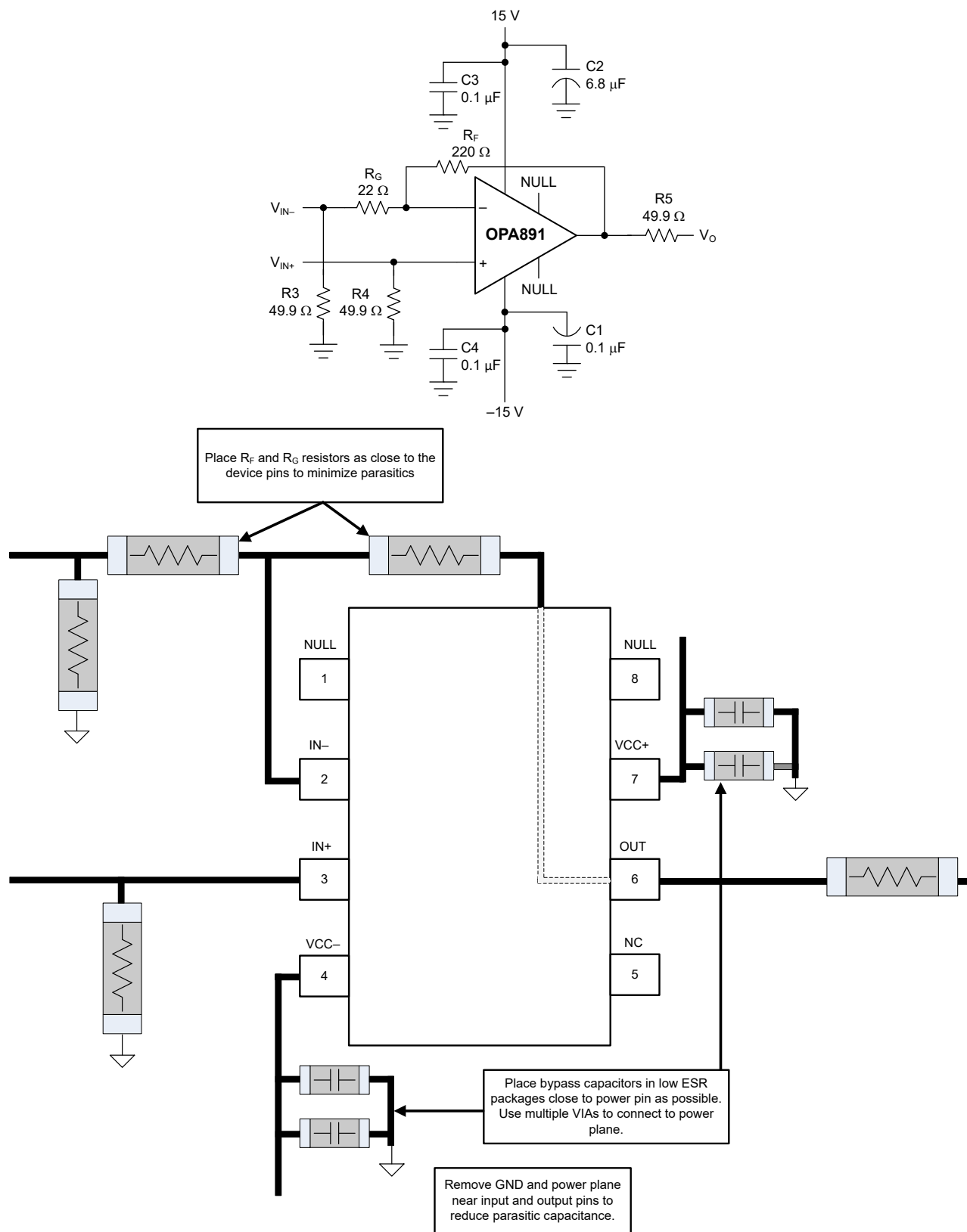


図 7-11. Layout Recommendations

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Noise Analysis for High-Speed Op Amps application note](#)
- Texas Instruments, [PowerPAD™ Thermally Enhanced Package application note](#)
- Texas Instruments, [DEM-OPA-SO-1A Demonstration Fixture user's guide](#)
- Texas Instruments, [DEM-OPA-SO-2A Demonstration Fixture user's guide](#)
- Texas Instruments, [DEM-OPA-MSOP-2A Demonstration Fixture user's guide](#)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

8.4 Trademarks

PowerPAD™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (June 2024) to Revision B (July 2024)	Page
• OPA2891 のステータスを「事前情報」から「量産データ」(アクティブ)に変更.....	1
• Added thermal pad information to Tables 4-1 and 4-2.....	3
• Updated <i>Thermal Information: OPA2891</i> for the D and DGN packages.....	6
• Deleted Supply voltage from <i>Electrical Characteristics</i> as included in <i>Recommended Operating Conditions</i>	7

Changes from Revision * (November 2023) to Revision A (June 2024)	Page
• Deleted erroneous V_O test condition for IMD in <i>Electrical Characteristics - THS4031</i> , $R_L = 1k\Omega$	9
• Changed unit from μA to nA for Input offset current in <i>Electrical Characteristics - $R_L = 1k\Omega$</i>	9

-
- Changed gain from +2V/V to +1V/V in *Typical Characteristics* 11
 - Changed abscissa axis label of Figure 5-23, *20V Step Response*, from 10ns/div to 100ns/div..... 11
-

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2891DGNR	Active	Production	HVSSOP (DGN) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2891
OPA2891DGNR.B	Active	Production	HVSSOP (DGN) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2891
OPA2891DR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2891
OPA2891DR.B	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2891
OPA891DGNR	Active	Production	HVSSOP (DGN) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	O891
OPA891DGNR.B	Active	Production	HVSSOP (DGN) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	O891
OPA891DR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	O891
OPA891DR.B	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	O891

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

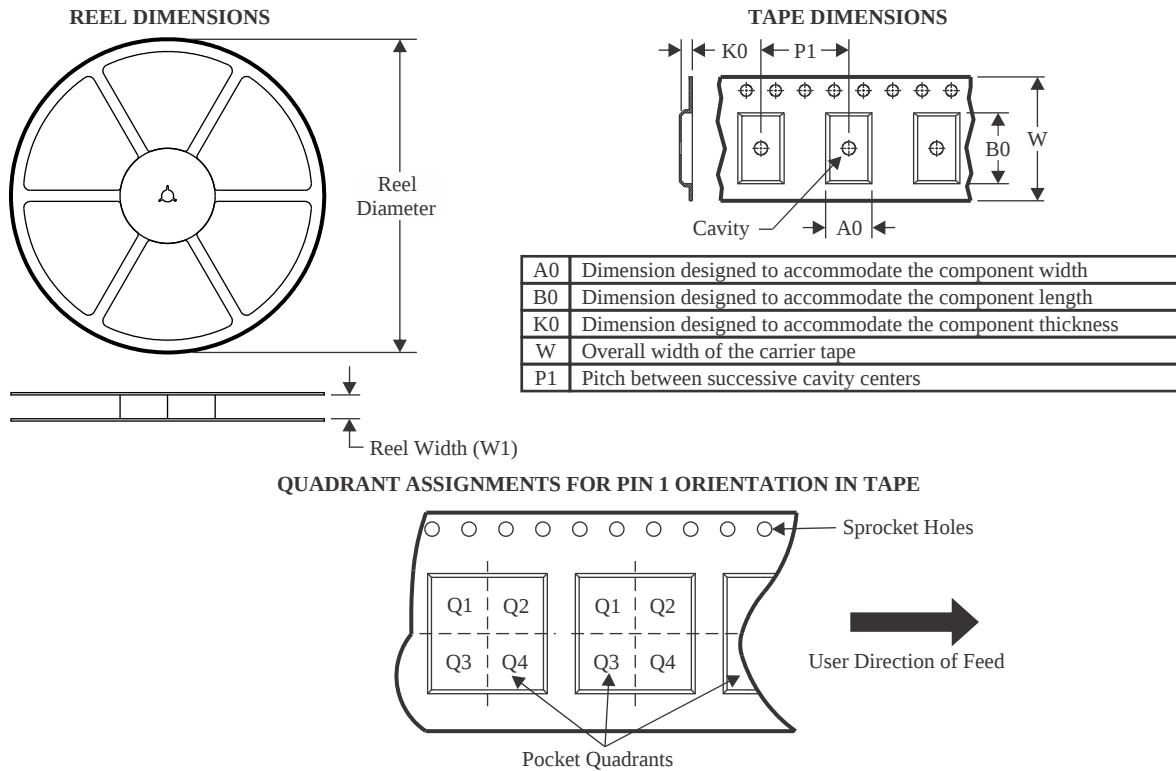
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

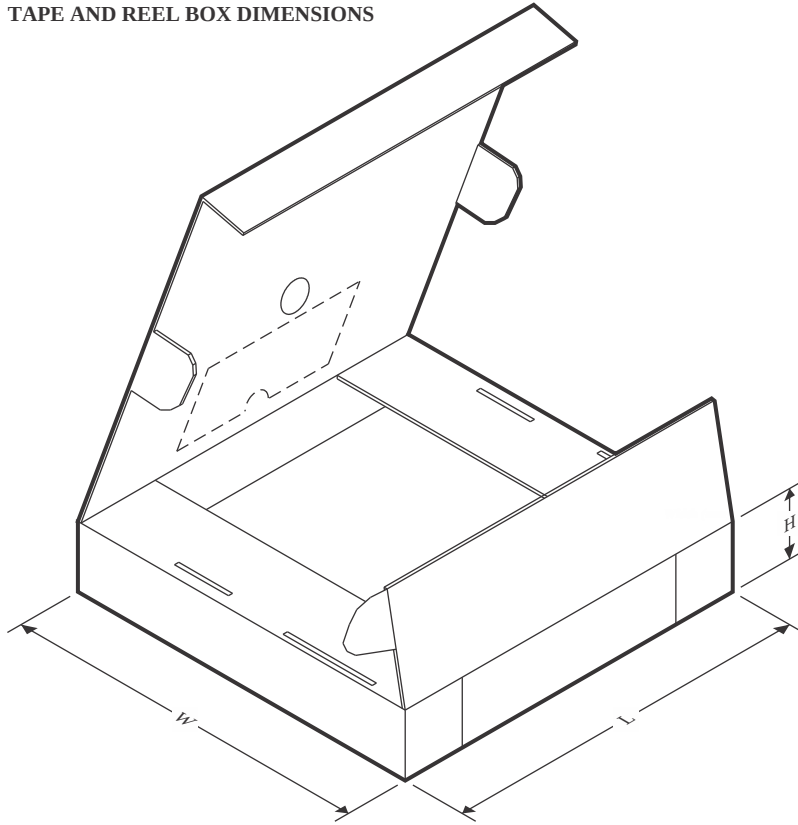
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2891DGNR	HVSSOP	DGN	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2891DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA891DGNR	HVSSOP	DGN	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA891DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2891DGNR	HVSSOP	DGN	8	3000	353.0	353.0	32.0
OPA2891DR	SOIC	D	8	3000	353.0	353.0	32.0
OPA891DGNR	HVSSOP	DGN	8	3000	356.0	356.0	35.0
OPA891DR	SOIC	D	8	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

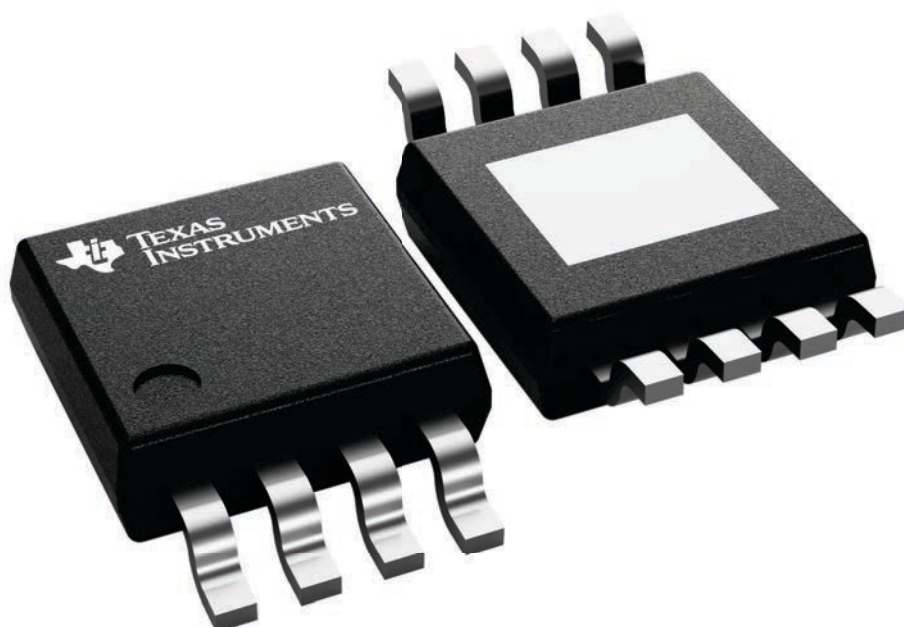
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

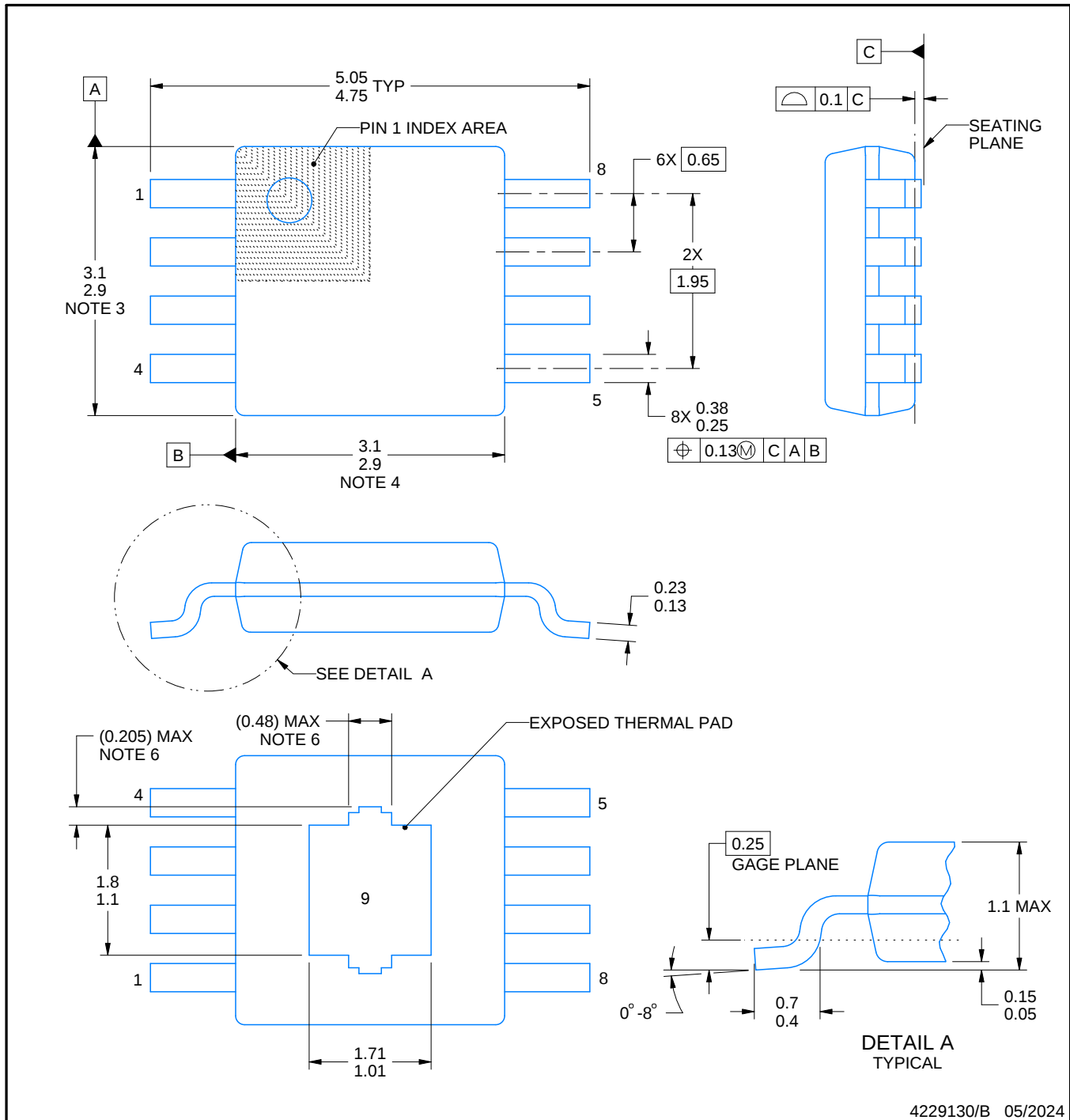
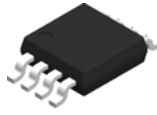
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B



4229130/B 05/2024

NOTES:

PowerPAD is a trademark of Texas Instruments.

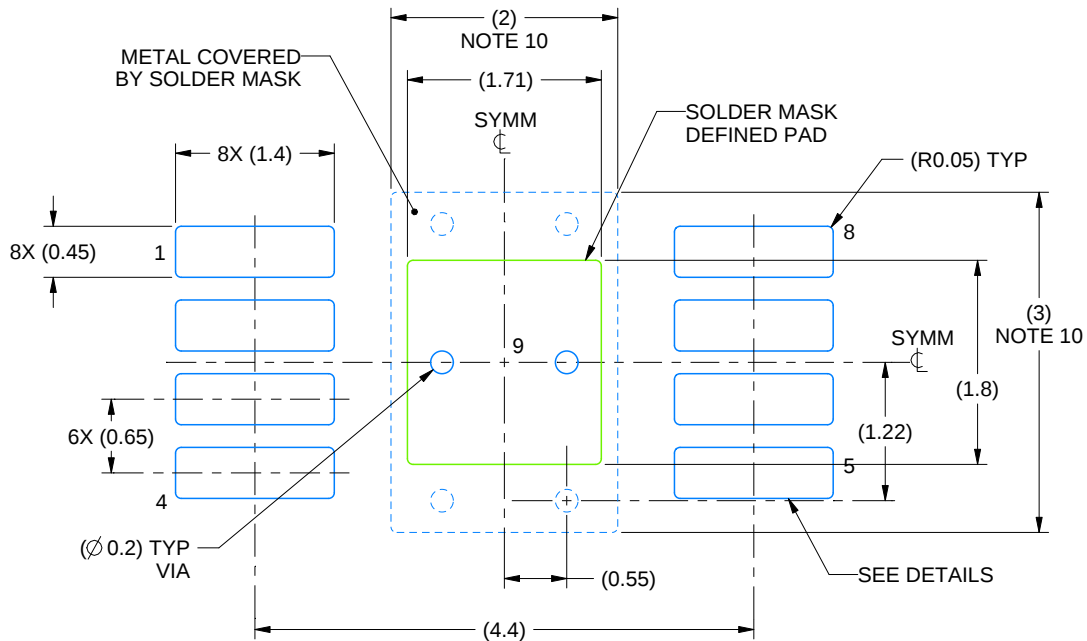
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

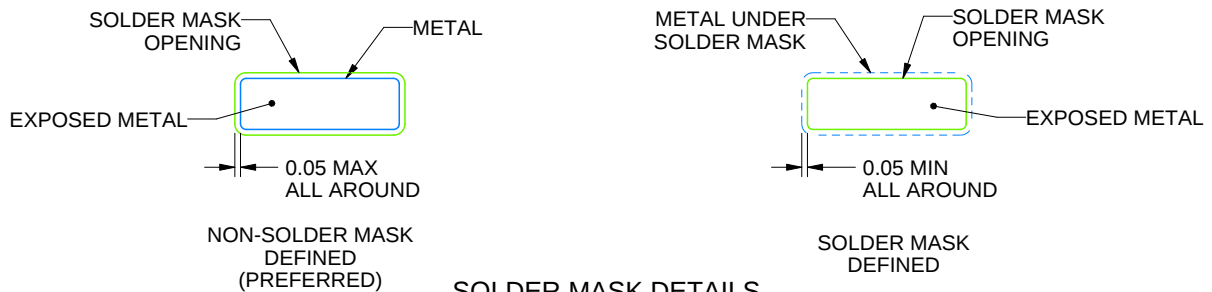
DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

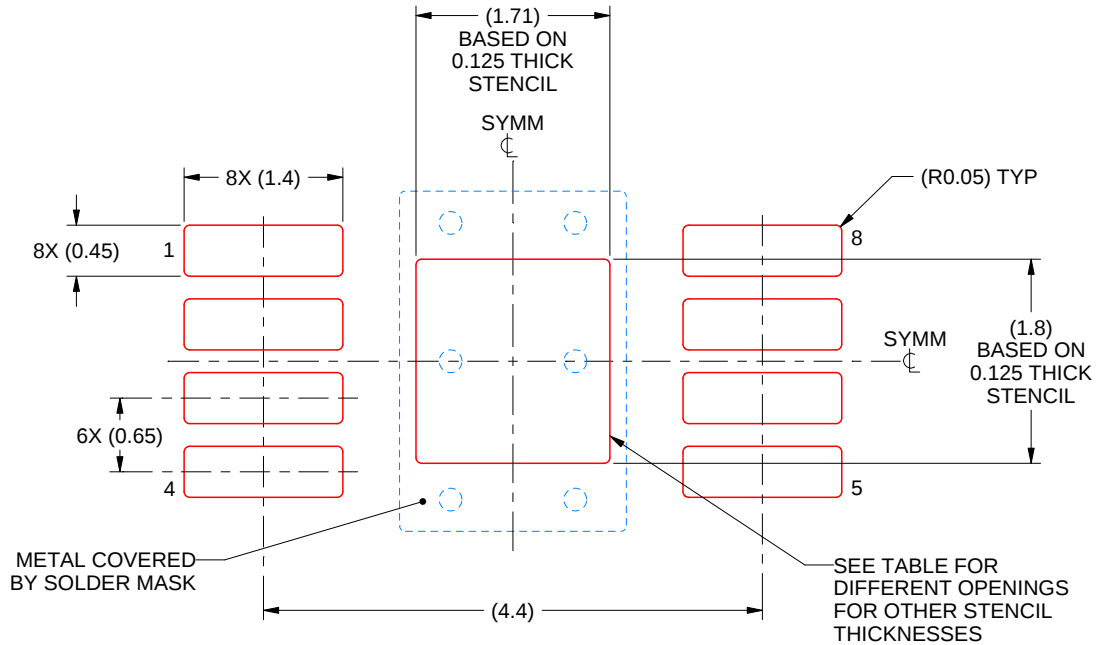
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



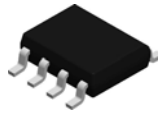
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

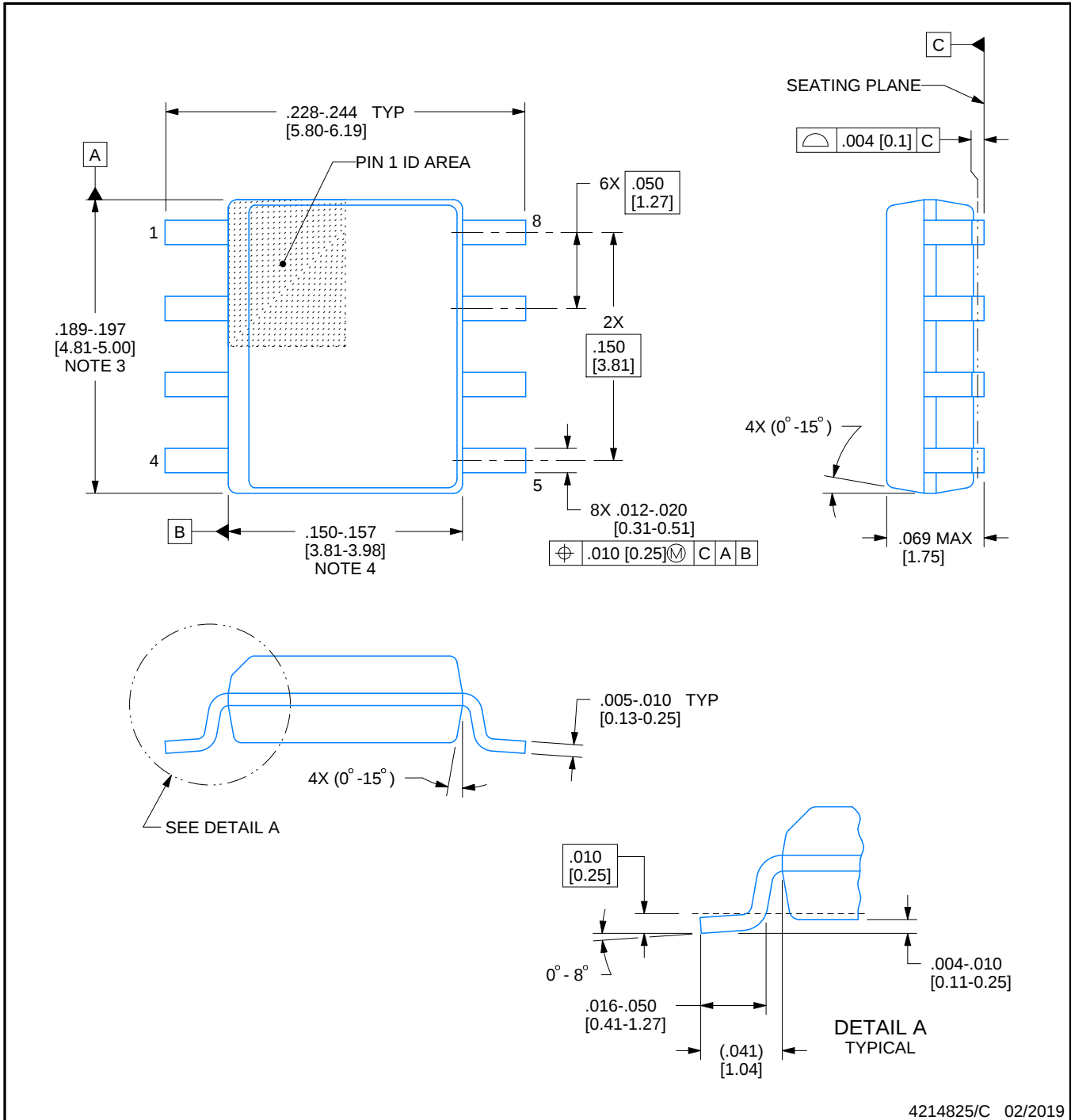


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

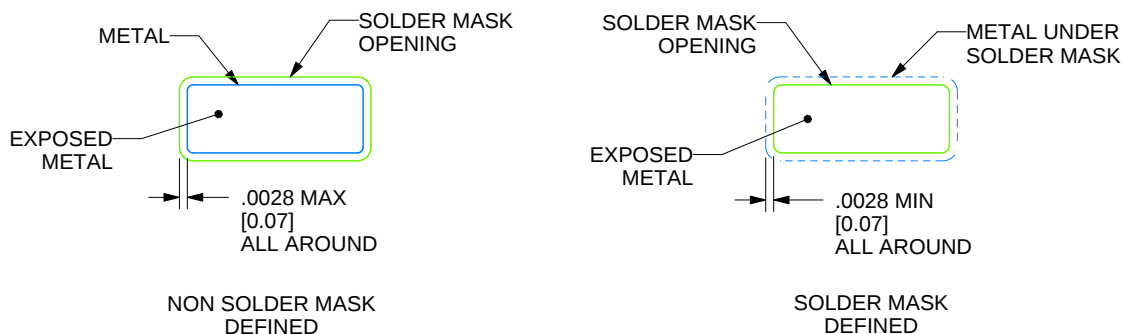
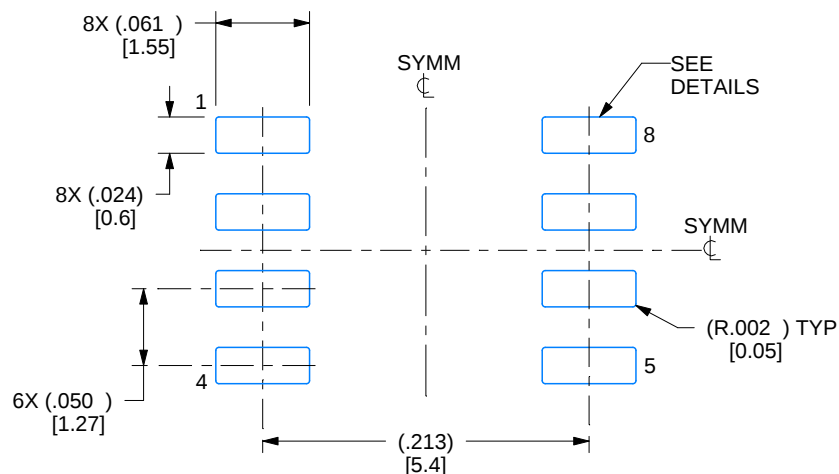
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

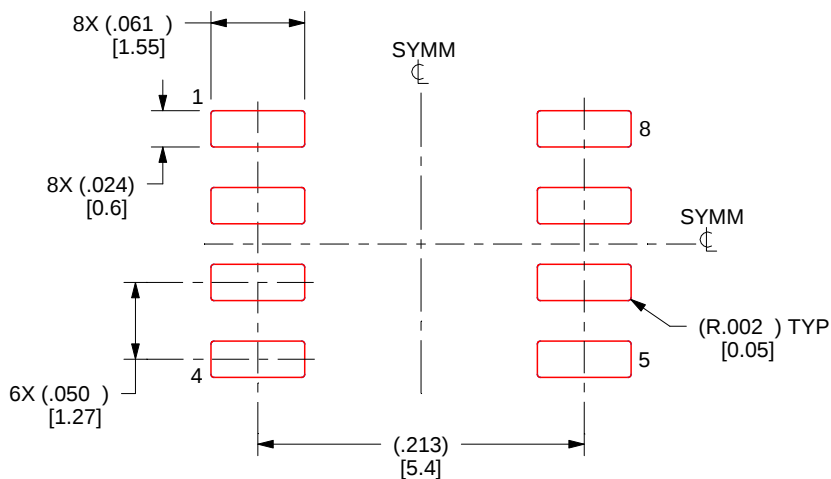
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated