OPA856 1.1GHz ユニティ･ゲイン帯域幅、0.9nV/ √ Hz、バイポーラ 入力アンプ

1 特長

- ユニティ・ ゲイン帯域幅：1.1GHz
- ゲイン帯域幅積：1.1GHz
- スルーレート：350V/µs
- 小さい入力電圧ノイズ：0.9nV/√Hz
- 低い入力容量：
  - 同相：0.4pF
  - 差動：0.7pF
- 電源電圧範囲：3.3V～5.25V
- パッケージ：8 ピン WSON
- 温度範囲：-40℃～+125℃

2 アプリケーション

- 光学時間領域反射率測定 (OTDR)
- 3D スキャナ
- レーザーによる測距
- ソリッド・ ステート・ スキャン LIDAR
- 光学 ToF 位置センサ
- ドローン・ ビジョン
- 産業用ロボットの LIDAR
- 掃除ロボットの LIDAR
- シリコン光電子増倍素子 (SiPM) バッファ・ アンプ
- フォトマルチプライヤ管のポスト・ アンプ

3 概要

OPA856 は、広帯域トランスインピーダンスおよび電圧アンプ・ アプリケーション用の広帯域、低ノイズのバイポーラ入力オペアンプです。デバイスがトランスインピーダンス・ アンプ (TIA) として構成されているとき、1.1GHz のゲイン帯域幅積 (GBWP) により、低容量のフォトダイオード・ アプリケーションで高い閉ループ帯域幅が可能になります。

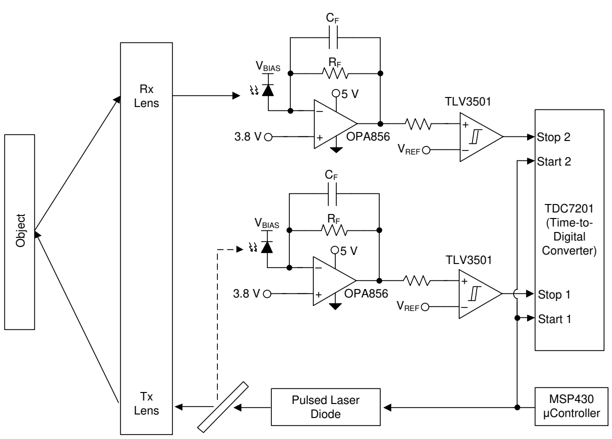
下のグラフは、アンプが TIA として構成されているときの OPA856 の帯域幅およびノイズ特性を、フォトダイオード容量の関数として示したものです。合計ノイズは、DC から左側のスケールで計算された周波数 (*f*) までの帯域幅の範囲にわたって計算されます。OPA856 のパッケージにはフィードバック・ ピン (FB) があるため、入力と出力の間の帰還回路接続が簡単になります。

OPA856 は、OPA856 を TDC7201 などの時間 / デジタル・ コンバータと組み合わせて使用する光学的タイム・ オブ・ フライト (ToF) システムで動作するよう最適化されています。OPA856 を使うと、THS4541 や LMH5401 などの差動出力アンプを接続した高分解能 LIDAR システムで高速 A/D コンバータ (ADC) を駆動できます。

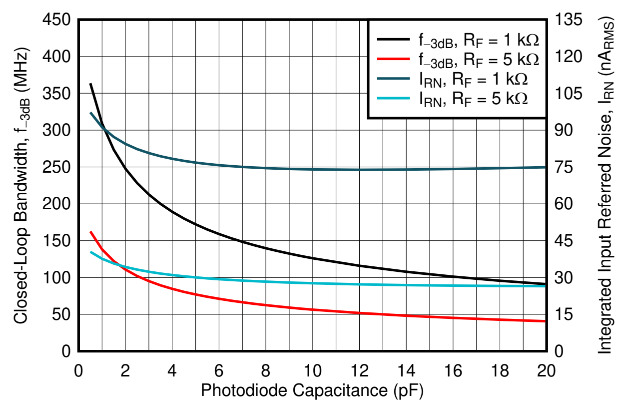
製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
OPA856	WSON (8)	2.00 mm × 2.00 mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・ オプションについての付録を参照してください。



高速タイム・ オブ・ フライト・ レシーバ



フォトダイオード容量と帯域幅およびノイズとの関係

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4 Revision History

DATE	REVISION	NOTES
October 2020	*	Initial Release

5 Device Comparison Table

DEVICE	INPUT TYPE	MINIMUM STABLE GAIN	VOLTAGE NOISE (nV/√Hz)	INPUT CAPACITANCE (pF)	GAIN BANDWIDTH (GHz)
OPA856	Bipolar	1 V/V	0.9	1.1	1.1
OPA855	Bipolar	7 V/V	0.98	0.8	8
OPA858	CMOS	7 V/V	2.5	0.8	5.5
OPA859	CMOS	1 V/V	3.3	0.8	0.9

6 Pin Configuration and Functions

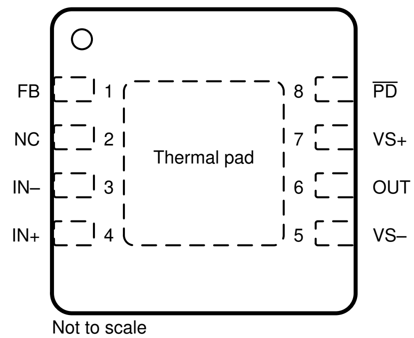


図 6-1. DSG Package
8-Pin WSON with Exposed Thermal Pad
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	1	I	Feedback connection to output of amplifier
IN–	3	I	Inverting input
IN+	4	I	Noninverting input
NC	2	—	Do not connect.
OUT	6	O	Amplifier output
$\overline{PD}$	8	I	Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VS–	5	—	Negative voltage supply
VS+	7	—	Positive voltage supply
Thermal pad		—	Connect the thermal pad to VS–.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_S	Total supply voltage ($V_{S+} – V_{S–}$)		5.5	V
V_{IN+}, $V_{IN–}$	Input voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
V_{ID}	Differential input voltage		1	V
VOUT	Output voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
I_{IN}	Continuous input current		±10	mA
I_{OUT}	Continuous output current[2]		±100	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Long-term continuous output current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±1500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage ($V_{S+} – V_{S–}$)	3.3	5	5.25	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		OPA856 DSG (WSON) 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	80.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	100	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	45	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	6.8	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	45.2	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at V_{S+} = 5 V, V_{S-} = 0 V, G = 1 V/V, R_F = 0 Ω, input common-mode biased at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		1.1		GHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		110		MHz
GBWP	Gain-bandwidth product			1.08		GHz
	Bandwdith for 0.1-dB flatness	V_{OUT} = 100 mV_{PP}		175		MHz
SR	Slew rate (10%-90%)	V_{OUT} = 2-V step		350		V/µs
t_r	Rise time	V_{OUT} = 100-mV step		0.75		ns
t_f	Fall time	V_{OUT} = 100-mV step		0.75		ns
	Settling time to 0.1%	V_{OUT} = 2-V step		7		ns
HD2	Second-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		85		dBc
		f = 50 MHz, V_{OUT} = 2 V_{PP}		50		
HD3	Third-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		95		dBc
		f = 50 MHz, V_{OUT} = 2 V_{PP}		45		
e_n	Input-referred voltage noise	f = 1 MHz		0.9		nV/√Hz
e_i	Input-referred current noise	f = 1 MHz		2.5		pA/√Hz
z_O	Closed-loop output impedance	f = 1 MHz		0.15		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain		70	76		dB
V_{OS}	Input offset voltage	T_A = 25°C	–1.5	±0.2	1.5	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	T_A = –40°C to 125°C		0.7		µV/°C
I_B	Input bias current (1)	T_A = 25°C	–20	–15	–5	µA
$\Delta I_B/\Delta T$	Input bias current drift	T_A = –40°C to +125°C		-0.1		µA/°C
I_{BOS}	Input offset current	T_A = 25°C	–1	±0.1	1	µA
$\Delta I_{BOS}/\Delta T$	Input offset current drift	T_A = –40°C to +125°C		0.75		nA/°C
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V referred to midsupply	90	106		dB
INPUT						
C_{CM}	Common-mode input capacitance			0.4		pF
C_{DIFF}	Differential input capacitance			0.7		pF
V_{IH}	Common-mode input range (high)	CMRR > 80 dB, V_{S+} = 3.3 V	2.7	2.9		V
V_{IL}	Common-mode input range (low)	CMRR > 80 dB, V_{S+} = 3.3 V		1.1	1.3	V
V_{IH}	Common-mode input range (high)	CMRR > 80 dB	4.4	4.6		V
V_{IH}	Common-mode input range (high)	T_A = –40°C to +125 °C, CMRR > 80 dB		4.3		V
V_{IL}	Common-mode input range (low)	CMRR > 80 dB		1.1	1.3	V
V_{IL}	Common-mode input range (low)	T_A = –40°C to +125°C, CMRR > 80 dB		1.3		V

7.5 Electrical Characteristics (continued)

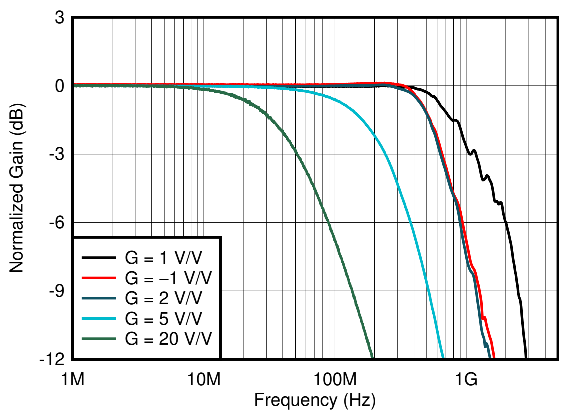
at V_{S+} = 5 V, V_{S-} = 0 V, G = 1 V/V, R_F = 0 Ω, input common-mode biased at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OH}	Output voltage (high)[2]	T_A = 25°C, V_{S+} = 3.3 V	2.35	2.4		V
V_{OH}	Output voltage (high)[2]	T_A = 25°C	3.95	4.1		V
		T_A = –40°C to +125°C		4		
V_{OL}	Output voltage (low)[2]	T_A = 25°C, V_{S+} = 3.3 V		1.05	1.15	V
V_{OL}	Output voltage (low)[2]	T_A = 25°C		1.05	1.15	V
		T_A = –40°C to +125°C		1.1		
I_{O_LIN}	Linear output drive (sink and source)	R_L = 10 Ω, A_{OL} > 60 dB	65	80		mA
		T_A = –40°C to +125°C, R_L = 10 Ω, A_{OL} > 60 dB		65		
I_{SC}	Output short-circuit current		85	105		mA
POWER SUPPLY						
I_Q	Quiescent current		15.4	17.2	19.5	mA
		T_A = –40°C		15.5		
		T_A = 125°C		19.5		
PSRR+	Positive power-supply rejection ratio		80	86		dB
PSRR–	Negative power-supply rejection ratio		70	80		
POWER DOWN						
	Disable voltage threshold	Amplifier OFF below this voltage	0.65	1		V
	Enable voltage threshold	Amplifier ON above this voltage		1.5	1.8	V
	Power-down quiescent current			70	85	µA
	$\overline{PD}$ bias current			70	85	µA
	Turnon time delay	Time to V_{OUT} = 90% of final value		15		ns
	Turnoff time delay			250		ns

(1) Current flowing into the input pin is considered negative.
(2) Amplifier output saturated.

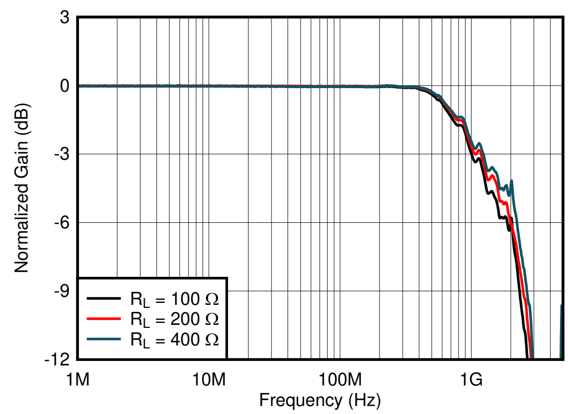
7.6 Typical Characteristics

at V_{S+} = +2.5 V, V_{S-} = –2.5 V, R_F = 0 Ω, Gain = 1 V/V, input common-mode biased at midsupply, R_L = 200 Ω, output load referenced to midsupply, and T_A = 25°C (unless otherwise noted)



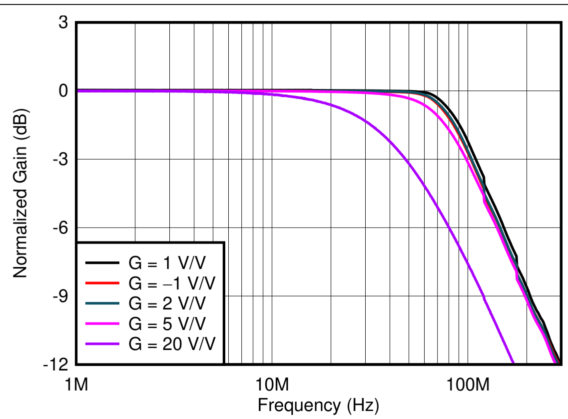
V_{OUT} = 100 mV_{PP}

図 7-1. Small-Signal Response vs Gain



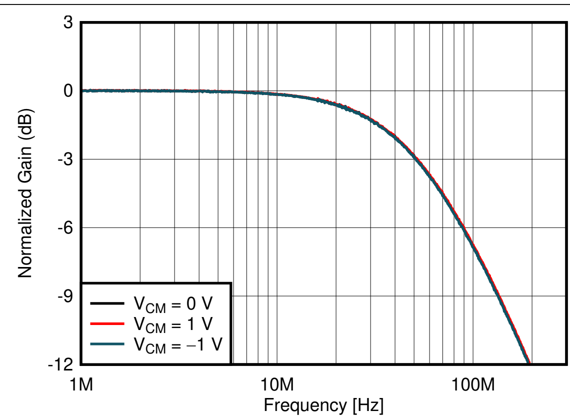
V_{OUT} = 100 mV_{PP}

図 7-2. Small-Signal Response vs Output Load



V_{OUT} = 2 V_{PP}

図 7-3. Large-Signal Response vs Gain



Gain = 20 V/V V_{OUT} = 100 mV_{PP}

図 7-4. Gain Bandwidth vs Common-Mode

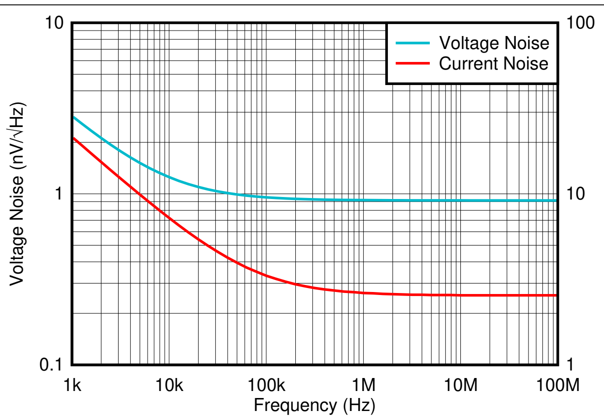
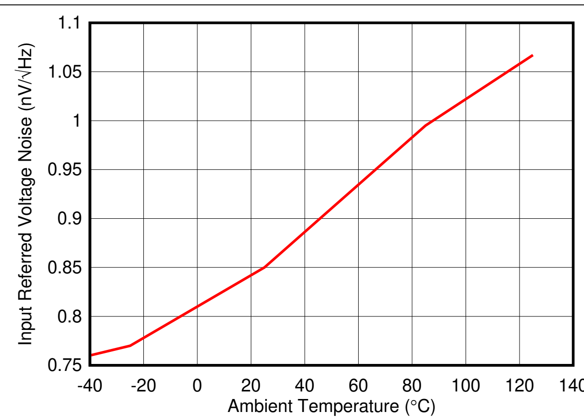


図 7-5. Voltage and Current Noise Density

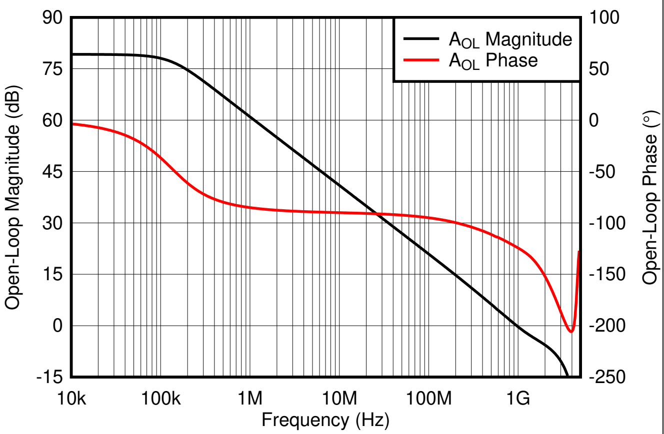


Frequency = 10 MHz

図 7-6. Voltage Noise vs Temperature

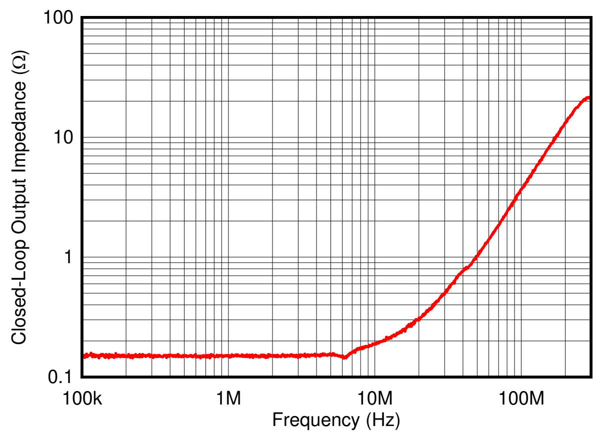
7.6 Typical Characteristics (continued)

at V_{S+} = +2.5 V, V_{S-} = –2.5 V, R_F = 0 Ω, Gain = 1 V/V, input common-mode biased at midsupply, R_L = 200 Ω, output load referenced to midsupply, and T_A = 25°C (unless otherwise noted)



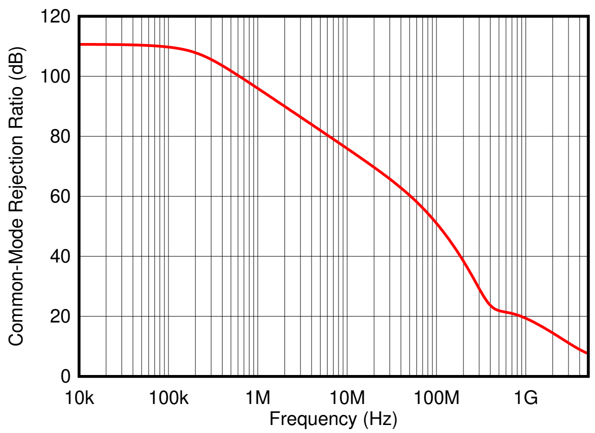
Small-Signal Response

図 7-7. Open-Loop Magnitude and Phase



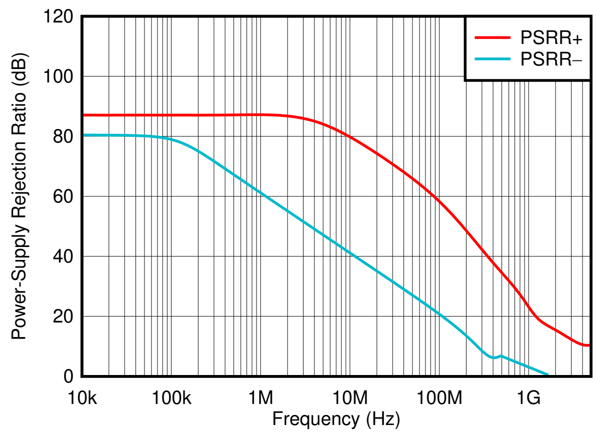
Small-Signal Response

図 7-8. Closed Loop Output Impedance



Small-Signal Response

図 7-9. Common-Mode Rejection Ratio



Small-Signal Response

図 7-10. Power Supply Rejection Ratio

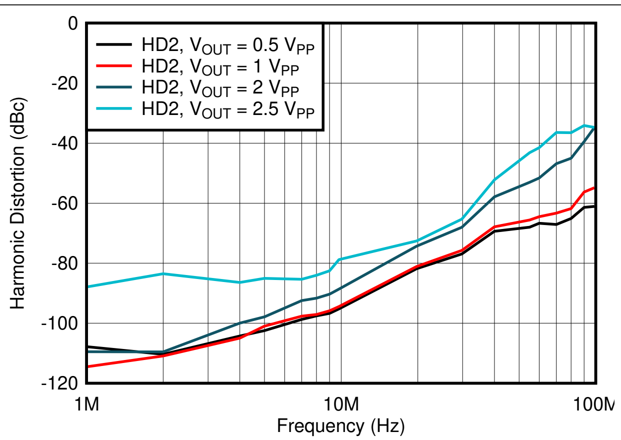


図 7-11. Harmonic Distortion (HD2) vs Output Swing

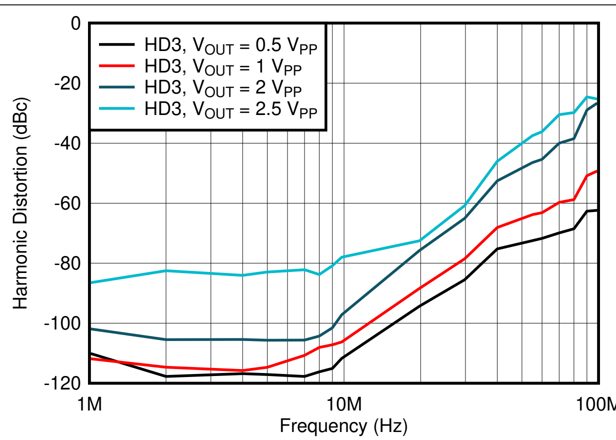
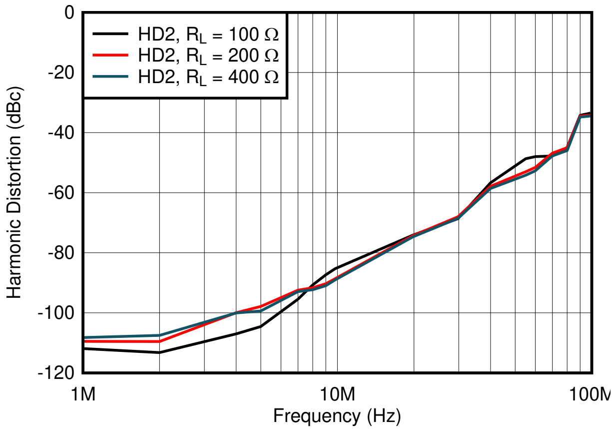


図 7-12. Harmonic Distortion (HD3) vs Output Swing

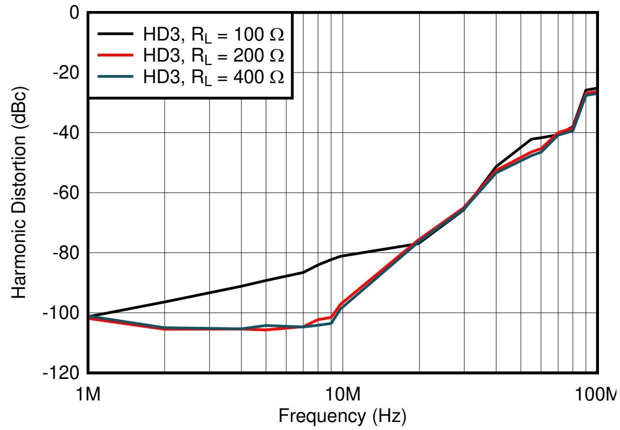
7.6 Typical Characteristics (continued)

at V_{S+} = +2.5 V, V_{S-} = –2.5 V, R_F = 0 Ω, Gain = 1 V/V, input common-mode biased at midsupply, R_L = 200 Ω, output load referenced to midsupply, and T_A = 25°C (unless otherwise noted)



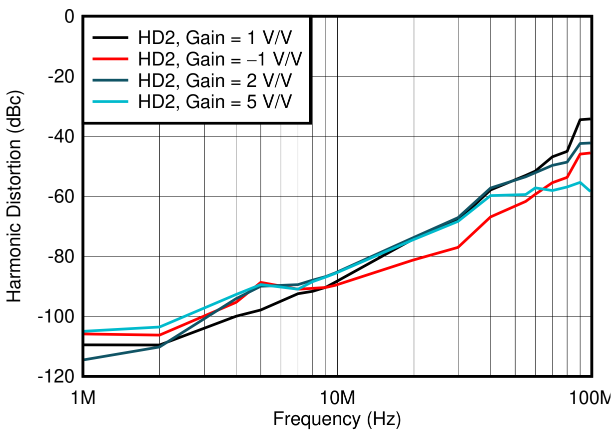
V_{OUT} = 2 V_{PP}

図 7-13. Harmonic Distortion (HD2) vs Load



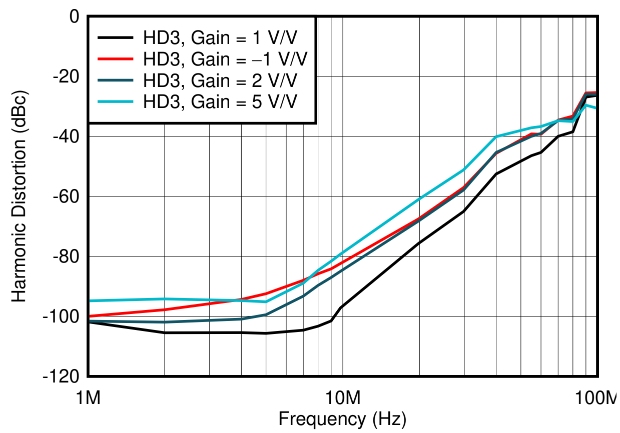
V_{OUT} = 2 V_{PP}

図 7-14. Harmonic Distortion (HD3) vs Load



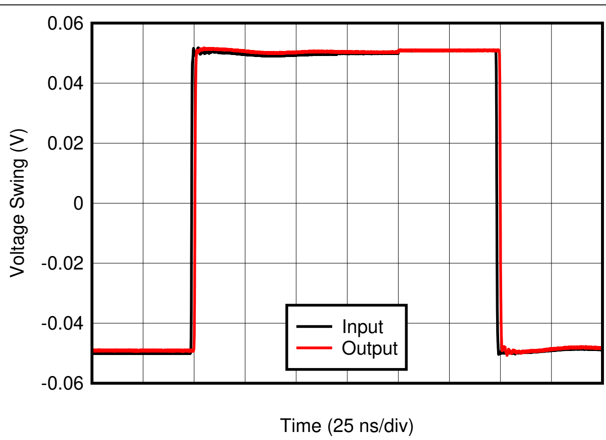
V_{OUT} = 2 V_{PP}

図 7-15. Harmonic Distortion (HD2) vs Gain



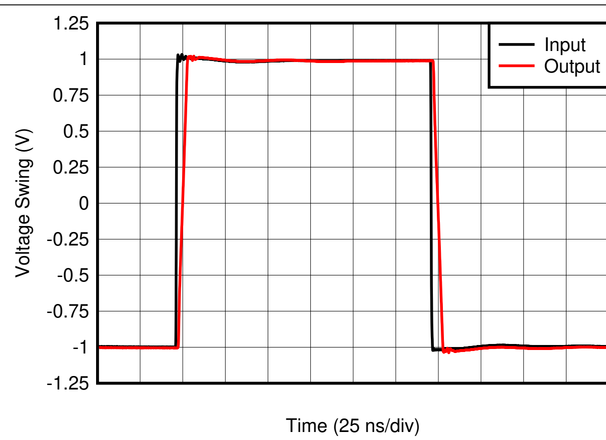
V_{OUT} = 2 V_{PP}

図 7-16. Harmonic Distortion (HD3) vs Gain



Average Rise and Fall Time (10% - 90%) = 680 ps

図 7-17. Small-Signal Transient Response



Slew Rate: Rising = 365 V/µs, Falling = 346 V/µs

図 7-18. Large-Signal Transient Response

7.6 Typical Characteristics (continued)

at V_{S+} = +2.5 V, $V_{S–}$ = –2.5 V, R_F = 0 Ω, Gain = 1 V/V, input common-mode biased at midsupply, R_L = 200 Ω, output load referenced to midsupply, and T_A = 25°C (unless otherwise noted)

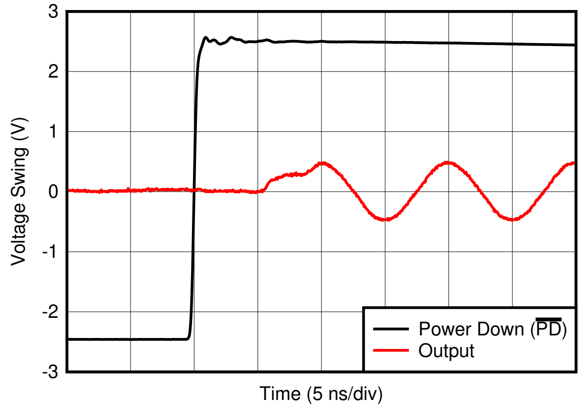


図 7-19. Turnon Transient Response

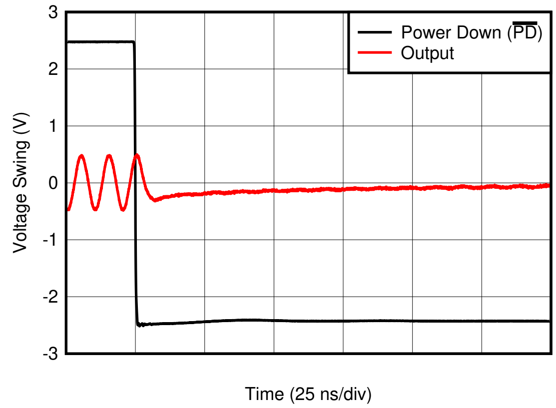
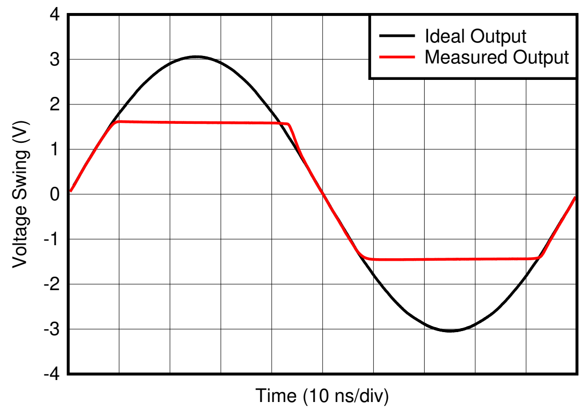


図 7-20. Turnoff Transient Response

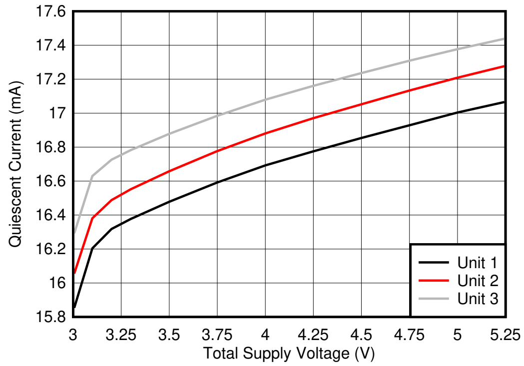


Gain = 5 V/V, R_F = 453 Ω, V_{IN} = 1.25 V_{PP} , 2x Output Overdrive

図 7-21. Output Overload Response

7.7 Typical Characteristics (continued)

at V_{S+} = +2.5 V, V_{S-} = –2.5 V, R_F = 0 Ω, Gain = 1 V/V, input common-mode biased at midsupply, R_L = 200 Ω, output load referenced to midsupply, and T_A = 25°C (unless otherwise noted)



3 Typical Units

図 7-22. Quiescent Current vs Supply Voltage

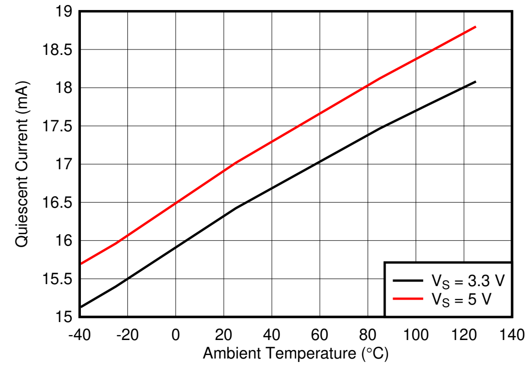
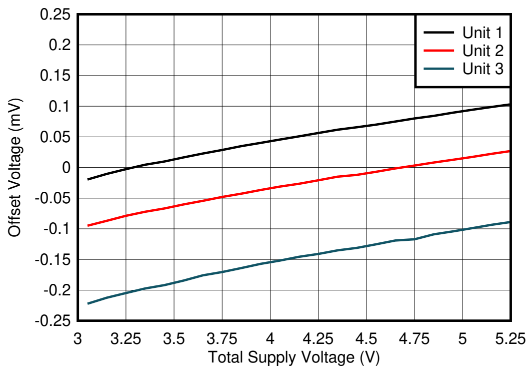
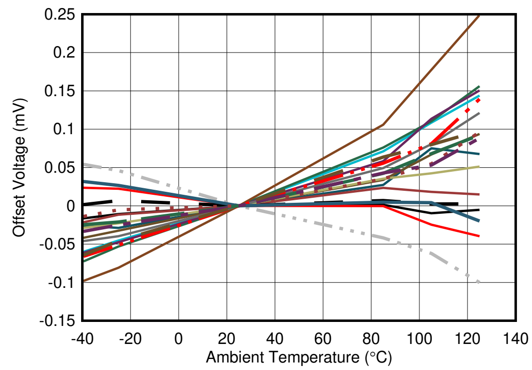


図 7-23. Quiescent Current vs Ambient Temperature



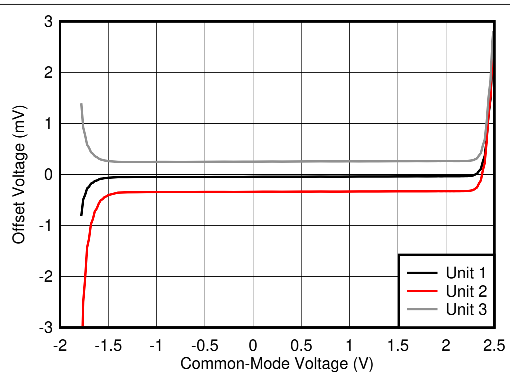
3 Typical Units

図 7-24. Offset Voltage vs Supply Voltage



σ = 0.7 µV/°C

図 7-25. Offset Voltage vs Ambient Temperature



3 Typical Units

図 7-26. Offset Voltage vs Input Common-Mode Voltage

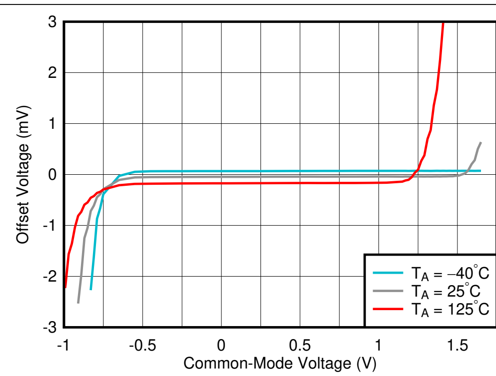
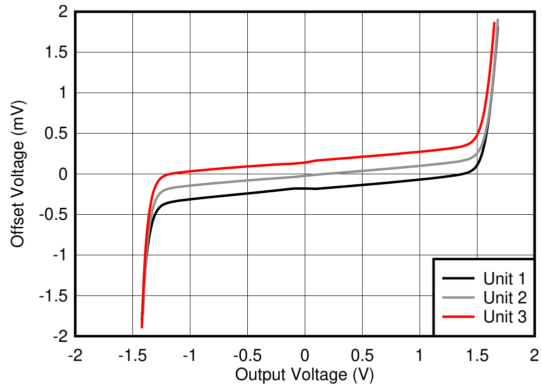


図 7-27. Offset Voltage vs Input Common-Mode Voltage vs Ambient Temperature

7.7 Typical Characteristics (continued) (continued)

at V_{S+} = +2.5 V, V_{S-} = –2.5 V, R_F = 0 Ω, Gain = 1 V/V, input common-mode biased at midsupply, R_L = 200 Ω, output load referenced to midsupply, and T_A = 25°C (unless otherwise noted)



3 Typical Units

図 7-28. Offset Voltage vs Output Swing

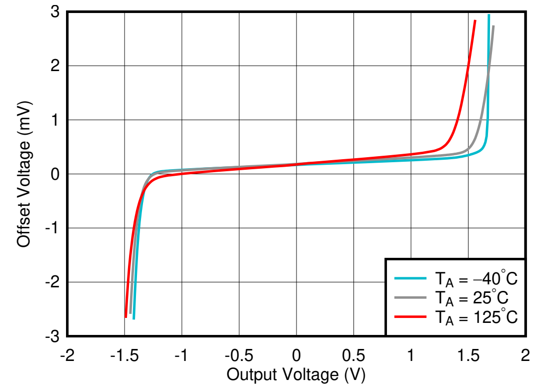
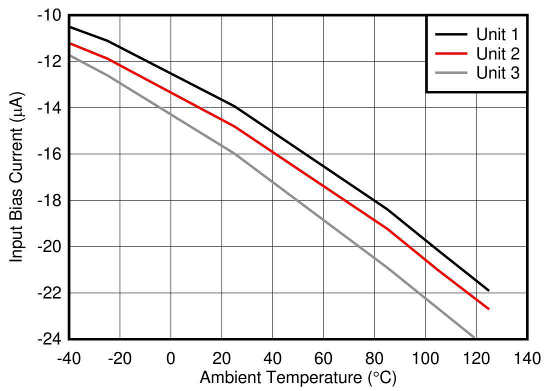


図 7-29. Offset Voltage vs Output Swing vs Ambient Temperature



3 Typical Units

図 7-30. Input Bias Current vs Ambient Temperature

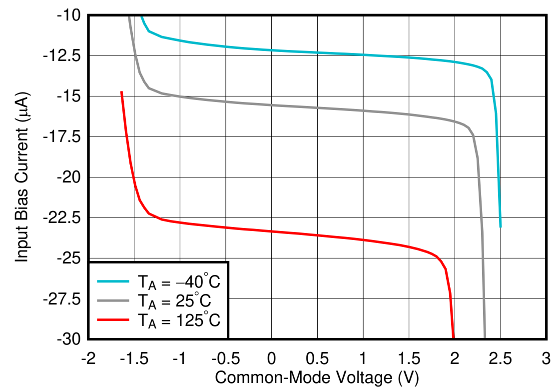
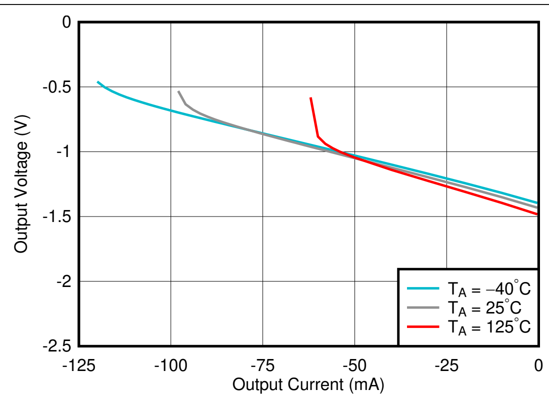
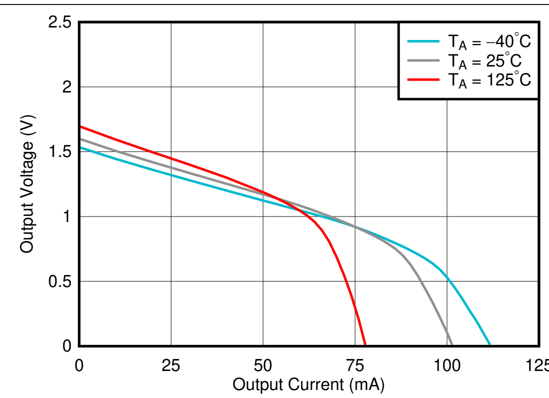


図 7-31. Input Bias Current vs Input Common-Mode Voltage



Output slammed to the negative rail

図 7-32. Output Swing vs Sinking Current



Output slammed to the positive rail

図 7-33. Output Swing vs Sourcing Current

7.7 Typical Characteristics (continued) (continued)

at V_{S+} = +2.5 V, $V_{S–}$ = –2.5 V, R_F = 0 Ω, Gain = 1 V/V, input common-mode biased at midsupply, R_L = 200 Ω, output load referenced to midsupply, and T_A = 25°C (unless otherwise noted)

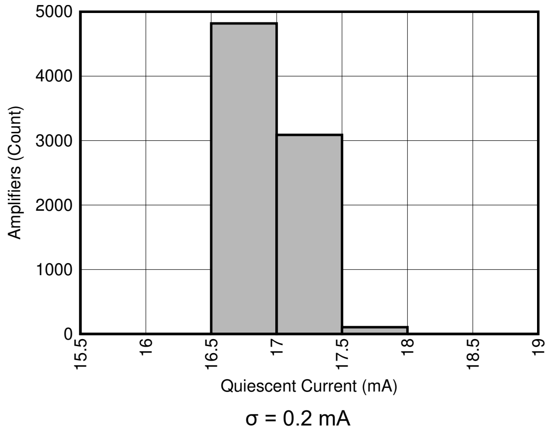


図 7-34. Quiescent Current Distribution

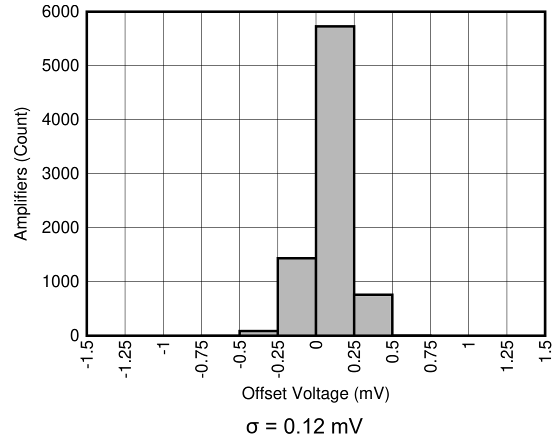


図 7-35. Offset Voltage Distribution

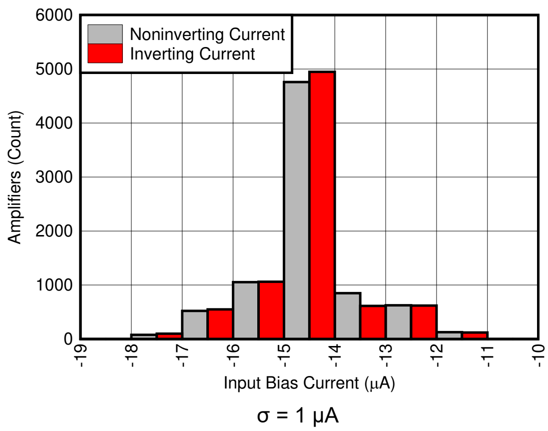


図 7-36. Input Bias Current Distribution

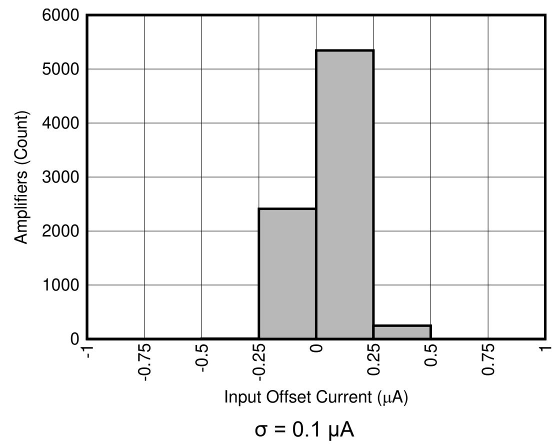


図 7-37. Input Offset Current Distribution

8 Detailed Description

8.1 Overview

The ultra-wide, 1.1-GHz gain bandwidth product (GBWP) of the OPA856, combined with the broadband voltage noise of 0.9 nV/√Hz, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA856 combines multiple features to optimize dynamic performance. In addition to the wide, small-signal bandwidth, the OPA856 has 110 MHz of large-signal bandwidth (V_{OUT} = 2 V_{PP}), and a slew rate of 350 V/µs.

The OPA856 is offered in a 2-mm × 2-mm, 8-pin WSON package that features a feedback (FB) pin for a simple feedback network connection between the amplifiers output and inverting input. Excess capacitance on an amplifiers input pin can reduce phase margin causing instability. This problem is exacerbated in the case of very wideband amplifiers like the OPA856. To reduce the effects of stray capacitance on the input node, the OPA856 pinout features an isolation pin (NC) between the feedback and inverting input pins that increases the physical spacing between them thereby reducing parasitic coupling at high frequencies. The OPA856 also features a very low capacitance input stage with only 1.1-pF of total input capacitance.

8.2 Functional Block Diagram

The OPA856 is a classic voltage feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, like the two basic options shown in 図 8-1 and 図 8-2. The resistor on the noninverting pin is used for bias current cancellation to minimize the output offset voltage. In a noninverting configuration the additional resistors on the noninverting pin add noise to the system so if SNR is critical, the resistor can be eliminated. In an inverting configuration the noninverting node is typically connected to a DC voltage, so the high-frequency noise contribution from the bias cancellation resistor can be bypassed by adding a large 1-µF capacitor in parallel to the resistor to shunt the noise. The DC operating point for each configuration is level-shifted by the reference voltage (V_{REF}), which is typically set to midsupply in single-supply operation. V_{REF} is typically connected to ground in split-supply applications.

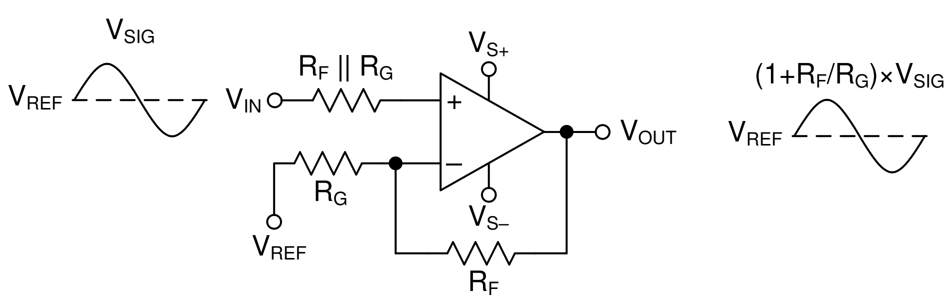


図 8-1. Noninverting Amplifier

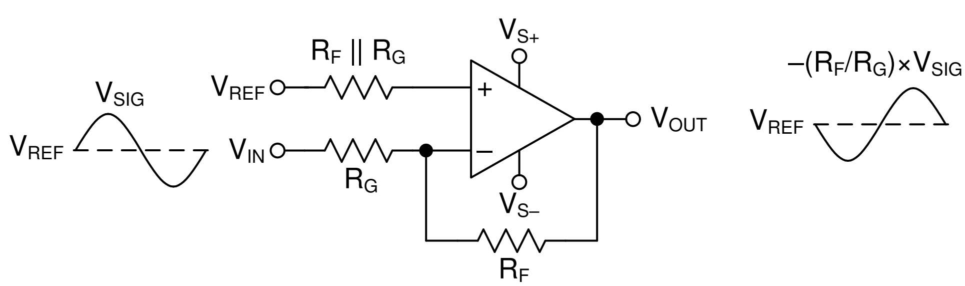


図 8-2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input and ESD Protection

The OPA856 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies as 図 8-3 shows. There are two antiparallel diodes between the inputs of the amplifier that clamp the inputs during an overrange or fault condition.

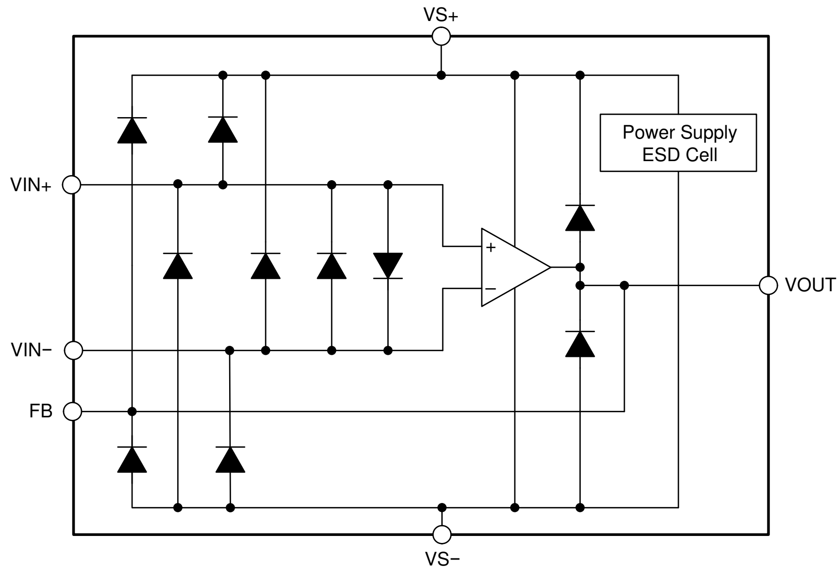


図 8-3. Internal ESD Structure

8.3.2 Feedback Pin

The OPA856 pin layout is optimized to minimize parasitic inductance and capacitance, which is a critical care about in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor (R_F) can connect between the FB and IN– pin on the same side of the package (see 図 8-4) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN– pins by increasing the physical separation between the pins.

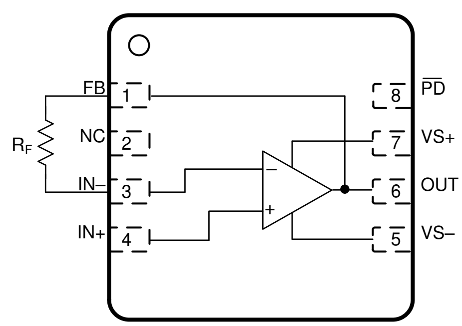


図 8-4. R_F Connection Between FB and IN– Pins

8.3.3 Wide Gain-Bandwidth Product

図 7-7 shows the open-loop magnitude and phase response of the OPA856. Calculate the gain bandwidth product of any op amp by determining the frequency at which the A_{OL} is 40 dB and multiplying that frequency by a factor of 100. The open-loop response shows the OPA856 to have approximately 57° of phase-margin when configured as a unity-gain buffer.

図 8-5 shows the open-loop magnitude (A_{OL}) of the OPA856 as a function of temperature. The results show minimal variation over the entire temperature range. Semiconductor process variation is the naturally occurring variation in the attributes of a transistor (Early-voltage, β, channel-length, and width) and other passive elements (resistors and capacitors) when fabricated into an integrated circuit. The process variation can occur across devices on a single wafer or across devices over multiple wafer lots over time. Typically the variation across a single wafer is tightly controlled. 図 8-6 shows the A_{OL} magnitude of the OPA856 as a function of process variation over time. The results show the A_{OL} curve for the nominal process corner and the variation one standard deviation from the nominal. The simulated results show less than 5° of phase-margin difference within a standard deviation of process variation when the amplifier is configured as a unity-gain bufffer.

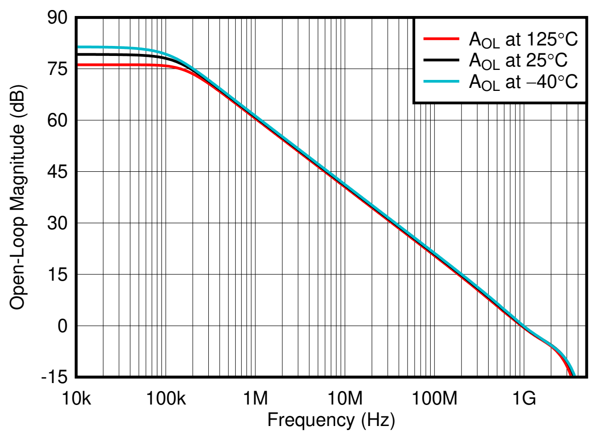


図 8-5. Open-Loop Gain vs Temperature

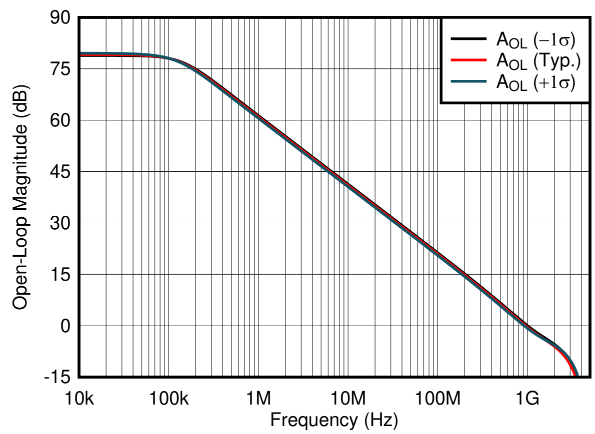


図 8-6. Open-Loop Gain vs Process Variation

8.3.4 Slew Rate and Output Stage

In addition to wide bandwidth, the OPA856 features a high slew rate of 2750 V/µs. The slew rate is a critical parameter in high-speed pulse applications with narrow sub-10-ns pulses, such as optical time-domain reflectometry (OTDR) and LIDAR. The high slew rate of the OPA856 implies that the device accurately reproduces a 2-V, sub-ns pulse edge, as seen in 図 7-18. The wide bandwidth and slew rate of the OPA856 make it an excellent amplifier for high-speed signal-chain front ends.

図 8-7 shows the open-loop output impedance of the OPA856 as a function of frequency. To achieve high slew rates and low output impedance across frequency, the output swing of the OPA856 is limited to approximately 3 V. The OPA856 is typically used in conjunction with high-speed pipeline ADCs and flash ADCs that have limited input ranges. Therefore, the OPA856 output swing range coupled with the class-leading voltage noise specification maximizes the overall dynamic range of the signal chain.

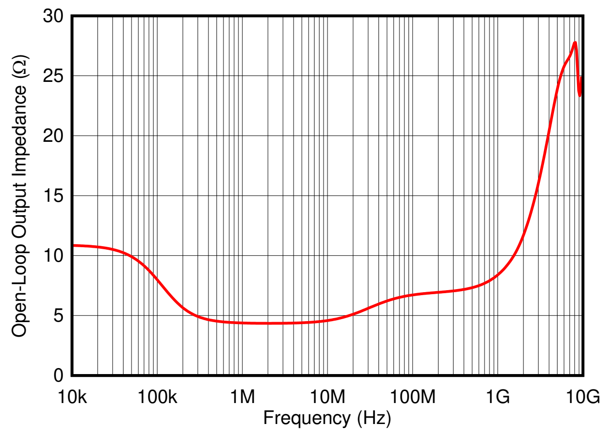


図 8-7. Open-Loop Output Impedance (Z_{OL}) vs Frequency

8.4 Device Functional Modes

8.4.1 Split-Supply and Single-Supply Operation

The OPA856 can be configured with single-sided supplies or split-supplies as shown in 図 10-1. Split-supply operation using balanced supplies with the input common-mode set to ground eases lab testing because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground. In split-supply operation, the thermal pad must be connected to the negative supply.

Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA856 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. In single-supply operation, level shift the DC input and output reference voltages by half the difference between the power supply rails. This configuration maintains the input common-mode and output load reference at midsupply. To eliminate gain errors, the source driving the reference input common-mode voltage must have low output impedance across the frequency range of interest. In this case, the thermal pad must be connected to ground.

8.4.2 Power-Down Mode

The OPA856 features a power-down mode to reduce the quiescent current to conserve power. 図 7-19 and 図 7-20 show the transient response of the OPA856 as the $\overline{PD}$ pin toggles between the disabled and enabled states.

The $\overline{PD}$ disable and enable threshold voltages are with reference to the negative supply. If the amplifier is configured with the positive supply at 3.3 V and the negative supply at ground, then the disable and enable threshold voltages are 0.65 V and 1.8 V, respectively. If the amplifier is configured with ±1.65 V supplies, then the threshold voltages are at –1 V and 0.15 V. If the amplifier is configured with ±2.5 V supplies, then the threshold voltages are at –1.85 V and –0.7 V.

図 8-8 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept down from the enabled state to the disabled state. Similarly, 図 8-9 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept up from the disabled state to the enabled state. The small difference in the switching thresholds between the down sweep and the up sweep is caused by the hysteresis designed into the amplifier to increase immunity to noise on the $\overline{PD}$ pin.

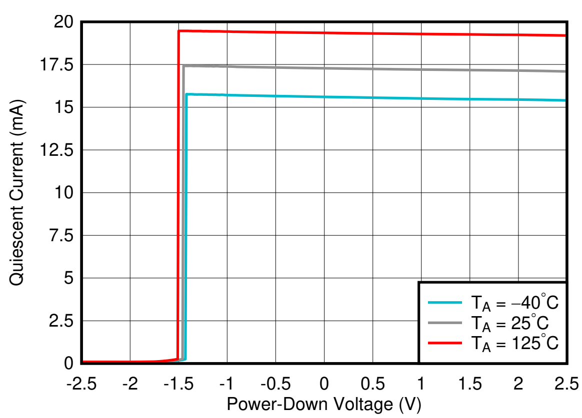


図 8-8. Switching Threshold ($\overline{PD}$ Pin Swept from High to Low)

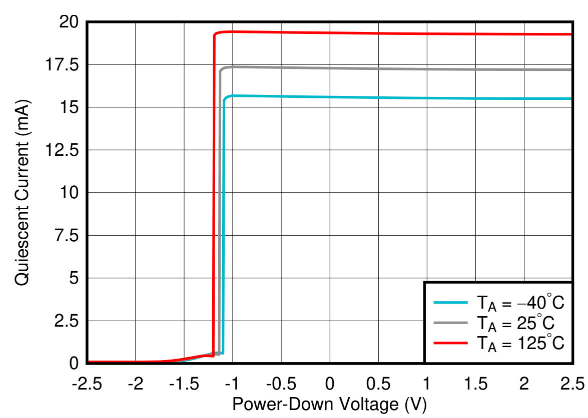


図 8-9. Switching Threshold ($\overline{PD}$ Pin Swept from Low to High)

Connecting the $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a noninverting amplifier, the feedback (R_F) and gain (R_G) resistor network form a parallel load to the output of the amplifier. To protect the input stage of the amplifier, the OPA856 uses internal, back-to-back protection diodes between the inverting and noninverting input pins as 図 8-3 shows. In the power-down state, if the differential voltage between the input pins of the amplifier exceeds a diode voltage drop, an additional low-impedance path is created between the noninverting input pin and the output pin.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA856 offers over 1 GHz of bandwidth, high slew-rate, low noise, excellent linearity, and is stable for unity gain applications. The low noise and unity gain stability make the OPA856 a great choice for use as a front-end buffer in high-speed data acquisition systems. Additionally the wide bandwidth allows the amplifier to perform excellently in transimpedance applications or in a high-gain active filter configuration.

9.2 Typical Application

The high GBWP of the OPA856 makes the device an excellent choice as a transimpedance amplifier while the unity gain stability allows for use of feedback clamping or other unity gain circuitry that would not work for a decompensated amplifier. 図 9-1 shows the OPA856 configured as a transimpedance amplifier with an option feedback clamping diode connection.

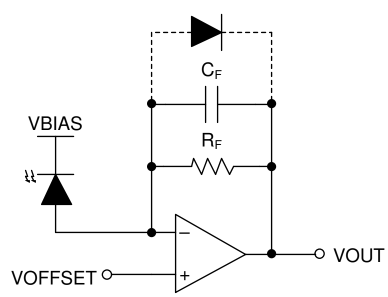


図 9-1. OPA856 Transimpedance Amplifier with Optional Diode Clamping

9.2.1 Design Requirements

The objective is to design a low noise, wideband optical front-end system using the OPA856

as a transimpedance amplifier. The design requirements are:

- Amplifier supply voltage: ± 2.5 V
- 1 kΩ transimpedance gain
- Transimpedance bandwidth > 100 MHz
- Total input capacitance 4 pF (1.1 pF from amplifier)

9.2.2 Detailed Design Procedure

The OPA856 meets the growing demand for wideband, low-noise photodiode amplifiers. The closed-loop bandwidth of a transimpedance amplifier is a function of the following:

1. The total input capacitance (C_{IN}). This total includes the photodiode capacitance, the input capacitance of the amplifier (common-mode and differential capacitance) and any stray capacitance from the PCB.
2. The op amp gain bandwidth product (GBWP).
3. The transimpedance gain (R_F).

図 9-1 shows the OPA856 configured as a TIA, with the photodiode reverse biased so that the diode cathode is tied to a positive bias voltage. In this configuration, the diode sources current into the op amp feedback loop so that the output swings in a negative direction relative to the input common-mode (VOFFSET) voltage. The feedback resistance (R_F) and the input capacitance (C_{IN}) form a zero in the noise gain that results in instability if left unchecked. To counteract the effect of the zero, a pole is inserted into the noise gain transfer function by adding the feedback capacitor (C_F).

The *Transimpedance Considerations for High-Speed Amplifiers Application Report* discusses theories and equations that show how to compensate a transimpedance amplifier for a particular transimpedance gain and input capacitance. The bandwidth and compensation equations from the application report are available in a Microsoft Excel ™ calculator. *What You Need To Know About Transimpedance Amplifiers – Part 1* provides a link to the calculator. Calculating the expected bandwidth with an approximate input capacitance of 4 pF and a feedback capacitor of 1 pF yields a bandwidth of approximately 200 MHz.

The amplifier was tested in a transimpedance configuration by using a photodiode with an optical fiber input connection. A tunable laser connected through an optical modulator was used to create the modulated optical excitation to the photodiode. 図 9-2 shows the test setup configuration for the frequency response measurement. The network analyzer's swept frequency output drives the optical modulators electrical input which in turn drives the photodiode. The OPA856 output drives the network analyzer's input.

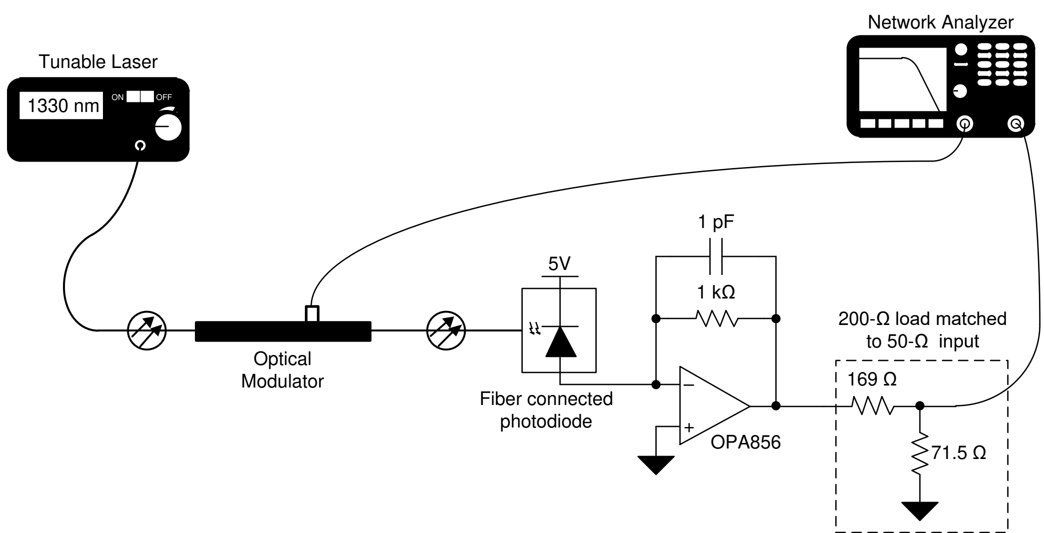


図 9-2. OPA856 Transimpedance Frequency Response Test Setup

図 9-4 shows the frequency response measurements for a small signal and large signal (~1 Vpp) output. The plot contains noticeable noise and variations because the test environment did not have complete capability to accurately manage the thermal drift, perform optical connection integrity analysis, and calibrate the optical path. A more stringently controlled optical environment could achieve more stable results, but was beyond the scope of these measurements. The results in 図 9-4 correlate well with predicted results of approximately 200 MHz of bandwidth. It is expected that the results would not perfectly match calculated values because it is challenging to perfectly account for all parasitic capacitances that affect the input and feedback capacitance in the transimpedance calculations.

Many transimpedance applications can have unpredicted, large input currents that can cause the amplifier's output to saturate. It is often important to understand how the amplifier will behave when its output is saturated at various levels of overdrive. A typical linear amplifier like the OPA856 can be expected to have an output saturation recovery time that increases as the amount of output overdrive increases. When using a pulse based input signal, the output saturation recovery time effectively extends the duration of the pulse. 図 9-3 shows the test setup configuration to measure a pulsed optical input to the OPA856. The optical modulator used in the test setup had limited output amplitude capability to create a saturated signal. In order to prevent the modulator from saturating, the OPA856 output was saturated by adjusting VOFFSET close to the the amplifier's output swing limit on the negative rail.

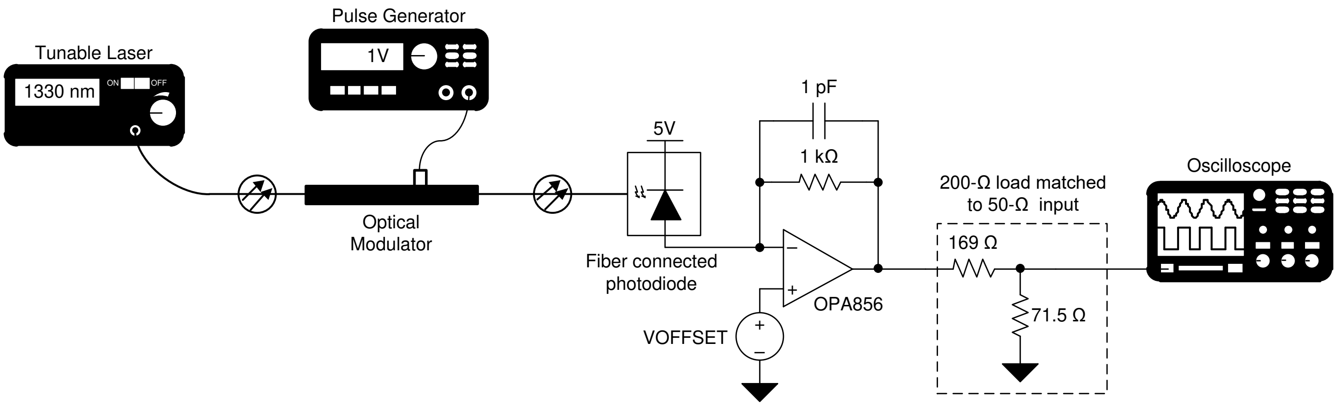


図 9-3. OPA856 Transimpedance Pulse Saturation Extention Test Setup

図 9-5 shows the resulting shifted output pulses labelled by the magnitude of voltage they are overdriving the amplifiers output saturation voltage level (V_{OV}). These values only serve as approximations of the overdrive level of the signal because of expected variances from the optical interface setup. 図 9-6 shows a magnified view of the rising edge of the measured pulse responses in order to better detail the pulse extension created by the signal overdrive. These plots have been scaled and normalized to be easier to read and compare. As expected, 図 9-6 shows that the pulse duration is extended as the overdrive level increases. The data only captured an overdrive voltage maximum of 640 mV, but it can be expected that larger voltages would extend the pulse further.

9.2.3 Application Curves

Note

図 9-6 output voltages are scaled for visual comparison purposes and are not the actual measured values. See 図 9-5 for actual measured values.

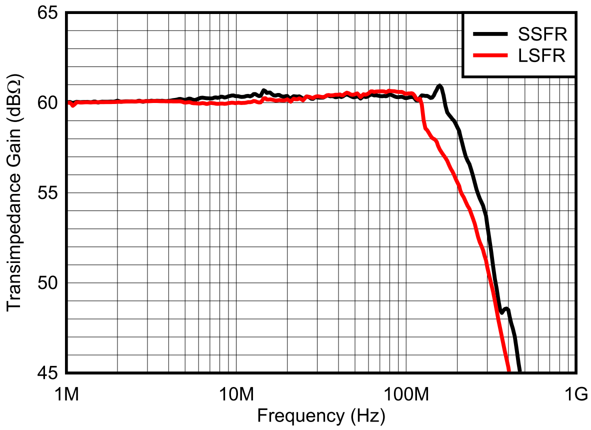


図 9-4. Transimpedance Frequency Response

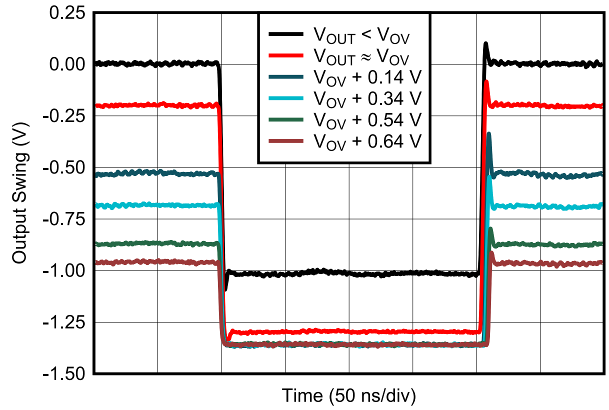


図 9-5. Transimpedance Pulse Response

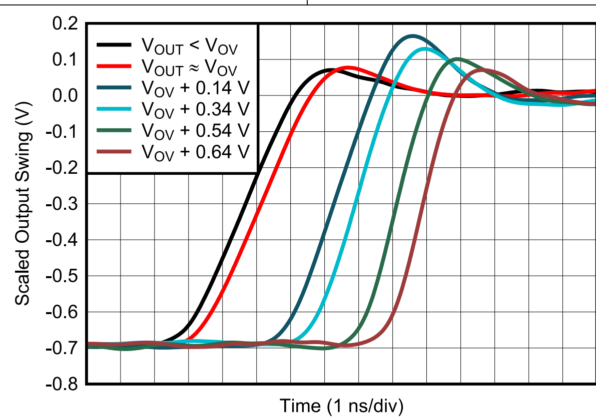


図 9-6. Transimpedance Pulse Response Magnified and Scaled

10 Power Supply Recommendations

The OPA856 operates on supplies from 3.3 V to 5.25 V. The OPA856 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA856 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

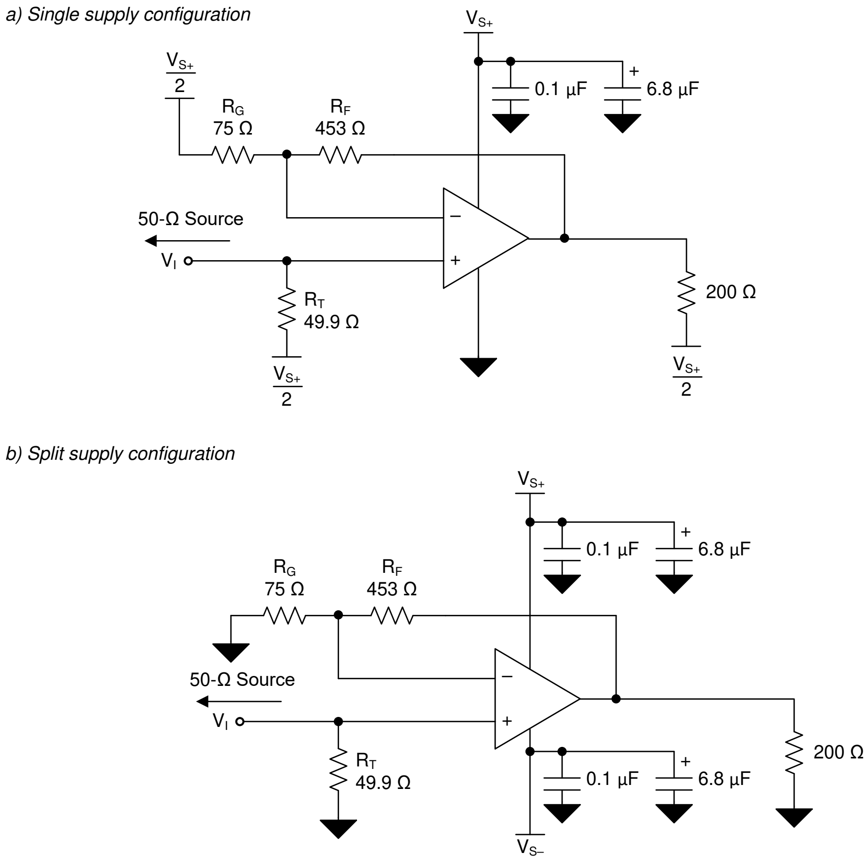


図 10-1. Split and Single Supply Circuit Configuration

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA856 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is less than 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
- **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency bypass capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).
- **Careful selection and placement of external components preserves the high-frequency performance of the OPA856.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wirewound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. When configuring the OPA856 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.

11.2 Layout Example

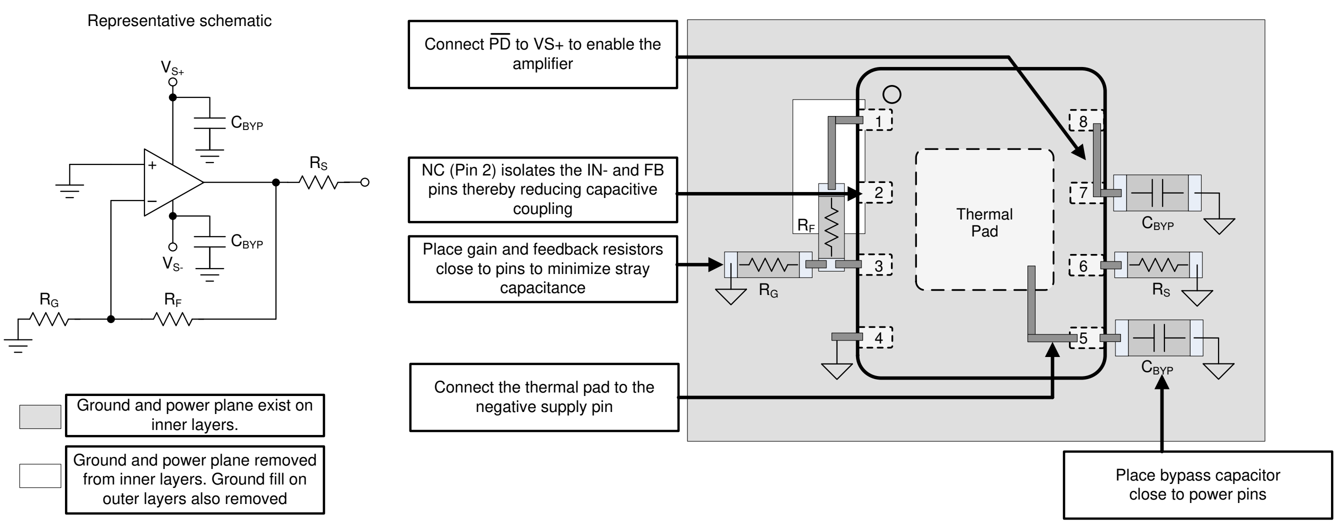


図 11-1. Layout Recommendation

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- *LIDAR Pulsed Time of Flight Reference Design*
- *LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters*
- *Wide Bandwidth Optical Front-end Reference Design*

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA855EVM user's guide*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers application report*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments *What You Need To Know About Transimpedance Amplifiers – Part 2*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA856IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	856
OPA856IDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	856

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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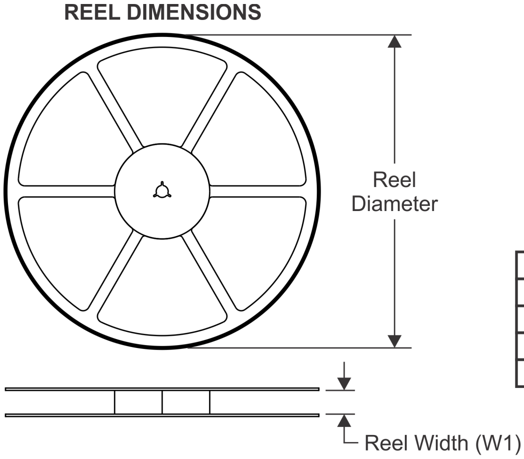
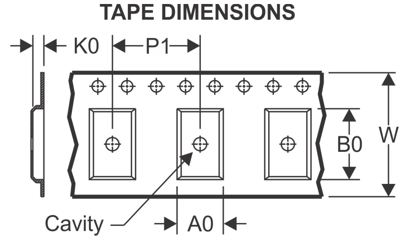
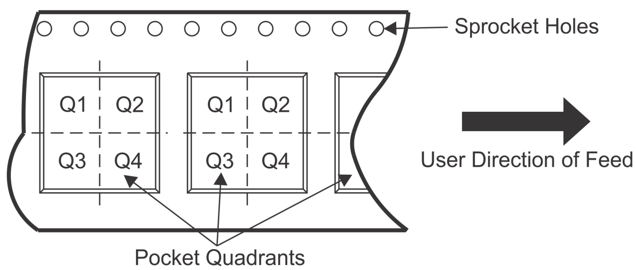
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

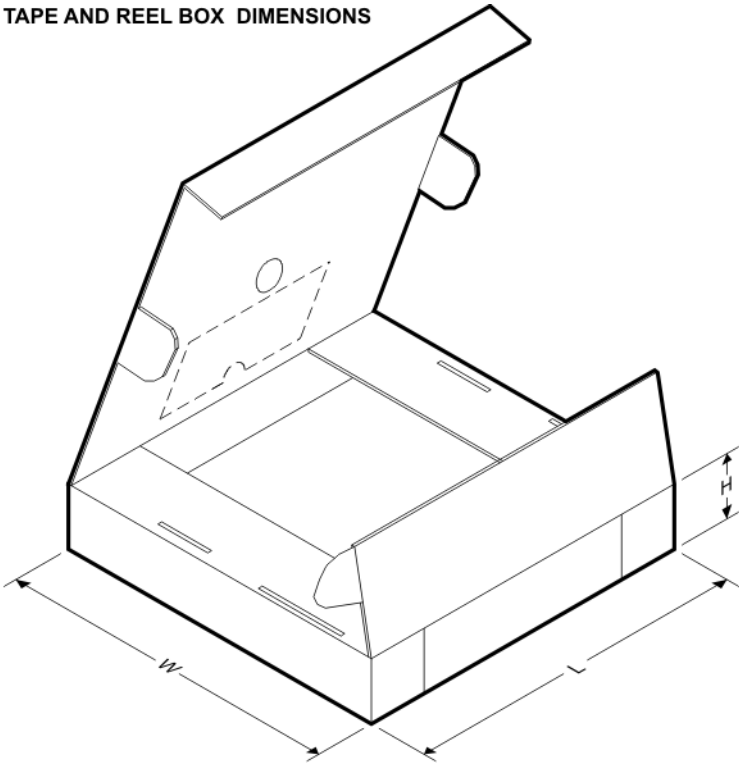
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA856IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

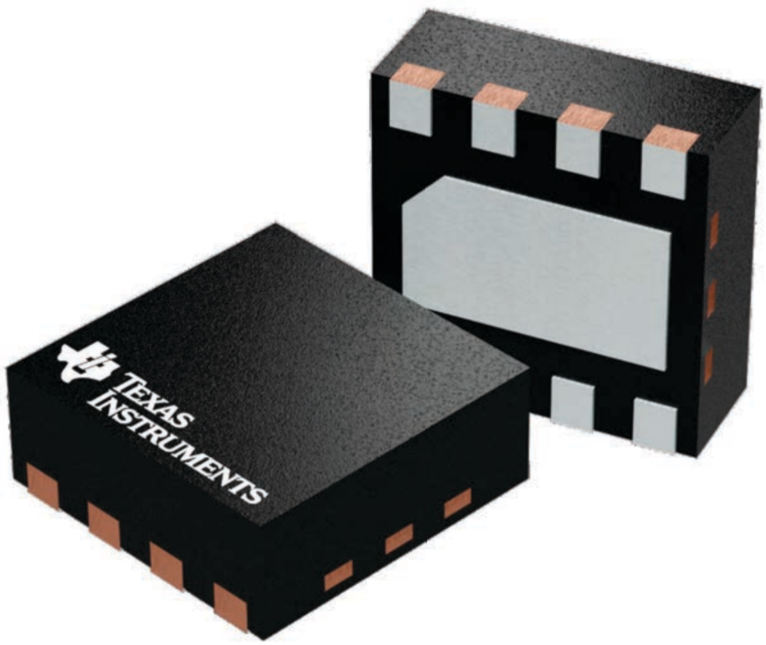
TAPE AND REEL BOX DIMENSIONS

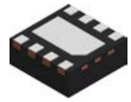


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA856IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



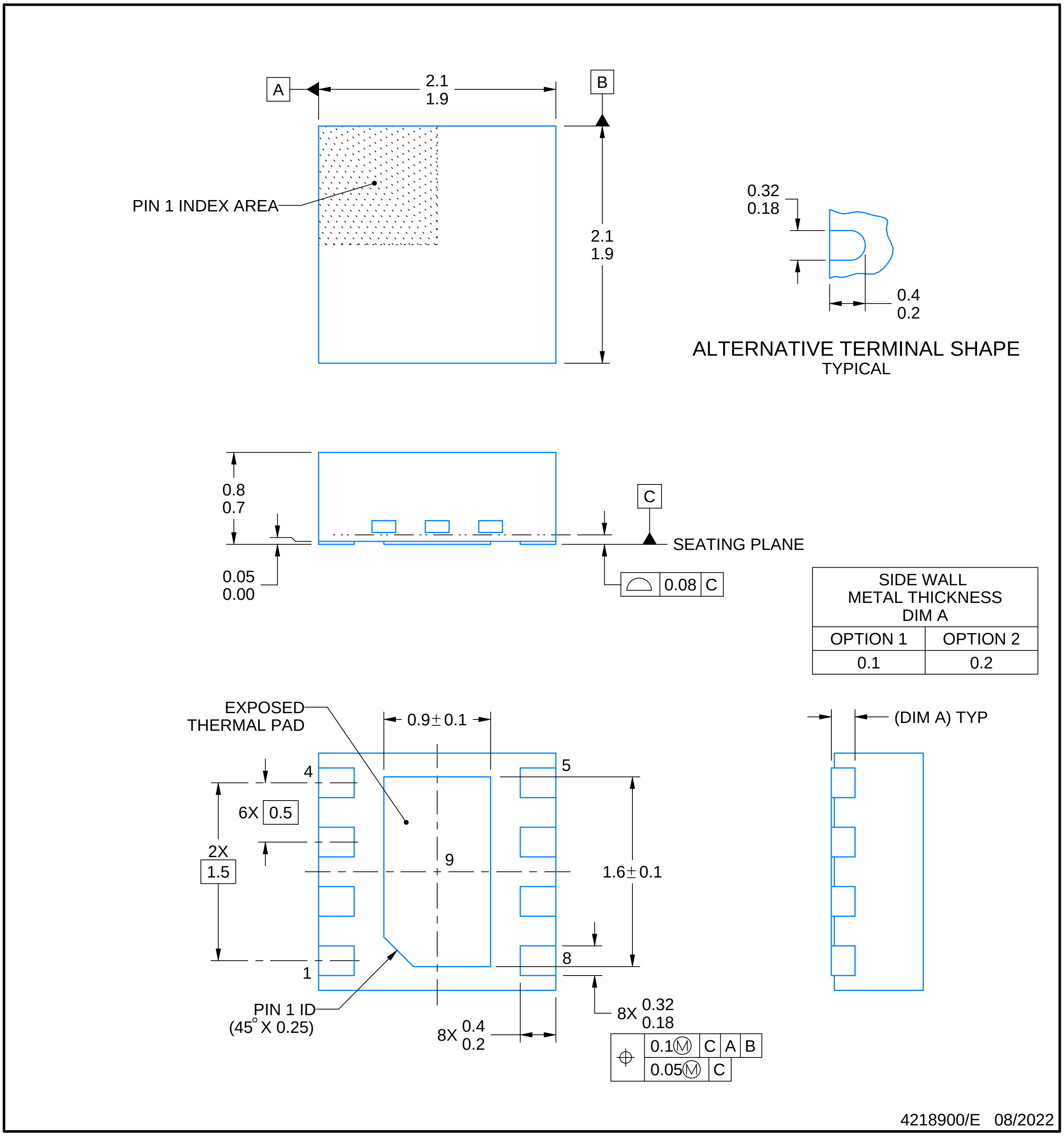


PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

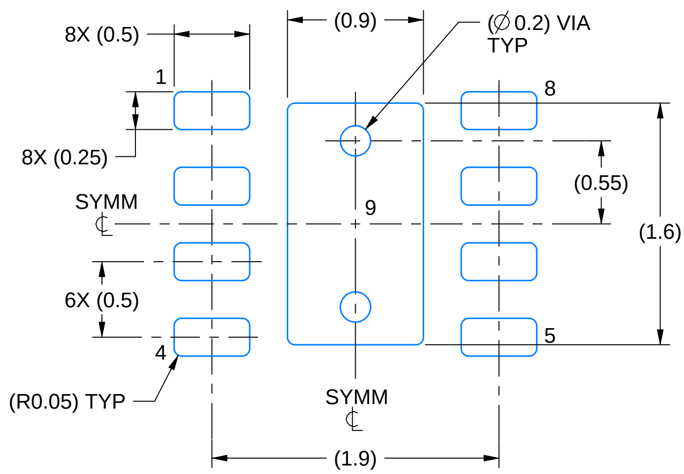
PLASTIC SMALL OUTLINE - NO LEAD



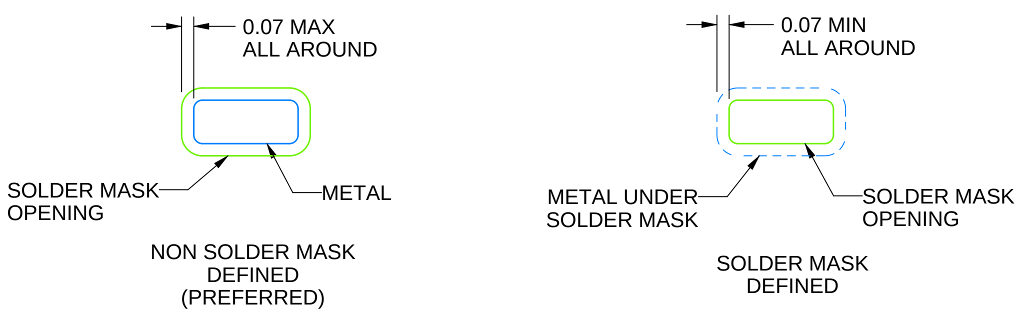
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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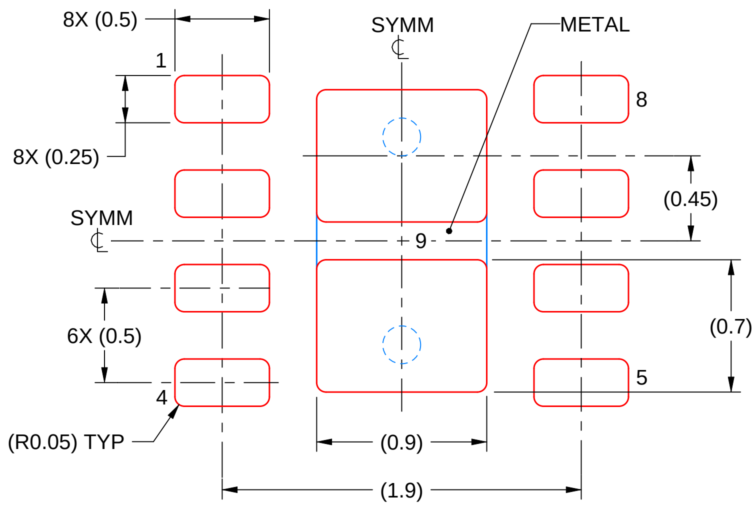
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月