OPAx837 低消費電力、高精度、105MHz電圧帰還型オペアンプ

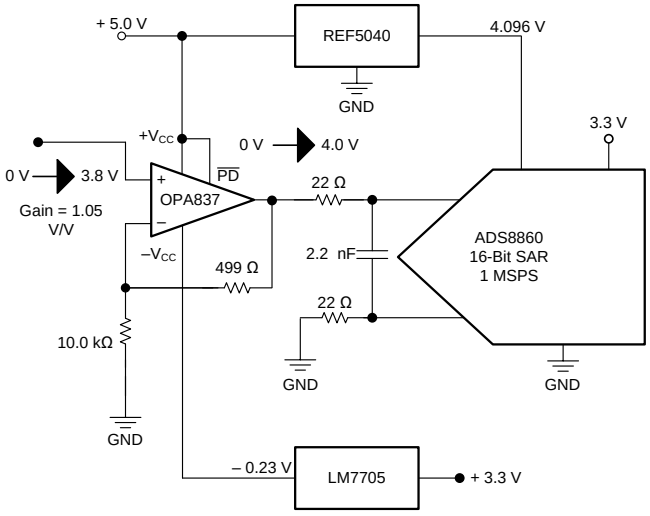
1 特長

- 帯域幅: 105MHz (A_V = 1V/V)
- 非常に低い(トリムされた)消費電流: 600µA
- ゲイン帯域幅積: 50MHz
- スルーレート: 105V/µs
- 負レール入力、レール・ツー・レール出力
- 単一電源動作電圧範囲: 2.7V～5.4V
- 25℃での入力オフセット: ±130µV (最大値)
- 入力オフセット電圧ドリフト(DCKパッケージ): < ±1.6µV/℃(最大値)
- 入力電圧ノイズ: 4.7nV/√Hz (> 100Hz)
- HD2: $2V_{PP}$、100kHzにおいて-120dBc
- HD3: $2V_{PP}$、100kHzにおいて-145dBc
- セトリング時間(0.1%) : 35ns (0.5Vステップ)
- シャットダウン電流: 5µA、パワー・スケーリング・アプリケーションでシャットダウンから高速でリカバリ

2 アプリケーション

- 12ビット～16ビットの低消費電力SARドライバ
- 高精度ADCリファレンス・バッファ
- 超低消費電力アクティブ・フィルタ
- 低消費電力トランスインピーダンス・アンプ
- センサ信号コンディショニング
- ウェアラブル・デバイス
- ローサイド電流センシング

真のグランド入力および出力範囲を備えた低消費電力、低ノイズ、高精度、シングルエンドSAR ADCドライバ



3 概要

OPA837およびOPA2837はシングルおよびデュアル・チャネルのユニティ・ゲイン安定、電圧帰還型アンプで、高精度オペアンプとして最高の電力対帯域幅比(MHz/mW)を実現しています。5Vの単一電源でチャネルごとの消費電流を600µAに抑えたこれらの3.0mWデバイスは、1V/Vのゲインで105MHzの帯域幅を提供します。±0.4µV/℃の標準(±1σ)ドリフトで、±130µV (最大値)という非常に低い値のトリムされたオフセット電圧を実現します。

OPAx837は、シングルエンドの逐次比較型(SAR)アナログ/デジタル・コンバータ(ADC)駆動アプリケーションに最適で、3mWの静止電力で4.7nV/√Hzという極めて低い入力スポット・ノイズ・レベルを実現します。50MHzの非常に高いゲイン帯域幅積により、SAR ADCドライバ・アプリケーションでの急速充電電流の供給に必要な高周波数に対して、低い出力インピーダンスを提供します。この低いダイナミック出力インピーダンスは、高精度ADCを搭載したリファレンス・バッファ・アプリケーションにも適しています。シングル・チャネルのOPA837は6ピンのSOT-23パッケージ(電源シャットダウン機能が含まれます)と、5ピンのSC70パッケージで供給され、デュアル・チャネルのOPA2837は8ピンのVSSOPパッケージと、10ピンのWQFNパッケージで供給されます。

OPAx837は、-40℃～+125℃の広い温度範囲で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA837	SOT-23 (6)	2.90mm×1.60mm
	SC70 (5)	2.00mm×1.25mm
OPA2837	VSSOP (8)	3.00mm×3.00mm
	WQFN (10)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (August 2018) から **Revision D** に変更 **Page**

- 「*概要*」セクションにWQFN (RUN)パッケージへの言及を 追加 ... 1
- Added OPA2837 RUN package thermal information to document. ... 6
- Changed values of maximum and minimum input-referred offset voltage at 25℃ and across temperature in 5 V and 3 V Electrical Characteristics tables. ... 7
- Changed value of maximum input offset current drift for OPA2837 in 5 V and 3 V Electrical Characteristics tables. ... 8
- Changed minimum value of CMRR in 5 V Electrical Characteristics table ... 8
- 追加 reference to TIDA-01565 reference design in *Power-Down Operation* section ... 24
- 追加 reference to TIDA-01565 reference design in*1-Bit PGA Operation* section ... 42

Revision B (July 2018) から **Revision C** に変更 **Page**

- OPA2837 RUNパッケージをドキュメントに 追加 ... 1

Revision A (April 2018) から **Revision B** に変更 **Page**

- Changed input common-mode impedance in 5V and 3V electrical characteristics tables ... 8

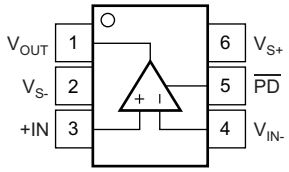
2017年9月発行のものから更新 **Page**

- ドキュメントにOPA2837を 追加 ... 1
- 「特長」の「*単一電源動作電圧範囲*」箇条書き項目を 追加 ... 1
- 表紙の図で「*1SPS*」を「*1MSPS*」に 変更 ... 1
- Added footnote to *Pin Functions* table ... 4
- Changed footnote describing method of computation of slew rate in Electrical Characteristics: V_S = 5 V table ... 7
- Changed default test condition in Electrical Characteristics: V_S = 3 V table ... 9

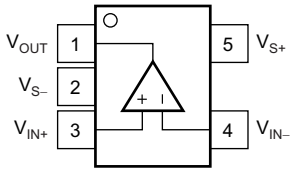
- Changed footnote describing method of computation of slew rate in Electrical Characteristics: V_S = 3 V table 9
- Changed values for common-mode input range, high in Electrical Characteristics: V_S = 3 V table 10
- Changed values for V_{OH} in Electrical Characteristics: V_S = 3 V table 10
- 変更 *V_O = 20 mV_{PP}* to *V_{OUT} = 200 mV_{PP}* in conditions of *Noninverting Response Flatness vs Gain* and *Inverting Response Flatness vs Gain* figures 11
- 変更 *gain –1 V/V* to *gain –2 V/V*, swapped legend colors in *Inverting Overdrive Recovery* figure 12
- 変更 V_{OUT} = 2 V_{PP} to V_{OUT} = 1 V_{PP} in conditions of *Typical Characteristics: V_S = 3.0 V* section 14
- 変更 *V_O = 20 mV_{PP}* to *V_{OUT} = 200 mV_{PP}* in *Noninverting Response Flatness vs Gain* and *Inverting Response Flatness vs Gain* figure conditions 14
- 変更 *V_{IN}* to *V_{IN} × –1 gain*, swapped legend colors in *Inverting Overdrive Recovery* figure 15
- 変更 *V_O = 2 V_{PP}* to *V_{OUT} = 1 V_{PP}* in *Harmonic Distortion vs R_{LOAD}* figure conditions 16
- 変更 *V_{OUT} = 2 V_{PP}* to *V_{OUT} = 1 V_{PP}* in *Harmonic Distortion vs Gain Magnitude* figure conditions 16
- 変更 y-axis caption in *Turn-On Time to Sinusoidal Input* and *Turn-Off Time to Sinusoidal Input* figures 19
- 追加 OPA838 row to *Device Family Comparison* table 23
- 変更 EVM link in *Split-Supply Operation* section from *OPA837DBV* to *OPA835DBV* 26
- 変更 V2 value from *2.5* to *–2.5 V* in *Characterization Test Circuit for Network, Spectrum Analyzer* figure 30
- 変更 V_{EE} value from *2.5 V* to *–2.5 V* in *Inverting Characterization Circuit for Network Analyzer* figure 32
- 変更 *1 SPS* to *1 MSPS* in *OPA837 and ADS8860 Example Circuit* figure 38

5 Pin Configuration and Functions

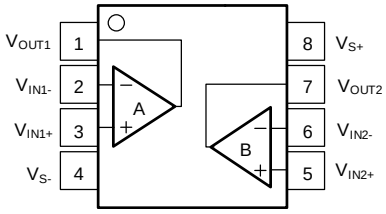
OPA837 DBV Package
6-Pin SOT-23
Top View



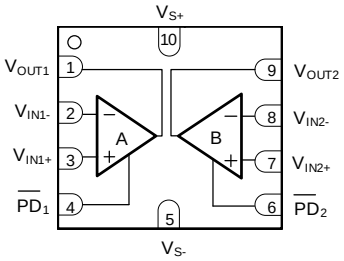
OPA837 DCK Package
5-Pin SC70
Top View



OPA2837 DGK Package
8-Pin VSSOP
Top View



OPA2837 RUN Package
10-Pin WQFN
Top View



Pin Functions

PIN					FUNCTION(1)	DESCRIPTION
NAME	OPA837		OPA2837			
	SOT-23	SC-70	VSSOP	WQFN		
$\overline{PD}$	5	—	—	—	I	Amplifier power down. Low = disabled, high = normal operation (pin must be driven).
$\overline{PD}_1$	—	—	—	4	I	Amplifier 1 power down. Low = disabled, high = normal operation (pin must be driven).
$\overline{PD}_2$	—	—	—	6	I	Amplifier 2 power down. Low = disabled, high = normal operation (pin must be driven).
$V_{IN–}$	4	4	—	—	I	Inverting input pin
V_{IN+}	3	3	—	—	I	Noninverting input pin
$V_{IN1–}$	—	—	2	2	I	Amplifier 1 inverting input pin
V_{IN1+}	—	—	3	3	I	Amplifier 1 noninverting input pin
$V_{IN2–}$	—	—	6	8	I	Amplifier 2 inverting input pin
V_{IN2+}	—	—	5	7	I	Amplifier 2 noninverting input pin
V_{OUT}	1	1	—	—	O	Output pin
V_{OUT1}	—	—	1	1	O	Amplifier 1 output pin
V_{OUT2}	—	—	7	9	O	Amplifier 2 output pin
$V_{S–}$	2	2	4	5	P	Negative power-supply pin
V_{S+}	6	5	8	10	P	Positive power-supply input

(1) I = input, O = output, and P = power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{S–}$ to V_{S+}	Supply voltage		5.5	V
	Supply turn-on/off maximum dV/dT(2)		1	V/µs
V_I	Input voltage	$V_{S–}$ – 0.5	V_{S+} + 0.5	V
V_{ID}	Differential input voltage		±1	V
I_I	Continuous input current		±10	mA
I_O	Continuous output current(3)		±20	mA
	Continuous power dissipation	See *Thermal Information: OPA837*		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Staying below this ± supply turn-on edge rate prevents the edge-triggered ESD absorption device across the supply pins from turning on.
(3) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single-supply voltage	2.7	5	5.4	V
T_A	Ambient temperature	–40	25	125	°C

6.4 Thermal Information: OPA837

THERMAL METRIC(1)		OPA837		UNIT
		DBV (SOT23-6)	DCK (SC70)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	194	203	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	129	152	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39	76	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26	58	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39	76	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information: OPA2837

THERMAL METRIC(1)		OPA2837		UNIT
		RUN (WQFN-10)	DGK (VSSOP-8)	
		10 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.9	182	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	72.0	63.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.2	103.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	7.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.0	101.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics: V_S = 5 V

at V_{S+} = 5 V, $V_{S–}$ = 0 V, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1	90	105		MHz	C
		V_{OUT} = 20 mV_{PP}, G = 2		45			C
		V_{OUT} = 20 mV_{PP}, G = 10		5			C
GBP	Gain-bandwidth product	V_{OUT} = 20 mV_{PP}, G = 10	45	50		MHz	C
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 2		26		MHz	C
	Bandwidth for 0.1-dB flatness	V_{OUT} = 200 mV_{PP}, G = 2		6		MHz	C
SR	Slew rate	From LSBW(2)		105		V/µs	C
t_R, t_F	Rise, fall time	V_{OUT} = 0.5-V step, G = 2, input t_R = 10 ns		10	11	ns	C
	Overshoot	V_{OUT} = 2-V step, G = 2, input t_R = 40 ns		7.0%			C
	Settling time to 0.1%	V_{OUT} = 2.0-V step, G = 1, input t_R = 4 ns		25		ns	C
	Settling time to 0.01%	V_{OUT} = 2.0-V step, G = 1, input t_R = 4 ns		40		ns	C
HD2	Second-order harmonic distortion	f = 100 kHz, V_O = 2 V_{PP}, G = 1 (see Figure 73)		–120		dBc	C
HD3	Third-order harmonic distortion	f = 100 kHz, V_O = 2 V_{PP}, G = 1 (see Figure 73)		–145		dBc	C
	Input voltage noise	f = 500 Hz		4.7		nV/√Hz	C
	Voltage noise 1/f corner frequency	See Figure 39		35		Hz	C
	Input current noise	f = 20 kHz		0.4		pA/√Hz	C
	Current noise 1/f corner frequency	See Figure 39		5		kHz	C
	Overdrive recovery time	G = 2, 2x output overdrive (see Figure 30)		75		ns	C
	Closed-loop output impedance	f = 1 MHz, G = 1 (see Figure 38)		0.14		Ω	C
	Channel-to-channel crosstalk (OPA2837)	f = 10 kHz		-126		dBc	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	V_O = ±2 V, R_L = 2 kΩ	120	135		dB	A
	Input-referred offset voltage	T_A ≈ 25°C	–165	±30	165	µV	A
		T_A = 0°C to +70°C (DCK package)	–205	±30	235		B
		T_A = –40°C to +85°C (DCK package)	–269	±30	261		B
		T_A = –40°C to +125°C (DCK package)	–269	±30	325		B
	Input offset voltage drift(3)	DCK package, T_A = –40°C to +125°C	–1.6	±0.4	1.6	µV/°C	B
		DBV, RUN package, T_A = –40°C to +125°C	–2.0	±0.4	2.0		B
		DGK package, T_A = –40°C to +125°C		±0.67			B
	Input bias current(4)	T_A ≈ 25°C	150	340	520	nA	A
		T_A = 0°C to +70°C	50	340	664		B
		T_A = –40°C to +85°C	50	340	718		B
		T_A = –40°C to +125°C	50	340	850		B
	Input bias current drift(3)	T_A = –40°C to +125°C	0.8	1.5	3.3	nA/°C	B
	Input offset current	T_A ≈ 25°C (OPA837)	–40	±6	40	nA	A
		T_A = 0°C to +70°C	–46	±6	52		B
		T_A = –40°C to +85°C	–56	±6	55		B
		T_A = –40°C to +125°C	–56	±6	65		B
		T_A ≈ 25°C (OPA2837)	-60	±8	60		A

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C, overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(0.8 \times V_{PEAK} / \sqrt{2}) \times 2\pi \times f_{-3dB}$ where this f_{-3dB} is the typical measured 2-V_{PP} bandwidth at gains of 1 V/V.
(3) Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range. Typical drift specifications are ±1sigma. Maximum drift specifications are set by min/max sample packaged test data using a wafer-level screened drift. Min/Max drift is not specified by final automated test equipment (ATE) nor by QA sample testing.
(4) Current is considered positive out of the pin.

Electrical Characteristics: V_S = 5 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = 0 V, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
	Input offset current drift(3)	T_A = –40°C to +125°C	–250	±40	250	pA/°C	B
		T_A = –40°C to +125°C (OPA2837)	–270	±80	330		B
	Input-referred offset voltage mismatch	T_A ≈ 25°C (OPA2837)	-220	50	220	µV	A
INPUT							
	Common-mode input range, low	T_A ≈ 25°C, < 3-dB degradation in CMRR limit		–0.2	0	V	A
		T_A = –40°C to +125°C, < 3-dB degradation in CMRR limit		–0.2	0		B
	Common-mode input range, high	T_A ≈ 25°C, < 3-dB degradation in CMRR limit	3.7	3.8		V	A
		T_A = –40°C to +125°C, < 3-dB degradation in CMRR limit	3.7	3.8			B
CMRR	Common-mode rejection ratio		91	110		dB	A
	Input impedance common-mode			175 || 1.5		MΩ || pF	C
	Input impedance differential mode			180 || 0.5		kΩ || pF	C
OUTPUT							
V_{OL}	Output voltage, low	T_A ≈ 25°C, G = 2		0.05	0.1	V	A
		T_A = –40°C to +125°C, G = 5		0.05	0.1		B
V_{OH}	Output voltage, high	T_A ≈ 25°C, G = 2	4.9	4.95		V	A
		T_A = –40°C to +125°C, G = 5	4.8	4.9			B
	Maximum current into a resistive load	T_A ≈ 25°C, ±1.6 V into 27 Ω, V_{IO} < 2 mV	±58	±70		mA	A
	Linear current into a resistive load	T_A ≈ 25°C, ±1.7 V into 37.4 Ω, A_{OL} > 80 dB	±45	±50		mA	A
	Linear current into a resistive load overtemperature	T_A = –40°C to +125°C, ±1.31 V into 37.4 Ω, A_{OL} > 80 dB	±35	±45		mA	C
	Closed-loop output impedance	Gain of 1 V/V, ±30-mA DC		0.6		mΩ	C
POWER SUPPLY							
	Specified operating voltage		2.7		5.4	V	B
	Quiescent operating current per amplifier (5-V supply)	T_A ≈ 25°C(5)	564	592	625	µA	A
		T_A = –40°C to +125°C	408	592	865		B
	Supply current temperature coefficient per amplifier	T_A = –40°C to +125°C (see Figure 57)	1.1	1.9	2.4	µA/°C	B
+PSRR	Positive power-supply rejection ratio		95	110		dB	A
–PSRR	Negative power-supply rejection ratio		92	108		dB	A
POWER DOWN (Pin Must be Driven)							
	Enable voltage threshold	Specified *on* above $V_{S–}$ + 1.5 V			1.5	V	A
	Disable voltage threshold	Specified *off* below $V_{S–}$ + 0.55 V	0.55			V	A
	Power-down pin bias current	$\overline{PD}$ = 0 V to V_{S+}	–50		50	nA	A
	Power-down quiescent current	$\overline{PD}$ ≤ 0.55 V	4	5	10	µA	A
	Power-down quiescent current over temperature	$\overline{PD}$ ≤ 0.55 V, T_A = –40°C to +125°C			10	µA	B
	Turnon time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		300		ns	C
	Turnoff time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value		100		ns	C

(5) The typical specification is at 25°C T_J. The min, max limits are expanded for the automated test equipment (ATE) to account for an ambient range from 22°C to 32°C with a 2-µA/°C temperature coefficient on the supply current.

6.7 Electrical Characteristics: V_S = 3 V

at V_{S+} = 3 V, $V_{S–}$ = 0 V, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1	85	105		MHz	C
		V_{OUT} = 20 mV_{PP}, G = 2		45			C
		V_{OUT} = 20 mV_{PP}, G = 10		5			C
GBP	Gain-bandwidth product	V_{OUT} = 20 mV_{PP}, G = 10	40	50		MHz	C
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}, G = 2		30		MHz	C
	Bandwidth for 0.1-dB flatness	V_{OUT} = 200 mV_{PP}, G = 2		6		MHz	C
SR	Slew rate	From LSBW(2)		65		V/µs	C
t_R, t_F	Rise, fall time	V_{OUT} = 0.5-V step, G = 2, input t_R = 10 ns		10	11	ns	C
	Overshoot	V_{OUT} = 2-V step, G = 2, input t_R = 40 ns		7%			C
	Settling time to 0.1%	V_{OUT} = 0.5-V step, G = 1, input t_R = 4 ns		35		ns	C
	Settling time to 0.01%	V_{OUT} = 0.5-V step, G = 1, input t_R = 4 ns		50		ns	C
HD2	Second-order harmonic distortion	f = 100 kHz, V_O = 1 V_{PP}, G = 1 (see Figure 73)		–125		dBc	C
HD3	Third-order harmonic distortion	f = 100 kHz, V_O = 1 V_{PP}, G = 1 (see Figure 73)		–138		dBc	C
	Input voltage noise	f = 500 Hz		4.9		nV/√Hz	C
	Voltage noise 1/f corner frequency	See Figure 39		35		Hz	C
	Input current noise	f = 10 kHz		0.4		pA/√Hz	C
	Current noise 1/f corner frequency	See Figure 39		5		kHz	C
	Overdrive recovery time	G = 2, 2x output overdrive (see Figure 29)		65		ns	C
	Closed-loop output impedance	f = 1 MHz, G = 1 (see Figure 38)		0.14		Ω	C
	Channel-to-channel crosstalk (OPA2837)	f = 10 kHz		-126		dBc	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	V_O = ±1 V, R_L = 2 kΩ	120	133		dB	A
		V_O = ±1 V, R_L = 2 kΩ (OPA2837)	110	133			A
	Input-referred offset voltage	T_A ≈ 25°C	–165	±30	165	µV	A
		T_A = 0°C to +70°C	–205	±30	235		B
		T_A = –40°C to +85°C	–269	±30	261		B
		T_A = –40°C to +125°C	–269	±30	325		B
	Input offset voltage drift(3)	DCK package, T_A = –40°C to +125°C	–1.6	±0.4	1.6	µV/°C	B
		DBV, RUN package, T_A = –40°C to +125°C	–2.0	±0.4	2.0		B
		DGK package, T_A = –40°C to +125°C		±0.67			B
	Input bias current(4)	T_A ≈ 25°C	145	320	510	nA	A
		T_A = 0°C to +70°C	50	320	659		B
		T_A = –40°C to +85°C	50	320	708		B
		T_A = –40°C to +125°C	50	320	840		B
	Input bias current drift(3)	T_A = –40°C to +125°C	0.8	1.5	3.3	nA/°C	B
	Input offset current	T_A ≈ 25°C (OPA837)	–40	±6	40	nA	A
		T_A = 0°C to +70°C	–46	±6	52		B
		T_A = –40°C to +85°C	–56	±6	55		B
		T_A = –40°C to +125°C	–56	±6	65		B
		T_A ≈ 25°C (OPA2837)	–60	±8	60		A

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C, overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(0.8 \times V_{PEAK} / \sqrt{2}) \times 2\pi \times f_{-3dB}$ where this f_{-3dB} is the typical measured 2-Vpp bandwidth at gains of 1V/V.
(3) Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range. Typical drift specifications are ±1sigma. Maximum drift specifications are set by min/max sample packaged test data using a wafer-level screened drift. Min/Max drift is not specified by final automated test equipment (ATE) nor by QA sample testing.
(4) Current is considered positive out of the pin.

Electrical Characteristics: V_S = 3 V (continued)

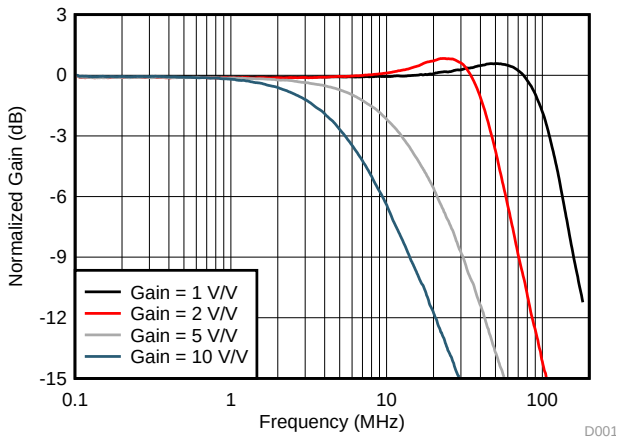
at V_{S+} = 3 V, $V_{S–}$ = 0 V, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
	Input offset current drift(3)	T_A = –40°C to +125°C	–250	±40	250	pA/°C	B
		T_A = –40°C to +125°C (OPA2837)	–250	±80	330		B
	Input-referred offset voltage mismatch	T_A ≈ 25°C (OPA2837)	-220	50	220	µV	A
INPUT							
	Common-mode input range, low	T_A ≈ 25°C, < 3-dB degradation in CMRR limit		–0.2	0	V	A
		T_A = –40°C to +125°C, < 3-dB degradation in CMRR limit		–0.2	0		B
	Common-mode input range, high	T_A ≈ 25°C, < 3-dB degradation in CMRR limit	1.7	1.8		V	A
		T_A = –40°C to +125°C, < 3-dB degradation in CMRR limit	1.7	1.8			B
CMRR	Common-mode rejection ratio		90	105		dB	A
	Input impedance common-mode			300 || 1.5		MΩ || pF	C
	Input impedance differential mode			180 || 0.5		kΩ || pF	C
OUTPUT							
V_{OL}	Output voltage, low	T_A ≈ 25°C, G = 2		0.05	0.1	V	A
		T_A = –40°C to +125°C, G = 2		0.10	0.2		B
V_{OH}	Output voltage, high	T_A ≈ 25°C, G = 2	2.9	2.95		V	A
		T_A = –40°C to +125°C, G = 2	2.8	2.9			B
	Maximum current into a resistive load	T_A ≈ 25°C, ±0.8 V into 17.5 Ω, V_{IO} < 2 mV	±45	±55		mA	A
	Linear current into a resistive load	T_A ≈ 25°C, ±0.9 V into 21.5 Ω, A_{OL} > 80 dB	±40	±45		mA	A
	Linear current into a resistive load overtemperature	T_A = –40°C to 125°C, ±0.7 V into 21.5 Ω, A_{OL} > 80 dB	±32	±40		mA	C
POWER SUPPLY							
	Specified operating voltage		2.7		5.4	V	B
	Quiescent operating current per amplifier (OPA837, 3-V supply)	T_A ≈ 25°C(5)	547	570	607	µA	A
		T_A = –40°C to +125°C	404	570	817		B
	Quiescent operating current per amplifier (OPA2837, 3-V supply)	T_A ≈ 25°C(5)	540	570	607	µA	A
	Supply current temperature coefficient per amplifier	T_A = –40°C to +125°C (see Figure 57)	0.8	1.7	2.2	µA/°C	B
+PSRR	Positive power-supply rejection ratio		90	110		dB	A
–PSRR	Negative power-supply rejection ratio		88	105		dB	A
POWER DOWN (Pin Must be Driven)							
	Enable voltage threshold	Specified *on* above $V_{S–}$ + 1.5 V			1.5	V	A
	Disable voltage threshold	Specified *off* below $V_{S–}$ + 0.55 V	0.55			V	A
	Power-down pin bias current	$\overline{PD}$ = 0 V to V_{S+}	–50		50	nA	A
	Power-down quiescent current	$\overline{PD}$ ≤ 0.55 V	1	3	8	µA	A
	Power-down quiescent current over temperature	$\overline{PD}$ ≤ 0.55 V, T_A = –40°C to +125°C			8	µA	B
	Turnon time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		300		ns	C
	Turnoff time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value		100		ns	C

(5) The typical spec is at 25°C T_j. The min, max limits are expanded for ATE to account for ambient range from 22°C to 32°C with a +4-uA/°C temperature coefficient on the supply current.

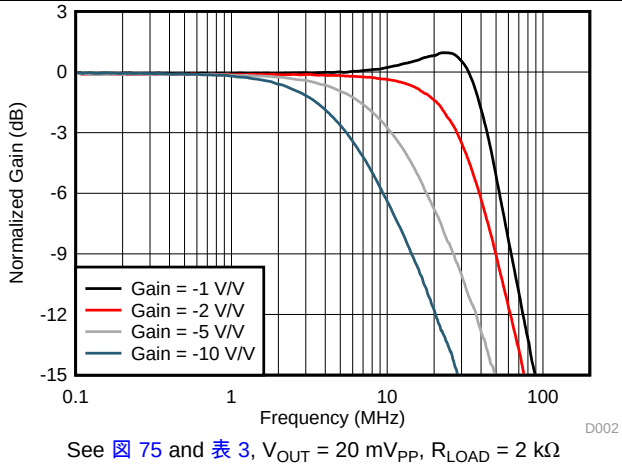
6.8 Typical Characteristics: V_S = 5.0 V

at V_{S+} = 5.0 V, $V_{S–}$ = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



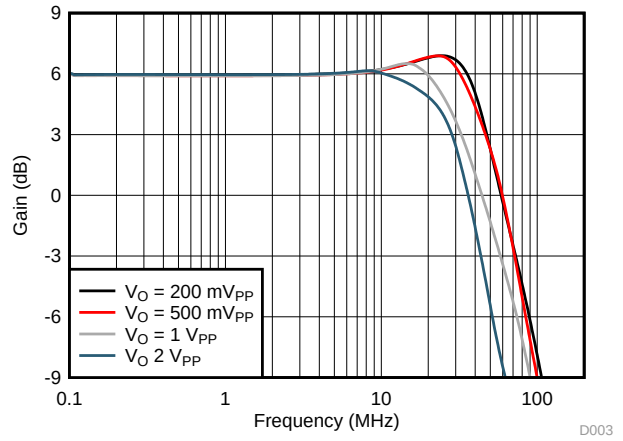
See 図 74 and 表 2, V_{OUT} = 20 mV_{PP}, R_{LOAD} = 2 kΩ

図 1. Noninverting Small-Signal Frequency Response vs Gain



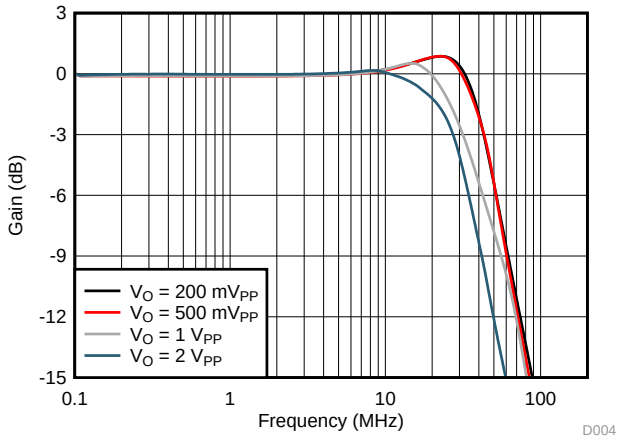
See 図 75 and 表 3, V_{OUT} = 20 mV_{PP}, R_{LOAD} = 2 kΩ

図 2. Inverting Small-Signal Frequency Response vs Gain



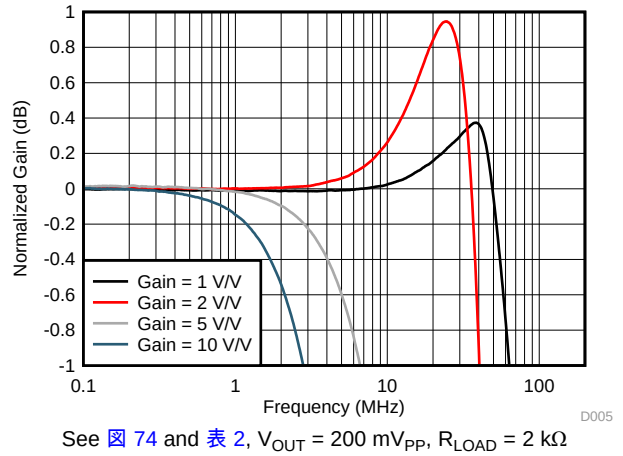
Gain = 2 V/V, R_{LOAD} = 2 kΩ

図 3. Noninverting Large-Signal Bandwidth vs V_{OPP}



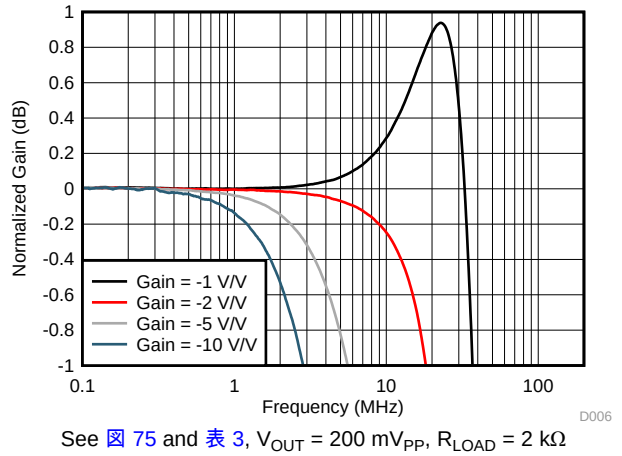
Gain = –1 V/V, R_{LOAD} = 2 kΩ

図 4. Inverting Large-Signal Bandwidth vs V_{OPP}



See 図 74 and 表 2, V_{OUT} = 200 mV_{PP}, R_{LOAD} = 2 kΩ

図 5. Noninverting Response Flatness vs Gain

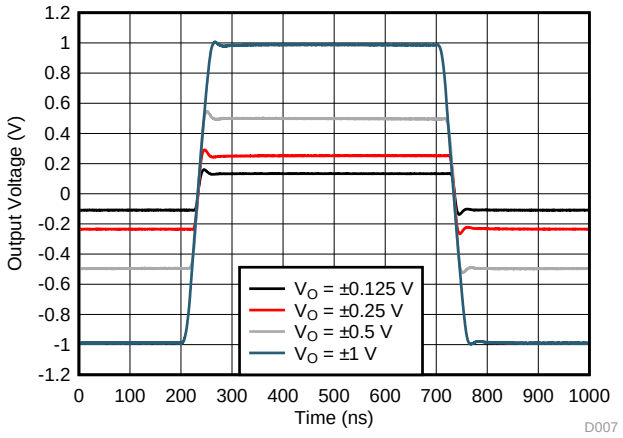


See 図 75 and 表 3, V_{OUT} = 200 mV_{PP}, R_{LOAD} = 2 kΩ

図 6. Inverting Response Flatness vs Gain

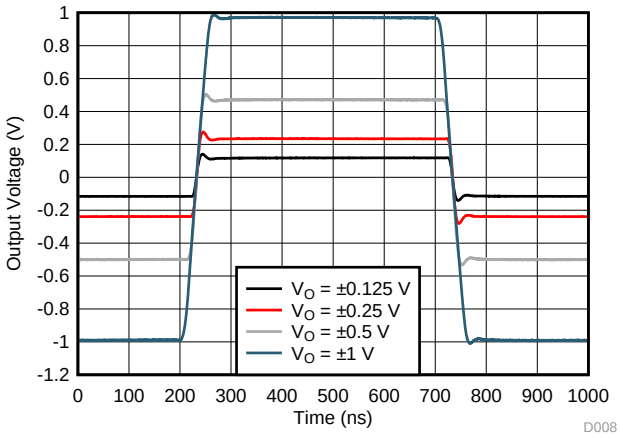
Typical Characteristics: V_S = 5.0 V (continued)

at V_{S+} = 5.0 V, $V_{S–}$ = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



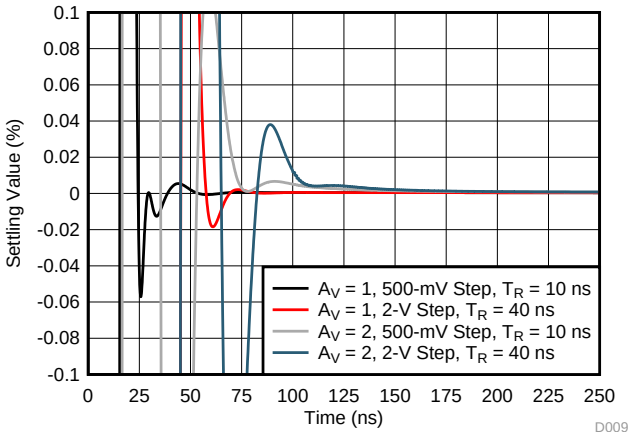
See 図 74, gain = 2 V/V,
input edge rate set to stay below slew limiting

図 7. Noninverting Step Response vs Time and V_{OPP}



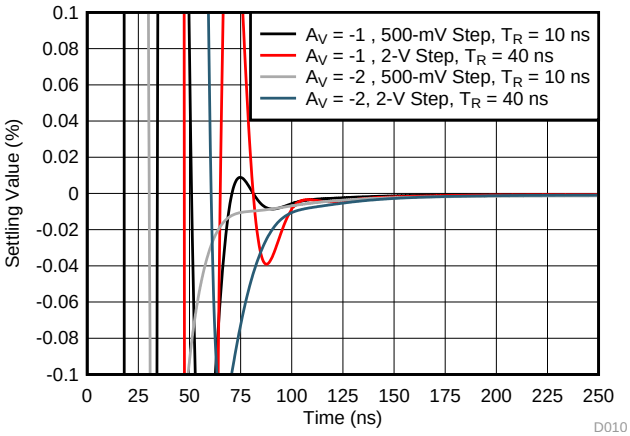
See 図 75, gain = –1 V/V,
input edge rate set to stay below slew limiting

図 8. Inverting Step Response vs Time and V_{OPP}



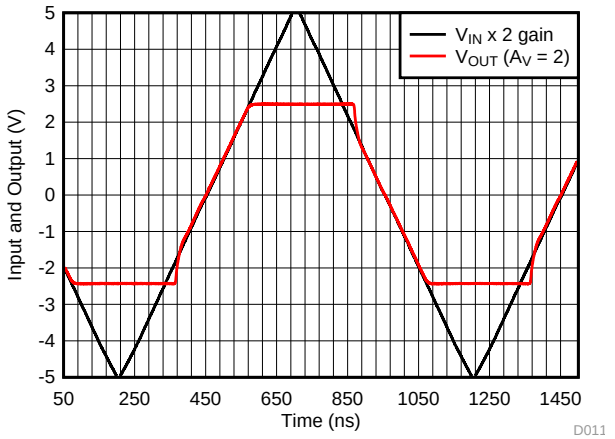
See 図 74 and 表 2

図 9. Simulated Noninverting Settling Time



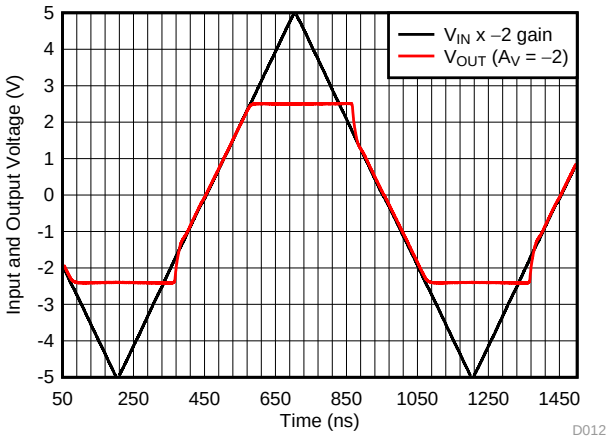
See 図 75 and 表 3

図 10. Simulated Inverting Settling Time



See 図 74 and 表 2, gain = 2 V/V

図 11. Noninverting Overdrive Recovery

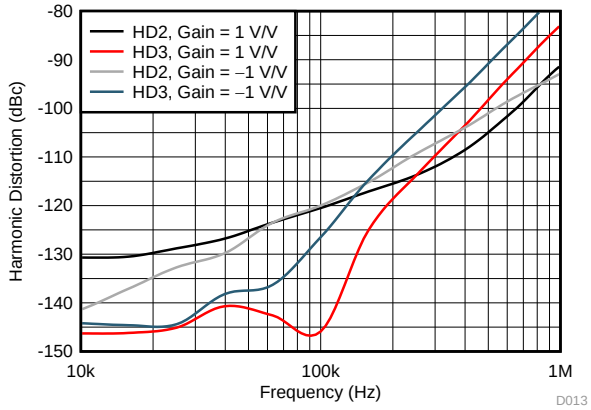


See 図 75 and 表 3, gain –2 V/V

図 12. Inverting Overdrive Recovery

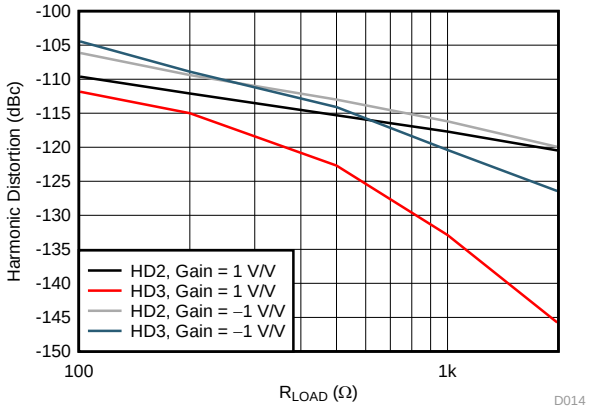
Typical Characteristics: V_S = 5.0 V (continued)

at V_{S+} = 5.0 V, $V_{S–}$ = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



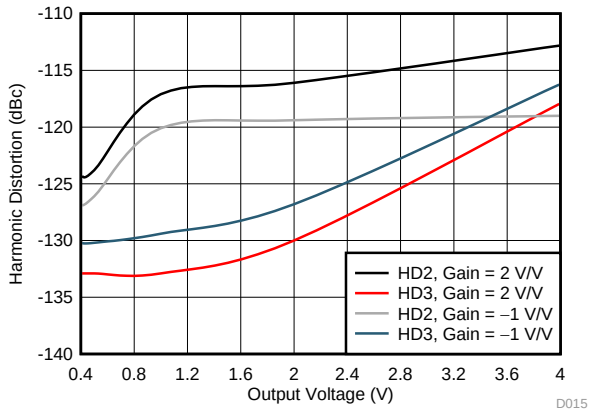
See 図 74, 図 75, 表 2, and 表 3, V_{OUT} = 2 V_{PP}

図 13. Harmonic Distortion vs Frequency



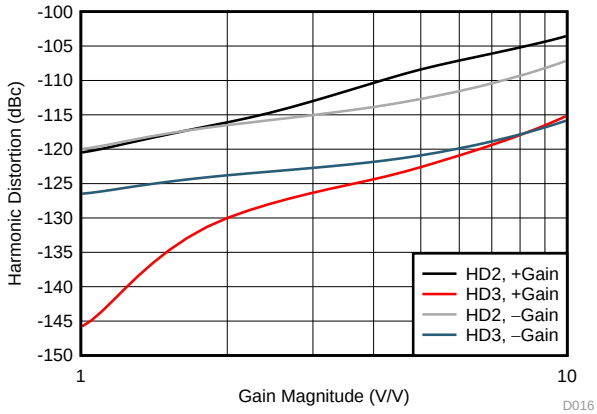
See 図 74, 図 75, 表 2, and 表 3, V_{OUT} = 2 V_{PP}, f = 100 kHz

図 14. Harmonic Distortion vs R_{LOAD}



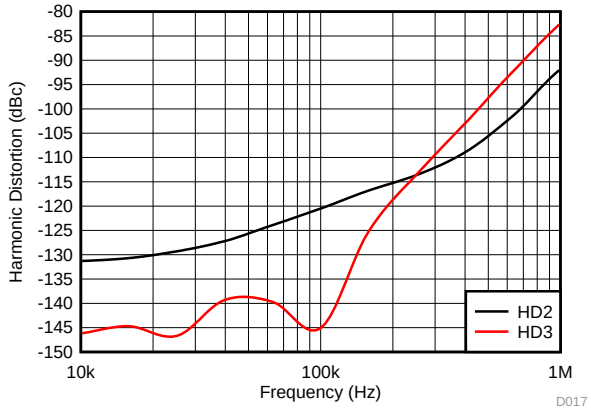
See 図 74, 図 75, 表 2, and 表 3, V_{OUT} = 2 V_{PP}, f = 100 kHz

図 15. Harmonic Distortion vs Output Voltage



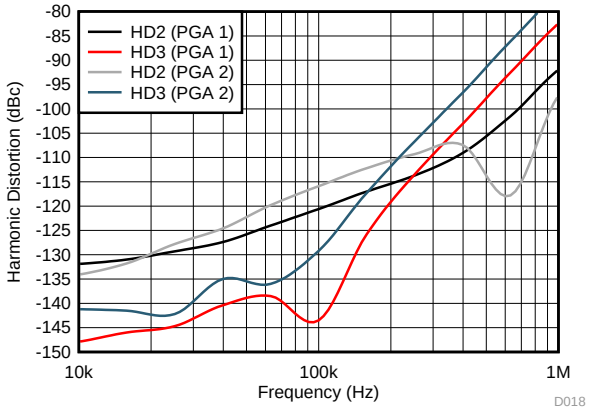
See 図 74, 図 75, 表 2, and 表 3, V_{OUT} = 2 V_{PP}, f = 100 kHz

図 16. Harmonic Distortion vs Gain Magnitude



See 図 87, V_{OUT} = 2 V_{PP}, f = 100 kHz

図 17. Harmonic Distortion as Active Mux

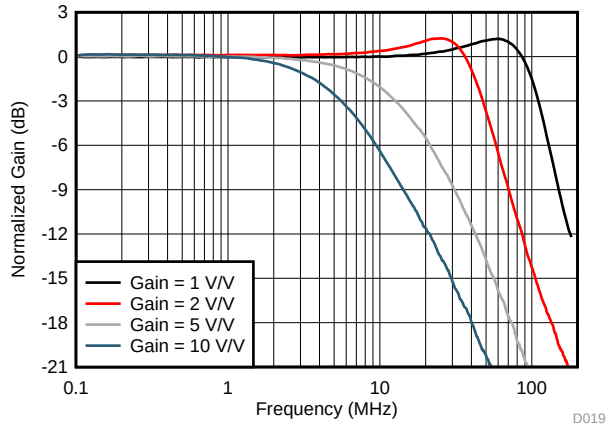


See 図 87, gain of 1 V/V or 2 V/V, V_{OUT} = 2 V_{PP}, f = 100 kHz

図 18. Harmonic Distortion as 1-Bit PGA

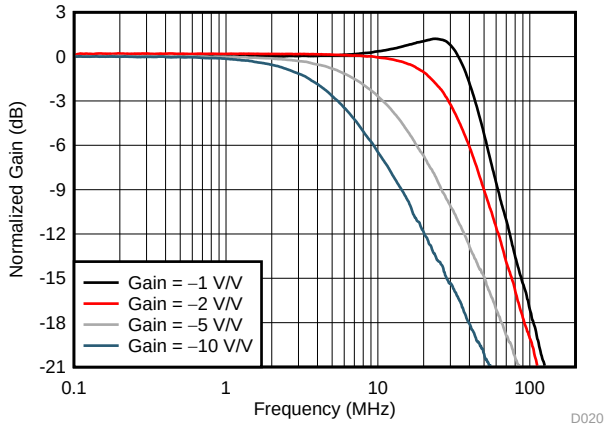
6.9 Typical Characteristics: V_S = 3.0 V

at V_{S+} = 3.0 V, $V_{S–}$ = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



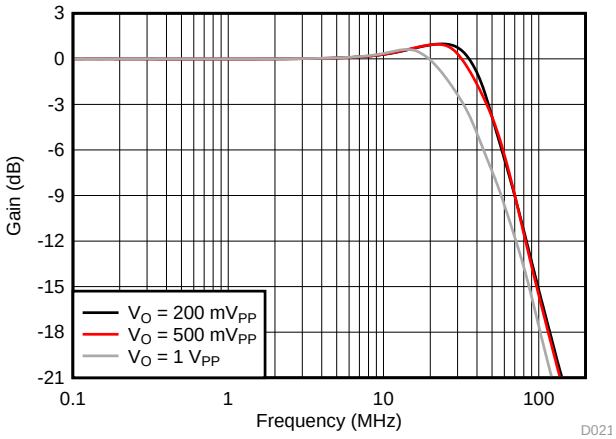
See 図 74 and 表 2, V_{OUT} = 20 mV_{PP}, R_{LOAD} = 2 kΩ

図 19. Noninverting Small-Signal Response vs Gain



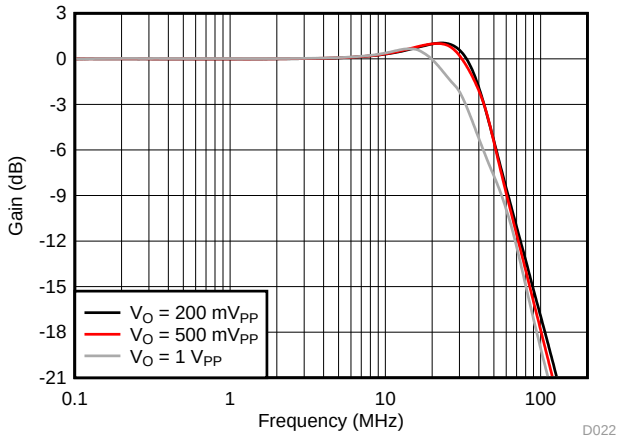
See 図 75 and 表 3, V_{OUT} = 20 mV_{PP}, R_{LOAD} = 2 kΩ

図 20. Inverting Small-Signal Response vs Gain



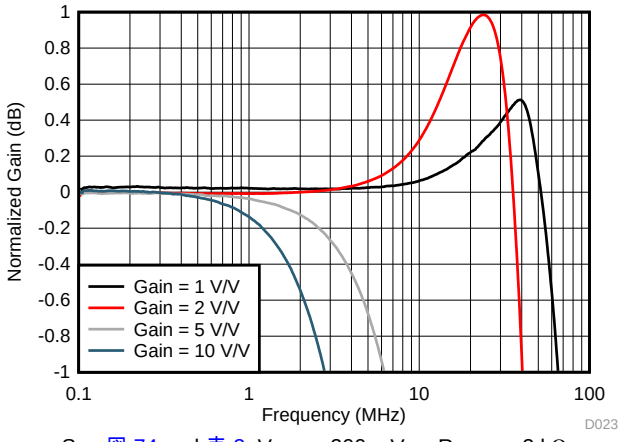
See 図 74, gain = 2 V/V

図 21. Noninverting Large-Signal Bandwidth vs V_{OPP}



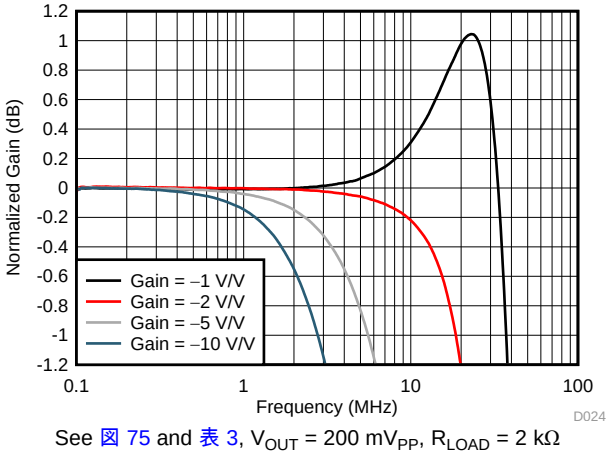
See 図 75, gain = –1 V/V

図 22. Inverting Large-Signal Bandwidth vs V_{OPP}



See 図 74 and 表 2, V_{OUT} = 200 mV_{PP}, R_{LOAD} = 2 kΩ

図 23. Noninverting Response Flatness vs Gain

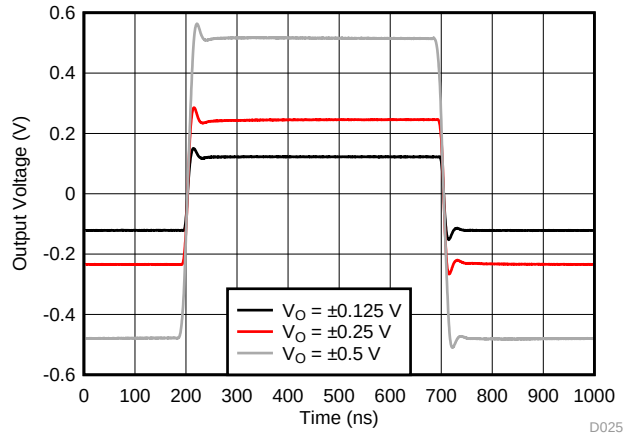


See 図 75 and 表 3, V_{OUT} = 200 mV_{PP}, R_{LOAD} = 2 kΩ

図 24. Inverting Response Flatness vs Gain

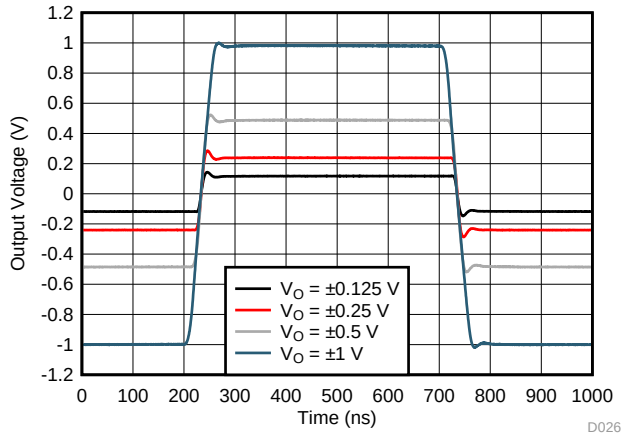
Typical Characteristics: V_S = 3.0 V (continued)

at V_{S+} = 3.0 V, $V_{S–}$ = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



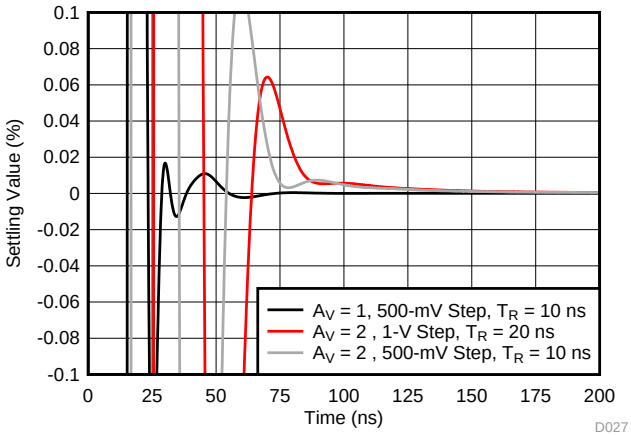
See 図 74 and 表 2, gain = 2 V/V, input edge rate set to stay below slew limiting

図 25. Noninverting Step Response vs V_{OPP}



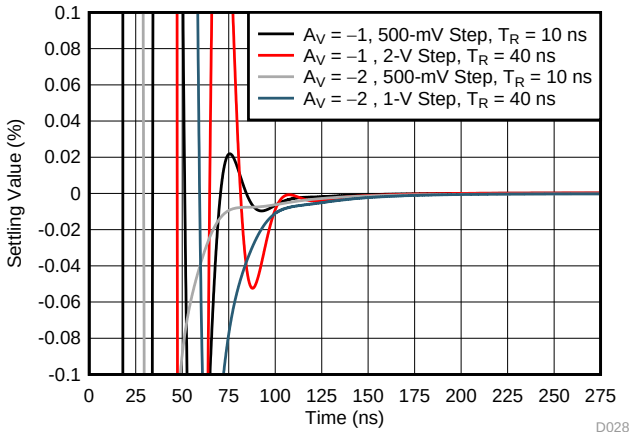
See 図 75 and 表 3, gain = –1 V/V, input edge rate set to stay below slew limiting

図 26. Inverting Step Response vs V_{OPP}



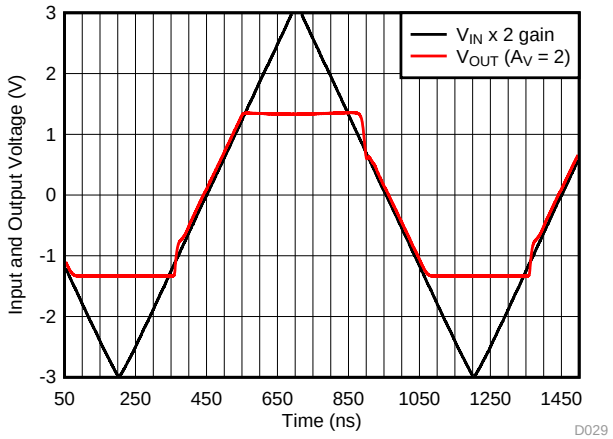
See 図 74 and 表 2

図 27. Simulated Noninverting Settling Time



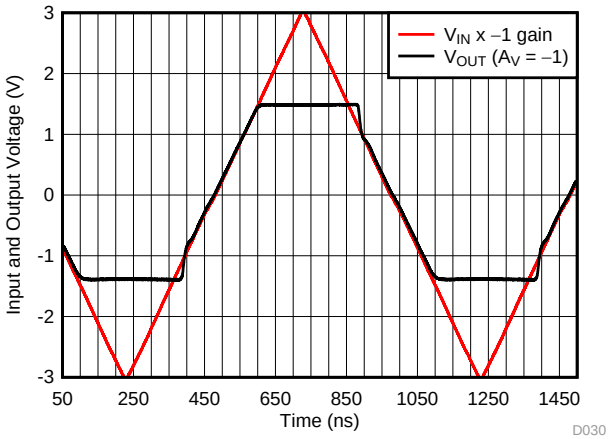
See 図 75 and 表 3

図 28. Simulated Inverting Settling Time



See 図 74 and 表 2, gain = 2 V/V

図 29. Noninverting Overdrive Recovery

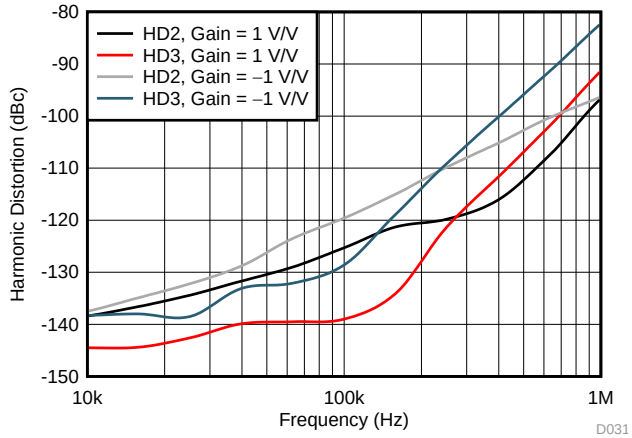


See 図 75 and 表 3, gain = –1 V/V

図 30. Inverting Overdrive Recovery

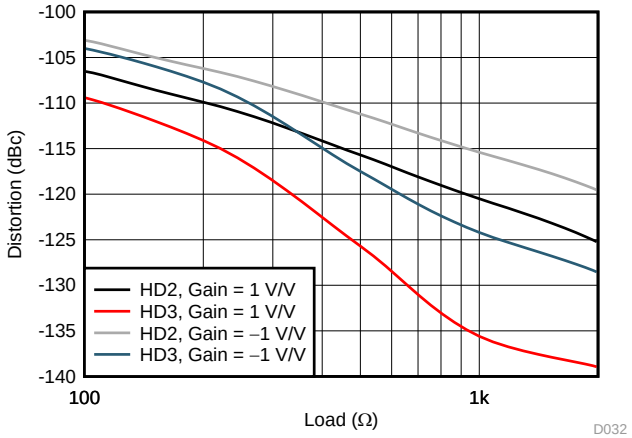
Typical Characteristics: V_S = 3.0 V (continued)

at V_{S+} = 3.0 V, $V_{S–}$ = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



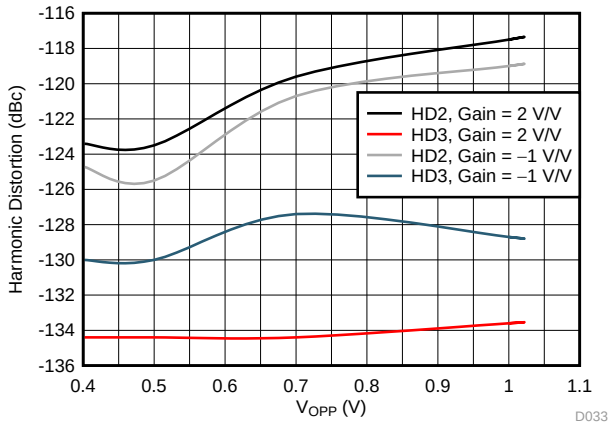
See 図 74, 図 75, 表 2, and 表 3, V_{OUT} = 1 V_{PP}, R_{LOAD} = 2 kΩ

図 31. Harmonic Distortion vs Frequency



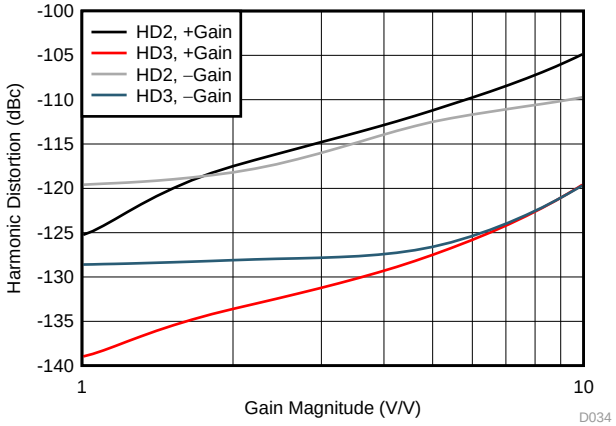
See 図 74, 図 75, 表 2, and 表 3, V_{OUT} = 1 V_{PP}, f = 100 kHz, R_{LOAD} = 2 kΩ

図 32. Harmonic Distortion vs R_{LOAD}



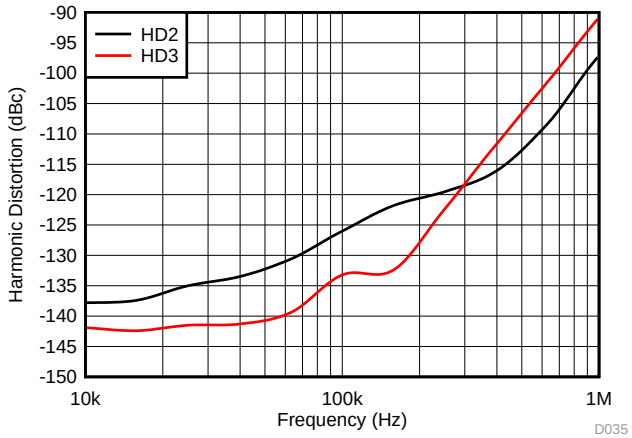
See 図 74, 図 75, 表 2, and 表 3, R_{LOAD} = 2 kΩ, f = 100 kHz

図 33. Harmonic Distortion vs Output Swing



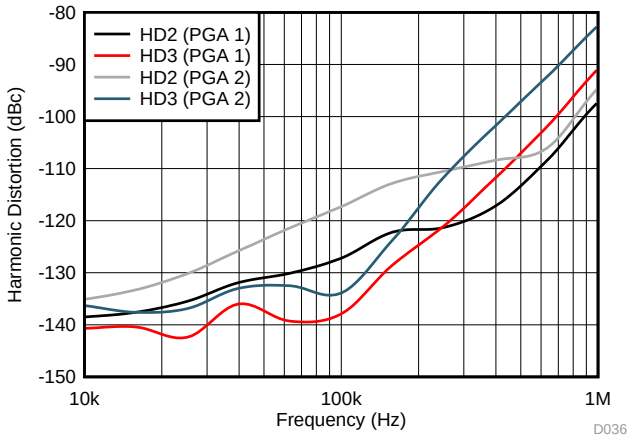
See 図 74, 図 75, 表 2, and 表 3, R_{LOAD} = 2 kΩ, f = 100 kHz, V_{OUT} = 1 V_{PP}

図 34. Harmonic Distortion vs Gain Magnitude



See 図 87, gain = 1 V/V, V_{OUT} = 1 V_{PP}, R_{LOAD} = 2 kΩ

図 35. Harmonic Distortion as Active Mux

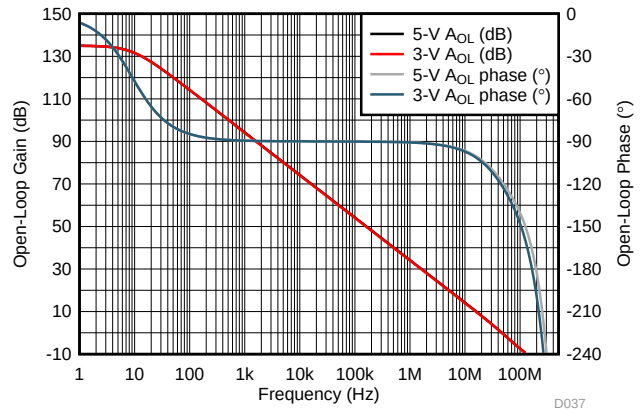


See 図 88, gain of 1 V/V and 2 V/V, V_{OUT} = 1 V_{PP}, R_{LOAD} = 2 kΩ

図 36. Harmonic Distortion as 1-Bit PGA

6.10 Typical Characteristics: ±2.5-V to ±1.5-V Split Supply

with $P_D = V_{CC}$ and $T_A \approx 25°C$ (unless otherwise noted)



No load simulation

図 37. Open-Loop Gain and Phase vs Frequency

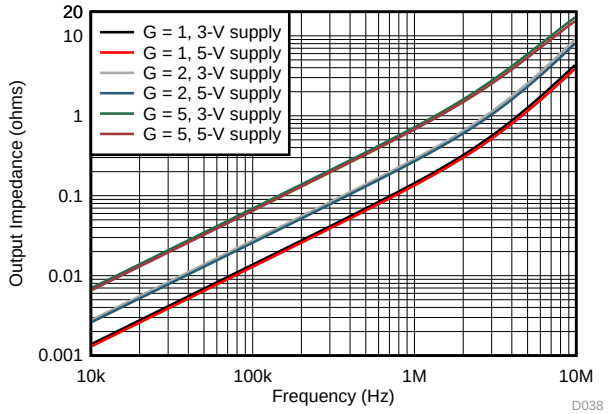
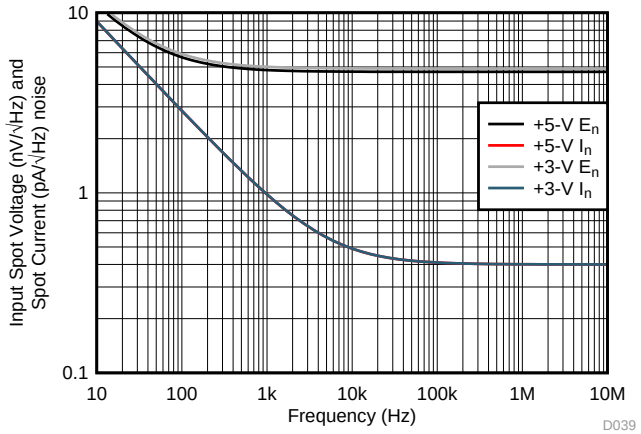


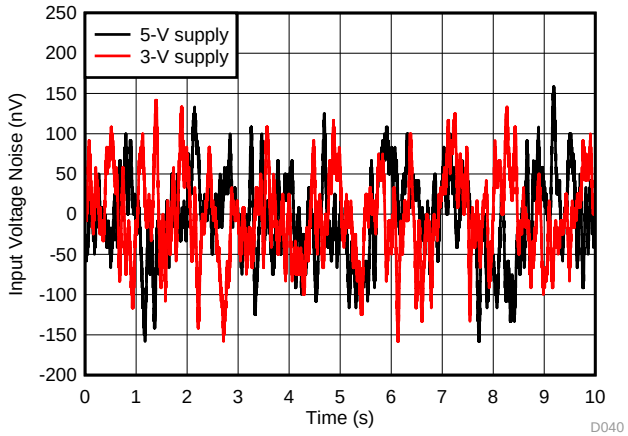
図 74 and 表 2 (simulation)

図 38. Closed-Loop Output Impedance vs Frequency



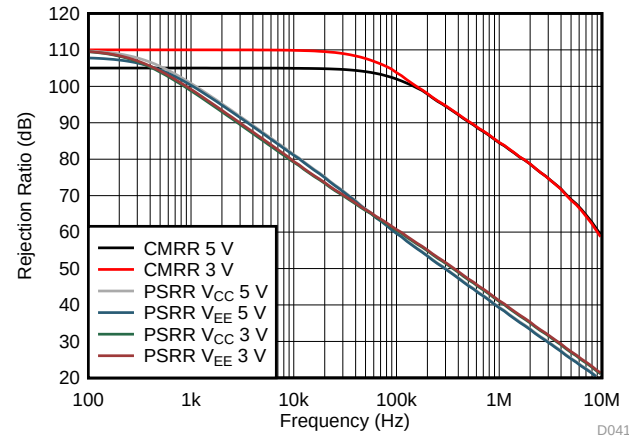
Measured then fit to ideal 1/f model

図 39. Input Spot Noise Density vs Frequency



Input-referred voltage noise $R_S = 0\ \Omega$

図 40. Low-Frequency Voltage Noise vs Time



Simulated curves

図 41. CMRR and PSRR vs Frequency

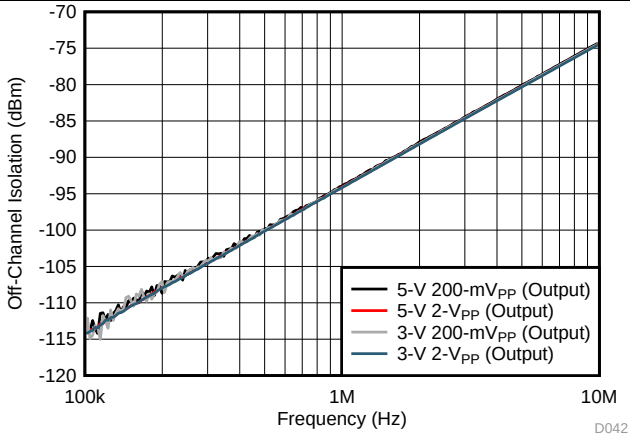
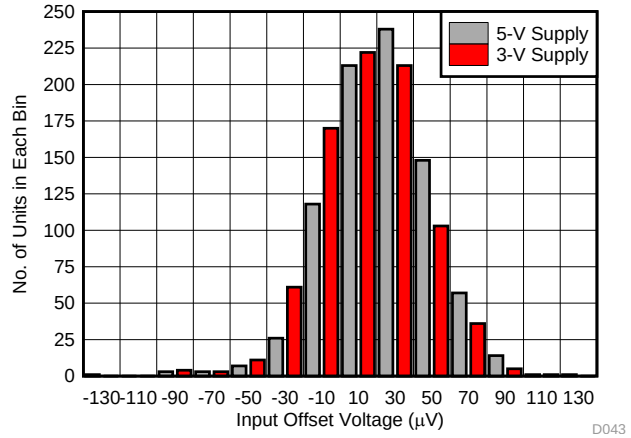


図 42. Disabled Isolation Noninverting Input to Output vs Frequency

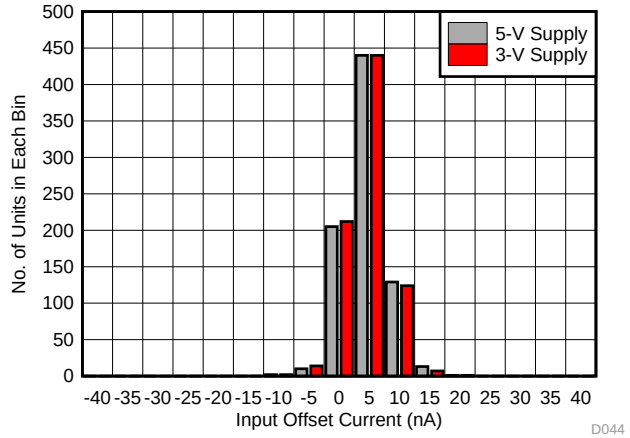
Typical Characteristics: ±2.5-V to ±1.5-V Split Supply (continued)

with $P_D = V_{CC}$ and $T_A \approx 25°C$ (unless otherwise noted)



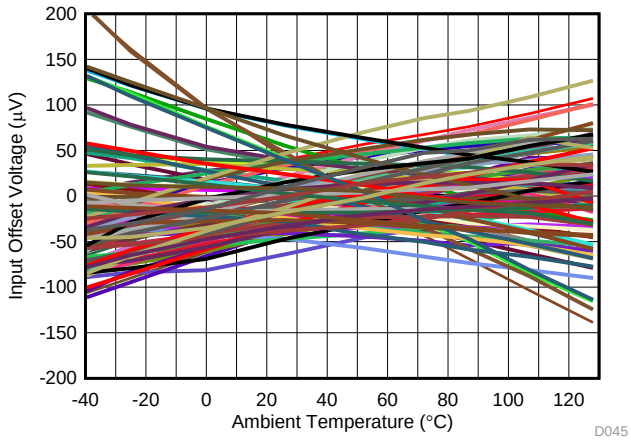
830 units at each supply voltage

図 43. Input Offset Voltage Distribution



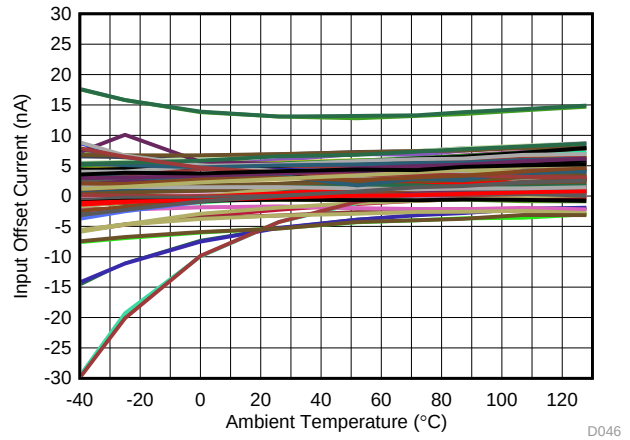
830 units at each supply voltage

図 44. Input Offset Current Distribution



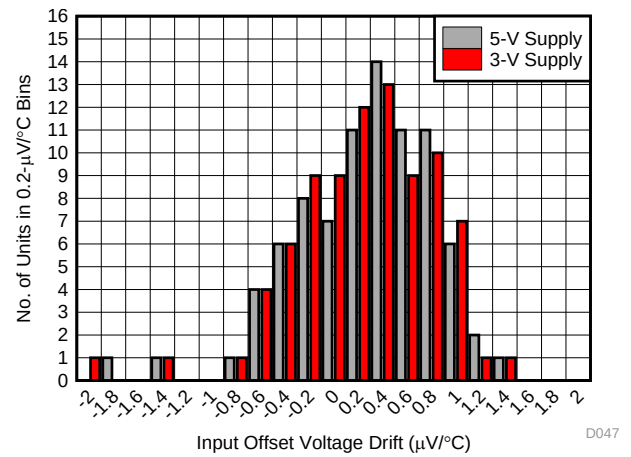
50 units at 5-V and 3-V supply

図 45. Input Offset Voltage vs Ambient Temperature



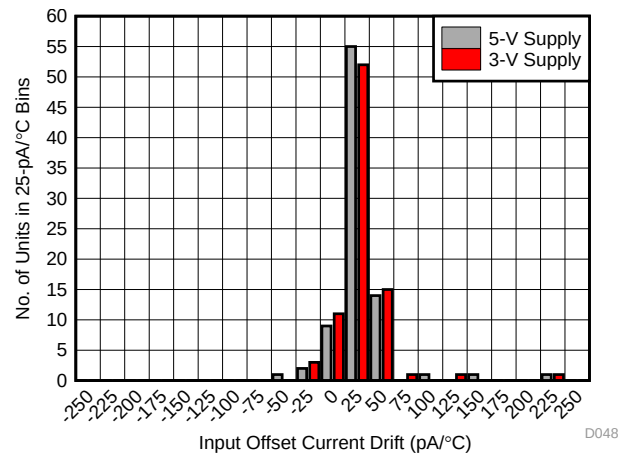
50 units at 5-V and 3-V supply

図 46. Input Offset Current vs Ambient Temperature



–40°C to +125°C fit, 82 units, DBV package

図 47. Input Offset Voltage Drift Distribution

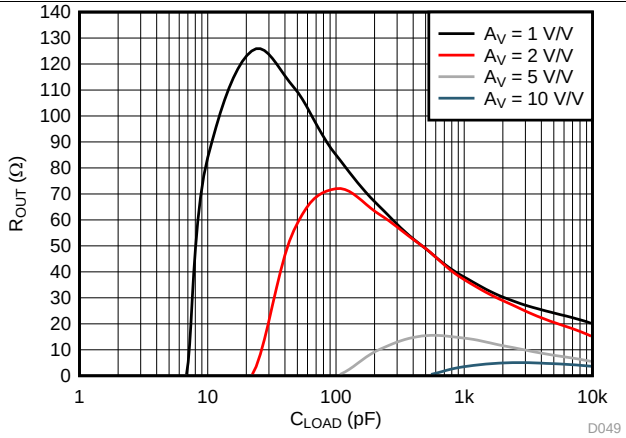


–40°C to +125°C fit, 82 units, DBV package

図 48. Input Offset Current Drift Distribution

Typical Characteristics: ±2.5-V to ±1.5-V Split Supply (continued)

with $P_D = V_{CC}$ and $T_A \approx 25°C$ (unless otherwise noted)



See 図 66 and 表 2, small signal, targeting 30° phase margin

図 49. Output Resistor vs C_{LOAD}

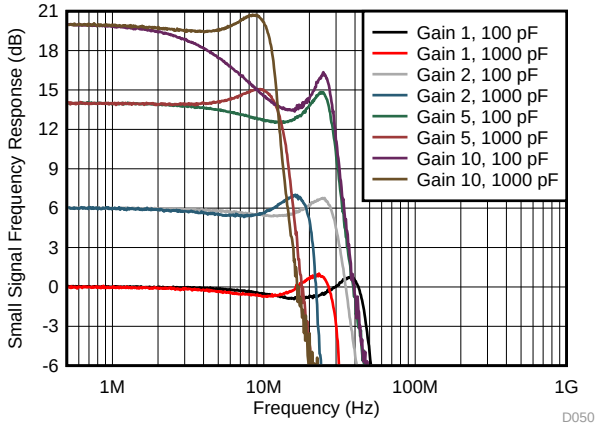


図 50. Small-Signal Frequency Response vs C_{LOAD} With Recommended R_{OUT}

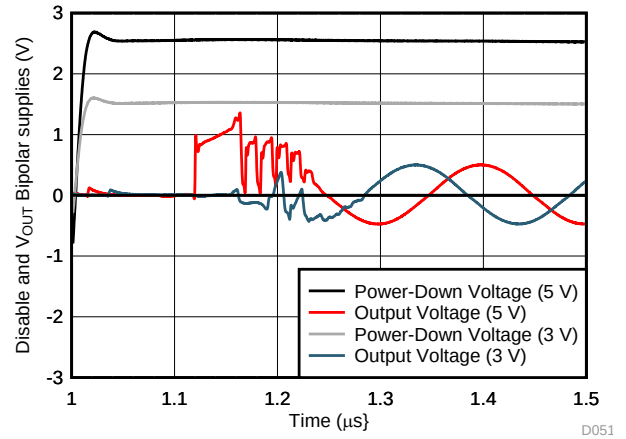


図 51. Turn-On Time to Sinusoidal Input

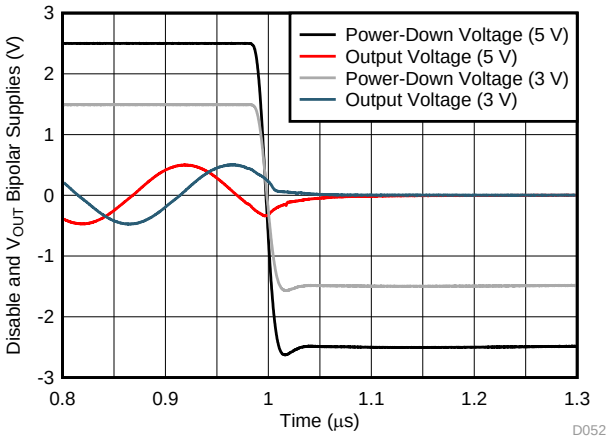


図 52. Turn-Off Time to Sinusoidal Input

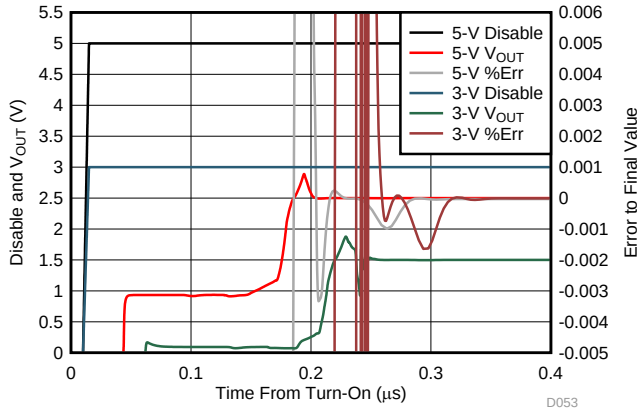


図 53. Gain of 1 Turn-On Time to Final DC Value at Midscale (Simulated)

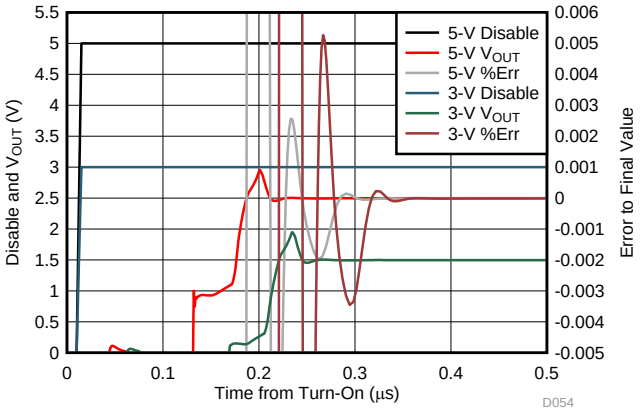


図 54. Gain of 2 Turn-On Time to Final DC Value at Midscale (Simulated)

Typical Characteristics: ±2.5-V to ±1.5-V Split Supply (continued)

with $P_D = V_{CC}$ and $T_A \approx 25°C$ (unless otherwise noted)

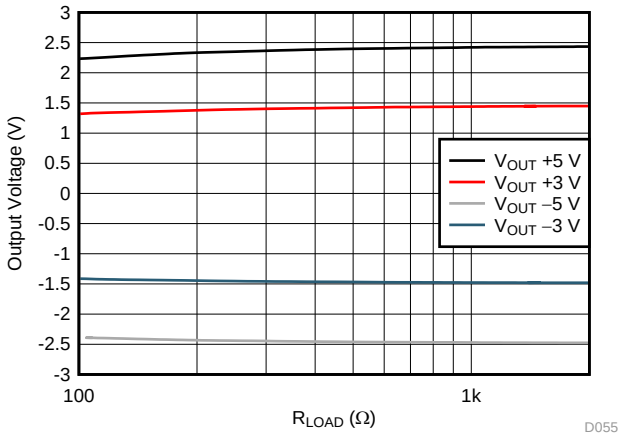


図 55. Output Voltage Swing vs Load Resistor

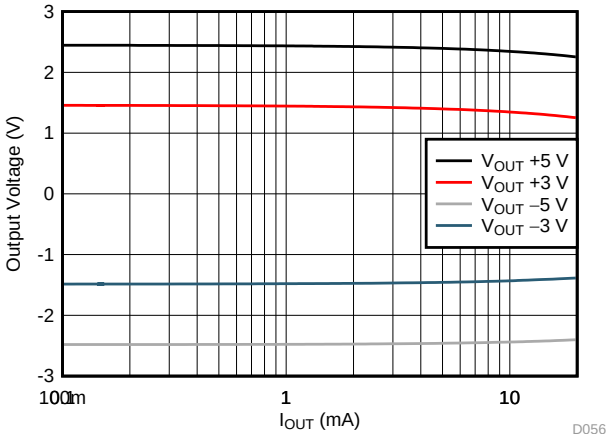
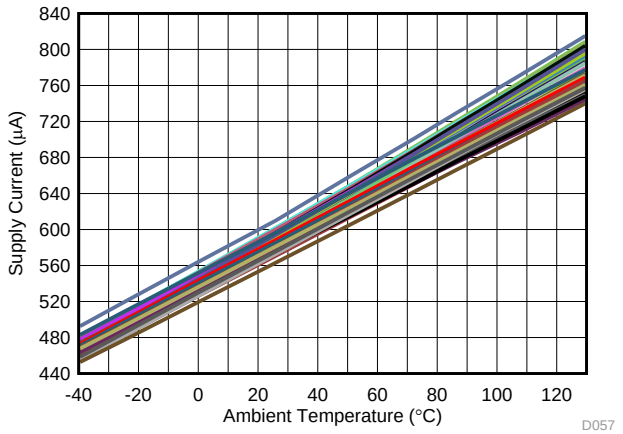


図 56. Output Saturation Voltage vs Load Current



50 units at 5-V and 3-V supply

図 57. Supply Current vs Ambient Temperature

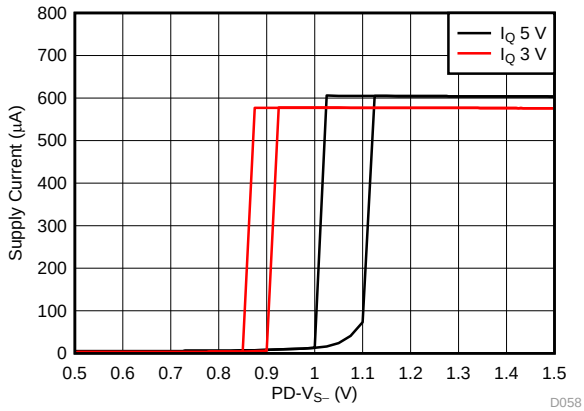
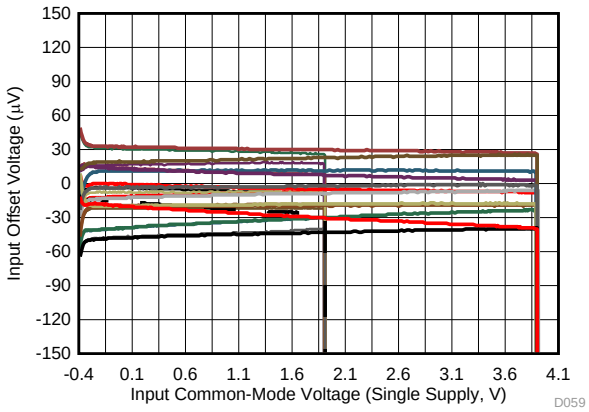
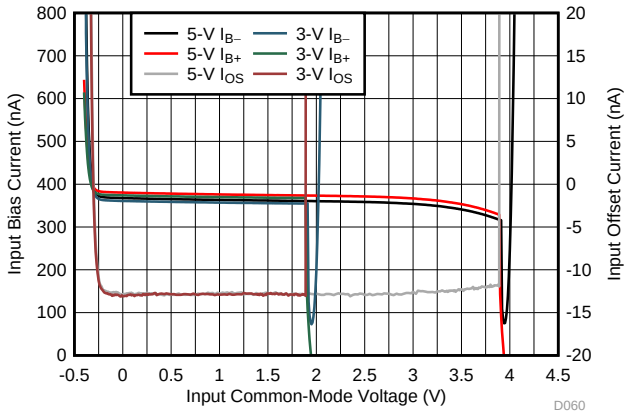


図 58. Supply Current vs Power-Down Voltage (Turn-On Higher Than Turn-Off)



12 units, 5-V and 3-V supplies

図 59. Input Offset Voltage vs Input Common-Mode Voltage

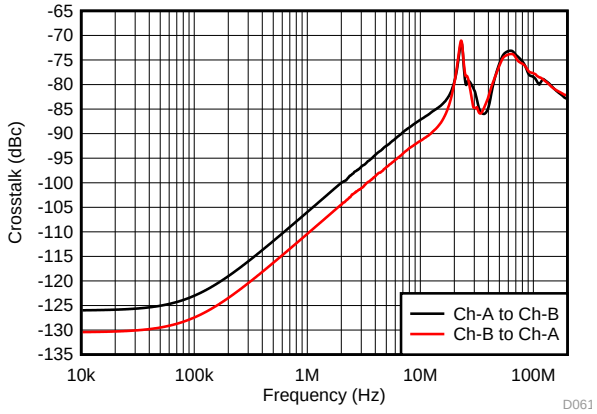


Measured single device, 5-V and 3-V supplies

図 60. Input Bias and Offset Current vs V_{ICM}

Typical Characteristics: ±2.5-V to ±1.5-V Split Supply (continued)

with $P_D = V_{CC}$ and $T_A \approx 25°C$ (unless otherwise noted)



Crosstalk for the OPA2837 only

図 61. Crosstalk vs Frequency

7 Detailed Description

7.1 Overview

The OPA837 and OPA2837 are single- and dual-channel, power efficient, unity-gain stable, voltage-feedback amplifiers (VFAs). Combining a negative rail input stage and a rail-to-rail output (RRO) stage, the OPAx837 provides a flexible solution where exceptional precision and wide bandwidth at low power are required. This 50-MHz gain bandwidth product (GBP) amplifier requires less than 0.65 mA of supply current per channel over a 2.7-V to 5.4-V total supply operating range. A shutdown feature on the OPA837 6-pin package version provides power savings where the system requires less than 10 µA when shut down. Offering a unity-gain bandwidth greater than 100 MHz, the OPAx837 provides less than –118-dBc THD at 100 kHz and a 2-V_{PP} output.

7.2 Functional Block Diagrams

The OPAx837 is a standard voltage-feedback op amp with two high-impedance inputs and a low-impedance output. 図 62 and 図 63 show the supported standard applications circuits. These application circuits are shown with a DC V_{REF} on the inputs that set the DC operating points for single-supply designs. The V_{REF} is often ground, especially for split-supply applications.

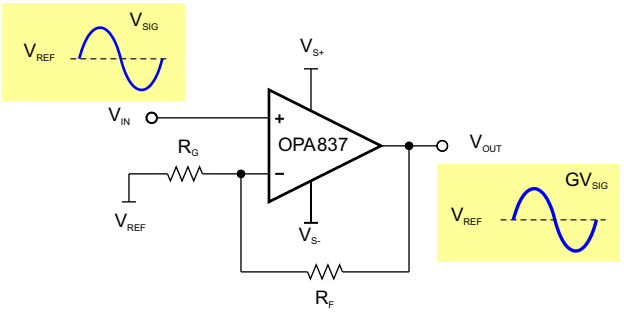


図 62. Noninverting Amplifier

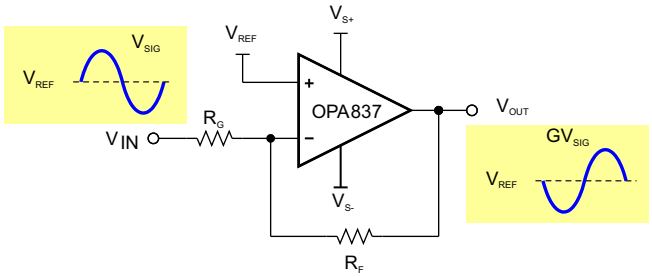


図 63. Inverting Amplifier

7.3 Feature Description

7.3.1 OPA837 Comparison

表 1 lists several members of the device family that includes the OPA837.

表 1. Device Family Comparison(1)

PART NUMBER	A_V = +1 BANDWIDTH (MHz)	5-V I_Q (mA, Max 25°C)	INPUT NOISE VOLTAGE (nV/√Hz)	2-V_{PP} THD (dBc, 100 kHz)	RAIL-TO-RAIL INPUT/OUTPUT	DUALS
OPA837	105	0.63	4.7	–118	V_S–, output	OPA2837
OPA838	—	0.99	1.9	–110	V_S–, output	—
LMV118	45	0.9	40	—	V_S–, output	—
LMH6647	55	1.6	17	–75	Input, output	LMH6646
OPA835	56	0.35	9.4	–104	V_S–, output	OPA2835
OPA625	120	2.2	2.5	–120	V_S–, output	OPA2625
OPA836	205	1.0	4.6	–118	V_S–, output	OPA2836

(1) For a complete selection of TI high speed amplifiers, visit www.ti.com.

7.3.2 Input Common-Mode Voltage Range

When the primary design goal is a linear amplifier with high CMRR, the design must remain within the input common-mode voltage range (V_{ICR}) of an op amp. These ranges are referenced off of each supply as an input headroom requirement. Ensured operation at 25°C is maintained to the negative supply voltage and to within 1.3 V of the positive supply voltage. The common-mode input range specifications in the *Electrical Characteristics* table use CMRR to set the limit. The limits are selected to ensure CMRR does not degrade more than 3 dB below the minimum CMRR value if the input voltage is within the specified range.

Assuming the op amp is in linear operation, the voltage difference between the input pins is small (ideally 0 V); and the input common-mode voltage is analyzed at either input pin with the other input pin assumed to be at the same potential. The voltage at V_{IN+} is simple to evaluate. In the noninverting configuration of 図 62, the input signal, V_{IN}, must not violate the V_{ICR}. In the inverting configuration of 図 63, the reference voltage, V_{REF}, must be within the V_{ICR}.

The input voltage limits have fixed headroom to the power rails and track the power-supply voltages. For one 5-V supply, the typical linear input voltage ranges from –0.2 V to 3.8 V and –0.2 V to 1.5 V for a 2.7-V supply. The delta headroom from each power-supply rail is the same in either case: –0.2 V and 1.2 V, respectively.

7.3.3 Output Voltage Range

The OPAx837 is a rail-to-rail output op amp. Rail-to-rail output typically means that the output voltage swings to within 100 mV of the supply rails. There are two different ways to specify this feature: one is with the output still in linear operation and another is with the output saturated. Saturated output voltages are closer to the power-supply rails than the linear outputs, but the signal is not a linear representation of the input. Saturation and linear operation limits are affected by the output current, where higher currents lead to more voltage loss in the output transistors; see 図 55.

The *Electrical Characteristics* tables list saturated output voltage specifications with a 2-kΩ load. 図 55 illustrates the saturated voltage-swing limits versus output load resistance, and 図 56 illustrates the output saturation voltage versus load current. Given a light load, the output voltage limits have nearly constant headroom to the power rails and track the power-supply voltages. For example, with a 2-kΩ load and a single 5-V supply, the linear output voltage ranges from 0.10 V to 4.9 V and ranges from 0.1 V to 2.6 V for a 2.7-V supply. The delta from each power-supply rail is the same in either case: 0.1 V.

With devices like the OPA837 and OPA2837 where the input range is lower than the output range, typically the input limits the available signal swing only in a noninverting gain of 1 V/V. Signal swing in noninverting configurations in gains greater than +1 V/V and inverting configurations in any gain are typically limited by the output voltage limits of the op amp.

7.3.4 Power-Down Operation

The OPA837 includes a power-down mode in the 6-pin SOT23-6 package. Under logic control, the amplifier can switch from normal operation to a standby current of less than 10 µA. When the $\overline{PD}$ pin is connected high, the amplifier is active. Connecting the $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a unity-gain buffer, the output stage is in a high DC-impedance state. A new feature in the OPA837 is a switch from the external inverting input pin to the internal active transistors. This switch operates with the disable pin function to open up the connection to the internal devices when powered down. Operating in unity gain provides a high-impedance voltage into both the output and inverting input pins. This feature allows direct active multiplexer operation to be implemented; see 図 87. The *TIDA-01565 Wired OR MUX and PGA Reference Design* demonstrates the use of the OPAx837 in wired-OR multiplexer and programmable gain amplifier applications. When disabled, the internal input devices on the inverting input approximately follow the noninverting input on the other side of the open switch through the back-to-back protection diodes across the inputs. When powered up, these diodes (two in each direction) act to limit overdrive currents into the active transistors.

The $\overline{PD}$ pin must be actively driven high or low and must not be left floating. If the power-down mode is not used, $\overline{PD}$ must be tied to the positive supply rail.

$\overline{PD}$ logic states are referenced relatively low to the negative supply rail, V_{S-}. When the op amp is powered from a single-supply and ground, and the disable line is driven from logic devices with similar V_{DD} voltages to the op amp, the disable operation does not require any special consideration. The OPA837 is specified to be off with $\overline{PD}$ driven to within 0.55 V of the negative supply and specified to be on when driven more than 1.5 V above the negative supply. Slight hysteresis is provided around a nominal 1-V switch point; see 図 58. When the op amp is powered from a split supply with V_{S-} below ground, a level shift logic swing below ground is required to operate the disable function.

7.3.5 Low-Power Applications and the Effects of Resistor Values on Bandwidth

The OPAx837 can use a direct short in the feedback for a gain of 1 V/V. 表 2 gives a list of recommended values over gain for an increasing noninverting gain target. This table was produced by increasing the R values until they added 50% of the total output noise power. Higher values can be used to reduce power at the cost of higher noise. Lower values can be used to reduce the total output noise at the cost of more load power in the feedback network. Stability is also impaired going to very high values because of the pole introduced into the feedback path with the inverting input capacitance (1.5-pF common-mode). In low-power applications, reducing the current in the feedback path is preferable by increasing the resistor values. Using larger value resistors has two primary side effects (other than lower power) because of the interactions with the inverting input parasitic capacitance. Using large value resistors lowers the bandwidth and lowers the phase margin. When the phase margin is lowered, peaking in the frequency response and overshoot and ringing in the pulse response results.

図 64 shows the gain = 2 V/V (6 dB) small-signal frequency response with R_F and R_G equal to 1 kΩ, 2 kΩ, 5 kΩ, 10 kΩ, and 20 kΩ. This test was done with R_L = 2 kΩ. Lower R_L values can reduce the peaking because of R_L loading effects, but higher values do not have a significant effect.

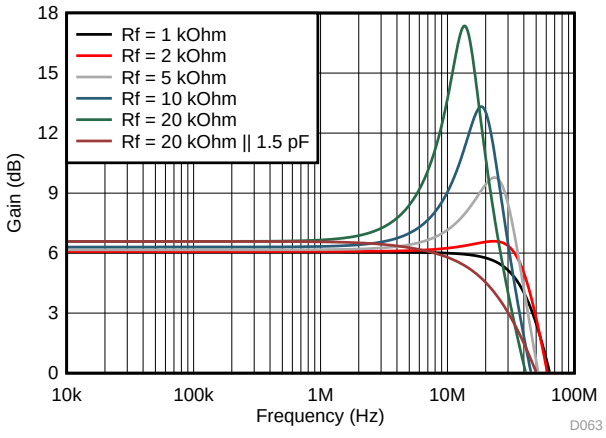


図 64. Frequency Response With Various $R_F = R_G$ Resistor Values

As expected, larger value resistors cause lower bandwidth and peaking in the response (peaking in frequency response is synonymous with overshoot and ringing in pulse response). Adding a 1.5-pF capacitor in parallel with R_F (equal to the input common-mode capacitance) helps compensate the phase margin loss and restores flat frequency response. 図 65 shows the test circuit.

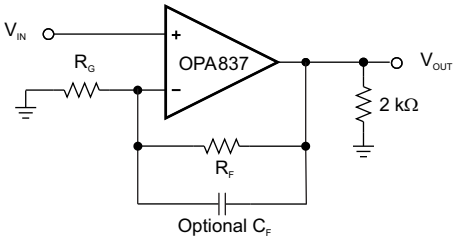


図 65. G = 2 Test Circuit for Various Gain-Setting Resistor Values

7.3.6 Driving Capacitive Loads

The OPAx837 can drive a parasitic load capacitance up through 4 pF on the output with no special considerations. When driving capacitive loads greater than 4 pF, TI recommends using a small resistor (R_O) in series with the output as close to the device as possible. Without R_O, output capacitance interacts with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that reduces the phase margin. This reduction causes peaking in the frequency response and overshoot and ringing in the pulse response. Inserting R_O isolates the phase shift from the loop-gain path and restores the phase margin; however R_O can also limit bandwidth to the capacitive load.

図 66 shows the test and 図 49 illustrates the recommended values of R_O versus capacitive loads, C_L using a 30° phase margin target for the op amp. See 図 50 for the frequency responses with various values of C_L and R_{OUT} parametric on gain.

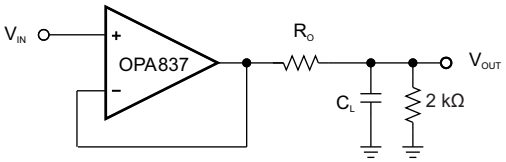


図 66. R_{OUT} versus C_L Test Circuit

7.4 Device Functional Modes

7.4.1 Split-Supply Operation (±1.35 V to ±2.7 V)

To facilitate testing with common lab equipment, the OPA837EVM (see the *OPA835DBV and OPA836DBV EVM User's Guide*) allows split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers, and other lab equipment have inputs and outputs that prefer a ground reference for DC-coupled testing.

図 67 shows a simple noninverting configuration analogous to 図 62 with a ±2.5-V supply and V_{REF} equal to ground. The input and output swing symmetrically around ground. For ease of use, split supplies are preferred in systems where signals swing around ground. In this example, an optional bias current cancellation resistor is used in series with the noninverting input. For DC-coupled applications, set this resistor to be equal to the parallel combination of R_F and R_G. This resistor increases the noise contribution at the input because of that resistor noise (see the *Output Noise Calculations* section).

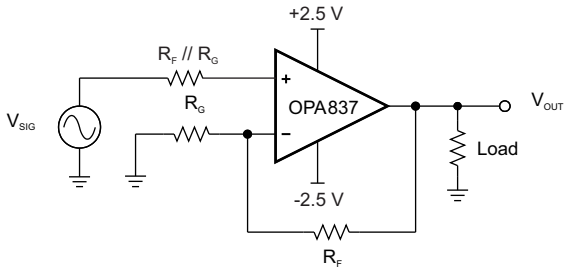


図 67. Split-Supply Operation

図 68 shows the step response for this gain of 2-V/V circuit with a ±1-V input to a ±2-V output. For a 4-V output step, the input edge rate is set to 40 ns to avoid slew limiting.

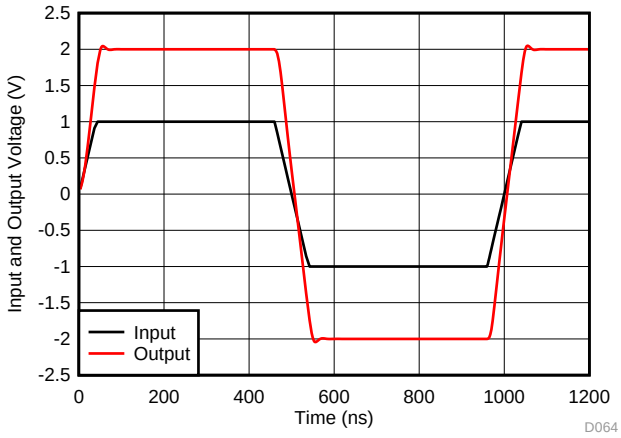


図 68. V_{IN} and V_{OUT} vs Time

Device Functional Modes (continued)

7.4.2 Single-Supply Operation (2.7 V to 5.4 V)

Most newer systems use a single power supply to improve efficiency and to simplify power-supply design. The OPAx837 can be used with single-supply power (ground for the negative supply) with no change in performance from split supply, as long as the input and output pins are biased within the linear operating region of the device. The outputs nominally swing rail-to-rail with approximately a 100-mV headroom required for linear operation. The inputs can typically swing 0.2 V below the negative rail (typically ground) and to within 1.2 V of the positive supply. For DC-coupled single-supply operation, the input swing is below the available output swing range for noninverting gains greater than 1.30 V/V. Typically, the 1.2-V input headroom required to the positive supply only limits output swing range for a unity-gain buffer.

To change the circuit from split supply to single-supply, level shift all voltages by half the difference between the power-supply rails. For example, 図 69 depicts changing from a ±2.5-V split supply to a 5-V single-supply. The load is shown as mid-supply referenced but can be grounded as well.

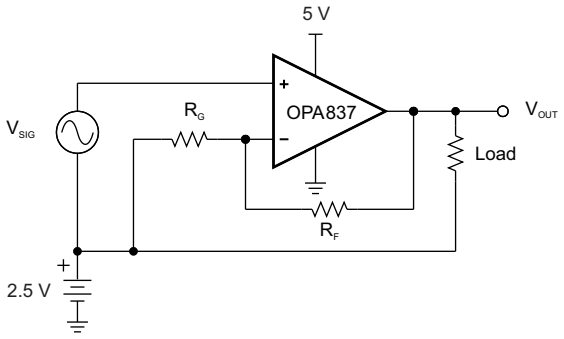


図 69. Single-Supply Concept

A practical circuit has an amplifier or other circuit providing the bias voltage for the input, and the output of this amplifier stage provides the bias for the next stage.

図 70 shows a typical noninverting amplifier circuit. With 5-V single-supply, a mid-supply reference generator is needed to bias the negative side through R_G. To cancel the voltage offset that is otherwise caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G. For example, if a gain of 2 V/V is required and R_F = 2 kΩ, select R_G = 2 kΩ to set the gain, and R_1 = 1 kΩ for bias current cancellation which reduces the output DC error to $I_{OS} \times R_F$. The value for C is dependent on the reference, and TI recommends a value of at least 0.1 µF to limit noise. The frequency response flatness is impacted by the AC impedance, including the reference and capacitor added to the R_G element.

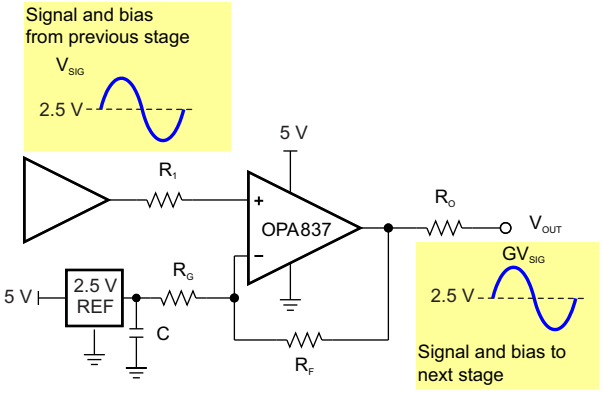


図 70. Noninverting Single-Supply Operation With Reference

Device Functional Modes (continued)

図 71 shows a similar noninverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_G' and R_G" form a resistor divider from the 5-V supply and are used to bias the negative side with the parallel sum equal to the equivalent R_G to set the gain. To cancel the voltage offset that is otherwise caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G' in parallel with R_G" (R_1= R_F || R_G' || R_G"). For example, if a gain of 2 V/V is required and R_F = 2 kΩ, selecting R_G' = R_G" = 4 kΩ gives an quivalent parallel sum of 2 kΩ, sets the gain to 2, and references the input to mid-supply (2.5 V). R_1 is set to 1 kΩ for bias current cancellation. The resistor divider costs less than the 2.5-V reference in 図 70 but increases the current from the 5-V supply. Any noise or variation on the 5-V supply now also comes into the circuit as an input through the biasing path.

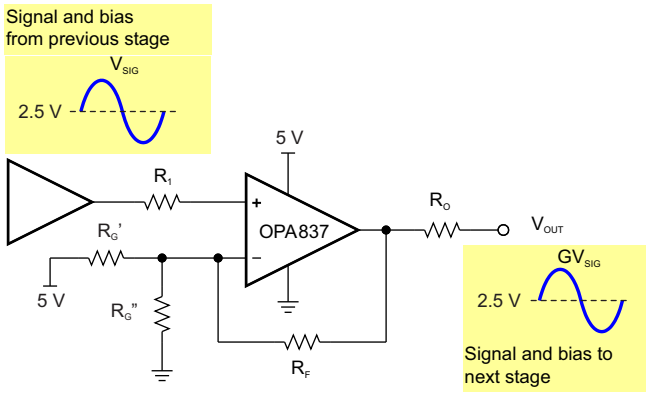


図 71. Noninverting Single-Supply Operation With Resistor Mid-Supply Biasing

図 72 shows a typical inverting amplifier circuit. With a 5-V single supply, a mid-supply reference generator is needed to bias the positive side through R_1. To cancel the voltage offset that is otherwise caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G. For example, if a gain of –2 V/V is required and R_F = 2 kΩ, select R_G = 1 kΩ to set the gain and R_1 = 667 Ω for bias current cancellation. The value for C is dependent on the reference, but TI recommends a value of at least 0.1 µF to limit noise into the op amp.

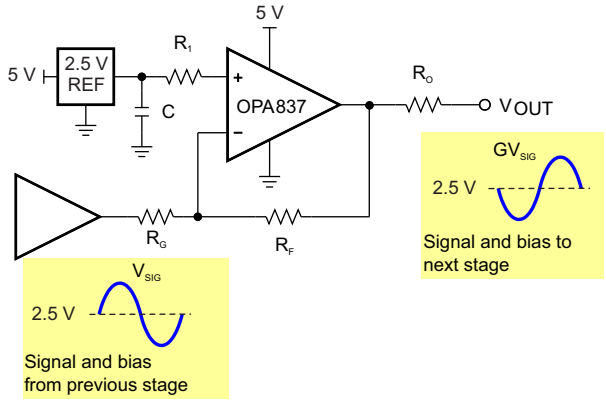


図 72. Inverting Single-Supply Operation With Reference

Device Functional Modes (continued)

図 73 shows a similar inverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_1 and R_2 form a resistor divider from the 5-V supply and are used to bias the positive side. To cancel the voltage offset that is otherwise caused by the input bias currents, set the parallel value of R_1 and R_2 equal to the parallel value of R_F and R_G. C must be added to limit coupling of noise into the positive input. For example, if gain of –2 V/V is required and R_F = 2 kΩ, select R_G = 1 kΩ to set the gain. $R_1 = R_2 = 2 \times 667\ \Omega = 1.33$ kΩ for the mid-supply voltage bias and for op-amp input-bias current cancellation. A good value for C is 0.1 µF. The resistor divider costs less than the 2.5-V reference in 図 72 but increases the current from the 5-V supply. Any noise or variation in the 5-V supply also comes into the circuit through this bias setup but be band-limited by the pole formed with R_1 || R_2 and C.

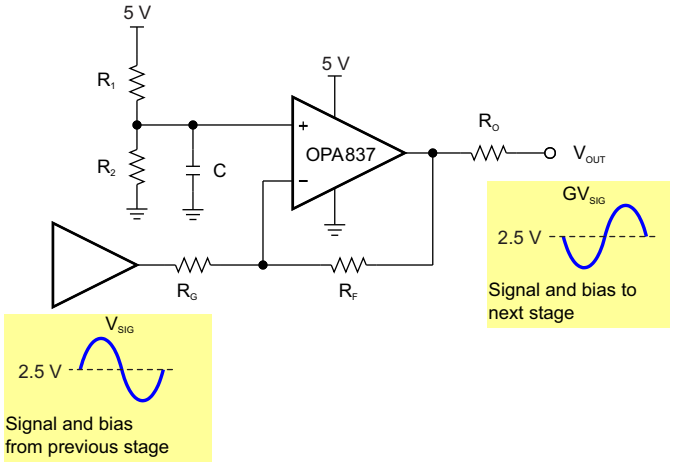


図 73. Inverting Single-Supply Operation With Resistor Midsupply Biasing

These examples are only a few of the ways to implement a single-supply design. Many other designs exist that can often be simpler if AC-coupled inputs are allowed. A good compilation of options can be found in the *Single-Supply Op Amp Design Techniques* application report.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Noninverting Amplifier

The OPAx837 can be used as a noninverting amplifier with a signal input to the noninverting input, V_{IN+}. A basic block diagram of the circuit is illustrated in 図 62. V_{REF} is often ground when split supplies are used.

Calculate the amplifier output according to 式 1 if $V_{IN} = V_{REF} + V_{SIG}$.

$$V_{OUT} = V_{SIG} \left(1 + \frac{R_F}{R_G}\right) + V_{REF} \quad (1)$$

The signal gain of the circuit is set by 式 2, and V_{REF} provides a reference around which the input and output signals swing. Output signals are in-phase with the input signals within the flat portion of the frequency response. For a high-speed, low-noise device such as the OPAx837, the values selected for R_F (and R_G for the desired gain) can strongly influence the operation of the circuit. For the characteristic curves, the noninverting circuit of 図 74 shows the test configuration set for a gain of 2 V/V. 表 2 lists the recommended resistor values over gain.

$$G = 1 + \frac{R_F}{R_G} \quad (2)$$

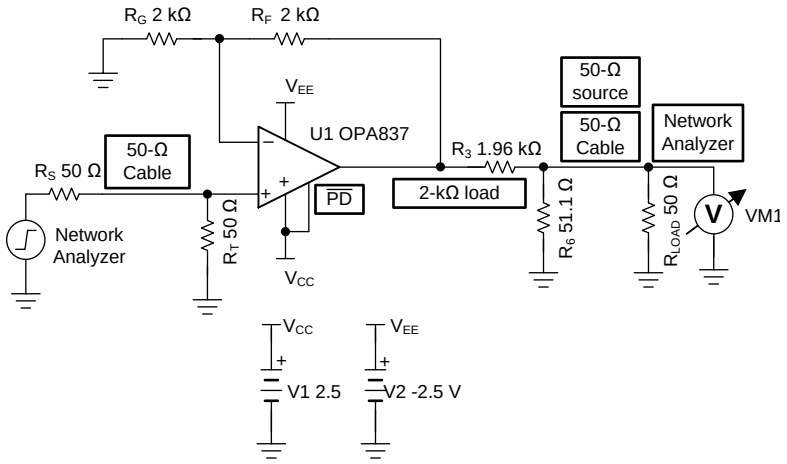


図 74. Characterization Test Circuit for Network, Spectrum Analyzer

Application Information (continued)

表 2 lists the recommended resistor values from target gains of 1 V/V to 10 V/V where standard E96 values are shown. This table controls the R_F and R_G values to set the resistor noise contribution at approximately 50% of the total output noise power. These values increase the spot noise at the output over what the op amp voltage noise produces by 41%. Lower values reduce the output noise of any design at the cost of more power in the feedback circuit. Using the TINA model and simulation tool shows the impact of different resistor value choices on response shape and noise.

表 2. Noninverting Recommended Resistor Values

TARGET GAIN (V/V)	R_F (Ω)	R_G (Ω)	ACTUAL GAIN (V/V)	GAIN (dB)
1	0	Open	1.00	0.00
1.5	1190	2370	1.50	3.53
2	2000	2000	2.00	6.02
3	2260	1130	3.00	9.54
4	2370	787	4.01	12.07
5	2490	619	5.02	14.02
6	2550	511	5.99	15.55
7	2610	432	7.04	16.95
8	2670	383	7.97	18.03
9	2670	332	9.04	19.13
10	2670	294	10.08	20.07

8.1.2 Inverting Amplifier

The OPAx837 can be used as an inverting amplifier with a signal input to the inverting input, $V_{IN–}$, through the gain-setting resistor R_G. A basic block diagram of the circuit is illustrated in 図 63.

The output of the amplifier can be calculated according to 式 3 if $V_{IN} = V_{REF} + V_{SIG}$ and the noninverting input is biased to V_{REF}.

$$V_{OUT} = V_{SIG}\left(\frac{-R_F}{R_G}\right) + V_{REF} \quad (3)$$

The signal gain of the circuit is set by 式 4 and V_{REF} provides a reference point around which the input and output signals swing. For bipolar-supply operation, V_{REF} is often ground. The output signal is 180° out-of-phase with the input signal in the pass band of the application. 図 75 shows the 50-Ω input matched configuration used for the inverting characterization plots set up for a gain of –1 V/V. In this case, an added termination resistor, R_T, is placed in parallel with the input R_G resistor to provide an impedance match to 50-Ω test equipment. The output network appears as a 2-kΩ load but with a 50-Ω source to the network analyzer. This output interface network does add a 37.9-dB insertion loss that is normalized out in the characterization curves. 表 3 lists the suggested values for R_F, R_G, and R_T for inverting gains from –0.5 V/V to –10 V/V. If a 50-Ω input match is not required, eliminate the R_T element.

$$G = \frac{-R_F}{R_G} \tag{4}$$

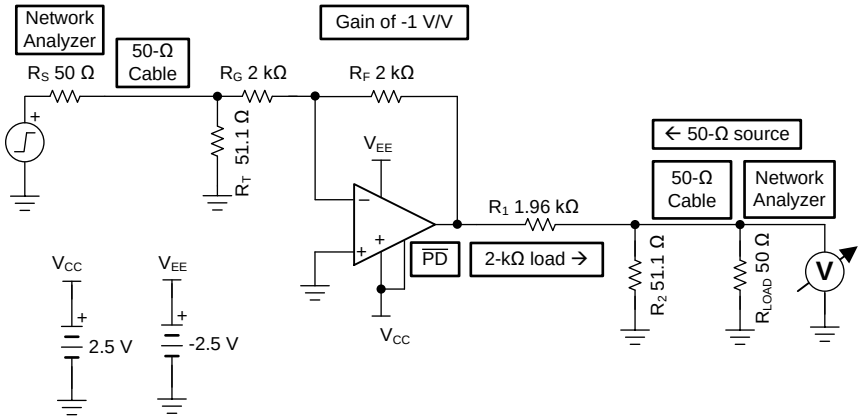


図 75. Inverting Characterization Circuit for Network Analyzer

表 3. Inverting Recommended Resistor Values

INVERTING GAIN (V/V)	R_F (Ω)	R_G (Ω)	STANDARD R_T (Ω)	INPUT Z_I (Ω)	ACTUAL (V/V)	GAIN (dB)
–0.5	1190	2370	51.1	50.02	–0.50	–5.98
–1	2000	2000	51.1	49.83	–1.00	0.00
–2	2260	1130	52.3	49.99	–2.00	6.02
–3	2370	787	53.6	50.18	–3.01	9.58
–4	2490	619	54.9	50.43	–4.02	12.09
–5	2550	511	54.9	49.57	–4.99	13.96
–6	2610	432	56.2	49.73	–6.04	15.62
–7	2670	383	57.6	50.07	–6.97	16.87
–8	2670	332	59	50.10	–8.04	18.11
–9	2670	294	60.4	50.11	–9.08	19.16
–10	2670	267	61.9	50.25	–10.00	20.00

8.1.3 Output DC Error Calculations

The OPAx837 can provide excellent DC signal accuracy because of its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of this low input offset voltage, pay careful attention to input bias current cancellation. The low-noise input stage for the OPAx837 has a relatively high input bias current (0.34 µA typical out the pins) but with a close match between the two input currents. The OPAx837 is a negative rail input device using PNP input devices where the base current flows out of the device pins. A large resistor to ground on the V+ input shifts the pin voltage positively because of the input bias current. The mismatch between the two input bias currents is very low, typically only ±10 nA of input offset current. Match the DC source impedances out of the two inputs to reduce the total output offset voltage. 図 67 illustrates an example of resistor matching for bias current cancellation. Analyzing the simple circuit of 図 67 (using a gain of 2-V/V target with $R_F = R_G = 2$ kΩ) illustrates that the noise gain for the input offset voltage drift is 1 + 2 kΩ / 2 kΩ = 2 V/V. This value results in an output drift term of ±1.6 µV/°C × 2 = ±3.2 µV/°C (DCK package). Because the two impedances out of the inputs are matched, the residual error from the maximum ±250 pA/°C offset current drift is this maximum I_{OS} drift times the 2-kΩ feedback resistor value, or ±50 µV/°C. The total output DC error drift band is ±53.2 µV/°C. If the output DC drift is more important than reduced feedback currents, lower the resistor values to reduce the dominant drift term resulting from the I_{OS} term.

8.1.4 Output Noise Calculations

The unity-gain stable, voltage-feedback OPAx837 op amp offers among the lowest input voltage and current noise terms for any device with a supply current less than 0.7 mA. 図 76 shows the op amp noise analysis model that includes all noise terms. In this model, all noise terms are shown as noise voltage or current density terms in nV/√Hz or pA/√Hz.

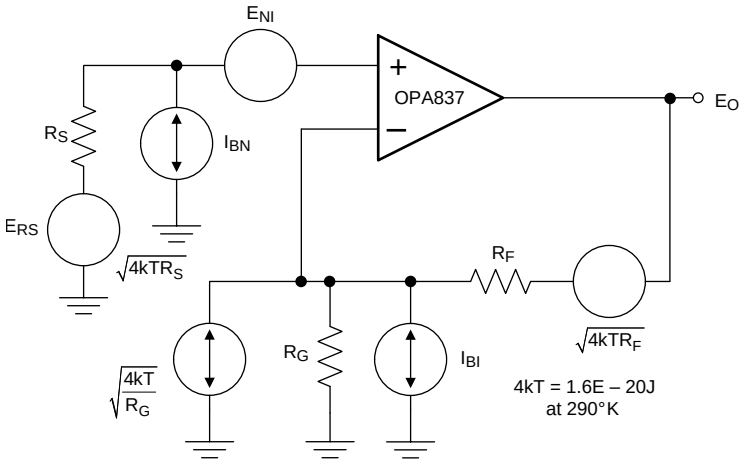


図 76. Op Amp Noise Analysis Model

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to return to a spot noise voltage. The last term includes the noise for both the R_G and R_F resistors. 式 5 shows the general form for this output noise voltage using the terms presented in 図 76.

$$E_O = \sqrt{\left[E_{NI}^2 + \left(I_{BN}R_S\right) + 4kTR_S\right]NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \tag{5}$$

Dividing this expression by the noise gain (NG = 1 + R_F / R_G), as shown in 式 6, gives the equivalent input referred spot noise voltage at the noninverting input.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \tag{6}$$

Using the resistor values listed in 表 2 with R_S = 0 Ω results in a constant input-referred voltage noise of < 7 nV/√Hz. Reducing the resistor values can reduce this noise value towards the 4.7 nV/√Hz intrinsic to the OPA837. As shown in 式 5, adding the R_S for bias current cancellation in noninverting mode adds the noise from the R_S to the total output noise. In inverting mode, bypass the R_S bias current cancellation resistor with a capacitor for the best noise performance. For more details on op amp noise analysis, see the *Noise Analysis for High-Speed Op Amps* application report.

8.1.5 Instrumentation Amplifier

図 77 is an instrumentation amplifier that combines the high input impedance of the differential-to-differential amplifier circuit and the common-mode rejection of the differential-to-single-ended amplifier circuit. This circuit is often used in applications where high input impedance is required (such as taps from a differential line) or in cases where the signal source is a high impedance.

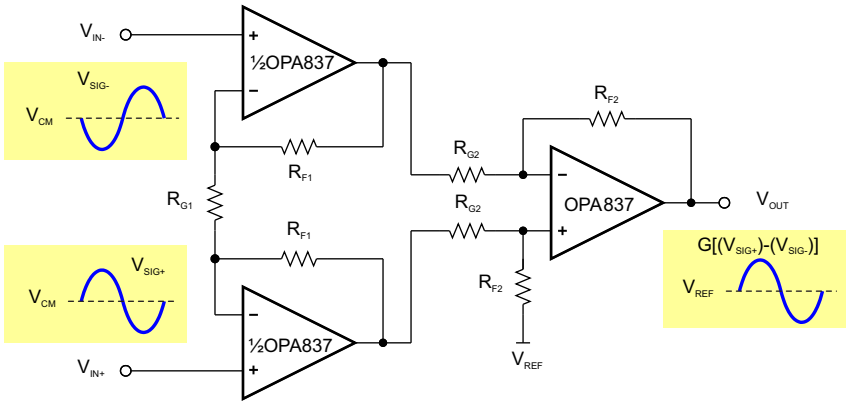


図 77. Instrumentation Amplifier (INA)

The output of the amplifier can be calculated according to 式 7 if $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right) + V_{REF} \quad (7)$$

式 8 shows the signal gain of the circuit. The input V_{CM} is rejected, and V_{REF} provides a reference voltage or level shift around which the output signal swings. The single-ended output signal is in-phase to the lower input signal polarity.

$$G = \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right) \quad (8)$$

Integrated INA solutions are available, but the OPAx837 device provides a high-frequency solution at relatively low power (< 1.8 mA for the three op-amp solution). For best CMRR performance, resistors must be matched. A good rule of thumb is CMRR ≈ the resistor tolerance; so a 0.1% tolerance provides approximately 60-dB CMRR. For higher gain INA implementations with higher bandwidths, apply the OPA838 to the circuit of 図 77.

8.1.6 Attenuators

The noninverting circuit of 図 62 has a minimum gain of 1. To implement attenuation, a resistor divider can be placed in series with the positive input, and the amplifier set for a gain of 1 V/V by shorting V_{OUT} to V_{IN-} and removing R_G. Because the op amp input is high impedance, the resistor divider sets the attenuation.

The inverting circuit of 図 63 is used as an attenuator by making R_G larger than R_F. The attenuation is the resistor ratio. For example, a 10:1 attenuator can be implemented with R_F = 2 kΩ and R_G = 20 kΩ.

8.1.7 Differential to Single-Ended Amplifier

図 78 shows a differential amplifier that converts differential signals to single-ended in a single stage and provides gain (or attenuation) and level shifting. This circuit can be used in applications such as a line receiver for converting a differential signal from a Cat5 cable to a single-ended output signal.

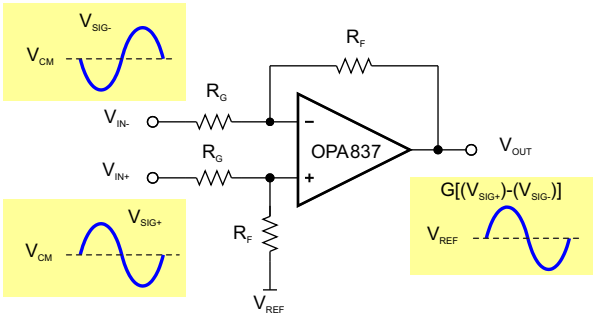


図 78. Differential to Single-Ended Amplifier

The output of the amplifier can be calculated according to 式 9 if $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN–} = V_{CM} + V_{SIG–}$.

$$V_{OUT} = \left(V_{IN+} - V_{IN-}\right) \times \left(\frac{R_F}{R_G}\right) + V_{REF} \tag{9}$$

The signal gain of the circuit is shown in 式 10, V_{CM} is rejected, and V_{REF} provides a level shift or reference voltage around which the output signal swings. The single-ended output signal is in-phase with the noninverting input signal. V_{REF} is often ground when split supplies are used on the op amp.

$$G = \frac{R_F}{R_G} \tag{10}$$

Line termination can be accomplished by adding a shunt resistor across the V_{IN+} and $V_{IN–}$ inputs. The differential impedance is the shunt resistance in parallel with the input impedance of the amplifier circuit, which is usually much higher. For low gain and low line impedance, the resistor value to add is approximately the impedance of the line. For example, if a 100-Ω Cat5 cable is used with a gain of 1 V/V amplifier and $R_F = R_G = 2$ kΩ, adding a 100-Ω shunt across the input gives a differential impedance of 99 Ω, which is an adequate match for most applications.

For best CMRR performance, resistors must be matched. Assuming CMRR ≈ the resistor tolerance, a 0.1% tolerance provides approximately 60-dB CMRR.

8.1.8 Differential-to-Differential Amplifier

図 79 shows a differential amplifier that is used to amplify differential signals to a differential output. This circuit has high input impedance and is used in differential line driver applications where the signal source is a high-impedance driver (for example, a differential DAC) that must drive a line.

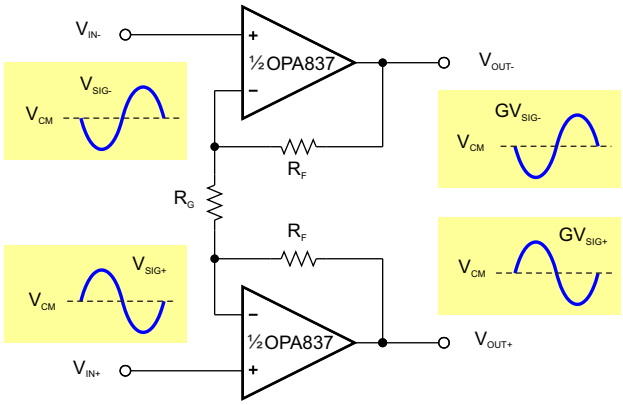


図 79. Differential-to-Differential Amplifier

The output of the amplifier can be calculated according to 式 11 if $V_{IN\pm}$ is set to $V_{CM} + V_{SIG\pm}$.

$$V_{OUT\pm} = V_{IN\pm} \times \left(1 + \frac{2R_F}{R_G}\right) + V_{CM} \tag{11}$$

The signal gain of the circuit is shown in 式 12, and V_{CM} passes with unity gain. The amplifier combines two noninverting amplifiers into one differential amplifier that shares the R_G resistor, which makes R_G effectively half its value when calculating the gain. The output signals are in-phase with the input signals.

$$G = 1 + \frac{2R_F}{R_G} \tag{12}$$

8.1.9 Pulse Application With Single-Supply Circuit

For pulsed applications where the signal is at ground and pulses to a positive or negative voltage, the circuit bias-voltage considerations differ from those in an application with a signal that swings symmetrically around a reference point. 図 80 shows a circuit where the signal is at ground (0 V) and pulses to a positive value. The waveforms are shown slightly above ground because the output stage requires approximately 100 mV headroom to the supplies. To operate with the I/O swing truly to ground on a single-supply setup, consider using the fixed –0.23-V output LM7705.

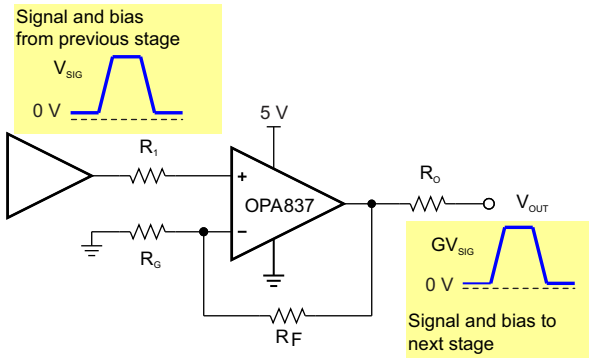


図 80. Noninverting Single-Supply Circuit With Pulse

As shown in 図 81, an inverting amplifier is more appropriate if the input signal pulses negative from ground. A key consideration in noninverting and inverting cases is that the input and output voltages are kept within the limits of the amplifier. Because the V_{ICR} of the OPA837 includes the negative supply rail, the OPA837 op amp is well-suited for this application.

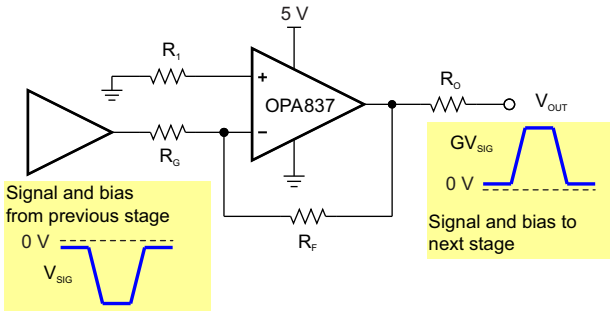


図 81. Inverting Single-Supply Circuit With Pulse

8.1.10 ADC Driver Performance

The OPAx837 provides excellent performance when driving high-performance delta-sigma (ΔΣ) or successive-approximation-register (SAR) ADCs in low-power audio and industrial applications.

図 82 repeats the front page diagram. Many designs prefer to work with a true 0-V input range to 0-V output at the ADC. The 100-mV output headroom requirement for the OPAx837 then requires a small negative supply to hold the output linearity to ground. This supply is provided in this example using the low-cost LM7705 fixed negative, –0.23-V output regulator. On a 5-V supply, the input headroom requires at least a 1.2-V headroom to that supply. As shown in 図 82, this requirement limits the maximum input to 3.8 V. The SAR operates with a precision 4.096-V reference provided by the REF5040, where the gain of 1.05 V/V takes the 3.8-V maximum input to a 4.0-V maximum output. The RC values have been set to limit the overshoot at the OPAx837 output pin to reduce clipping on fast (50 ns) transitions.

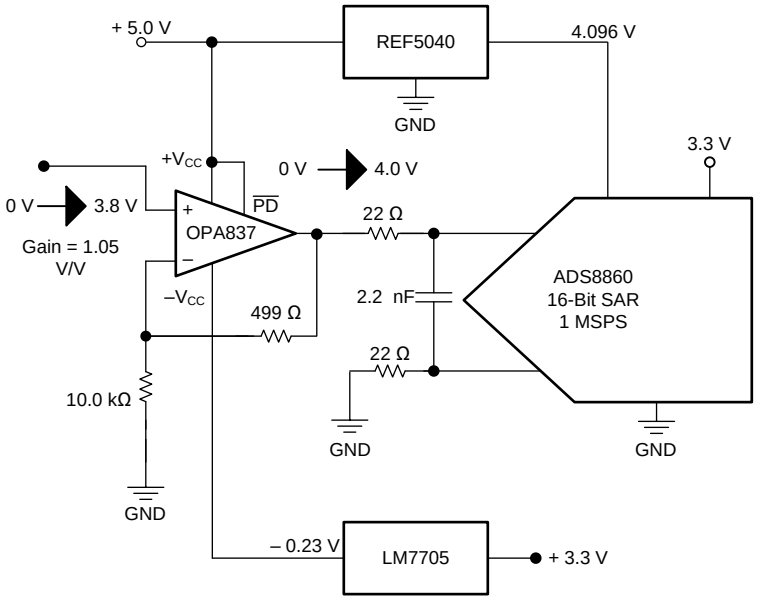


図 82. OPA837 and ADS8860 Example Circuit

8.2 Typical Applications

8.2.1 Active Filters

The OPAx837 is a good choice for active filters. 図 83 and 図 84 show MFB and Sallen-Key circuits designed implementing second-order, low-pass Butterworth filter circuits. 図 85 illustrates the frequency response.

The main difference is that the MFB active filter provides an inverting amplifier in the pass band and the Sallen-Key active filter is noninverting. The primary advantage for each active filter is that the Sallen-Key filter in unity gain has no resistor gain error term or feedback resistor noise contribution. The MFB active filter has better attenuation properties beyond the bandwidth of the op amp. The example circuits are assuming a split-supply operation but single-supply operation is possible with midscale biasing.

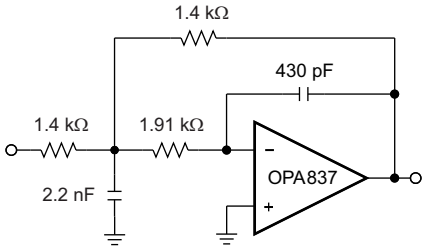


図 83. MFB Active Filter, 100-kHz, Second-Order, Low-Pass Butterworth Filter Circuit

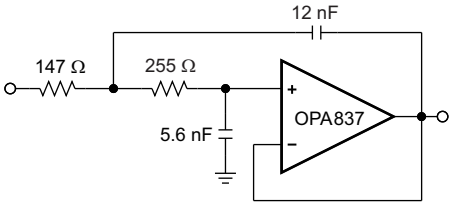


図 84. Sallen-Key Active Filter, 100-kHz, Second-Order, Low-Pass Butterworth Filter Circuit

8.2.1.1 Design Requirements

For both designs, target the following filter shape characteristic:

- Gain of 1 V/V
- 100-kHz Butterworth response
- Q = 0.707 gives a flat Butterworth design

Scale the resistors down to reduce their noise contribution. In the MFB design, the input resistor is the in-band load to the prior stage. Use values slightly below the gain of –1 V/V in 表 3. The Sallen-Key filter shows a high impedance input in-band, so scale those resistors down further to improve noise.

The output DC error and drift can be improved by adding bias current cancellation resistors. For the MFB filter that is a resistor (and a noise filter capacitor) on the noninverting input to ground equal to the resistor inside the loop times the noise gain. For the Sallen-Key design, add a feedback resistor equal to the sum of the two input resistors.

8.2.1.2 Detailed Design Procedure

The filter designs shown in this section used an improved design flow that reduces the resistor noise and noise gain peaking. For the MFB filter, the design was based on the information in the *Design Methodology for MFB Filters in ADC Interface Applications* application note.

For the Sallen-Key design, the solution is based on the information in the *Component Pre-Distortion for Sallen Key Filters* application note.

Typical Applications (continued)

8.2.1.3 Application Curves

図 85 shows the comparative response curves for each of the filter design examples. Both filters hit the desired response shape exactly. However, notice the loss of stop-band rejection in the Sallen-Key design. This loss results from the op amp output impedance increasing at higher frequencies and allowing the signal to feed through the feedback capacitor to the output.

図 86 shows a comparison of the output spot noise for the two designs. The Sallen-Key is much lower because of the lower resistor values used. Also, the MFB shows a noise gain of 2 V/V versus the Sallen-Key gain of 1 V/V. This difference immediately increases the MFB output noise by at least twice the input voltage noise from the op amp. The higher resistor values also increase the total output noise for the MFB.

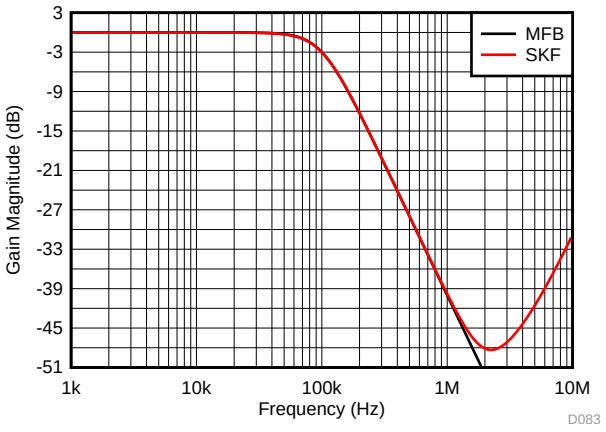


図 85. MFB and Sallen-Key Active Filters, Second-Order, Low-Pass Butterworth Filter Response

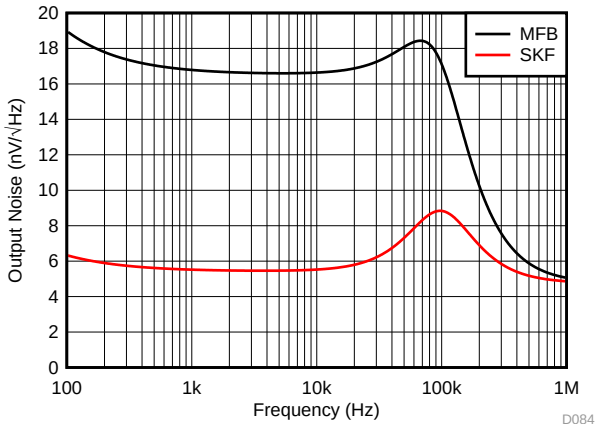


図 86. Output Spot Noise Comparison

8.2.2 Implementing a 2:1 Active Multiplexer

The OPA837 includes a unique feature that enables a much improved wired-or mux operation. When disabled, an internal switch opens from the inverting input to the active transistors isolating those nonlinear loads from the signal being driven back into the inverting input through the active channel. 図 87 illustrates a simple example of this multiplexer. In this figure, one of two signals are selected to be passed on to a shared output. The logic control turns both amplifiers off (logic low) prior to turning one of them on. This control eliminates both outputs being active at the same time. If both amplifiers must be on, as in the simple switch illustrated in 図 87, adding 100-Ω isolating resistors inside the loop at the outputs limits the current flow when both amplifiers are turned on. This solution offers a very high input impedance to both inputs, very low buffered output drive, and nearly perfect channel-to-channel isolation. The example of 図 87 also includes a –0.23-V supply generator to allow true swing to ground on the output pins. This negative supply generator is optional if the outputs are more than 0.1 V above ground or intended to be AC-coupled. Testing with a single channel active and an off channel attached to the output showed no degradation in harmonic distortion; see 図 17 and 図 35. This approach can be expanded to more than two channels or to operate with gain in the channels. Adding more than two select channels in parallel should add 100-Ω feedback resistors to isolate the inverting input capacitance from the active output channel.

Typical Applications (continued)

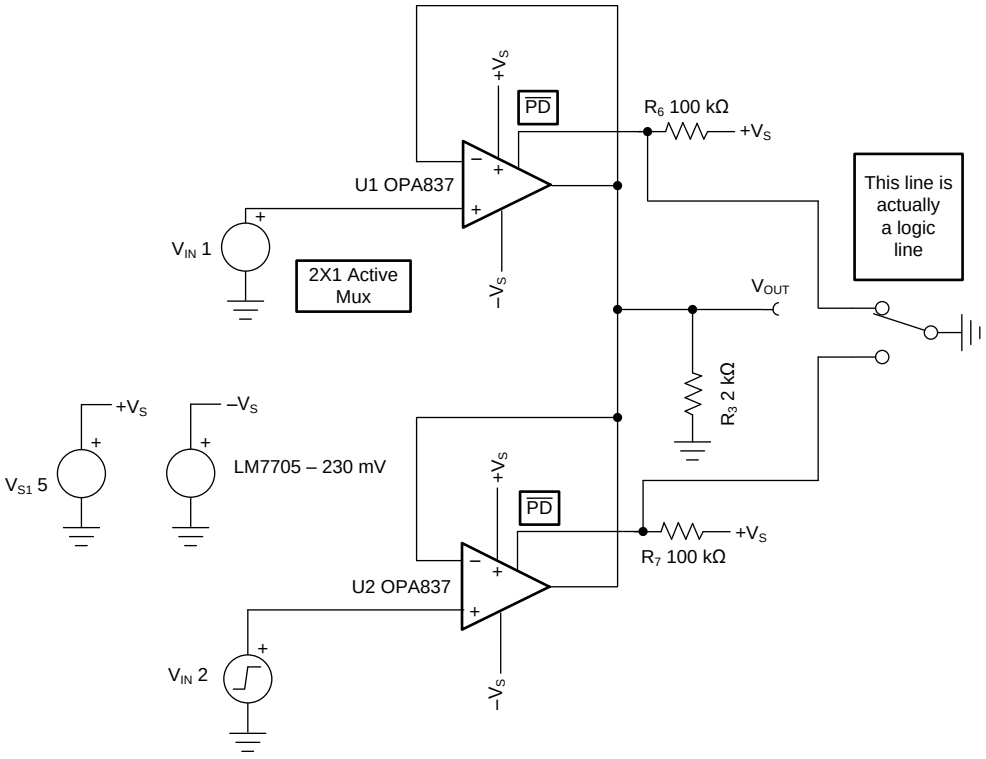


図 87. 2:1 Active Multiplexer

8.2.2.1 Design Requirements

To implement a 2:1 active mux, connect the outputs of two OPA837 devices together with separate input signals. If termination is required for the input signals, add this termination as a resistor to ground on the noninverting inputs. The inputs accept an input range from 0 V to 3.8 V by using a negative 0.23-V supply generator, such as the LM7705.

8.2.2.2 Detailed Design Procedure

Aside from simply connecting the two outputs together as shown in 図 87, there are several other considerations as well:

- If the source impedance is not 0 Ω, consider adding a resistor in the feedback networks equal to that source impedance to reduce the output DC error resulting from bias currents
- If the logic control can place both channels on at the same time, place 100-Ω resistors inside the feedback loop to limit supply currents when both outputs are active
- If a matched gain is desired for the two inputs, configure the op amps for that gain instead of gain of 1 V/V
- If the load is capacitive, add the required R_{OUT} before the summing point on each op amp output

Typical Applications (continued)

8.2.3 1-Bit PGA Operation

Using the internal inverting input switch that operates along with the power disable function can also allow a simple gain selection on a single input signal. 図 88 shows an example gain select of either 1 V/V or 2 V/V from a single input to a single output. The logic disables both channels before turning one of them on to avoid high currents in both outputs to be active at the same time. If this approach is not possible, as in the simple switch shown in 図 88, insert 100-Ω resistors inside the loop of each op amp output. A bipolar supply is shown in 図 88, but any of the single-supply options are also possible. Any combination of gains can be implemented, but wide gain ranges show a larger change in signal bandwidth. This approach can be expanded to more than two gain settings. Testing with the circuit of 図 88 showed no change in harmonic distortion; see 図 18 and 図 36.

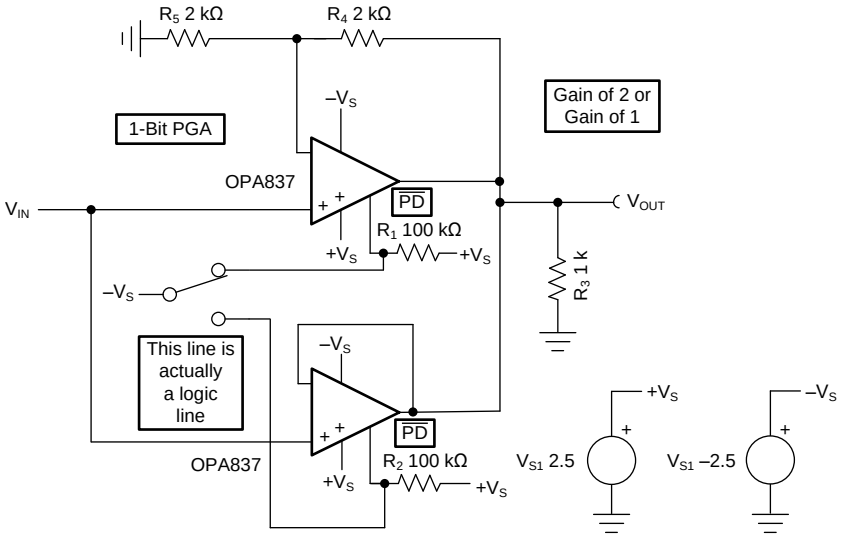


図 88. 1-Bit PGA

8.2.3.1 Design Requirements

Configure two OPA837 device outputs in different gains when driving the noninverting input with the same input signal. Select one the two channels using the disable control. Set one channel to a gain of 1 V/V and the second channel to a gain of 2 V/V using the recommended 2-kΩ values from 表 2.

8.2.3.2 Detailed Design Procedure

The simple design of 図 88 has several options and details to consider, which include:

- For split-supply operation, the disable control line must operate to within 0.55 V of the negative supply to disable a channel. A logic level shift is required.
- Any combination of gains can be implemented. However, the signal bandwidths may vary widely through the gain bandwidth product effect between the two channels if the gains are widely separated. If a more constant bandwidth between gains is desired, consider adding a fixed RC filter after the combined outputs at a lower cutoff frequency than the slowest gain setting.

The *TIDA-01565 Wired OR MUX and PGA Reference Design* demonstrates the use of the OPAx837 in wired-OR multiplexer and programmable gain amplifier applications.

9 Power Supply Recommendations

The OPAx837 is intended to work in a nominal supply range of 3.0 V to 5 V. Supply-voltage tolerances are supported with the specified operating range of 2.7 V (–10% on a 3-V supply) and 5.4 V (+8% on a 5-V supply). Good power-supply bypassing is required. Minimize the distance (< 0.1 inch) from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. A larger capacitor (2.2 µF is typical) is used along with a high-frequency, 0.1-µF supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) reduces second harmonic distortion.

The OPA837 has a positive supply current temperature coefficient; see 図 57. This coefficient helps improve the input offset voltage drift. Supply current requirements in the system design must account for this effect using the maximum intended ambient and 図 57 to size the supply required. The very low power dissipation for the OPA837 typically does not require any special thermal design considerations. For the extreme case of 125°C operating ambient, use the approximate maximum 200°C/W for the two packages, and a maximum internal power of 5.4-V supply × 0.8-mA 125°C supply current from 図 57 gives a maximum internal power of 4.3 mW. This power only gives a 0.86°C rise from ambient to junction temperature, which is well below the maximum 150°C junction temperature. Load power adds to this value, but also increases the junction temperature only slightly over ambient temperature.

10 Layout

10.1 Layout Guidelines

The *OPA837EVM* can be used as a reference when designing the circuit board. TI recommends following the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. General guidelines are listed below:

1. Signal routing must be direct and as short as possible into and out of the op amp.
2. The feedback path must be short and direct avoiding vias if possible, especially with G = 1 V/V.
3. Ground or power planes must be removed from directly under the negative input and output pins of the amplifier.
4. TI recommends placing a series output resistor as close to the output pin as possible. See 図 49 for recommended values for the expected capacitive load. These values are derived targeting a 30° phase margin to the output of the op amp.
5. A 2.2-µF power-supply decoupling capacitor must be placed within two inches of the device and can be shared with other op amps. For split supply, a capacitor is required for both supplies.
6. A 0.1-µF power-supply decoupling capacitor must be placed as close to the supply pins as possible, preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.
7. The $\overline{\text{PD}}$ pin uses low logic swing levels. If the pin is not used, $\overline{\text{PD}}$ must be tied to the positive supply to enable the amplifier. If the pin is used, $\overline{\text{PD}}$ must be actively driven. A bypass capacitor is not necessary, but can be used for robustness in noisy environments.

10.2 Layout Example

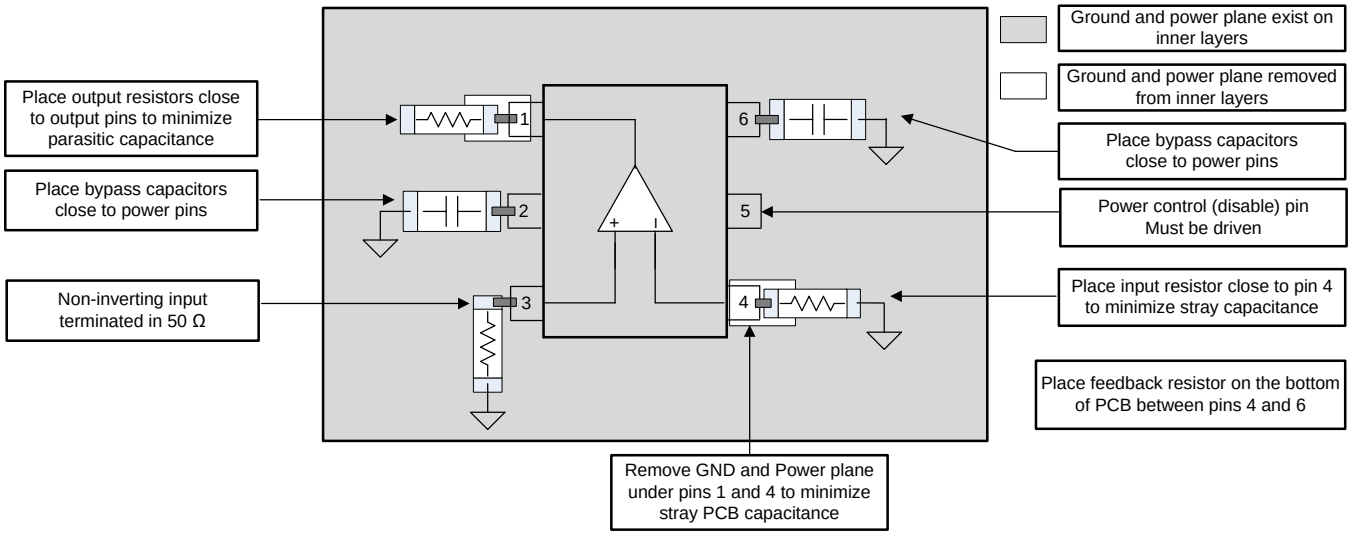


図 89. EVM Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『ADS8860 16ビット、1MSPS、シリアル・インターフェイス、microPower、小型、シングルエンド入力、SARアナログ・デジタル・コンバータ』データシート
- テキサス・インスツルメンツ、『LM7705 低ノイズ、負のバイアス・ジェネレータ』データシート
- テキサス・インスツルメンツ、『OPA838 1mA、300MHzゲイン帯域幅、電圧帰還型オペアンプ』データシート
- テキサス・インスツルメンツ、『REF50xx 低ノイズ、超低ドリフト、高精度基準電圧』データシート
- テキサス・インスツルメンツ、『OPA837DBV、OPA836DBV EVM』ユーザー・ガイド
- テキサス・インスツルメンツ、『単一電源オペアンプの設計テクニック』アプリケーション・レポート
- テキサス・インスツルメンツ、『高速オペアンプのノイズ解析』アプリケーション・レポート
- テキサス・インスツルメンツ、『ADCインターフェイス・アプリケーションにおけるMFBフィルタ用の設計方法論』アプリケーション・ノート
- テキサス・インスツルメンツ、『サレン・キー・フィルタのコンポーネント・プリディストーション』アプリケーション・ノート
- テキサス・インスツルメンツ、『TIDA-01565 有線OR MUXおよびPGAのリファレンス・デザイン』デザイン・ガイド
- テキサス・インスツルメンツ、TINAモデルおよびシミュレーション・ツール

11.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA837	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2837	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.5 商標

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2837IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	2837
OPA2837IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2837
OPA2837IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	2837
OPA2837IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2837
OPA2837IRUNR	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2837
OPA2837IRUNR.B	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2837
OPA2837IRUNRG4.B	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2837
OPA2837IRUNT	Active	Production	QFN (RUN) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2837
OPA2837IRUNT.B	Active	Production	QFN (RUN) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2837
OPA837IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19FF
OPA837IDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19FF
OPA837IDBVR2	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19FF
OPA837IDBVR2.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19FF
OPA837IDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19FF
OPA837IDBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19FF
OPA837IDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16K
OPA837IDCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16K
OPA837IDCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16K
OPA837IDCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16K
OPA837IDCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16K

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

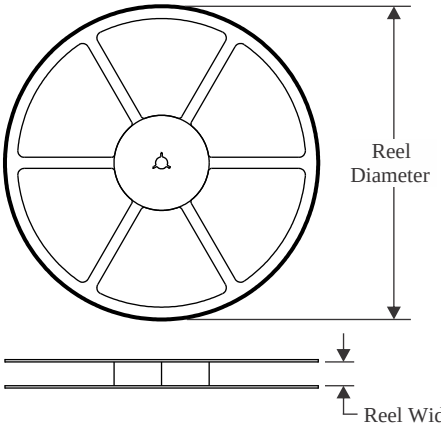
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

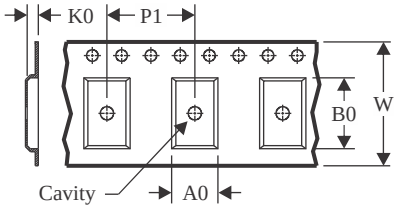
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

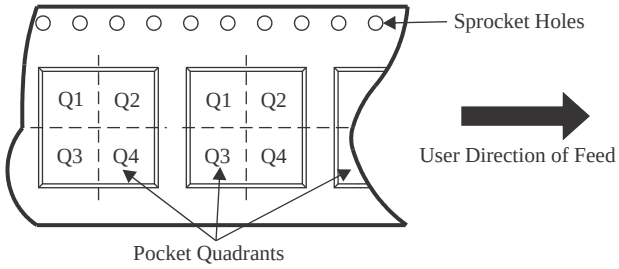


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

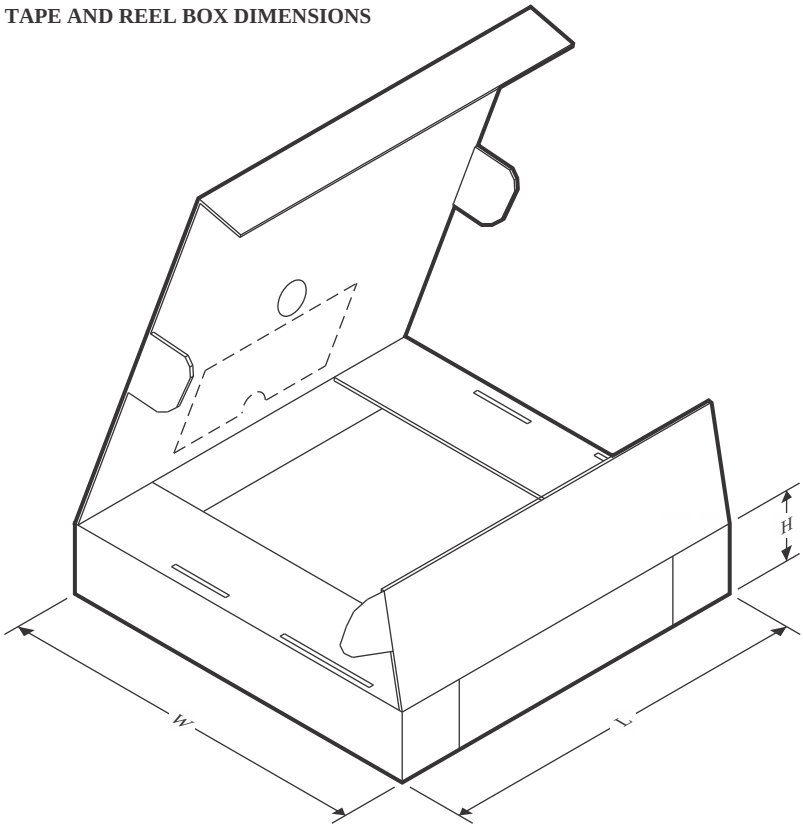
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2837IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2837IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2837IRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2837IRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA837IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA837IDBVR2	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q2
OPA837IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA837IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA837IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

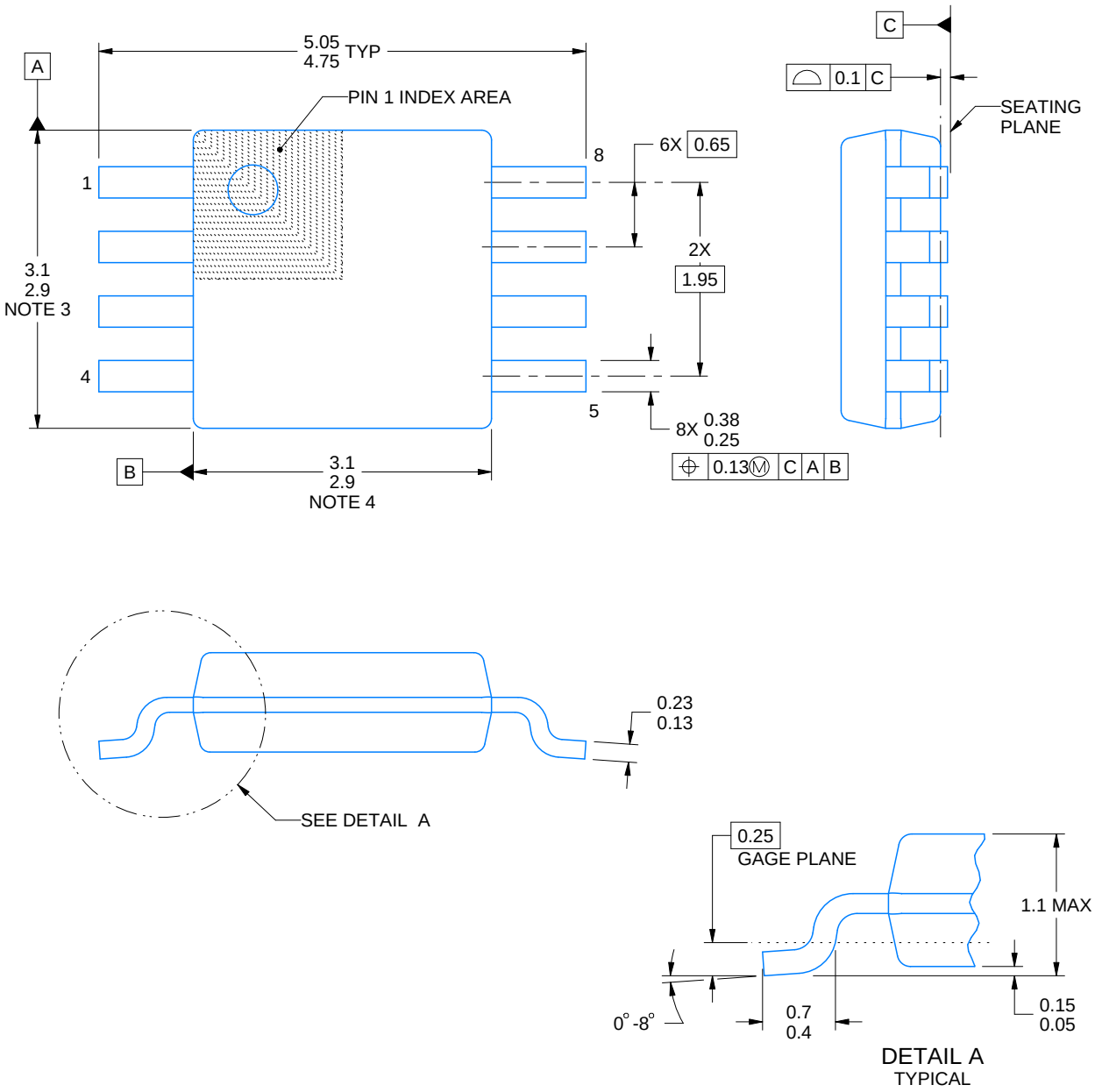
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2837IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2837IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2837IRUNR	QFN	RUN	10	3000	210.0	185.0	35.0
OPA2837IRUNT	QFN	RUN	10	250	210.0	185.0	35.0
OPA837IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA837IDBVR2	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA837IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
OPA837IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA837IDCKT	SC70	DCK	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

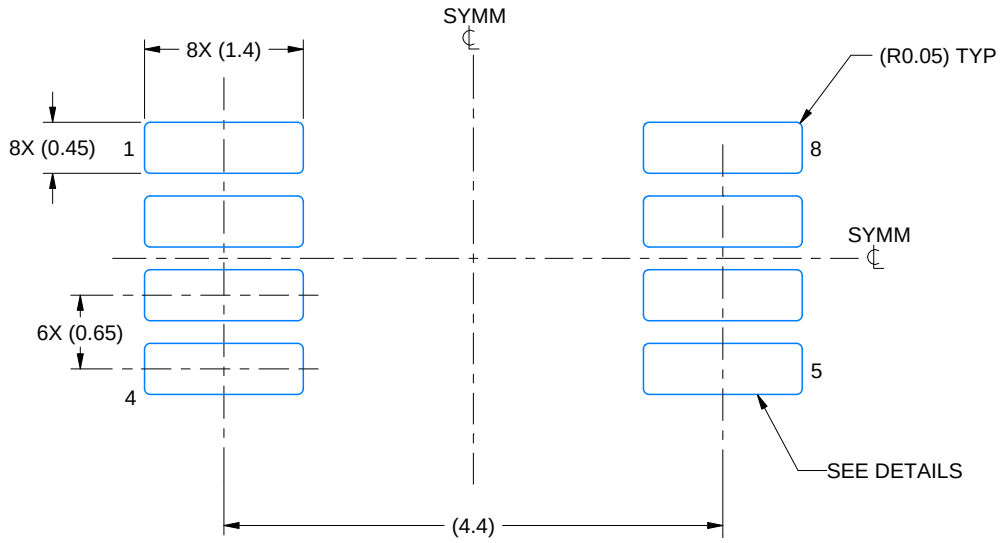
SMALL OUTLINE PACKAGE



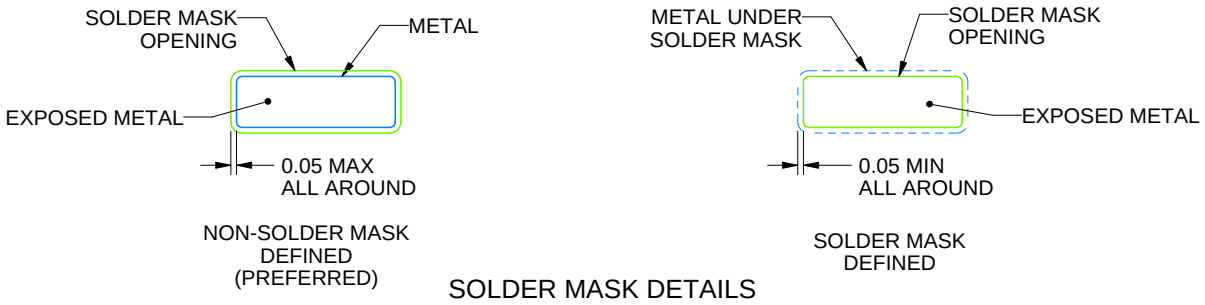
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

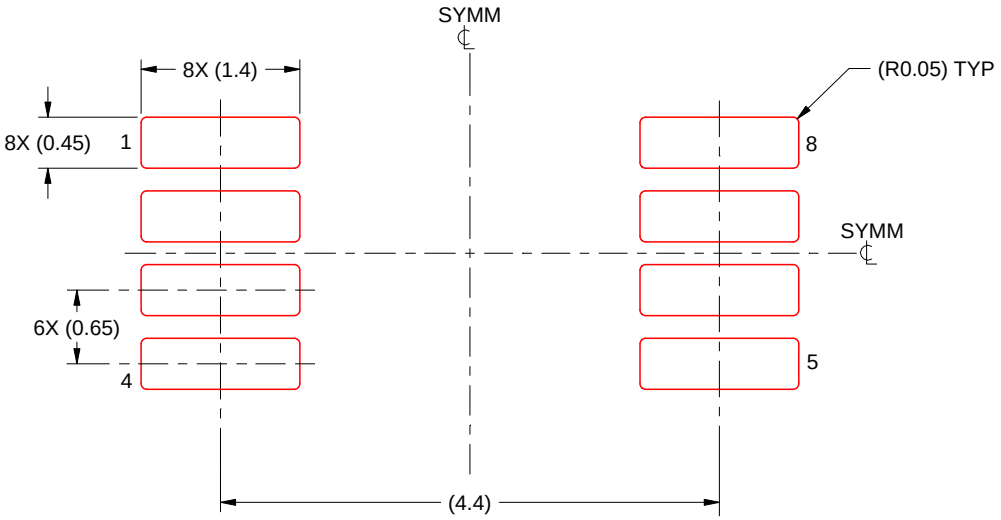


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

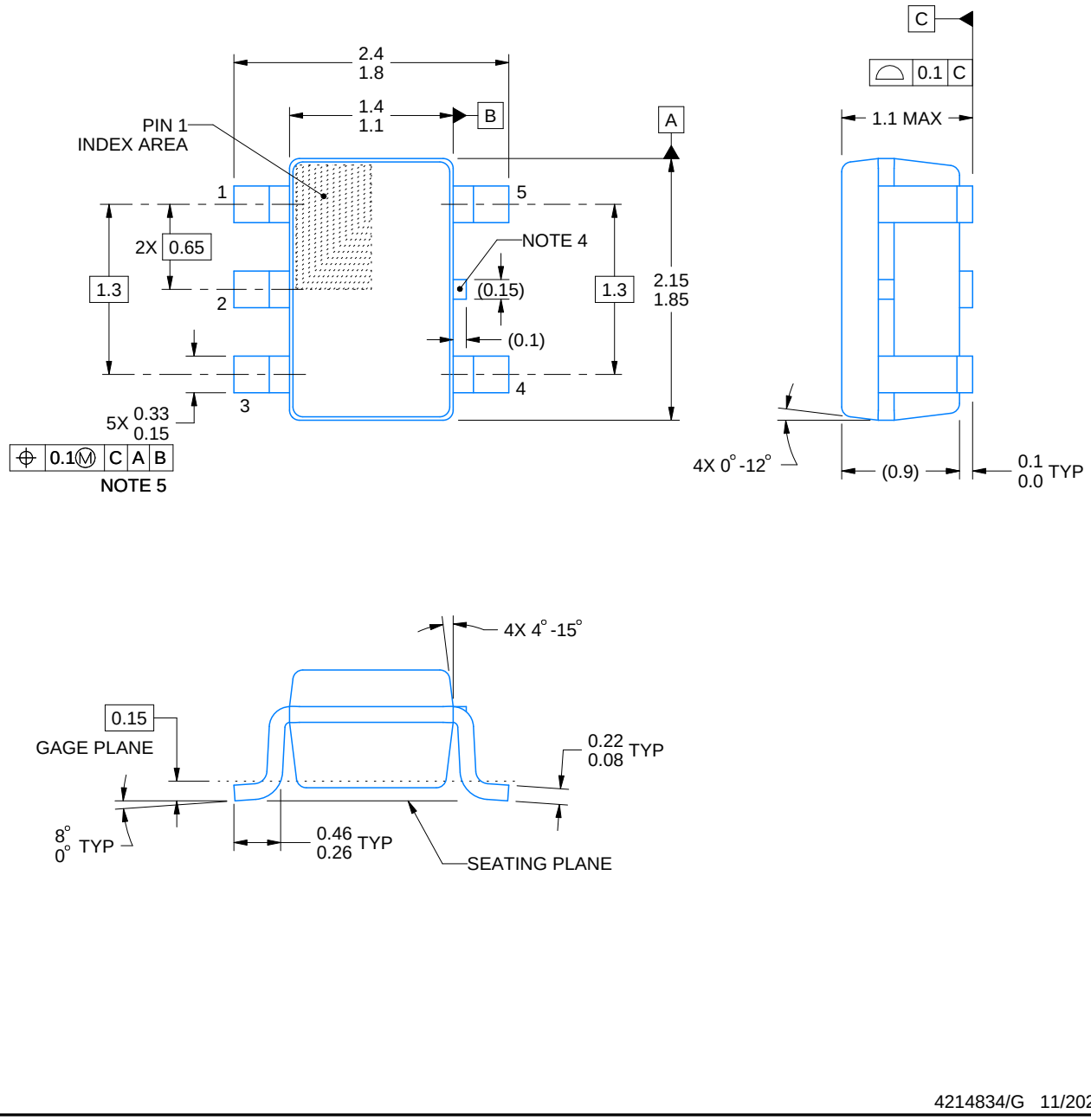
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

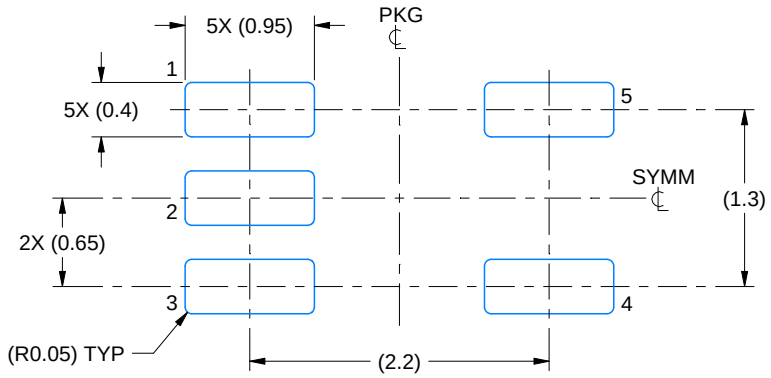
SMALL OUTLINE TRANSISTOR



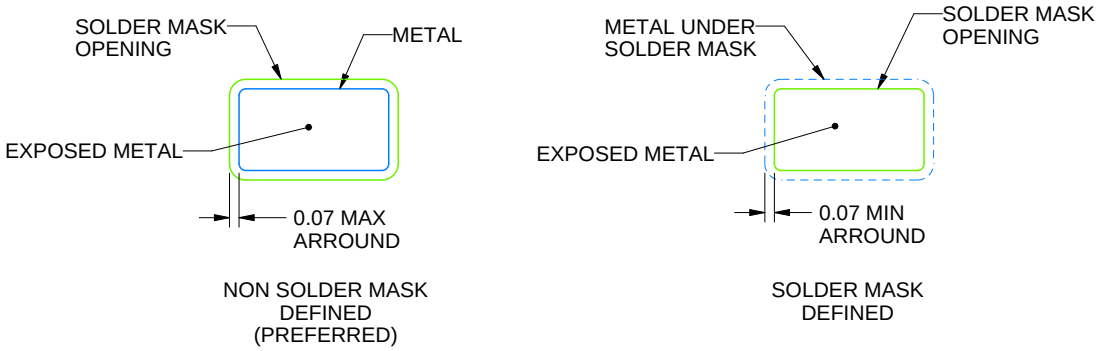
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

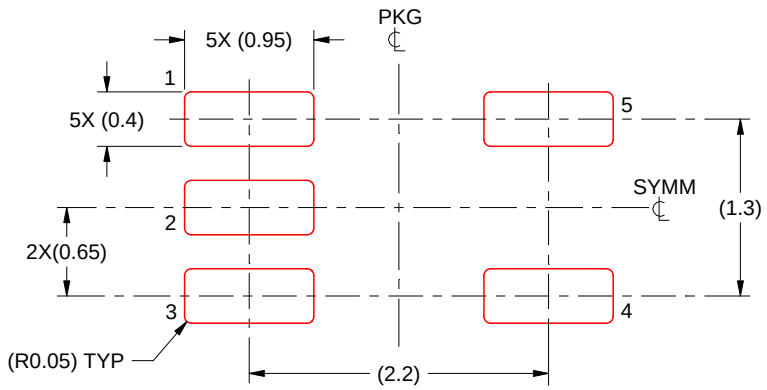


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

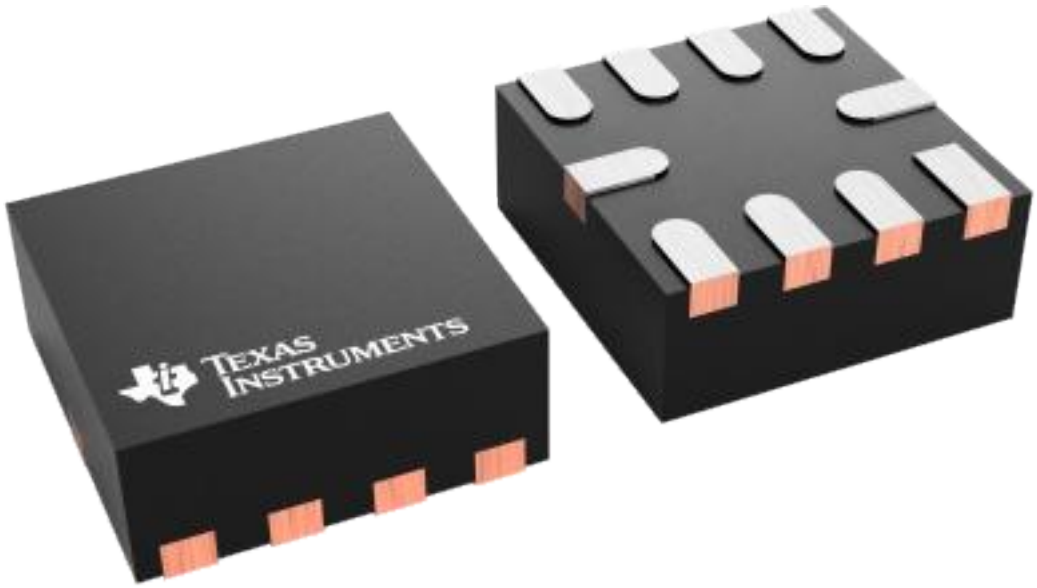
RUN 10

WQFN - 0.8 mm max height

2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



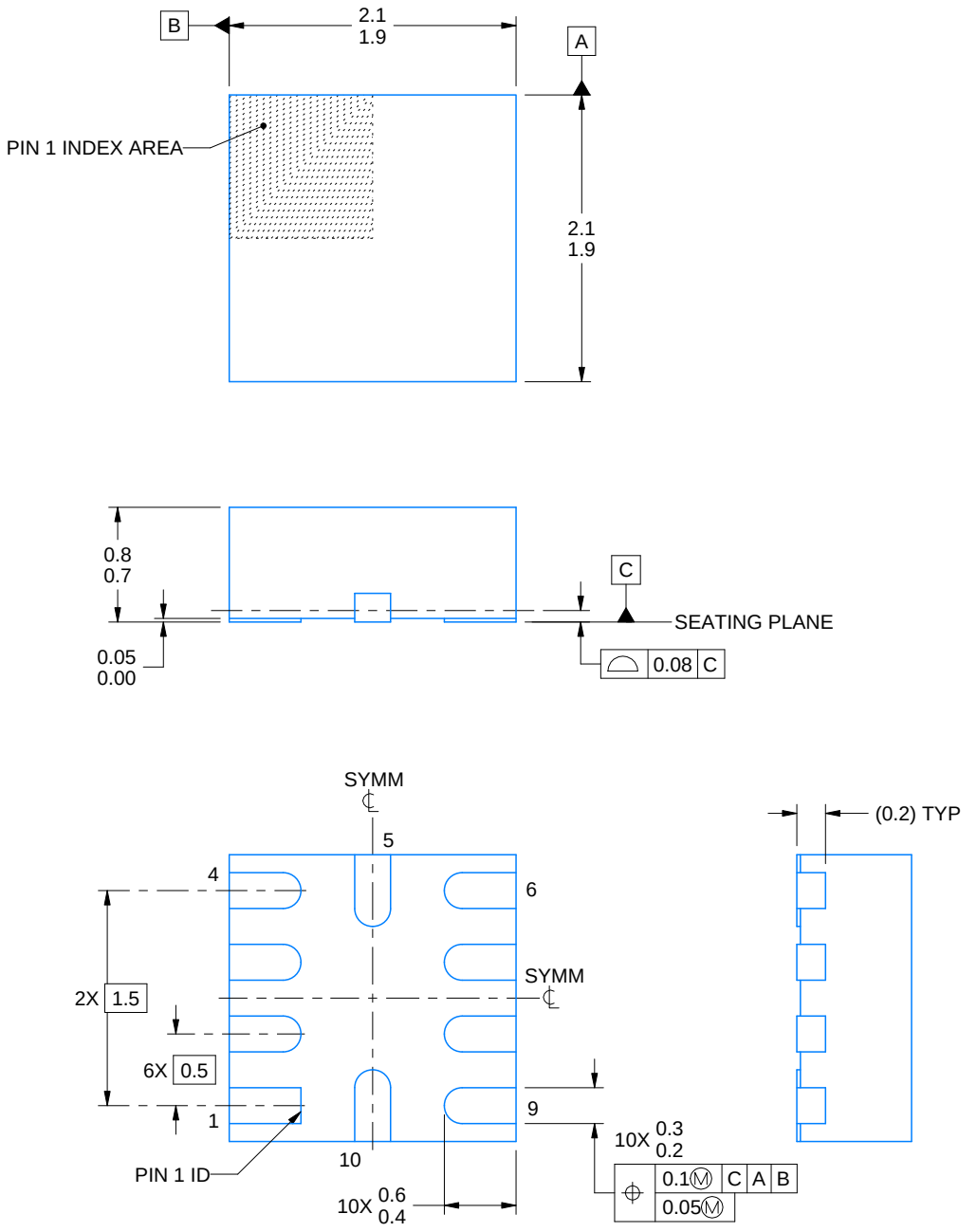
4228249/A

RUN0010A

PACKAGE OUTLINE

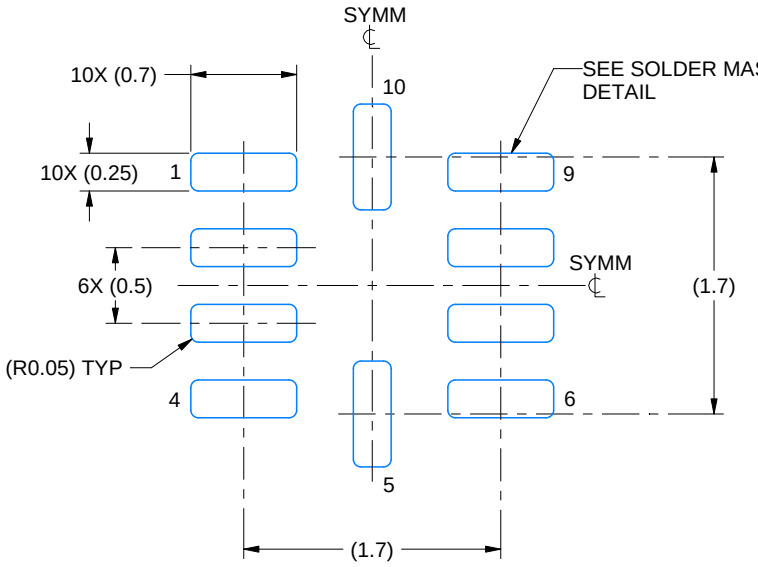
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

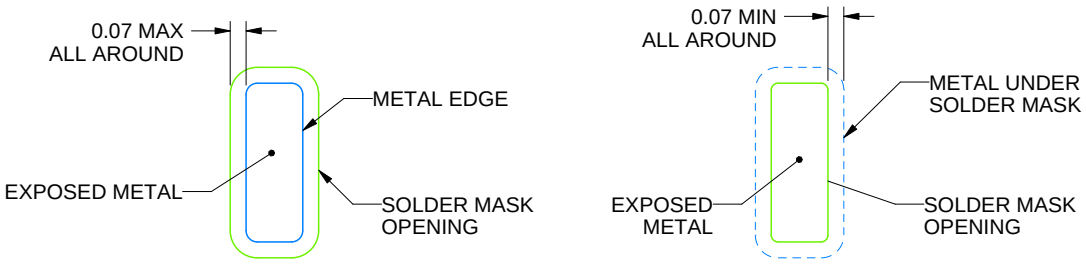


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4220470/A 05/2020

NOTES: (continued)

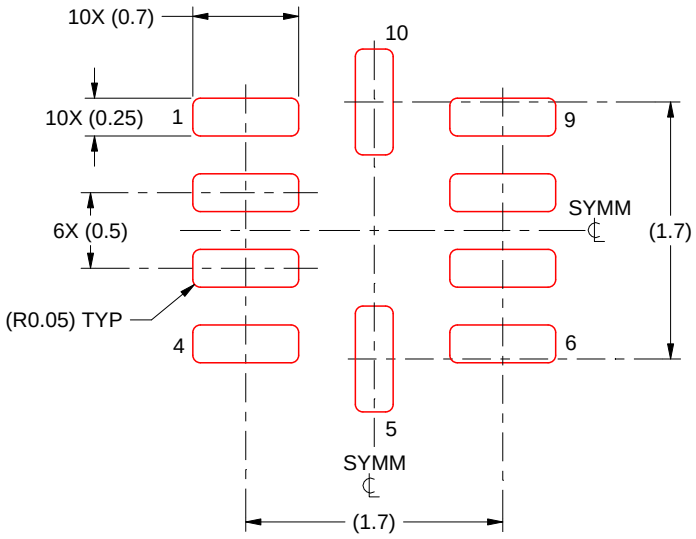
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4220470/A 05/2020

NOTES: (continued)

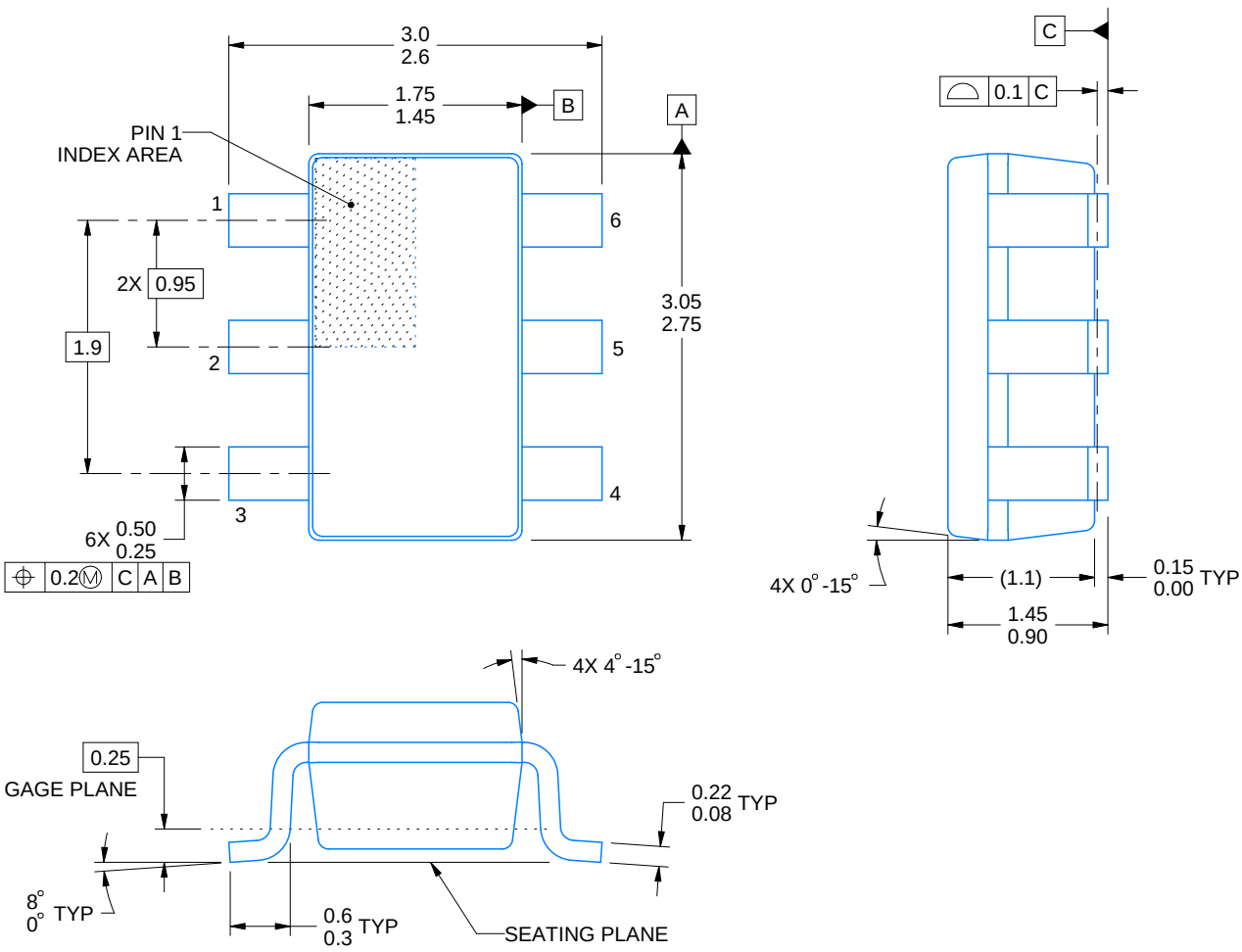
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

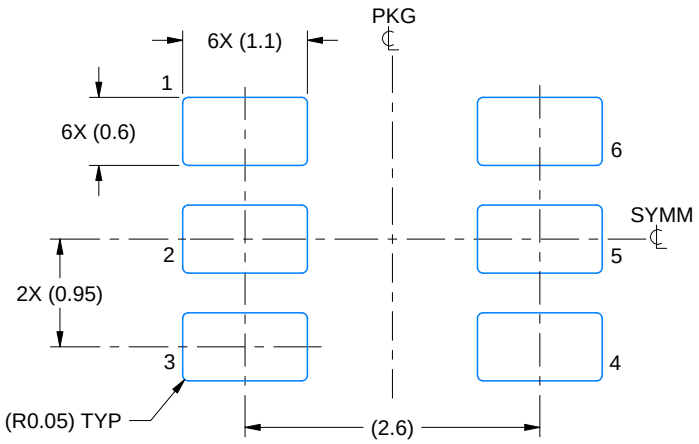
SMALL OUTLINE TRANSISTOR



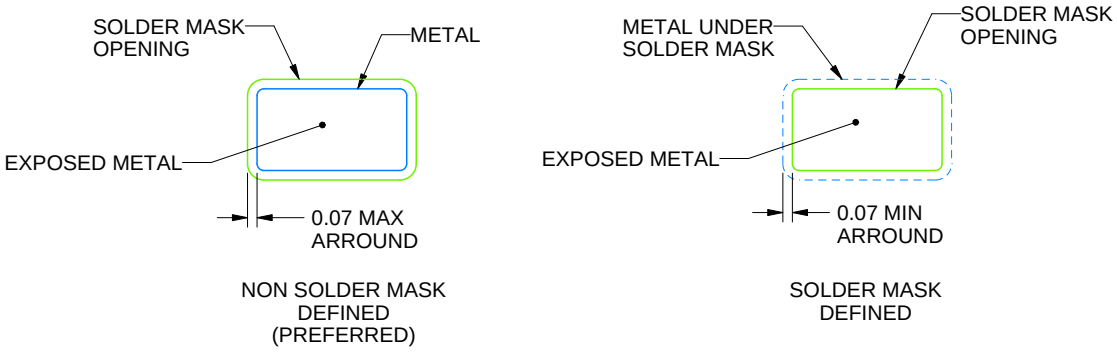
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

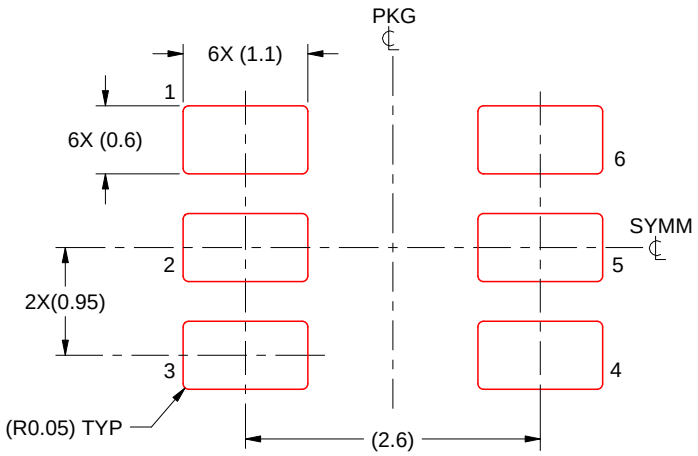


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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