OPA810 140MHz、レール ツー レール入出力、FET 入力のオペアンプ

1 特長

- ゲイン帯域幅積:70 MHz
- 小信号帯域幅:140MHz
- スルーレート:200V/µs
- 幅広い電源電圧範囲:4.75V～27V
- 低ノイズ:
  - 入力電圧ノイズ: 6.3nV/√Hz (f = 500kHz)
  - 入力電流ノイズ:5fA/√Hz (f = 10kHz)
- レール ツー レール入出力
  - FET 入力段:2pA (標準値) の入力バイアス電流
  - 高リニア出力電流:75mA
- 入力オフセット:±500µV (最大値)
- オフセット ドリフト:±2.5µV/℃ (標準値)
- 低消費電力:3.7mA/ チャネル
- 拡張温度範囲:-40℃～+125℃
- デュアルチャネル バージョン: *OPA2810*

2 アプリケーション

- 広帯域フォトダイオード トランスインピーダンス アンプ
- アナログ入出力モジュール
- インピーダンス測定
- 電力アナライザ
- 高インピーダンスの電圧および電流測定
- データ アクイジション
- マルチチャネルのセンサ インターフェイス
- オプトエレクトロニクス ドライバ

3 概要

OPA810 は、ピコアンペア (pA) の範囲のバイアス電流を持つ、シングル チャネル、電界効果トランジスタ (FET) 入力、電圧帰還型オペアンプです。OPA810 は 140MHz の小信号ユニティ ゲイン帯域幅でユニティ ゲイン安定であり、チャネルあたり 3.7mA (標準値) の小さな静止電流 (I_Q) で優れた DC 精度と動的 AC 性能を実現しています。テキサス・インスツルメンツ独自の高速 SiGe BiCMOS プロセスで製造されており、静止電流が同等である他の FET 入力アンプに比べて大幅に性能が向上しています。70MHz のゲイン帯域幅積 (GBWP)、200V/µs のスルーレート、6.3nV/√Hz の小さい電圧ノイズを特長とする OPA810 は、広範な高忠実度データ アクイジションおよび信号処理アプリケーションで使うために設計されています。

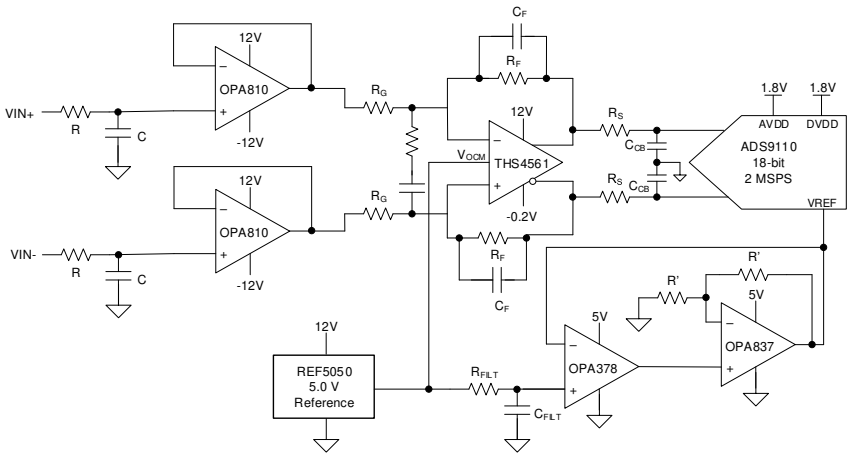
OPA810 はレール ツー レールの入出力を持ち、オプトエレクトロニクス部品とアナログ / デジタル コンバータ (ADC) の入力の駆動や、デジタル / アナログ コンバータ (DAC) の出力で重い負荷を駆動する際のバッファリングのための 75mA のリニア出力電流を供給します。

OPA810 は、-40℃～+125℃の拡張産業用温度範囲にわたって仕様が規定されています。OPA2810 は OPA810 のデュアルチャネル バリアントであり、8 ピン SOIC、SOT-23、VSSOP パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
OPA810	D (SOIC、8)	4.9mm × 6 mm
	DBV (SOT-23、5)	2.9mm × 2.8 mm
	DCK (SC70、5)	2mm × 2.1 mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



高インピーダンス入力のデータ アクイジション フロント エンド

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4 Device Comparison Table

DEVICE	$V_{S\pm}$ (V)	I_Q/CHANNEL (mA)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA2810	±12	3.6	70	192	6	Unity-gain stable FET input
OPA607	±2.5	0.9	50	24	3.8	Gain of 6, stable, low-cost CMOS amplifier
THS4631	±15	13	210	900	7	Unity-gain stable FET input
OPA859	±2.625	20.5	1800	1150	3.3	Unity-gain stable FET input
OPA818	±6.5	27.7	2700	1400	2.2	Gain of 7, stable FET input

5 Pin Configuration and Functions

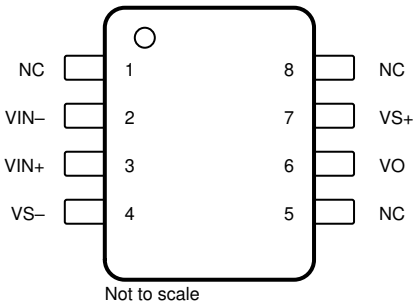


図 5-1. D Package, 8-Pin SOIC (Top View)

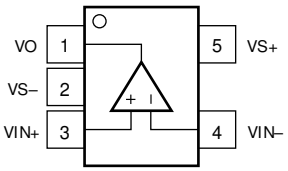


図 5-2. DBV Package, 5-Pin SOT23 and DCK Package, 5-Pin SC70 (Top View)

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC)	DBV (SOT-23), DCK (SC70)		
NC	1, 5, 8	—	—	No internal connection
VIN–	2	4	Input	Inverting input pin
VIN+	3	3	Input	Noninverting input pin
VO	6	1	Output	Output pin
VS–	4	2	Power	Negative power-supply pin
VS+	7	5	Power	Positive power-supply pin

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

			MIN	MAX	UNIT
V_S	Supply voltage (total bipolar supplies)(4)			±14	V
V_{IN}	Input voltage		$V_{S–}$ – 0.5	V_{S+} + 0.5	V
$V_{IN,Diff}$	Differential input voltage(2)			±7	V
I_I	Continuous input current			±10	mA
I_O	Continuous output current(3)	T_A = –40℃ to +85℃		±40	mA
		T_A = 125℃		±15	mA
P_D	Continuous power dissipation		See セクション 6.4		
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Equal to the lower of ±7 V or total supply voltage.
(3) Long-term continuous output current for electromigration limits.
(4) V_S is the total supply voltage given by $V_S = V_{S+} – V_{S–}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	4.75		27	V
T_A	Ambient temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA810			UNIT
		D (SOIC)	DBV (SOT-23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	134.8	174.3	190.8	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	75.2	94.7	140.1	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	78.2	45.4	69.0	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	25.2	21.6	45.9	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	77.4	45.0	68.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 10 V

at T_A = 25°C, V_{S+} = 5 V, $V_{S–}$ = –5 V, common-mode voltage (V_{CM}) = mid-supply, and R_L = 1 kΩ connected to mid-supply[1] (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL[2]
AC PERFORMANCE							
SSBW	Small-signal bandwidth	G = 1, V_O = 20 mV_{PP}, R_F = 0 Ω		135		MHz	C
		G = 1, V_O = 20 mV_{PP}, R_F = 0 Ω, C_L = 10 pF		140			C
		G = –1, V_O = 20 mV_{PP}		68			C
LSBW	Large-signal bandwidth	G = 2, V_O = 2 V_{PP}		41		MHz	C
GBWP	Gain-bandwidth product			70		MHz	C
	Bandwidth for 0.1-dB flatness	G = 2, V_O = 20 mV_{PP}		16		MHz	C
SR	Slew rate (20%-80%)[3]	G = 2, V_O = –2-V to 2-V step		200		V/µs	C
	Rise time	V_O = 200-mV step		4		ns	C
	Fall time	V_O = 200-mV step		4		ns	C
	Settling time to 0.1%	G = 2, V_O = 2-V step		47		ns	C
		G = 2, V_O = 8-V step		65			C
	Settling time to 0.001%	G = 2, V_O = 2-V step		330		ns	C
		G = 2, V_O = 8-V step		230			C
	Input overdrive recovery	G = 1, R_F = 0 Ω, ($V_{S–}$ – 0.5 V) to (V_{S+} + 0.5 V) input		55		ns	C
	Output overdrive recovery	G = –1, ($V_{S–}$ – 0.5 V) to (V_{S+} + 0.5 V) input		55		ns	C
HD2	Second-order harmonic distortion	f = 100 kHz, R_L = 1 kΩ, V_O = 2 V_{PP}		–120		dBc	C
		f = 1 MHz, R_L = 1 kΩ, V_O = 2 V_{PP}		–101			C
HD3	Third-order harmonic distortion	f = 100 kHz, R_L = 1 kΩ, V_O = 2 V_{PP}		–137		dBc	C
		f = 1 MHz, R_L = 1 kΩ, V_O = 2 V_{PP}		–101			C
e_n	Input-referred voltage noise	Flat-band, 1/f corner at 1.5 kHz		6.3		nV/√Hz	C
i_n	Input-referred current noise	f = 10 kHz		5		fA/√Hz	C
z_O	Closed-loop output impedance	f = 100 kHz		0.007		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	f = dc, V_O = ±2.5 V	108	120		dB	A
V_{OS}	Input offset voltage	SOIC package		100	500	µV	A
		DBV and DCK packages		100	715		
	Input offset voltage drift	T_A = –40°C to +125°C		2.5	10	µV/°C	B
	Input bias current			2	20	pA	A
	Input offset current			1	20	pA	A
CMRR	Common-mode rejection ratio	f = dc, V_{CM} = –3 V to 1 V, SOIC package	80	100		dB	A
		T_A = –40°C to +125°C, SOIC package	80				B

6.5 Electrical Characteristics: 10 V (続き)

at T_A = 25°C, V_{S+} = 5 V, $V_{S–}$ = –5 V, common-mode voltage (V_{CM}) = mid-supply, and R_L = 1 kΩ connected to mid-supply(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(2)
INPUT							
	Allowable input differential voltage	See 図 6-54		±7		V	C
	Common-mode input impedance	In closed-loop configuration		12 || 2		GΩ||pF	C
	Differential input capacitance	In open-loop configuration		0.5		pF	C
	Most positive input voltage	ΔV_{OS} < 5 mV(4)	V_{S+} + 0.2	V_{S+} + 0.3		V	A
	Most negative input voltage	ΔV_{OS} < 5 mV(4)	$V_{S–}$ – 0.2	$V_{S–}$ – 0.3		V	A
	Most positive input voltage for main-JFET stage	See 図 6-17	V_{S+} – 2.9	V_{S+} – 2.5		V	C
OUTPUT							
V_{OCRH}	Output voltage range high	R_L = 667 Ω	V_{S+} – 0.18	V_{S+} – 0.11		V	A
V_{OCRH}	Output voltage range high	T_A = –40°C to +125°C, R_L = 667 Ω	V_{S+} – 0.2			V	B
V_{OCRL}	Output voltage range low	R_L = 667 Ω		$V_{S–}$ + 0.08	$V_{S–}$ + 0.15	V	A
V_{OCRL}	Output voltage range low	T_A = –40°C to +125°C, R_L = 667 Ω			$V_{S–}$ + 0.2	V	B
$I_{O(max)}$	Linear output drive (sourcing and sinking)	V_O = 2.65 V, R_L = 51 Ω, ΔV_{OS} < 1 mV	52	75		mA	A
I_{SC}	Output short-circuit current			100		mA	B
C_L	Capacitive load drive	< 3-dB peaking, R_S = 0 Ω		10		pF	C
POWER SUPPLY							
I_Q	Quiescent current per channel			3.7	4.6	mA	A
PSRR	Power-supply rejection ratio	ΔV_S = ±2 V(5), SOIC package	79	100		dB	A
		T_A = –40°C to +125°C, SOIC package	79				B
AUXILIARY CMOS INPUT STAGE							
	Gain-bandwidth product			27		MHz	C
	Input-referred voltage noise	f = 1 MHz		20		nV/√Hz	C
	Input offset voltage	V_{CM} = V_{S+} – 1.5 V, no load, SOIC package			1.6	mV	A
	Input bias current	V_{CM} = V_{S+} – 1.5 V		2	20	pA	A

(1) For ac specifications, G = 2 V/V, R_F = 1 kΩ and C_L = 4.7 pF (unless otherwise noted).
(2) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C, overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.
(3) Lower of the measured positive and negative slew rate.
(4) Change in input offset from the value when input is biased to midsupply.
(5) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

6.6 Electrical Characteristics: 24 V

at T_A = 25°C, V_{S+} = 12 V, $V_{S–}$ = –12 V, common-mode voltage (V_{CM}) = mid-supply, and R_L = 1 kΩ connected to mid-supply[1] (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level[2]
AC PERFORMANCE							
SSBW	Small-signal bandwidth	G = 1, V_o = 20 mV_{PP}, R_F = 0 Ω		135		MHz	C
		G = 1, V_o = 20 mV_{PP}, R_F = 0 Ω, C_L= 10 pF		140			C
		G = –1, V_o = 20 mV_{PP}		68			C
LSBW	Large-signal bandwidth	G = 2 V_o = 2 V_{PP}		44		MHz	C
		G = 2 V_o = 10 V_{PP}		14			C
GBWP	Gain-bandwidth product			70		MHz	C
	Bandwidth for 0.1-dB flatness	G = 2, V_o = 20 mV_{PP}		16		MHz	C
SR	Slew rate (20%-80%)[3]	G = 2, V_o = –2-V to 2-V step		237		V/µs	C
		G = –1, V_o = –2-V to 2-V step		222			C
		G = 2, V_o = –4.5-V to 3.5-V step		254			C
	Rise time	V_o = 200-mV step		4		ns	C
	Fall time	V_o = 200-mV step		4		ns	C
	Settling time to 0.1%	G = 2, V_o = 2-V step		47		ns	C
		G = 2, V_o = 10-V step		70			C
	Settling time to 0.001%	G = 2, V_o = 2-V step		320		ns	C
		G = 2, V_o = 10-V step		200			C
	Input overdrive recovery	G = 1, R_F = 0 Ω, ($V_{S–}$ – 0.5 V) to (V_{S+} + 0.5 V) input		35		ns	C
	Output overdrive recovery	G = –1, ($V_{S–}$ – 0.5 V) to (V_{S+} + 0.5 V) input		45		ns	C
HD2	Second-order harmonic distortion	f = 100 kHz, R_L = 1 kΩ, V_o = 2 V_{PP}		–118		dBc	C
		f = 100 kHz, R_L =1 kΩ, V_o = 10 V_{PP}		–108			C
		f = 1 MHz, R_L = 1 kΩ, V_o = 2 V_{PP}		–112			C
		f = 1 MHz, RL=1 kΩ, V_o = 10 V_{PP}		–91			C
HD3	Third-order harmonic distortion	f = 100 kHz, R_L = 1 kΩ, V_o = 2 V_{PP}		–136		dBc	C
		f = 100 kHz, R_L =1 kΩ, V_o = 10 V_{PP}		–130			C
		f = 1 MHz, R_L = 1 kΩ, V_o = 2 V_{PP}		–104			C
		f = 1 MHz, R_L =1 kΩ, V_o = 10 V_{PP}		–91			C
e_n	Input-referred voltage noise	Flat-band, 1/f corner at 1.5 kHz		6.3		nV/√Hz	C
i_n	Input-referred current noise	f = 10 kHz		5		fA/√Hz	C
z_O	Closed-loop output impedance	f = 100 kHz		0.007		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	f = dc, V_o = ±8 V	108	120		dB	A
V_{OS}	Input offset voltage	SOIC package		100	500	µV	A
		DBV and DCK packages		100	550		
	Input offset voltage drift	T_A = –40°C to +125°C		2.5	10	µV/°C	B
	Input bias current			2	20	pA	A
	Input offset current			1	20	pA	A
CMRR	Common-mode rejection ratio	f = dc, V_{CM} = ±5 V, SOIC package	90	105		dB	A
		T_A = –40°C to +125°C, SOIC package	90				B

6.6 Electrical Characteristics: 24 V (続き)

at T_A = 25°C, V_{S+} = 12 V, $V_{S–}$ = –12 V, common-mode voltage (V_{CM}) = mid-supply, and R_L = 1 kΩ connected to mid-supply(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level(2)
INPUT							
	Allowable input differential voltage	see 図 6-54		±7		V	C
	Common-mode input impedance	In closed-loop configuration		12 || 2.5		GΩ||pF	C
	Differential input capacitance	In open-loop configuration		0.5		pF	C
	Most positive input voltage	ΔV_{OS} < 5 mV(4)	V_{S+} + 0.2	V_{S+} + 0.3		V	A
	Most negative input voltage	ΔV_{OS} < 5 mV(4)	$V_{S–}$ – 0.2	$V_{S–}$ – 0.3		V	A
	Most positive input voltage for main-JFET stage	See 図 6-33	V_{S+} – 2.9	V_{S+} – 2.5		V	C
OUTPUT							
V_{OCRH}	Output voltage range high	R_L = 667 Ω	V_{S+} – 0.33	V_{S+} – 0.22		V	A
		T_A = –40°C to +125°C, R_L = 667 Ω	V_{S+} – 0.36				B
V_{OCRL}	Output voltage range low	R_L = 667 Ω		$V_{S–}$ + 0.15	$V_{S–}$ + 0.23	V	A
		T_A = –40°C to +125°C, R_L = 667 Ω			$V_{S–}$ + 0.33		B
$I_{O(max)}$	Linear output drive (sourcing and sinking)	V_o = 7.25 V, R_L = 151 Ω, ΔV_{OS} < 1 mV	48	64		mA	A
I_{SC}	Output short-circuit current			108		mA	B
C_L	Capacitive load drive	< 3-dB peaking, R_S = 0 Ω		10		pF	C
POWER SUPPLY							
I_Q	Quiescent current per channel			3.8	4.7	mA	A
PSRR	Power supply rejection ratio	ΔV_S = ±2 V(5), SOIC package	90	105		dB	A
		T_A = –40°C to +125°C, SOIC package	90				B
AUXILIARY CMOS INPUT STAGE							
	Gain-bandwidth product			27		MHz	C
	Input-referred voltage noise	f = 1 MHz		20		nV/√Hz	C
	Input offset voltage	V_{CM} = V_{S+} – 1.5 V, no load, SOIC package			1.6	mV	A
	Input bias current	V_{CM} = V_{S+} – 1.5 V		2	24	pA	A

(1) For ac specifications, G = 2 V/V, R_F = 1 kΩ and C_L = 4.7 pF (unless otherwise noted).
(2) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C, overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.
(3) Lower of the measured positive and negative slew rate.
(4) Change in input offset from the value when input is biased to midsupply.
(5) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

6.7 Electrical Characteristics: 5 V

at T_A = 25°C, V_{S+} = 5 V, $V_{S–}$ = 0 V, common-mode voltage (V_{CM}) = 1.25 V, and R_L = 1 kΩ connected to 1.25 V[1] (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level[2]
AC PERFORMANCE							
SSBW	Small-signal bandwidth	G = 1, V_o = 20 mV_{PP}, R_F = 0 Ω		133		MHz	C
		G = 1, V_o = 20 mV_{PP}, R_F= 0 Ω, C_L= 10 pF		135			C
		G = –1, V_o = 20 mV_{PP}		65			C
LSBW	Large-signal bandwidth	G = 2 V_o = 2 V_{PP}		36		MHz	C
GBWP	Gain-bandwidth product			70		MHz	C
	Bandwidth for 0.1-dB flatness	G = 2, V_o = 20 mV_{PP}		16		MHz	C
SR	Slew rate (20%-80%)[3]	G = 2, V_o = –1-V to 1-V step		134		V/µs	C
		G = 2, V_o = –2-V to 2-V step, V_S = ±2.5 V		78			C
	Rise time	V_o = 200-mV step		4		ns	C
	Fall time	V_o = 200-mV step		4		ns	C
	Settling time to 0.1%	G = 2, V_o = –2-V to 0-V step, V_S = ±2.5 V		100		ns	C
	Settling time to 0.001%	G = 2, V_o = –2-V to 0-V step, V_S = ±2.5 V		565		ns	C
	Input overdrive recovery	G = 1, ($V_{S–}$ – 0.5 V) to (V_{S+} + 0.5 V) input, V_S = ±2.5 V		76		ns	C
	Output overdrive recovery	G = –1, ($V_{S–}$ – 0.5 V) to (V_{S+} + 0.5 V) input, V_S = ±2.5 V		93		ns	C
HD2	Second-order harmonic distortion	f = 100 kHz, R_L = 1 kΩ, V_o = 2 V_{PP}		–102		dBc	C
		f = 1 MHz, R_L = 1 kΩ, V_o = 2 V_{PP}		–81			C
HD3	Third-order harmonic distortion	f = 100 kHz, R_L = 1 kΩ, V_o = 2 V_{PP}		–114		dBc	C
		f = 1 MHz, R_L = 1 kΩ, V_o = 2 V_{PP}		–92			C
e_n	Input-referred voltage noise	Flat-band, 1/f corner at 1.5 kHz		6.3		nV/√Hz	C
i_n	Input-referred current noise	f = 10 kHz		5		fA/√Hz	C
z_O	Closed-loop output impedance	f = 100 kHz		0.007		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	f = dc, V_o = 1.25 V to 3.25 V	104	118		dB	A
V_{OS}	Input offset voltage	SOIC package		100	550	µV	A
		DBV and DCK packages		100	760		
	Input offset voltage drift	T_A = –40°C to +125°C		2.5	10	µV/°C	B
	Input bias current			2	20	pA	A
	Input offset current			1	20	pA	A
CMRR	Common-mode rejection ratio	f = dc, V_{CM} = 0.75 V to 1.75 V, SOIC package	73	92		dB	A
		T_A = –40°C to +125°C, SOIC package	73				B
INPUT							
	Allowable input differential voltage	See 図 6-54		±5		V	C
	Common-mode input impedance	In closed-loop configuration		12 || 2.5		GΩ||pF	C
	Differential input capacitance	In open-loop configuration		0.5		pF	C

6.7 Electrical Characteristics: 5 V (続き)

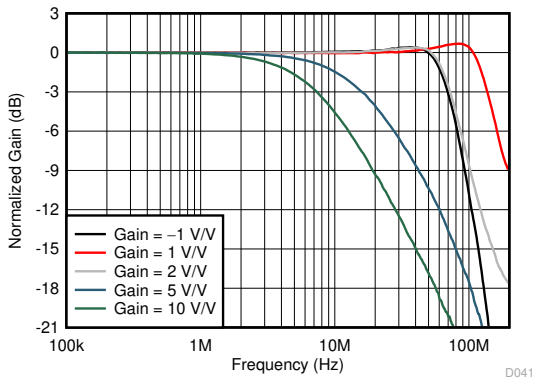
at T_A = 25°C, V_{S+} = 5 V, $V_{S–}$ = 0 V, common-mode voltage (V_{CM}) = 1.25 V, and R_L = 1 kΩ connected to 1.25 V(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level(2)
	Most positive input voltage	ΔV_{OS} < 5 mV(4)	V_{S+} + 0.2	V_{S+} + 0.3		V	A
	Most negative input voltage	ΔV_{OS} < 5 mV(4)	V_{S-} – 0.2	V_{S-} – 0.3		V	A
	Most positive input voltage for main-JFET stage	See 図 6-41	V_{S+} – 2.9	V_{S+} – 2.5		V	C
OUTPUT							
V_{OCRH}	Output voltage range high	R_L = 667 Ω	V_{S+} – 0.12	V_{S+} – 0.09		V	A
		T_A = –40°C to +125°C, R_{LOAD} = 667 Ω	V_{S+} – 0.15				B
V_{OCRL}	Output voltage range low	R_L = 667 Ω		$V_{S–}$ + 0.06	$V_{S–}$ + 0.11	V	A
		T_A = –40°C to +125°C, R_L = 667 Ω			$V_{S–}$ + 0.15		B
$I_{O(max)}$	Linear output drive (sourcing and sinking)	V_O = 1.4 V, R_L = 27.5 Ω, ΔV_{OS} < 1 mV, V_{S+} = 3 V and $V_{S–}$ = –2 V	50	64		mA	A
I_{SC}	Output short-circuit current			96		mA	B
C_L	Capacitive load drive	< 3-dB peaking, R_S = 0 Ω		10		pF	C
POWER SUPPLY							
I_Q	Quiescent current per channel		3.15	3.7	4.5	mA	A
PSRR	Power-supply rejection ratio	ΔV_S = ±0.5 V(5), SOIC package	78	100		dB	A
		T_A = –40°C to +125°C, SOIC package	78				B
AUXILIARY CMOS INPUT STAGE							
	Gain-bandwidth product			27		MHz	C
	Input-referred voltage noise	f = 1 MHz		20		nV/√Hz	C
	Input offset voltage	V_{CM} = V_{S+} – 1.5 V, no load, SOIC package			1.6	mV	A
	Input bias current	V_{CM} = V_{S+} – 1.5 V		2	20	pA	A

(1) For ac specifications, V_{S+} = 3.5 V, $V_{S–}$ = –1.5 V, G = 2 V/V, R_F = 1 kΩ, C_L = 4.7 pF, V_{CM} = 0 V (unless otherwise noted).
(2) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C, overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.
(3) Lower of the measured positive and negative slew rate.
(4) Change in input offset from the value when input is biased to 0 V.
(5) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

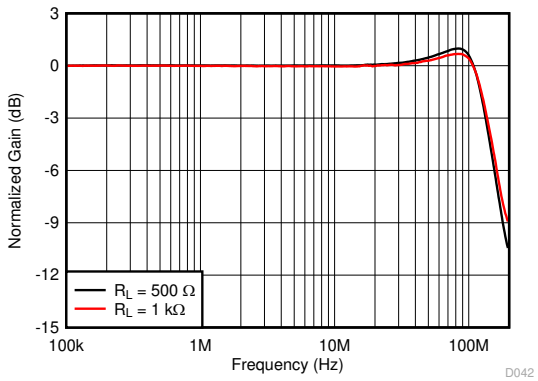
6.8 Typical Characteristics: V_S = 10 V

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_L = 1 kΩ, input and output are biased to midsupply, and T_A ≈ 25°C. For AC specifications, V_O = 2 V_{PP}, G = 2 V/V, R_F = 1 kΩ, and C_L = 4.7 pF (unless otherwise noted)



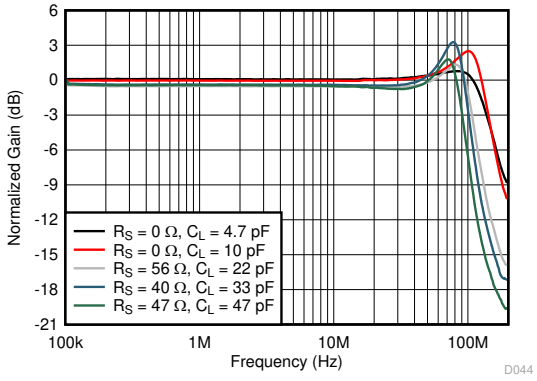
See 図 8-1 and 図 8-2, V_O = 20 mV_{PP}

図 6-1. Small-Signal Frequency Response vs Gain



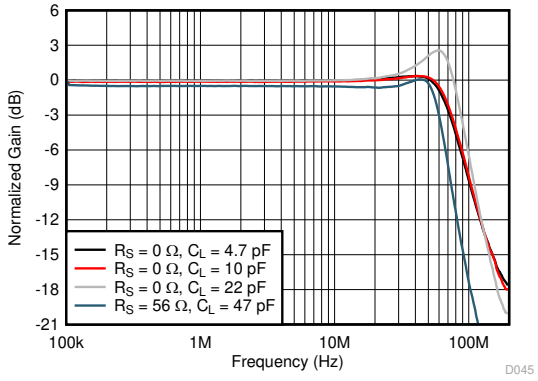
See 図 8-1, V_O = 20 mV_{PP}, gain = 1 V/V, R_F = 0 Ω

図 6-2. Small-Signal Frequency Response vs Output Load



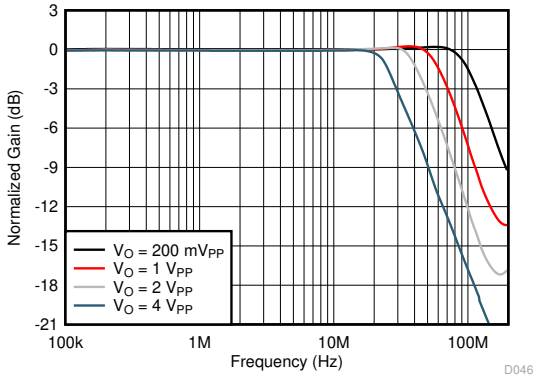
See 図 8-1 and 図 7-1,
V_O = 20 mV_{PP}, gain = 1 V/V, R_F = 0 Ω

図 6-3. Small-Signal Frequency Response vs C_L



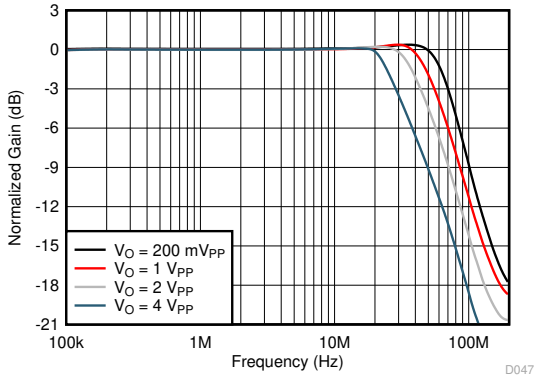
See 図 8-1and 図 7-1, V_O = 20 mV_{PP}, gain = 2 V/V

図 6-4. Small-Signal Frequency Response vs C_L



See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-5. Large-Signal Frequency Response vs Output Voltage

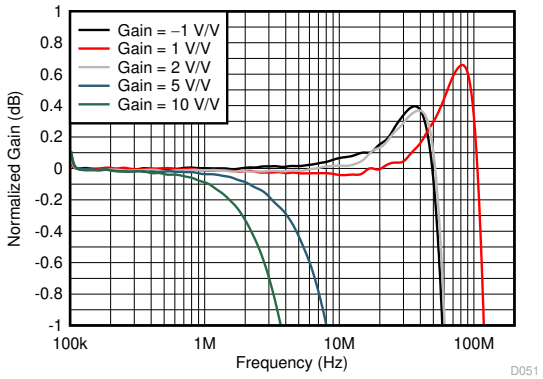


See 図 8-1, gain = 2 V/V

図 6-6. Large-Signal Frequency Response vs Output Voltage

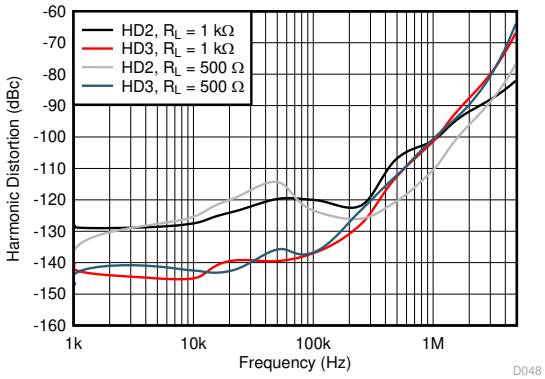
6.8 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_L = 1 kΩ, input and output are biased to midsupply, and T_A ≈ 25°C. For AC specifications, V_O = 2 V_{PP}, G = 2 V/V, R_F = 1 kΩ, and C_L = 4.7 pF (unless otherwise noted)



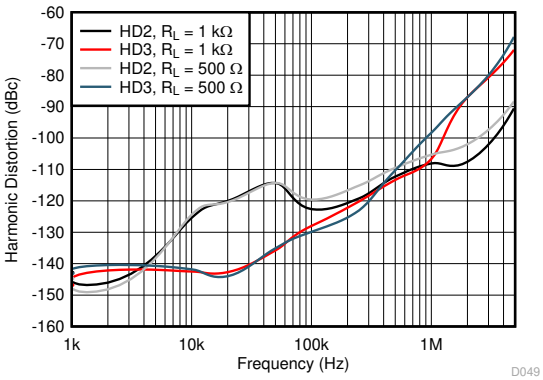
See 図 8-1 and 図 8-2, V_O = 20 mV_{PP}

図 6-7. Small-Signal Response Flatness vs Gain



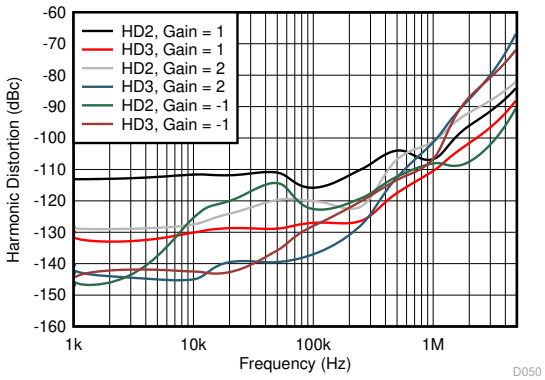
See 図 8-1, gain = 2 V/V

図 6-8. Harmonic Distortion vs Frequency



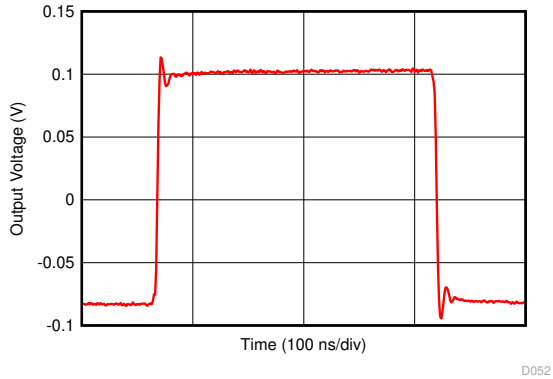
See 図 8-2, gain = –1 V/V

図 6-9. Harmonic Distortion vs Frequency



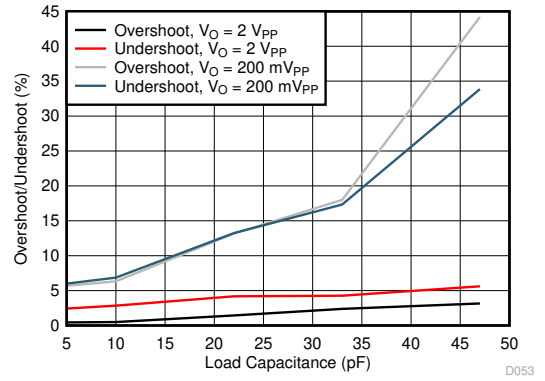
See 図 8-1 and 図 8-2, R_F = 0 Ω

図 6-10. Harmonic Distortion vs Gain



See 図 8-1, gain = 1 V/V, R_F = 0 Ω, C_L = 10 pF

図 6-11. Small-Signal Transient Response

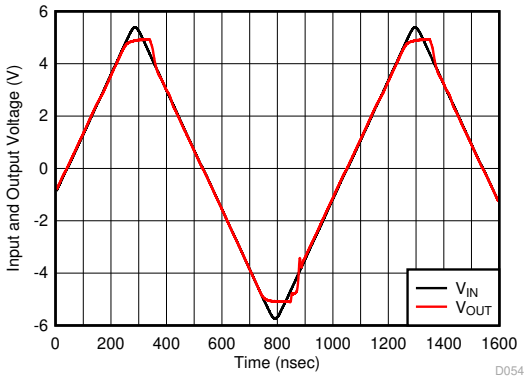


See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-12. Overshoot and Undershoot vs C_L

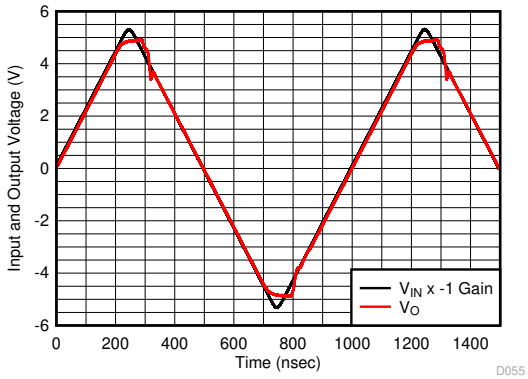
6.8 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_L = 1 kΩ, input and output are biased to midsupply, and T_A ≈ 25°C. For AC specifications, V_O = 2 V_{PP}, G = 2 V/V, R_F = 1 kΩ, and C_L = 4.7 pF (unless otherwise noted)



See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-13. Input Overdrive Recovery



See 図 8-2, gain = –1 V/V

図 6-14. Output Overdrive Recovery

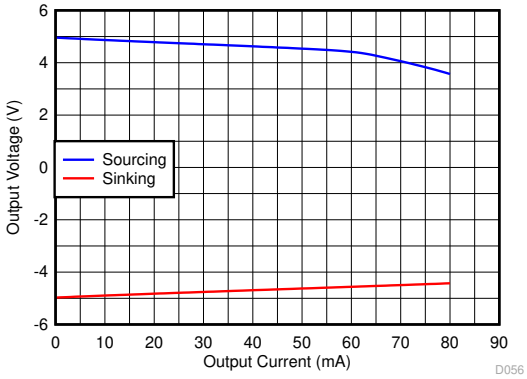
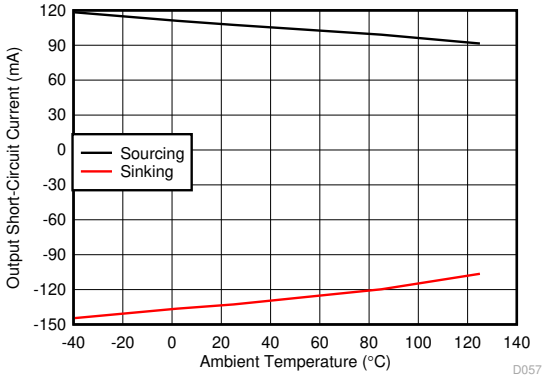
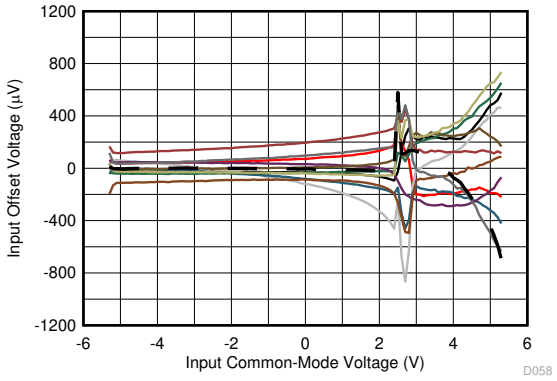


図 6-15. Output Voltage vs Load Current



Output saturated and then short-circuited

図 6-16. Output Short-Circuit Current vs Ambient Temperature

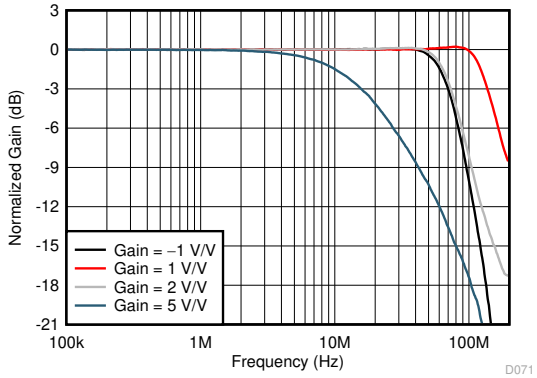


Measured for 12 units

図 6-17. Input Offset Voltage vs Input Common-Mode Voltage

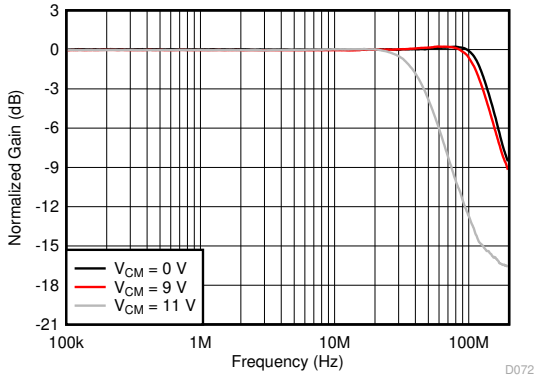
6.9 Typical Characteristics: V_S = 24 V

at V_{S+} = 12 V, $V_{S–}$ = –12 V, R_L = 1 kΩ, input and output are biased to midsupply, and $T_A \approx 25°C$. For AC specifications, V_O = 2 V_{PP}, G = 2 V/V, R_F = 1 kΩ, and C_L = 4.7 pF (unless otherwise noted)



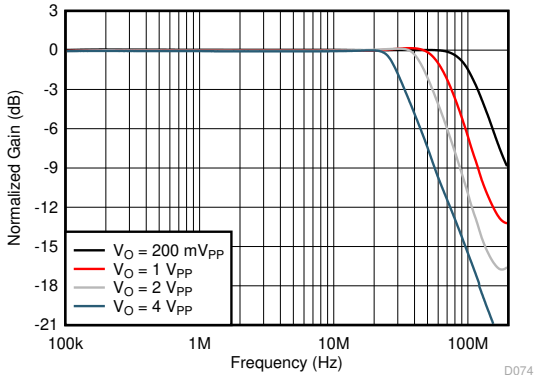
See 図 8-1 and 図 8-2, V_O = 20 mV_{PP}

図 6-18. Noninverting Small-Signal Frequency Response vs Gain



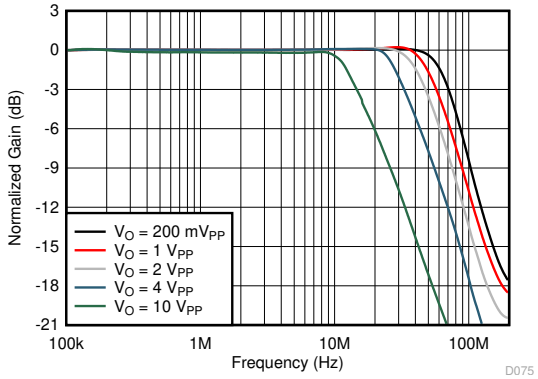
See 図 8-1, V_O = 20 mV_{PP}, gain = 1 V/V, C_L = 4.7 pF, R_F = 0 Ω

図 6-19. Small-Signal Frequency Response vs Output Common-Mode Voltage



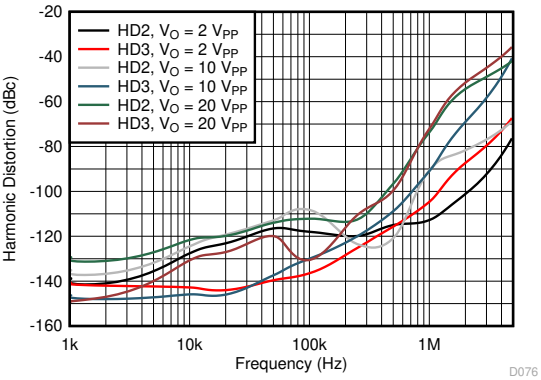
See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-20. Large-Signal Frequency Response vs Output Voltage



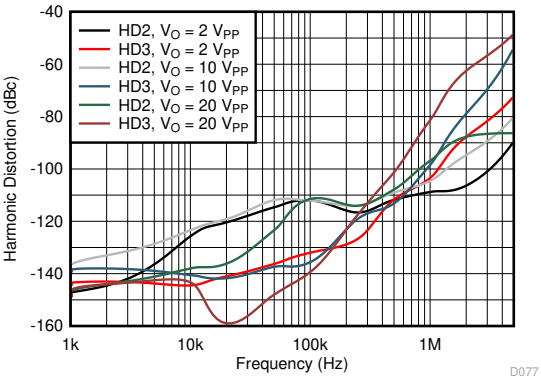
See 図 8-1, gain = 2 V/V

図 6-21. Large-Signal Frequency Response vs V_o



See 図 8-1, gain = 2 V/V

図 6-22. Harmonic Distortion vs Frequency vs V_o

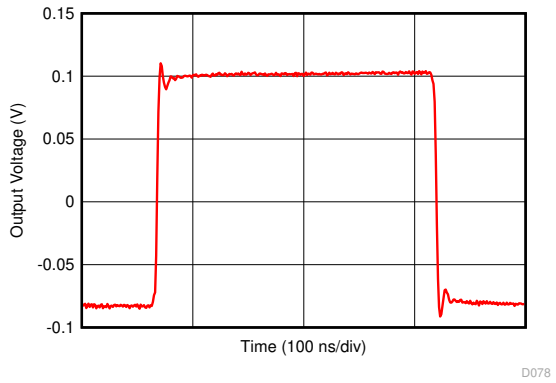


See 図 8-2, gain = –1 V/V

図 6-23. Harmonic Distortion vs Frequency vs V_o

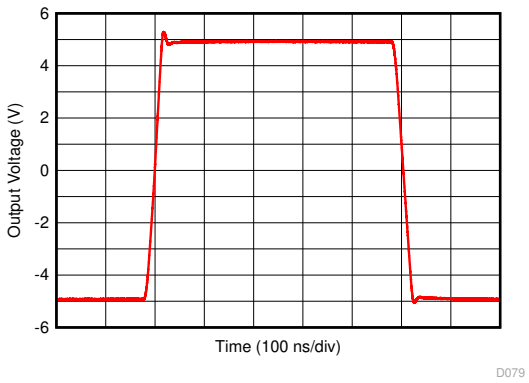
6.9 Typical Characteristics: V_S = 24 V (continued)

at V_{S+} = 12 V, $V_{S–}$ = –12 V, R_L = 1 kΩ, input and output are biased to midsupply, and $T_A \approx 25°C$. For AC specifications, V_O = 2 V_{PP}, G = 2 V/V, R_F = 1 kΩ, and C_L = 4.7 pF (unless otherwise noted)



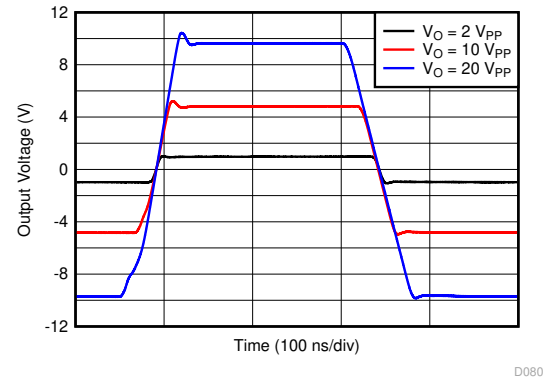
See 図 8-1, gain = 1 V/V, R_F = 0 Ω, C_L = 10 pF

図 6-24. Small-Signal Transient Response



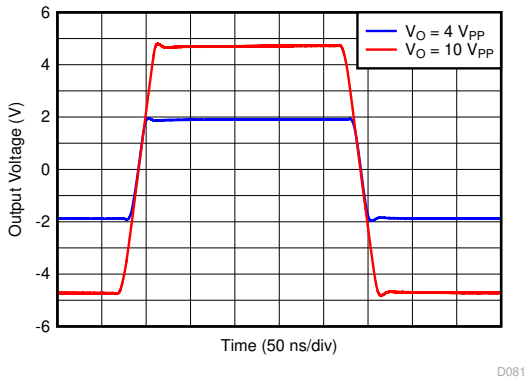
See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-25. Large-Signal Transient Response



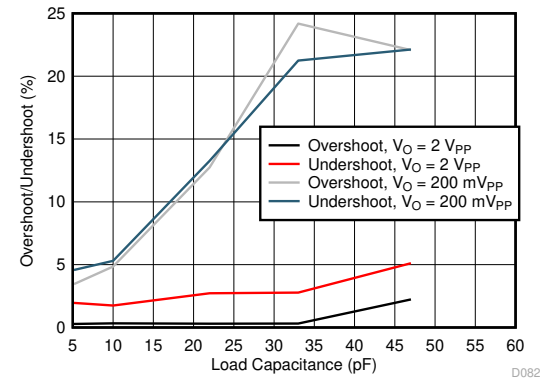
See 図 8-1, gain = 2 V/V

図 6-26. Large-Signal Transient Response



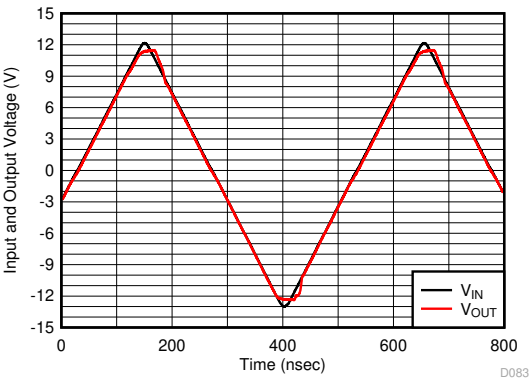
See 図 8-2, gain = –1 V/V

図 6-27. Large-Signal Transient Response



See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-28. Overshoot and Undershoot vs C_L

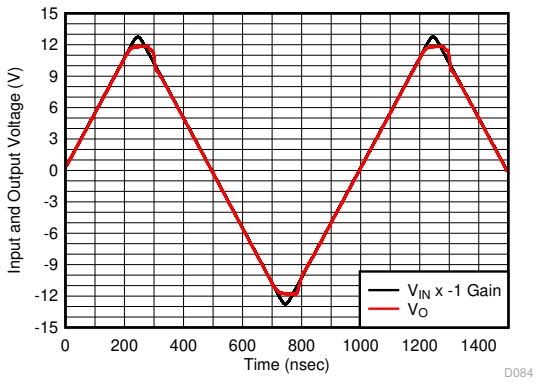


See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-29. Input Overdrive Recovery

6.9 Typical Characteristics: V_S = 24 V (continued)

at V_{S+} = 12 V, $V_{S–}$ = –12 V, R_L = 1 kΩ, input and output are biased to midsupply, and $T_A \approx 25°C$. For AC specifications, V_O = 2 V_{PP}, G = 2 V/V, R_F = 1 kΩ, and C_L = 4.7 pF (unless otherwise noted)



See 図 8-2, gain = –1 V/V

図 6-30. Output Overdrive Recovery

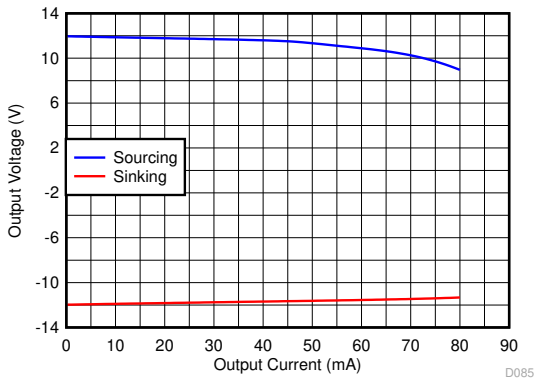
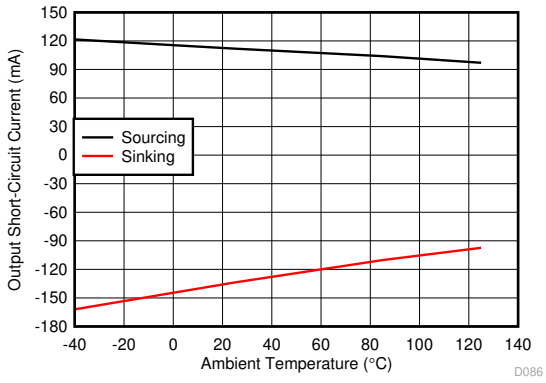
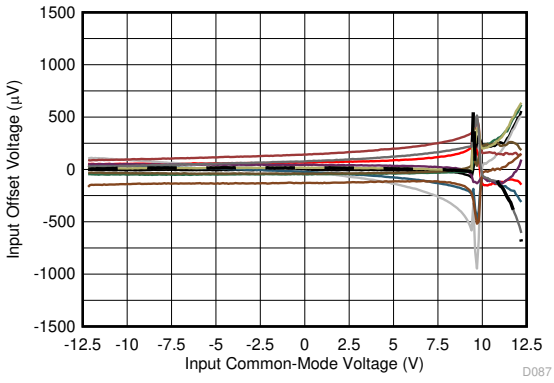


図 6-31. Output Voltage Range vs Load Current



Output saturated and then short-circuited

図 6-32. Output Short-Circuit Current vs Ambient Temperature

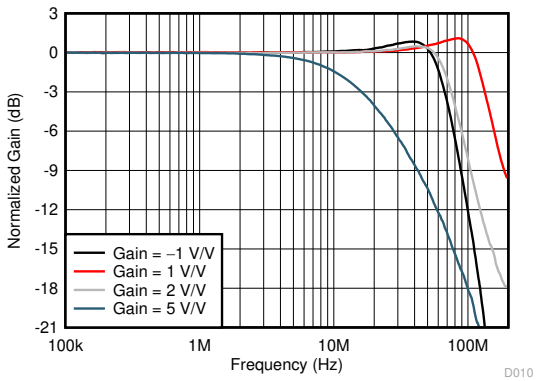


Measured for 12 units

図 6-33. Input Offset Voltage vs Input Common-Mode Voltage

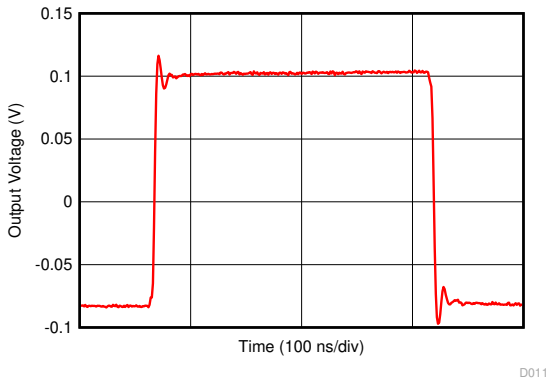
6.10 Typical Characteristics: V_S = 5 V

at V_{S+} = 5 V, $V_{S–}$ = 0 V, V_{CM}= 1.25 V, R_L = 1 kΩ, output is biased to midsupply, and T_A ≈ 25°C. For AC specifications, V_{S+} = 3.5 V, $V_{S–}$ = –1.5 V, V_{CM}= 0 V, V_O = 2 V_{PP}, G = 2 V/V, R_F = 1 kΩ, and C_L = 4.7 pF (unless otherwise noted)



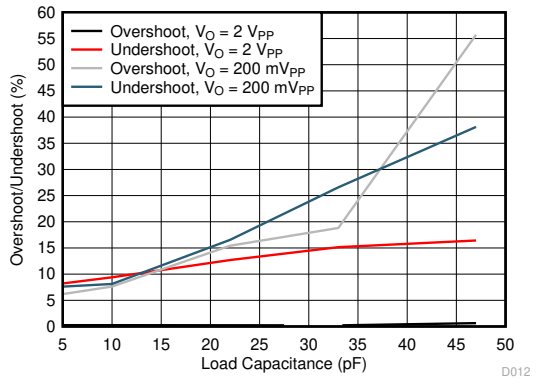
See 図 8-1 and 図 8-2, V_O = 20 mV_{PP}

図 6-34. Small-Signal Response vs Gain



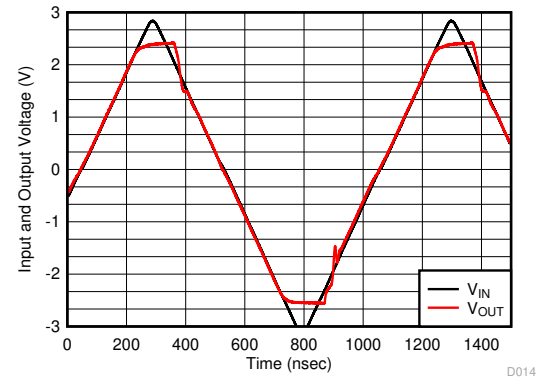
See 図 8-1, gain = 1 V/V, R_F = 0 Ω, C_L = 10 pF

図 6-35. Small-Signal Transient Response



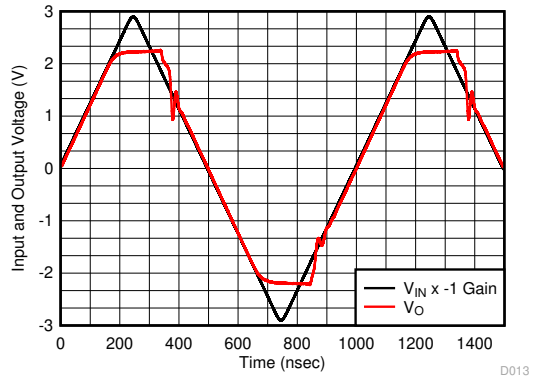
See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-36. Overshoot and Undershoot vs C_L



See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-37. Input Overdrive Recovery



See 図 8-2, gain = –1 V/V

図 6-38. Output Overdrive Recovery

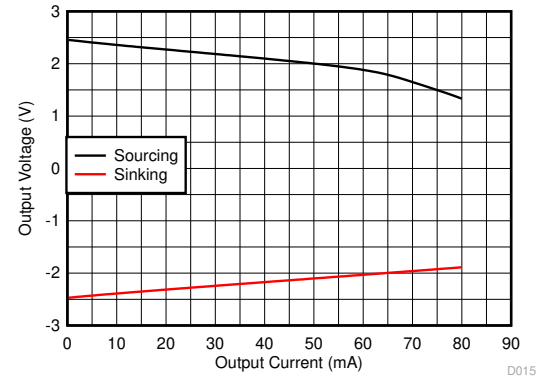
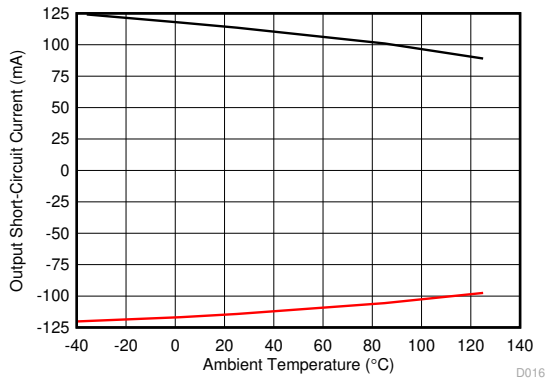


図 6-39. Output Voltage Range vs Output Current

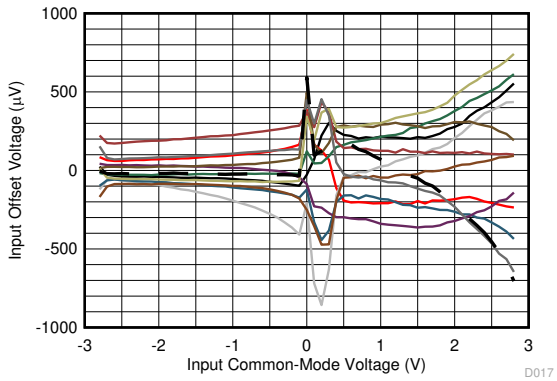
6.10 Typical Characteristics: V_S = 5 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = 0 V, V_{CM}= 1.25 V, R_L = 1 kΩ, output is biased to midsupply, and T_A ≈ 25°C. For AC specifications, V_{S+} = 3.5 V, $V_{S–}$ = –1.5 V, V_{CM}= 0 V, V_O = 2 V_{PP}, G = 2 V/V, R_F = 1 kΩ, and C_L = 4.7 pF (unless otherwise noted)



Output saturated and then short-circuited

図 6-40. Output Short-Circuit Current vs Ambient Temperature

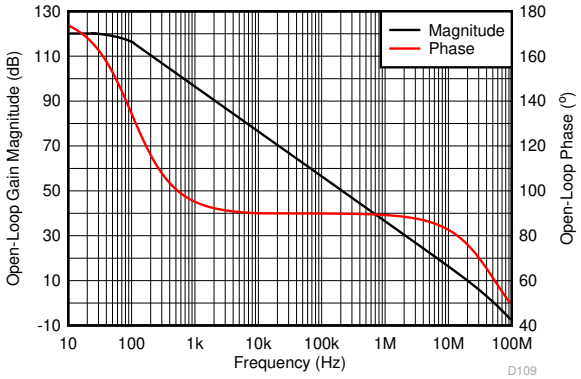


Measured for 12 units

図 6-41. Input Offset Voltage vs Input Common-Mode Voltage

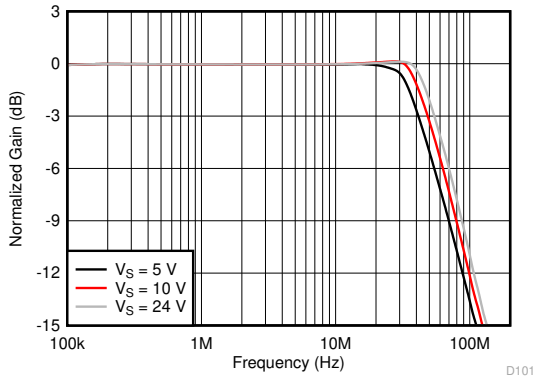
6.11 Typical Characteristics: ±2.375-V to ±12-V Split Supply

at V_O = 2 V_{PP}, R_F = 1 kΩ, R_L = 1 kΩ and T_A ≈ 25°C (unless otherwise noted)



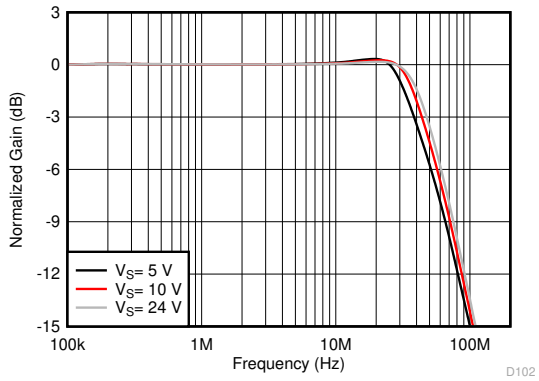
Simulated with no output load

図 6-42. Open-Loop Gain and Phase vs Frequency



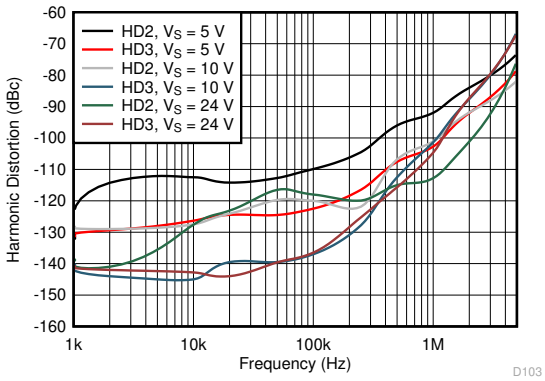
See 図 8-1, gain = 1 V/V, R_F = 0 Ω

図 6-43. Large-Signal Response vs Supply Voltage



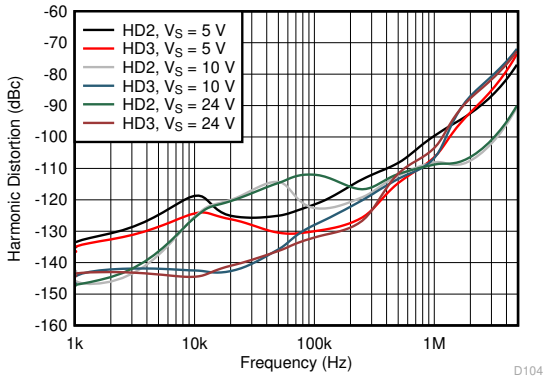
See 図 8-1, gain = 2 V/V

図 6-44. Large-Signal Response vs Supply Voltage



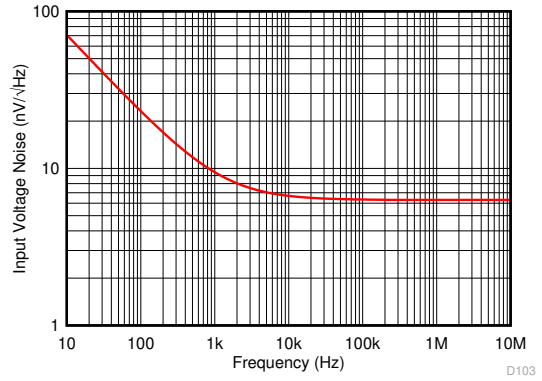
See 図 8-1, gain = 2 V/V

図 6-45. Harmonic Distortion vs Frequency vs Supply Voltage



See 図 8-2, gain = –1 V/V

図 6-46. Harmonic Distortion vs Frequency vs Supply Voltage

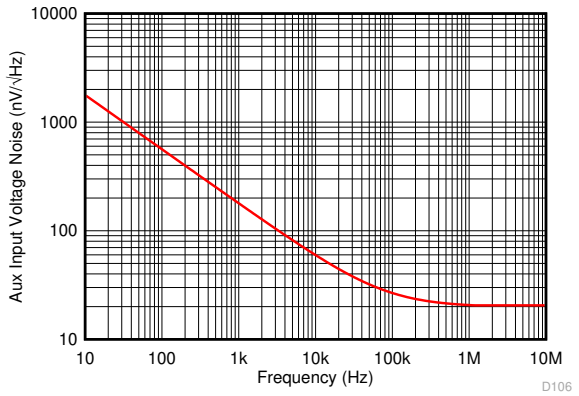


Measured then fit to ideal 1/f model

図 6-47. Input Voltage Noise Density vs Frequency

6.11 Typical Characteristics: ±2.375-V to ±12-V Split Supply (continued)

at V_O = 2 V_{PP}, R_F = 1 kΩ, R_L = 1 kΩ and T_A ≈ 25°C (unless otherwise noted)



Measured then fit to ideal 1/f model

図 6-48. Auxiliary Input Stage Voltage Noise Density vs Frequency

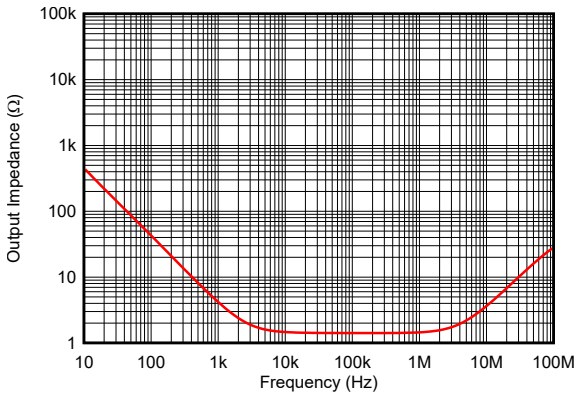
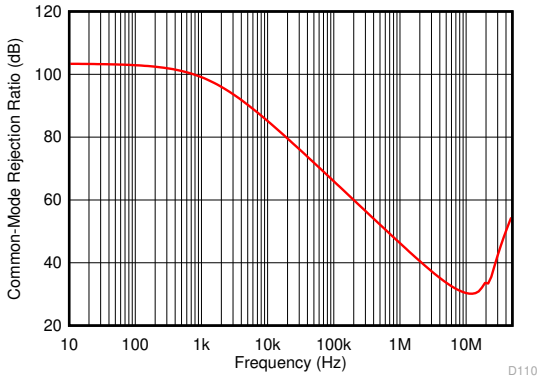
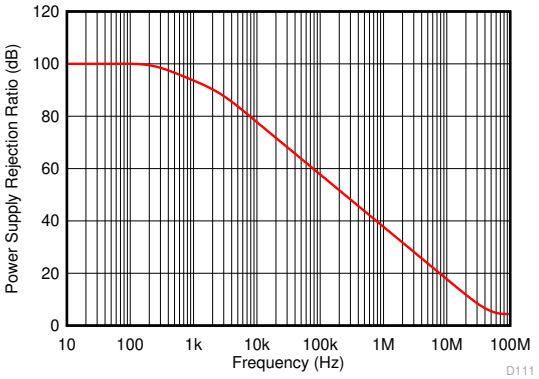


図 6-49. Open-Loop Output Impedance vs Frequency



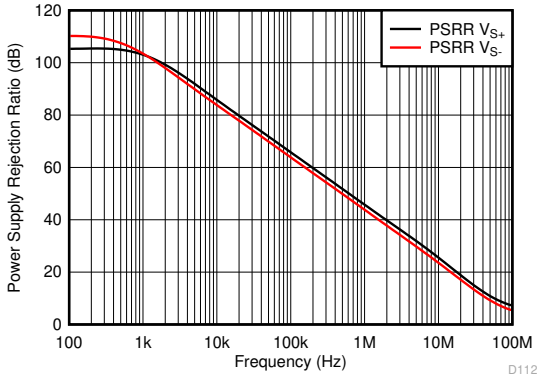
V_S = 10 V and 24 V

図 6-50. Common-Mode Rejection Ratio vs Frequency



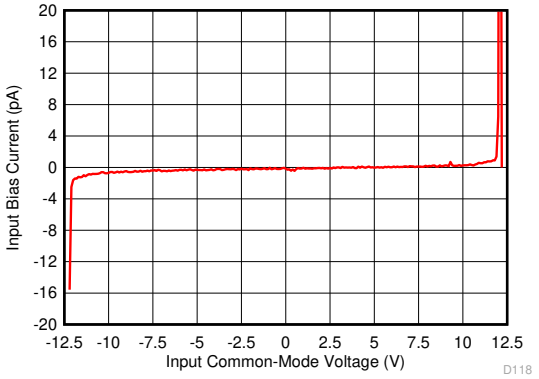
V_S = 5 V and 10 V

図 6-51. Power Supply Rejection Ratio vs Frequency



Simulated curves, V_S = 24 V

図 6-52. Power Supply Rejection Ratio vs Frequency

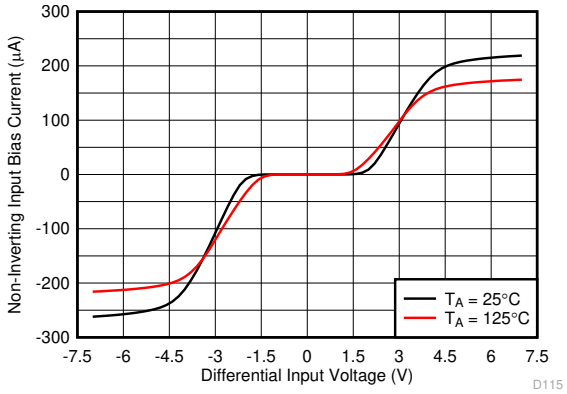


V_S = ±12 V

図 6-53. Input Bias Current vs Input Common-Mode Voltage

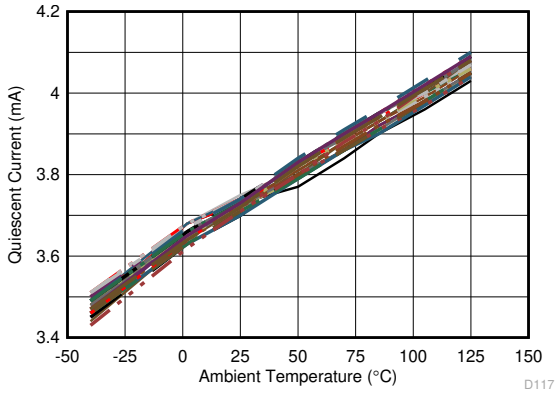
6.11 Typical Characteristics: ±2.375-V to ±12-V Split Supply (continued)

at V_O = 2 V_{PP}, R_F = 1 kΩ, R_L = 1 kΩ and T_A ≈ 25°C (unless otherwise noted)



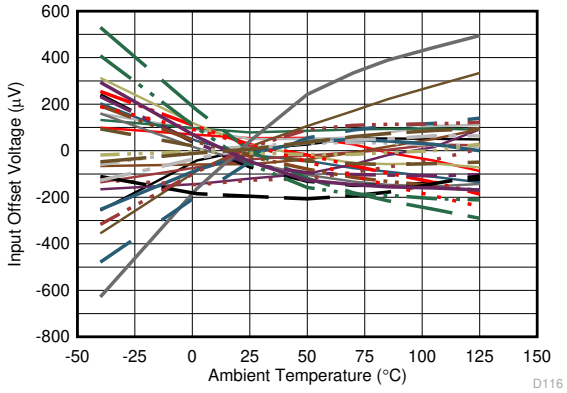
Abs ($V_{IN,Diff\ (max)}$) = V_S when V_S < 7 V

図 6-54. Input Bias Current vs Differential Input Voltage



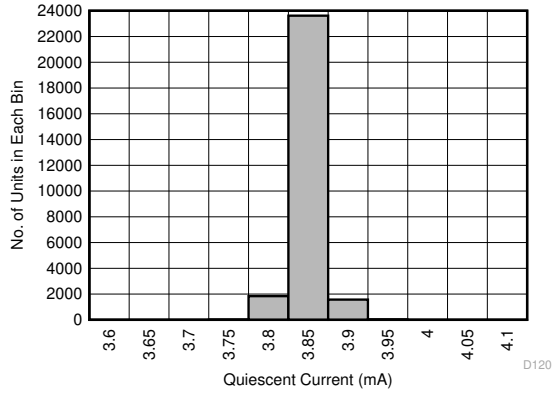
32 units, SOIC package, V_S = ±5 V

図 6-55. Quiescent Current vs Ambient Temperature



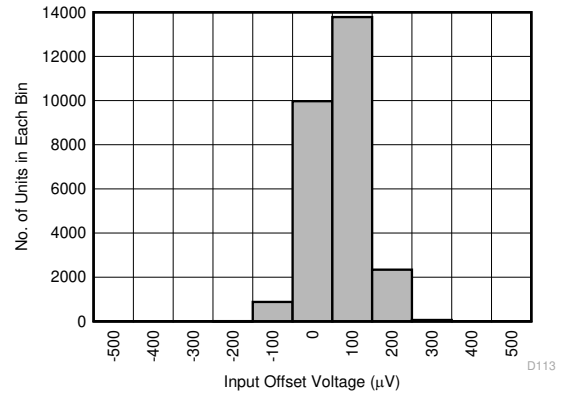
32 units, SOIC package

図 6-56. Input Offset Voltage vs Ambient Temperature



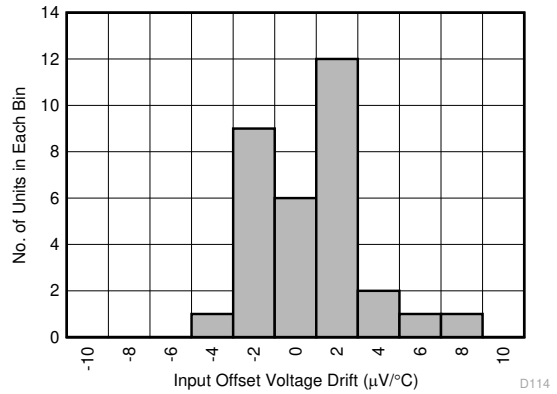
27000 units, µ = 3.82 mA, σ = 17 µA, V_S = 24 V

図 6-57. Quiescent Current Distribution



27000 units, µ = 16 µV, σ = 63 µV, V_S = 24 V

図 6-58. Input Offset Voltage Distribution



–40°C to +125°C fit, 32 units, µ = –0.15 µV/°C, σ = 2.5 µV/°C

図 6-59. Input Offset Voltage Drift Distribution

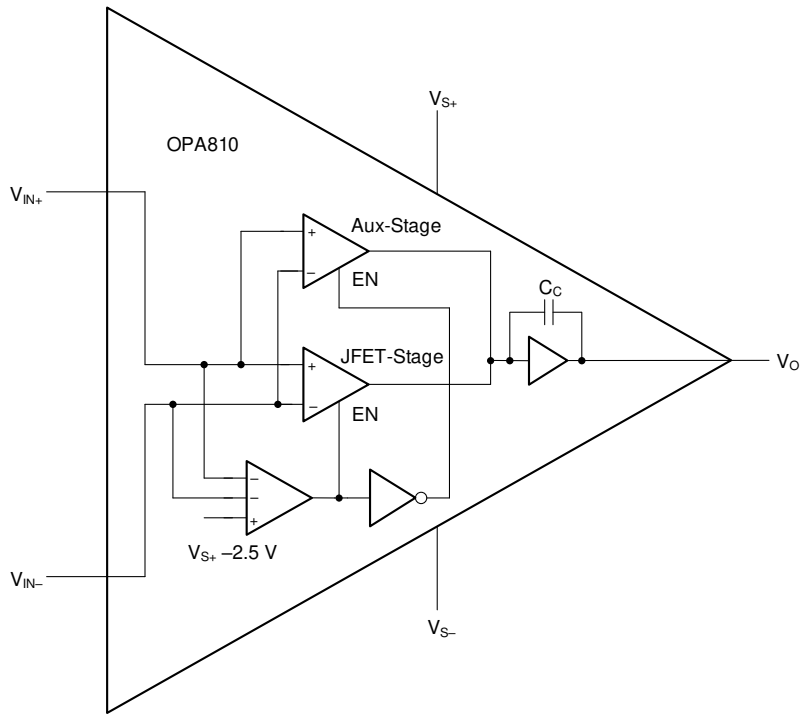
7 Detailed Description

7.1 Overview

The OPA810 is a single-channel, field-effect transistor (FET)-input, unity-gain stable, voltage-feedback operational amplifier with extremely low input bias current across the common-mode input voltage range. The OPA810, characterized to operate over a wide supply range of 4.75 V to 27 V, has a small-signal, unity-gain bandwidth of 140 MHz and offers both excellent dc precision and dynamic ac performance at low quiescent power. The OPA810 is fabricated on Texas Instruments' proprietary, high-speed SiGe BiCMOS process and achieves significant performance improvements over comparable FET-input amplifiers at similar levels of quiescent power. With a gain-bandwidth product (GBWP) of 70 MHz, extremely high slew rate (200 V/µs), and low noise (6.3 nV/√Hz), the OPA810 is designed for a wide range of data-acquisition and signal-processing applications. The OPA810 includes input clamps to allow maximum input differential voltage of up to 7 V, making this device an excellent choice for use with multiplexers and for processing signals with fast transients. The device achieves these benchmark levels of performance while consuming a typical quiescent current (I_Q) of 3.7 mA per channel.

The OPA810 can source and sink large amounts of current without degradation in linearity performance. The wide bandwidth of the OPA810 implies that the device has low output impedance across a wide frequency range, thereby allowing the amplifier to drive capacitive loads up to 10 pF without requiring output isolation. This device is designed for a wide range of data-acquisition, test-and-measurement, front-end buffer, impedance-measurement, power-analyzer, wideband photodiode transimpedance, and signal-processing applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 OPA810 Architecture

The OPA810 features a true high-impedance input stage including a JFET differential-input pair main stage and a CMOS differential-input auxiliary (aux) stage operational within 2.5 V of the positive supply voltage. The bias current is limited to a maximum of 20 pA throughout the common-mode input range of the amplifier. *セクション 7.2* provides a block diagram representation for the input stage of the OPA810. The amplifier exhibits excellent performance for high-speed signals (distortion, noise, and input offset voltage) while the aux stage enables rail-to-rail inputs and prevents phase reversal. The device exhibits a CMRR and PSRR of 75 dB (typical) when the input common-mode is in aux stage.

The OPA810 also includes input clamps that enable the maximum input differential voltage of up to 7 V (lower of 7 V and total supply voltage). This architecture offers significantly greater differential input voltage capability as compared to one to two times the diode forward voltage drop maximum rating in standard amplifiers, and makes this device an excellent choice for use with multiplexers and processing of signals with fast transients. The input bias currents are also clamped to maximum 300 µA, as 図 6-54 shows, which does not load the previous driver stage or require current-limiting resistors (except limiting current through the input ESD diodes when input common-mode voltages are greater than the supply voltages). This feature also enables this amplifier to be used as a comparator in systems that require an amplifier and a comparator for signal gain and fault detection, respectively. For the lowest offset, distortion, and noise performance, limit the common-mode input voltage to the main JFET-input stage (greater than 2.5 V away from the positive supply).

The OPA810 is a rail-to-rail output amplifier and swings to either of the rails at the output (see 図 6-15) for 10-V supply operation. The rail-to-rail output configuration is particularly useful for inputs biased near the rails or when the amplifier is configured in a closed-loop gain such that the output approaches the supply voltage. When the output saturates, the output recovers within 55 ns when the inputs exceed the supply voltages by 0.5 V in an G = –1 V/V inverting gain with a 10–V supply. The outputs are short-circuit protected with the limits of 図 6-16.

As 図 7-1 shows, an amplifier phase margin reduces and becomes unstable when driving a capacitive load (C_L) at the output. Using a series resistor (R_S) between the amplifier output and load capacitance introduces a zero that cancels the pole formed by the amplifier output impedance and C_L in the open-loop transfer function. The OPA810 drives capacitive loads of up to 10 pF without causing instability. Use a series resistor for larger load capacitance values, as 図 6-3 shows for OPA810 configured as a unity-gain buffer. 図 6-4 shows that when used in a gain larger than 1 V/V, the OPA810 is able to drive a load capacitance larger than 10 pF without the need for a series resistor at the output.

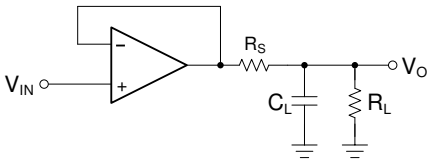


図 7-1. OPA810 Driving Capacitive Load

7.3.2 ESD Protection

As 図 7-2 shows, all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 10-mA continuous input and output currents. The differential input clamps only limit the bias current when the input common-mode voltages are within the supply voltage range, whereas current-limiting series resistors must be added at the inputs if common-mode voltages higher than the supply voltages are possible. Keep these resistor values as low as possible because using high values degrades noise performance and frequency response.

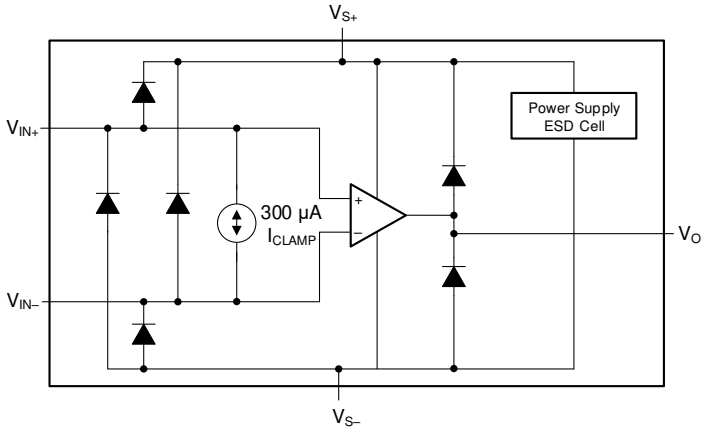


図 7-2. Internal ESD Protection

7.4 Device Functional Modes

7.4.1 Split-Supply Operation (±2.375 V to ±13.5 V)

To facilitate testing with common lab equipment, the OPA810 can be configured to allow for split-supply operation (see the *OPA2810DGK Evaluation Module* user guide). This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers, and other lab equipment reference the inputs and outputs to ground. 図 8-1 depicts the OPA810 configured as a noninverting amplifier and 図 8-2 illustrates the OPA810 configured as an inverting amplifier. For split-supply operation referenced to ground, the power supplies V_{S+} and V_{S-} are symmetrical around ground and V_{REF} is at GND. Split-supply operation is preferred in systems where the signals swing around ground because of the ease-of-use; however, the system requires two supply rails.

7.4.2 Single-Supply Operation (4.75 V to 27 V)

Many newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA810 can be used with a single supply (with the negative supply set to ground) with no change in performance if the input and output are biased within the linear operation of the device. To change the circuit from split supply to a balanced, single-supply configuration, level shift all voltages by half the difference between the power-supply rails. An additional advantage of configuring an amplifier for single-supply operation is that the effects of PSRR are minimized because the low-supply rail is grounded. See the *Single-Supply Op Amp Design Techniques* application report for examples of single-supply designs.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Amplifier Gain Configurations

The OPA810 is a classic voltage-feedback amplifier with each channel having two high-impedance inputs and a low-impedance output. Standard application circuits (as shown in 図 8-1 and 図 8-2) include the noninverting and inverting gain configurations. The DC operating point for each configuration is level-shifted by the reference voltage V_{REF} that is typically set to midsupply in single-supply operation. V_{REF} is often connected to ground in split-supply applications.

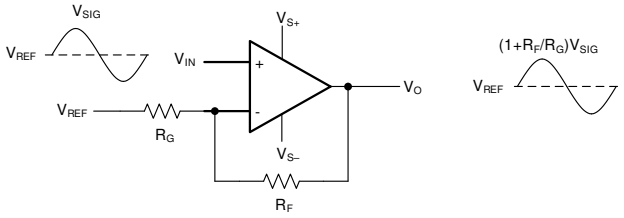


図 8-1. Noninverting Amplifier

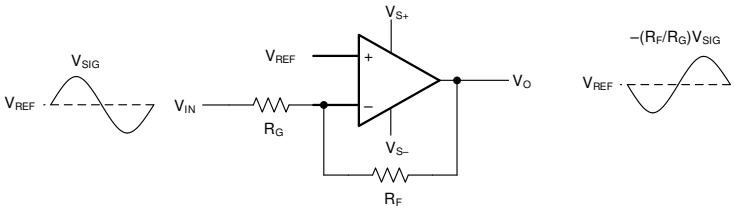


図 8-2. Inverting Amplifier

Equation 1 shows the closed-loop gain of an amplifier in a noninverting configuration.

$$V_O = V_{IN}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \quad (1)$$

Equation 2 shows the closed-loop gain of an amplifier in an inverting configuration.

$$V_O = V_{IN}\left(-\frac{R_F}{R_G}\right) + V_{REF} \quad (2)$$

8.1.2 Selection of Feedback Resistors

The OPA810 is a classic voltage-feedback amplifier with each channel having two high-impedance inputs and a low-impedance output. Standard application circuits (as shown in 図 8-3 and 図 8-4) include the noninverting and inverting gain configurations. The dc operating point for each configuration is level-shifted by the reference voltage V_{REF} which is typically set to midsupply in single-supply operation. V_{REF} is often connected to ground in split-supply applications.

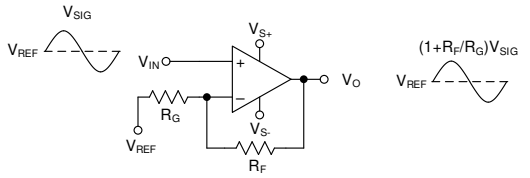


図 8-3. Noninverting Amplifier

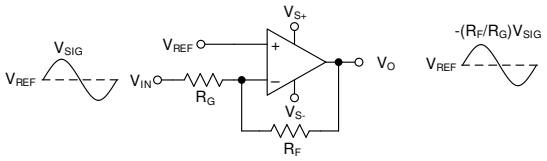


図 8-4. Inverting Amplifier

Equation 3 shows the closed-loop gain of an amplifier in noninverting configuration.

$$V_O = V_{IN}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \tag{3}$$

Equation 4 shows the closed-loop gain of an amplifier in an inverting configuration.

$$V_O = V_{IN}\left(-\frac{R_F}{R_G}\right) + V_{REF} \tag{4}$$

The magnitude of the low-frequency gain is determined by the ratio of the magnitudes of the feedback resistor (R_F) and the gain setting resistor R_G. The order of magnitudes of the individual values of R_F and R_G offer a trade-off between amplifier stability, power dissipated in the feedback resistor network, and total output noise. The feedback network increases the loading on the amplifier output. Using large values of the feedback resistors reduces the power dissipated at the amplifier output. Conversely, large feedback-resistor values increase the inherent voltage and amplifier current noise contribution seen at the output while lowering the frequency at which a pole occurs in the feedback factor (β). This pole causes a decrease in the phase margin at zero-gain crossover frequency and potential instability. Using small feedback resistors increases power dissipation and also degrades amplifier linearity due to a heavier amplifier output load. 図 8-5 illustrates a representative schematic of the OPA810 in an inverting configuration with the input capacitors shown.

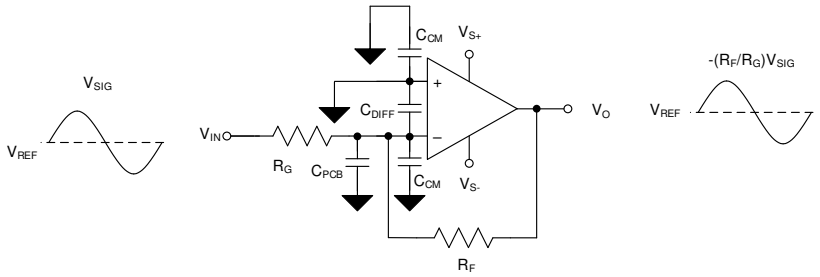


図 8-5. Inverting Amplifier With Input Capacitors

The effective capacitance at the amplifier inverting input pin is shown in Equation 5, which forms a pole in β at a cut-off frequency of Equation 6.

$$C_{IN} = C_{CM} + C_{DIFF} + C_{PCB} \tag{5}$$

where

- C_{CM} is the amplifier common-mode input capacitance
- C_{DIFF} is the amplifier differential input capacitance
- C_{PCB} is the printed circuit board (PCB) parasitic capacitance

$$F_C = \frac{1}{2\pi R_F C_{IN}} \tag{6}$$

For low-power systems, greater the values of the feedback resistors, the earlier in frequency does the phase margin begin to reduce and cause instability. 図 8-6 and 図 8-7 illustrate the loop gain magnitude and phase plots, respectively, for the OPA810 simulation in TINA-TI configured as an inverting amplifier with values of feedback resistors varying by orders of magnitudes.

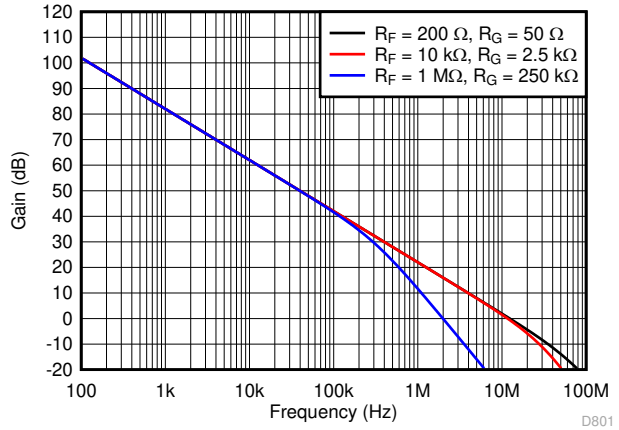


図 8-6. Loop-Gain vs Frequency for Circuit of 図 8-5

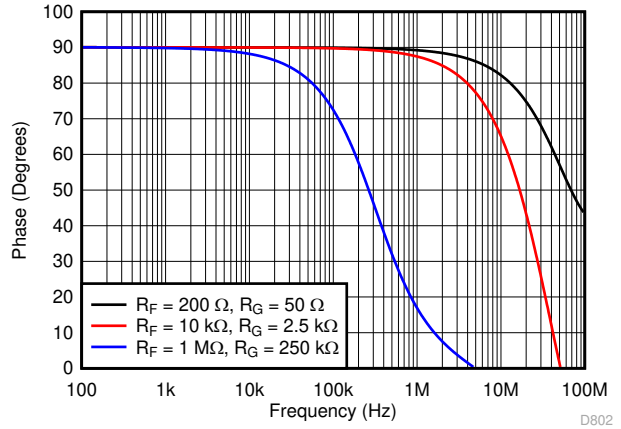


図 8-7. Loop-Gain Phase vs Frequency for Circuit of 図 8-5

A lower phase margin results in peaking in the frequency response and lower bandwidth as 図 8-8 shows, which is synonymous with overshoot and ringing in the pulse response results. The OPA810 offers a flat-band voltage noise density of 6.3 nV/√Hz. TI recommends selecting an R_F so the voltage noise contribution does not exceed that of the amplifier. 図 8-9 shows the voltage noise density variation with value of resistance at 25°C. A 2-kΩ resistor exhibits a thermal noise density of 5.75 nV/√Hz which is comparable to the flat-band noise of the

OPA810. Therefore, use an R_F less than 2 kΩ while still large enough to not dissipate excessive power for the output voltage swing and supply current requirements of the application. The *セクション 8.1.3* section shows a detailed analysis of the various contributors to noise.

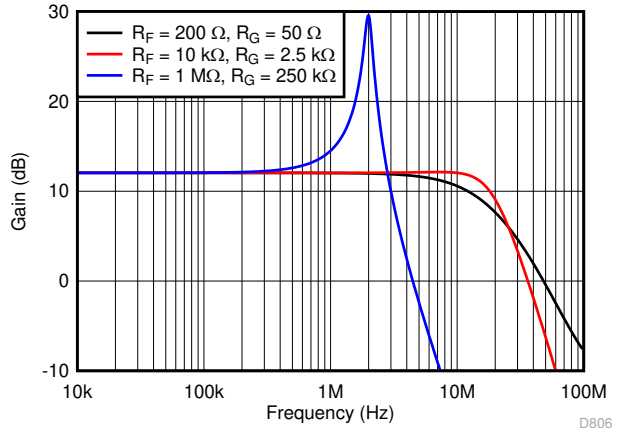


図 8-8. Closed-Loop Gain vs. Frequency for Circuit of 図 8-5

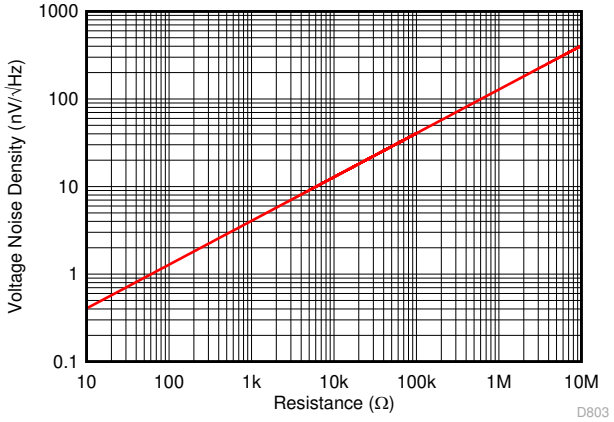


図 8-9. Thermal Noise Density vs Resistance

8.1.3 Noise Analysis and the Effect of Resistor Elements on Total Noise

The OPA810 provides a low input-referred broadband noise voltage density of 6.3 nV/√ Hz while requiring a low 3.7-mA quiescent supply current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. 図 8-10 shows the operational amplifier noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in nV/√ Hz or pA/√ Hz.

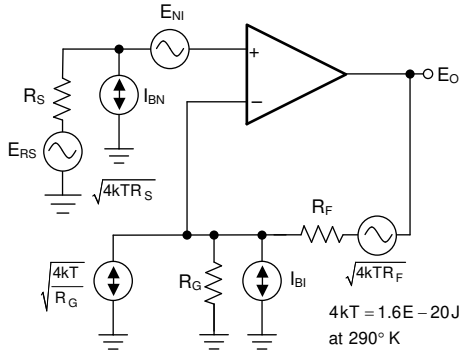


図 8-10. Operational Amplifier Noise Analysis Model

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation adds all the contributing noise powers at the output by superposition, then calculates the square root to get back to a spot noise voltage. 図 8-10 shows the general form for this output noise voltage using the terms shown in Equation 7.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (7)$$

Dividing this expression by the noise gain (NG = 1 + R_F / R_G) shows the equivalent input referred spot noise voltage at the noninverting input; see Equation 8.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (8)$$

Substituting large resistor values into Equation 8 can quickly dominate the total equivalent input referred noise. A source impedance on the noninverting input of 2-kΩ adds a Johnson voltage noise term similar to that of the amplifier (6.3 nV/√Hz).

表 8-1 compares the noise contributions from the various terms when the OPA810 is configured in a noninverting gain of 5 V/V as 図 8-11 shows. Two cases are considered where the resistor values in case 2 are 10x the resistor values in case 1. The total output noise in case 1 is 34 nV/√Hz while the noise in case 2 is 51.5 nV/√Hz. The large value resistors in case 2 dilute the benefits of selecting a low noise amplifier like the OPA810. To minimize total system noise, reduce the size of the resistor values. This increases the amplifiers output load and results in a degradation of distortion performance. The increased loading increases the dynamic power consumption of the amplifier. The circuit designer must make the appropriate tradeoffs to maximize the overall performance of the amplifier to match the system requirements.

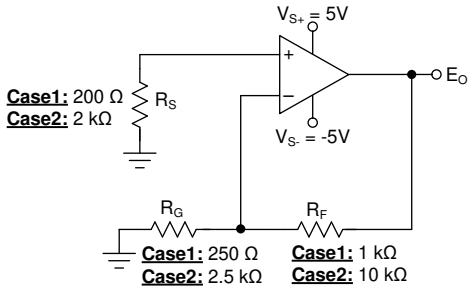


図 8-11. Comparing Noise Contributors for Two Cases with the Amplifier in a Noninverting Gain of 5 V/V

表 8-1. Comparing Noise Contributions for the Circuit in 図 8-11

NOISE SOURCE	OUTPUT NOISE EQUATION	CASE 1				CASE 2			
		NOISE SOURCE VALUE	VOLTAGE NOISE CONTRIBUTION (nV/√Hz)	NOISE POWER CONTRIBUTION (nV^2/Hz)	CONTRIBUTION (%)	NOISE SOURCE VALUE	VOLTAGE NOISE CONTRIBUTION (nV/√Hz)	NOISE POWER CONTRIBUTION (nV^2/Hz)	CONTRIBUTION (%)
Source resistor, R_S	E_{RS} (1 + R_F /R_G)	1.82 nV/√Hz	9.1	82.81	7.15	5.76 nV/√Hz	28.8	829.44	31.29
Gain resistor, R_G	E_{RG} (R_F / R_G)	2.04 nV/√Hz	8.16	66.59	5.75	6.44 nV/√Hz	25.76	663.58	25.03
Feedback resistor, R_F	E_{RF}	4.07 nV/√Hz	4.07	16.57	1.43	12.87 nV/√Hz	12.87	165.64	6.25
Amplifier voltage noise, E_{NI}	E_{NI} (1 + R_F / R_G)	6.3 nV/√Hz	31.5	992.25	85.67	6.3 nV/√Hz	31.5	992.25	37.43
Inverting current noise, I_{BI}	I_{BI} (R_F || R_G)	5 fA/√Hz	5.0E-3	—	—	5 fA/√Hz	50E-3	—	—
Noninverting current noise, I_{BN}	$I_{BN}R_S$ (1 + R_F/ R_G)	5 fA/√Hz	1.0E-3	—	—	5 fA/√Hz	10E-3	—	—

8.2 Typical Applications

8.2.1 Transimpedance Amplifier

The high GBWP and low input voltage and current noise for the OPA810 make this device an excellent wideband transimpedance amplifier for moderate to high transimpedance gains.

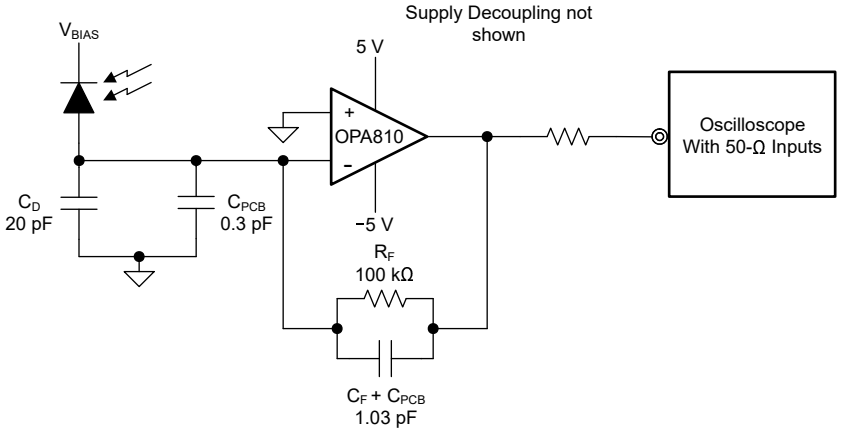


図 8-12. Wideband, High-Sensitivity, Transimpedance Amplifier

8.2.1.1 Design Requirements

表 8-2 lists the design requirements for a high-bandwidth, high-gain transimpedance amplifier circuit.

表 8-2. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Target bandwidth	> 2 MHz
Transimpedance gain	100 kΩ
Photodiode capacitance	20 pF

8.2.1.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low input voltage noise of the OPA810. This input voltage noise is peaked up over frequency by the diode source capacitance, and can (in many cases) become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage (V_{BIAS}) applied, the desired transimpedance gain, R_F, and the GBWP for the OPA810 (70 MHz). 図 8-12 shows a transimpedance circuit with the parameters as described in 表 8-2. With these three variables set (and including the parasitic input capacitance for the OPA810 and the printed circuit board (PCB) added to C_D), the feedback capacitor value (C_F) can be set to control the frequency response. The *Transimpedance Considerations for High-Speed Amplifiers* application report discusses using high-speed amplifiers for transimpedance applications. Set the feedback pole according to Equation 9 to achieve a maximally-flat second-order Butterworth frequency response:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBWP}{4\pi R_F C_D}} \tag{9}$$

The input capacitance of the amplifier is the sum of the common-mode and differential capacitance (2.0 + 0.5) pF. The parasitic capacitance from the photodiode package and the PCB is approximately 0.3 pF. Using Equation 5 gives a total input capacitance of C_D = 22.8 pF. From Equation 9, set the feedback pole at 1.55 MHz. Setting the pole at 1.55 MHz requires a total feedback capacitance of 1.03 pF.

Equation 10 shows the approximate –3-dB bandwidth of the transimpedance amplifier circuit:

$$f_{-3dB} = \sqrt{GBWP / (2\pi R_F C_D)} Hz \quad (10)$$

Equation 10 estimates a closed-loop bandwidth of 2.19 MHz. 図 8-13 and 図 8-14 show the loop-gain magnitude and phase plots from the TINA-TI simulations of the transimpedance amplifier circuit of 図 8-12. The 1/β gain curve has a zero from R_F and C_{IN} at 70 kHz and a pole from R_F and C_F canceling the 1/β zero at 1.5 MHz, resulting in a 20-dB per decade rate-of-closure at the loop-gain crossover frequency (the frequency where A_{OL} equals 1/β), providing a stable circuit. A phase margin of 62° is obtained with a closed-loop bandwidth of 3 MHz and a 100-kΩ transimpedance gain.

8.2.1.3 Application Curves

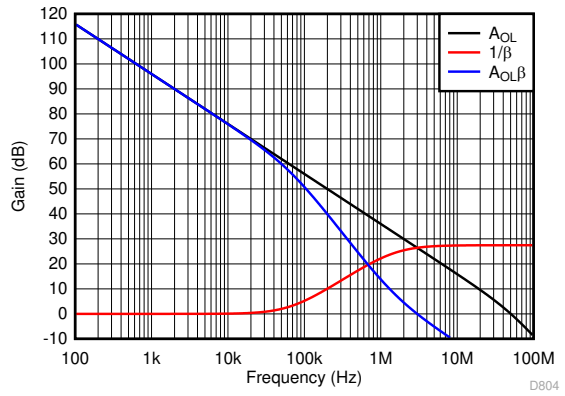


図 8-13. Loop-Gain Magnitude vs Frequency for the Transimpedance Amplifier Circuit of 図 8-12

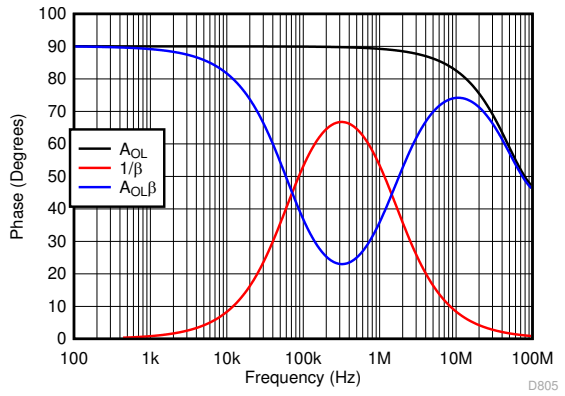


図 8-14. Loop-Gain Phase vs Frequency for the Transimpedance Amplifier Circuit of 図 8-12

8.2.2 High-Z Input Data Acquisition Front-End

An ideal data acquisition system must measure a parameter without altering the measurand. When measuring a voltage or current from sensors with a large output impedance, an extremely high input impedance front-end with a pA range bias current is needed. 図 8-15 shows an example circuit with the OPA810 used at the front-end. For systems with large input voltage attenuated with the MΩ range resistor divider, the OPA810 with pA range bias currents adds negligible offset voltage and distortion because of the bias current induced resistor voltage drops. This circuit shows a funneling architecture with the OPA810 FET-input amplifier used as a unity-gain buffer, followed by attenuation to the ADS9110 5-V, full-scale input range and the ADC input drive using the THS4561 fully-differential amplifier (FDA). The THS4561 helps achieve better SNR and ENOB than a similar 5-V FDA, with a higher 12.6-V supply voltage and signal swings up to the ADC full-scale input range.

As a result of the capacitive switching and current inrush on the ADC VREF input pin, a wide bandwidth amplifier such as the OPA837 is used with the OPA378 in a composite loop as a reference buffer. The OPA378, driven from the REF5050 5-V voltage reference, offers high precision and the OPA837 gives fast-settling performance for the ADC reference input drive. See the *Reference Design Maximizing Signal Dynamic Range for True 10 Vpp Differential Input to 20 bit ADC* design guide for more a detailed analysis of this high-Z front-end.

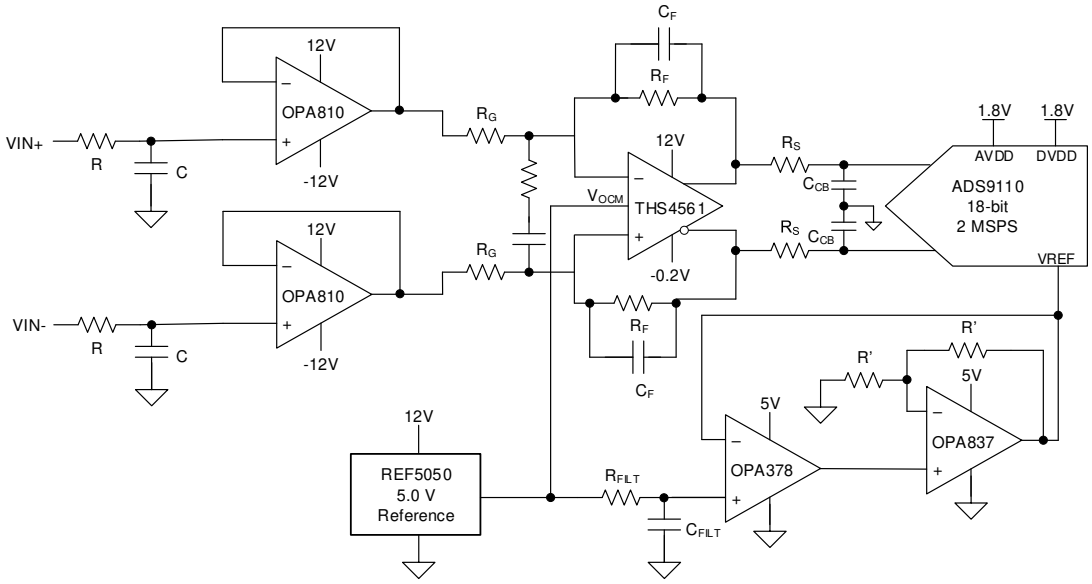


図 8-15. High-Z Input Data Acquisition Front-End

8.2.3 Multichannel Sensor Interface

High-Z input amplifiers are particularly useful when interfaced with sensors that have relatively high output impedance. Such multichannel systems usually interface these sensors with the signal chain through a multiplexer. 図 8-16 shows one such implementation using an amplifier for the interface with each sensor, and driving into an ADC through a multiplexer. An alternate circuit, shown in 図 8-17, can use a single higher GBWP and fast-settling amplifier at the output of the multiplexer. This architecture gives rise to large signal transients when switching between channels, where the settling performance of the amplifier and maximum allowed differential input voltage limits signal chain performance and amplifier reliability, respectively.

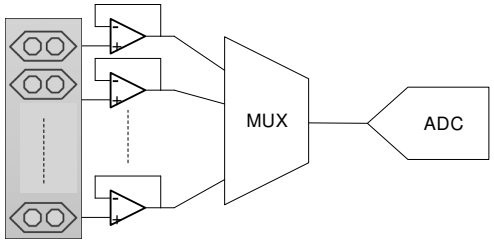


図 8-16. Multichannel Sensor Interface Using Multiple Amplifiers

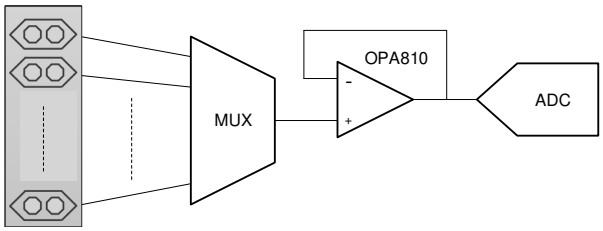


図 8-17. Multichannel Sensor Interface Using a Single Higher GBWP Amplifier

図 8-18 shows the output voltage and input differential voltage when a 8-V step is applied at the noninverting terminal of the OPA810 configured as a unity-gain buffer of 図 8-17.

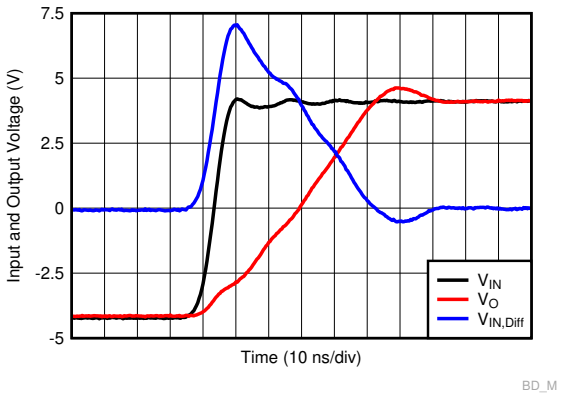


図 8-18. Large-Signal Transient Response Using the OPA810

Because of the fast input transient, the amplifier is slew-limited and the inputs cease to track each other (a maximum $V_{IN,Diff}$ of 7 V is shown in 図 8-18) until the output reaches the final value and the negative feedback loop is closed. For standard amplifiers with a 0.7-V to 1.5-V maximum $V_{IN,Diff}$ rating, current-limiting resistors must be used in series with the input pins to protect the device from irreversible damage, which also limits the device frequency response. The OPA810 has built-in input clamps that allow the application of as much as 7 V of $V_{IN,Diff}$, with no external resistors required and no damage to the device or a shift in performance specifications.

Such an input-stage architecture, coupled with the fast settling performance, makes the OPA810 a good fit for multichannel sensor multiplexed systems.

8.3 Power Supply Recommendations

The OPA810 is intended for operation on supplies ranging from 4.75 V to 27 V. The OPA810 can be operated on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply can have numerous advantages. With the negative supply at ground, the DC errors resulting from the –PSRR term can be minimized. Typically, AC performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance (< 0.1 in) from the power-supply pins to high-frequency, 0.01-µF decoupling capacitors. A larger capacitor (2.2 µF typical) is used along with a high-frequency, 0.01-µF, supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors from each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

8.4 Layout

8.4.1 Layout Guidelines

Achieving optimized performance with a high-frequency amplifier such as the OPA810 requires careful attention to board layout parasitics and external component types. The *OPA2810EVM* can be used as a reference when designing the circuit board. Recommendations that optimize performance include:

1. **Minimize parasitic capacitance** to any ac ground for all signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, this capacitance can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1 in) from the power-supply pins to high-frequency, 0.01-µF decoupling capacitors. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Always decouple the power-supply connections with these capacitors. Use larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, on the supply pins. Place these capacitors somewhat farther from the device and share these capacitors among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserve the high-frequency performance of the OPA810.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values greater than 10 kΩ, this parasitic capacitance can add a pole or zero close to the GBWP of 70 MHz and subsequently affects circuit operation. Keep resistor values as low as possible and consistent with load driving considerations. Lowering the resistor values keeps the resistor noise terms low, and minimizes the effect of parasitic capacitance, however lower resistor values increase the dynamic power consumption because R_F and R_G become part of the amplifiers output load network. Transimpedance applications (see the *セクション 8.2.1* section) can use whatever feedback resistor is required by the application as long as the feedback compensation capacitor is set considering all parasitic capacitance terms on the inverting node.

4. **Connections to other wideband devices** on the board can be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S for sufficient phase margin and stability. Low parasitic capacitive loads (< 10 pF) do not always require an R_S because the OPA810 is nominally compensated to operate with a 10-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed with increase in signal gain (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and a higher impedance environment improves distortion. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA810 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device—this total effective impedance must be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value to obtain sufficient phase margin and stability. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, the signal attenuates because of the voltage divider formed by the series output into the terminating impedance.
5. **Take care to design the PCB layout for optimized thermal dissipation.** For the extreme case of 125°C operating ambient, using the approximate 134.8°C/W for the SOIC package, and an internal power of 24-V supply × 4.7-mA 125°C supply current gives a maximum internal power dissipation of 113 mW. This power gives a 15°C increase from ambient to junction temperature. Load power adds to this value and this dissipation must also be calculated to determine the worst-case safe operating point.
6. **Socketing a high-speed device such as the OPA810 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can almost make achieving a smooth, stable frequency response impossible. Best results are obtained by soldering the OPA810 onto the board.

8.4.1.1 Thermal Considerations

The OPA810 does not require a heat sink or airflow in most applications. Maximum allowed junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load, but for a grounded resistive load, is at a maximum when the output is fixed at a voltage equal to half of either supply voltage (for equal split-supplies). Under this condition, $P_{DL} = V_S{}^2 / (4 \times R_L)$ where R_L includes feedback network loading.

The power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using a DCK (SC70 package) configured as a unity gain buffer, operating on ±12-V supplies at an ambient temperature of 25°C and driving a grounded 500-Ω load.

$P_D = 24\ V \times 4.7\ mA + 12^2 / (4 \times 500\ \Omega) = 184.8\ mW$

Maximum $T_J = 25°C + (0.185\ W \times 190.8°C/W) = 60°C$, which is much less than the maximum allowed junction temperature of 150°C.

8.4.2 Layout Example

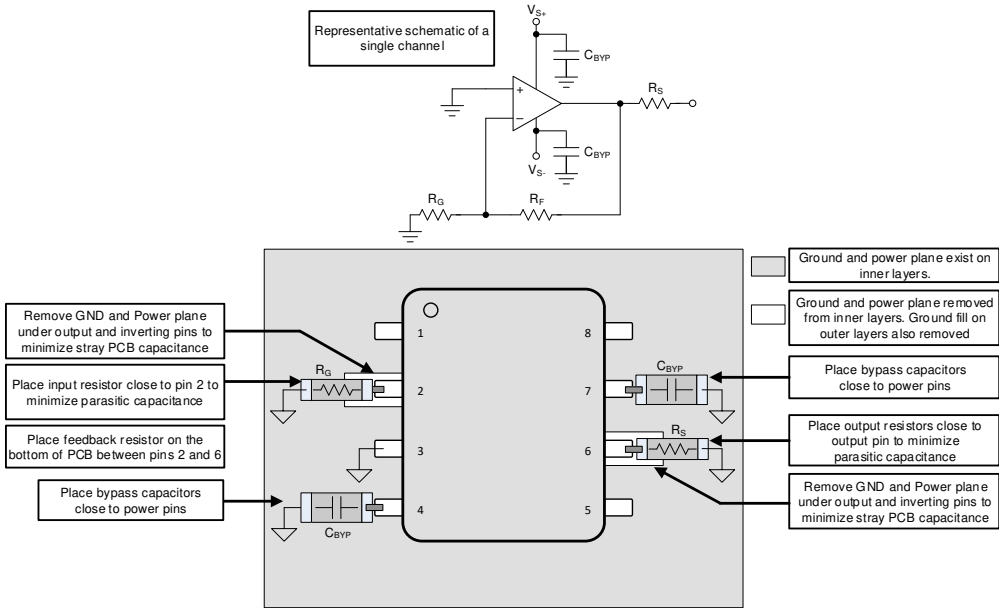


図 8-19. Layout Recommendation

9 Device and Documentation Support

9.1 サード・パーティ製品に関する免責事項

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA2810 Dual-Channel, 27-V, Rail-to-Rail Input/Output FET-Input Operational Amplifier* data sheet.
- Texas Instruments, *ADS9110 18-Bit, 2-MSPS, 15-mW, SAR ADC With Enhanced Performance Features* data sheet
- Texas Instruments, *THS4561 Low-Power, High Supply Range, 70-MHz, Fully Differential Amplifier* data sheet
- Texas Instruments, *OPAx837 Low-Power, Precision, 105-MHz, Voltage-Feedback Op Amp* data sheet
- Texas Instruments, *OPAx378 Low-Noise, 900kHz, RRIO, Precision Operational Amplifier Zerø-Drift Series* data sheet
- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *OPA2810DGK Evaluation Module* user's guide
- Texas Instruments, *Single-Supply Op Amp Design Techniques* application report
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report
- Texas Instruments, *Blog: What you need to know about transimpedance amplifiers – part 1*
- Texas Instruments, *Blog: What you need to know about transimpedance amplifiers – part 2*
- Texas Instruments, *Noise Analysis for High-Speed Op Amps* application report
- Texas Instruments, *TINA model and simulation tool*
- Texas Instruments, *TIDA-01057 Reference Design Maximizing Signal Dynamic Range for True 10 Vpp Differential Input to 20 bit ADC*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (August 2020) to Revision E (August 2024) **Page**

- 「パッケージ情報」表を更新し、新しい注 2 を追加 1
- Updated table note 1 in *Absolute Maximum Ratings* 4
- Updated CDM specification text in *ESD Ratings* 4
- Updated Figure 6-49, *Open-Loop Output Impedance vs Frequency*, with corrected data 19

Changes from Revision C (July 2020) to Revision D (August 2020) **Page**

- 選択的公開ヘッダーを削除し、ページ 1 に上部ナビゲーション ヘッダーを追加 1

Changes from Revision B (June 2020) to Revision C (July 2020) **Page**

- DCK パッケージのステータスを次のように変更：*プレビュー*から*量産出荷中* 1

Changes from Revision A (December 2019) to Revision B (June 2020) **Page**

- DBV パッケージのステータスを次のように変更：*プレビュー*から*量産出荷中* 1
- Added noise corner information to 10 V, 24 V and 5 V electrical characteristics tables 5
- Changed offset voltage test conditions for 10 V, 24 V and 5 V supplies for SOIC, SOT23 and SC70 packages 5
- Updated Figure 62. Noninverting Amplifier 25

Changes from Revision * (August 2019) to Revision A (December 2019) **Page**

- ドキュメントのステータスを次のように変更：「事前情報」から*「量産データ」* 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA810IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1ZQ5
OPA810IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1ZQ5
OPA810IDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1ZQ5
OPA810IDBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1ZQ5
OPA810IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1ZQ5
OPA810IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1ZQ5
OPA810IDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1GG
OPA810IDCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1GG
OPA810IDCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1GG
OPA810IDCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1GG
OPA810IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	810
OPA810IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	810
OPA810IDT	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	810
OPA810IDT.B	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	810

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA810 :

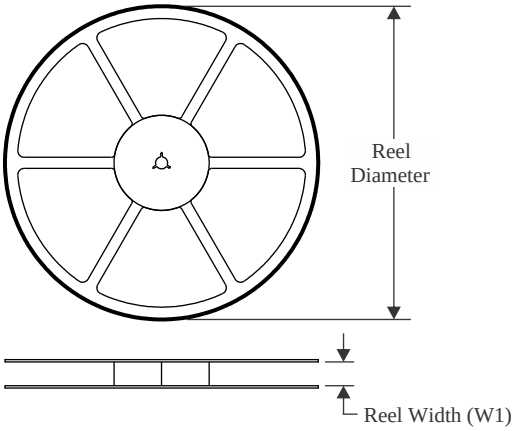
- Automotive : OPA810-Q1

NOTE: Qualified Version Definitions:

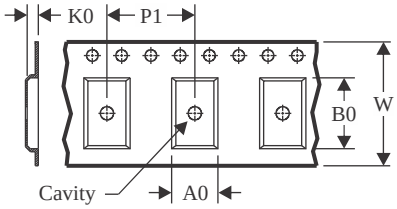
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

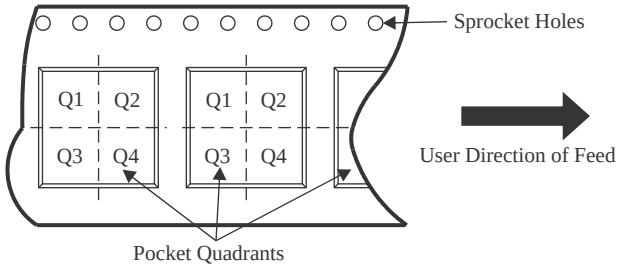


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

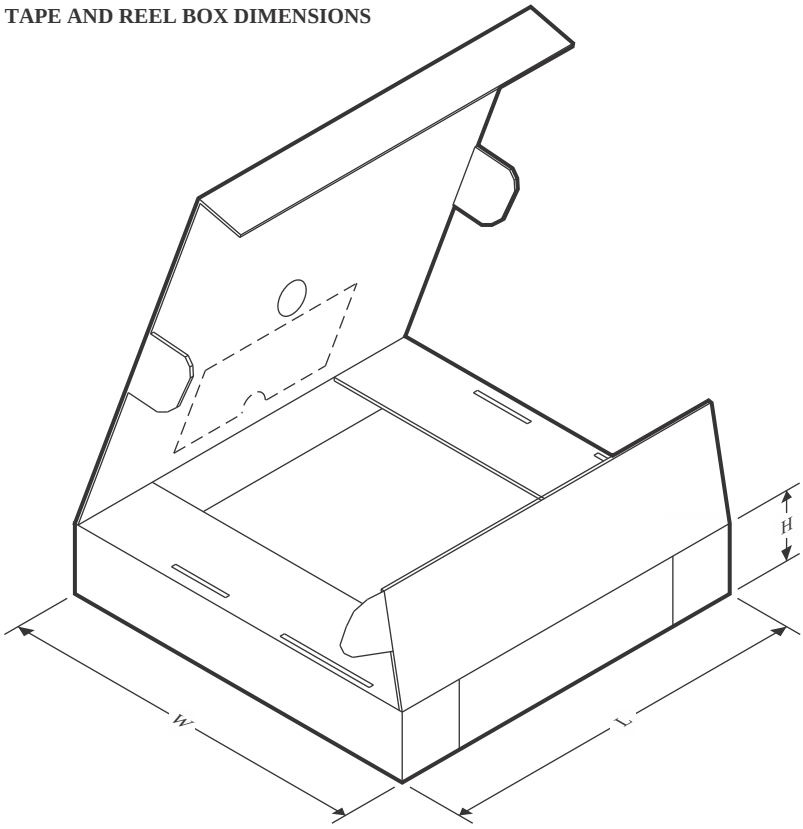
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA810IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA810IDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA810IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA810IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA810IDCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
OPA810IDCKRG4	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
OPA810IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA810IDT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

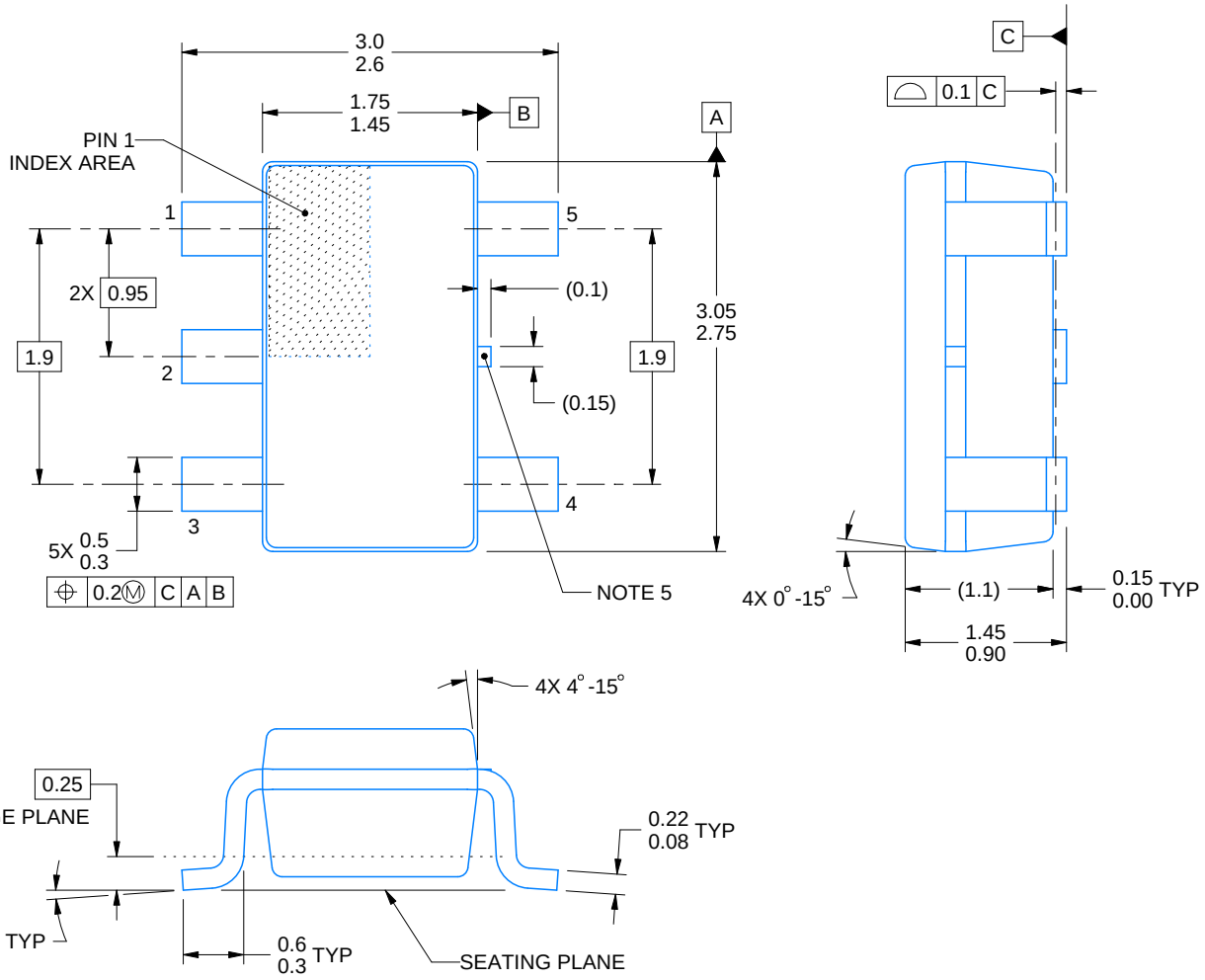
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA810IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA810IDBVRG4	SOT-23	DBV	5	3000	190.0	190.0	30.0
OPA810IDBVT	SOT-23	DBV	5	250	190.0	190.0	30.0
OPA810IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA810IDCKR	SC70	DCK	5	3000	213.0	191.0	35.0
OPA810IDCKRG4	SC70	DCK	5	3000	213.0	191.0	35.0
OPA810IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA810IDT	SOIC	D	8	250	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

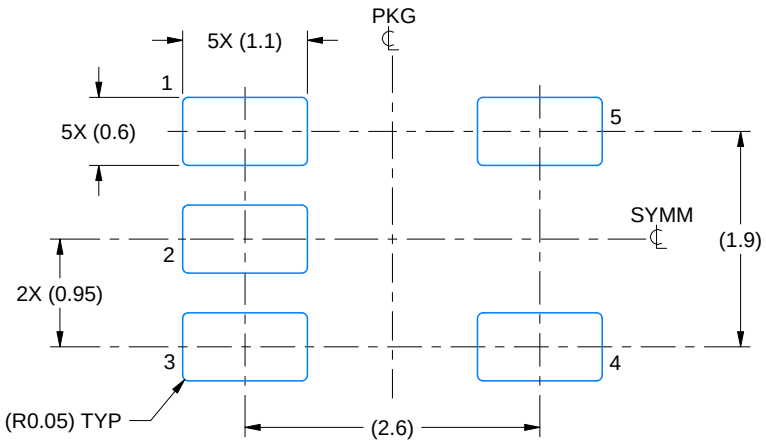
SMALL OUTLINE TRANSISTOR



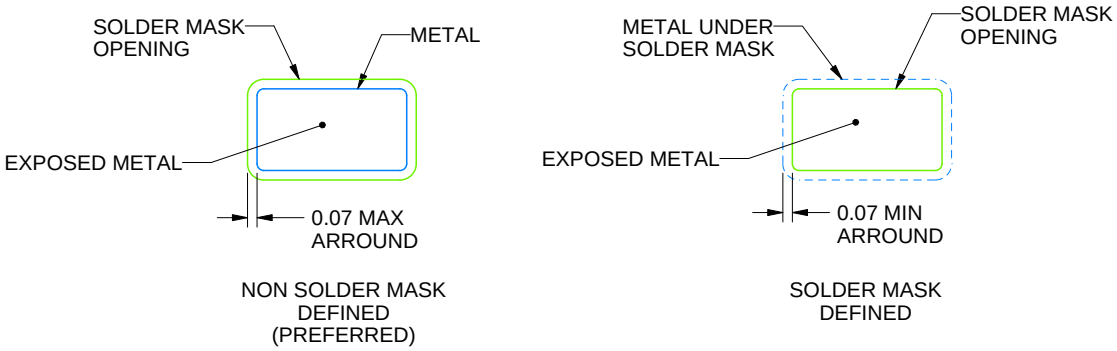
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

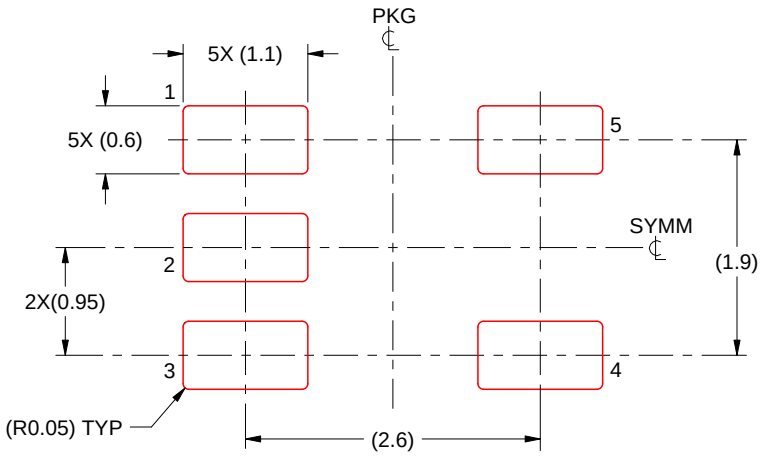


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

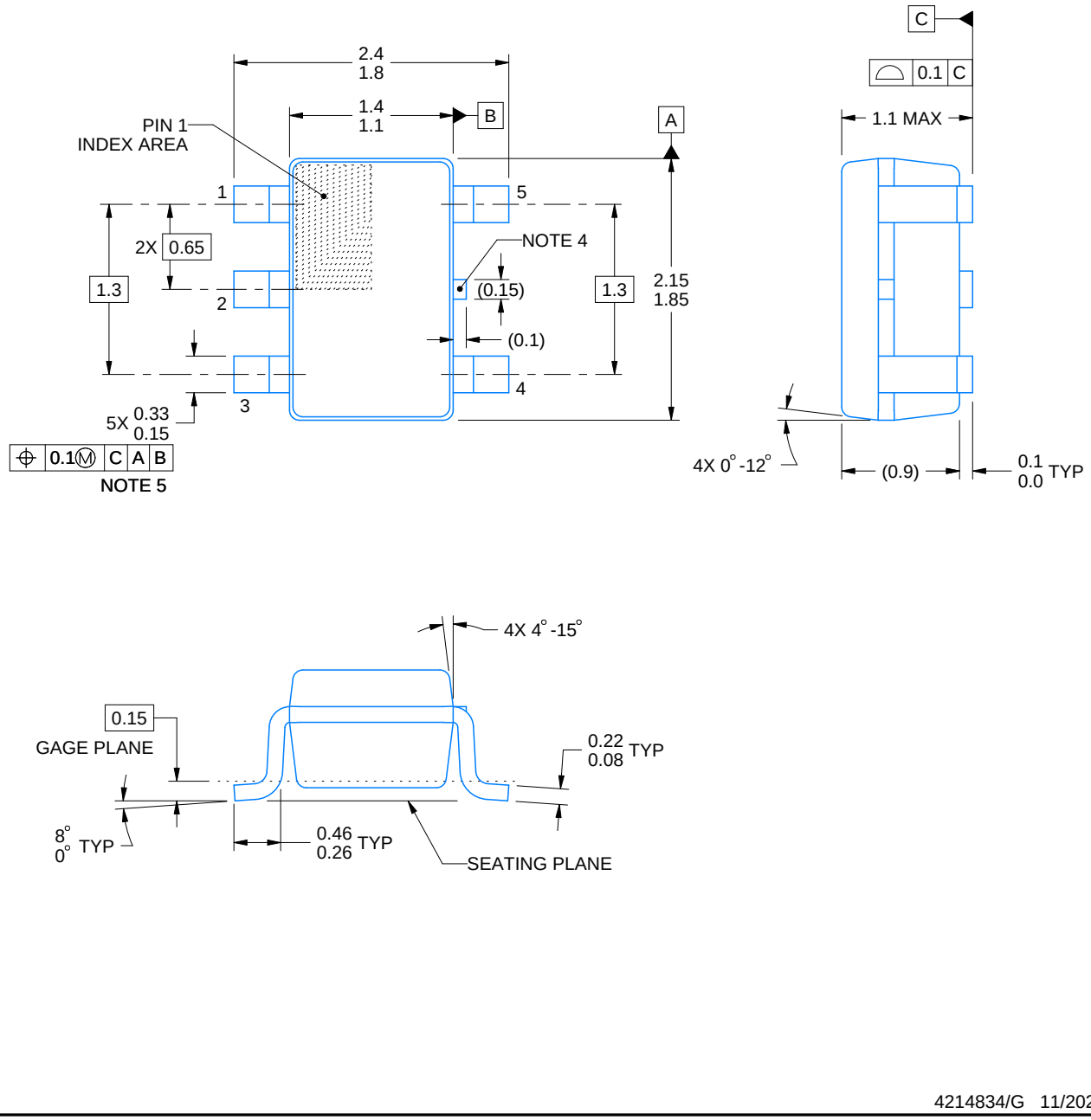
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

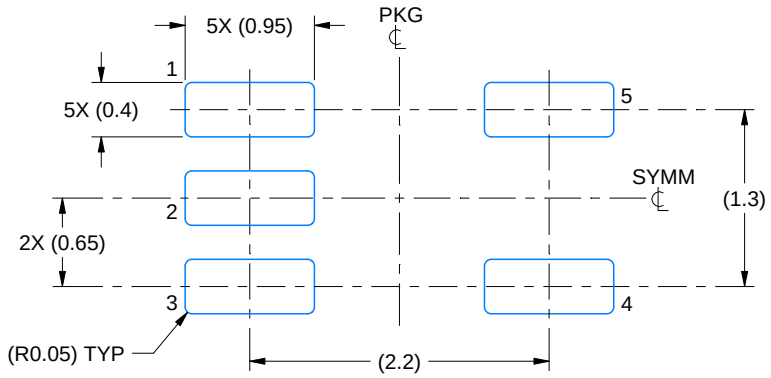
SMALL OUTLINE TRANSISTOR



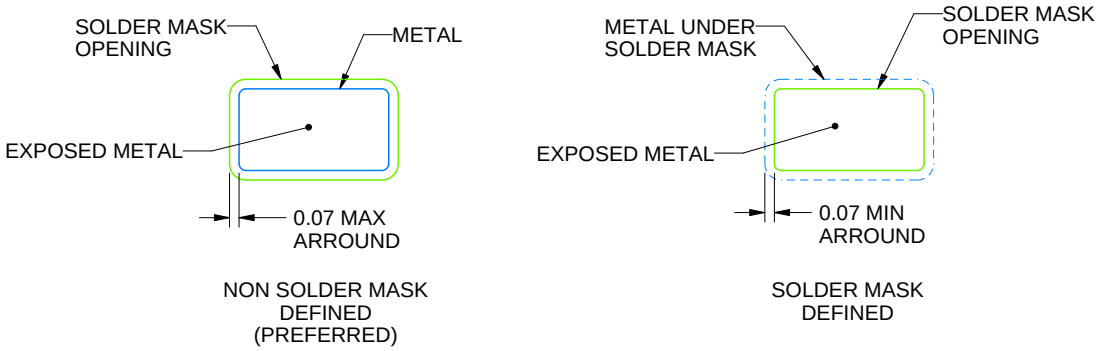
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

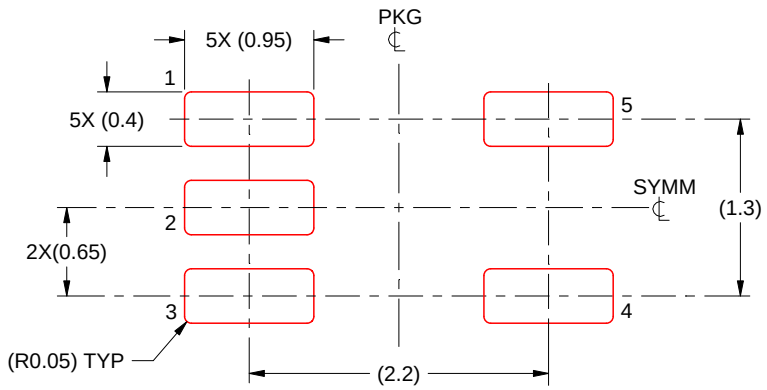


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

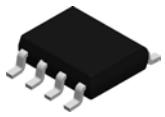


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

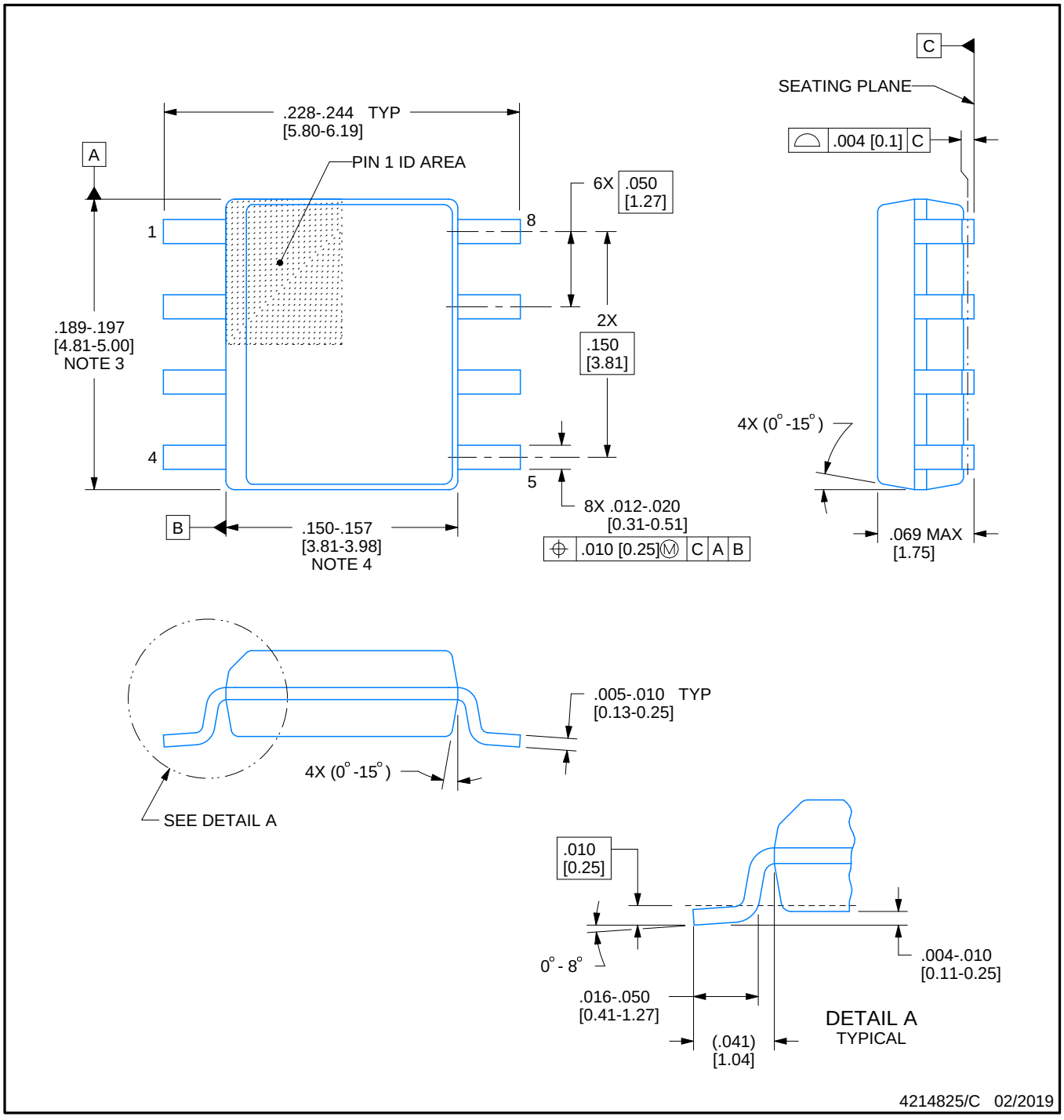


PACKAGE OUTLINE

D0008A

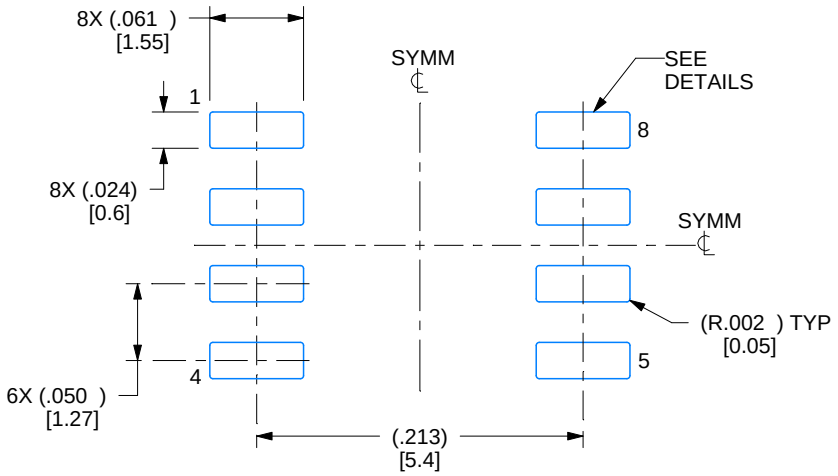
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

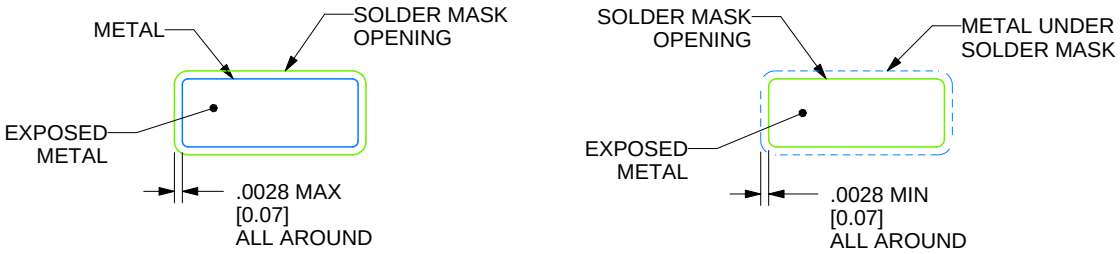


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

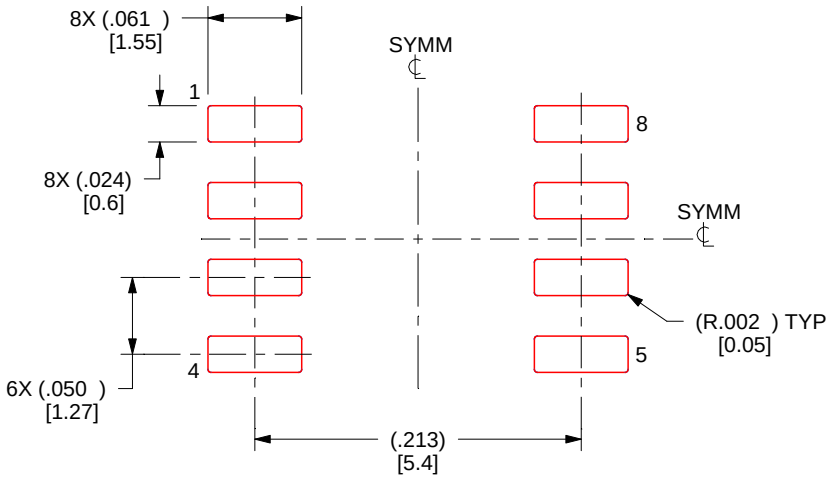
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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