OPA690 ディセーブル機能搭載、広帯域、電圧帰還オペアンプ

1 特長

- ユニティ ゲイン安定:535MHz (G = 1V/V)
- 大出力電流:215mA
- 高いスルーレート:1900V/µs
- 小さい入力電圧ノイズ:4.6nV/√Hz
- 低歪み (R_L = 100Ω、V_O = $2V_{PP}$):
  - 5MHz での HD2、HD3:–85dBc、–75dBc
- 出力電圧スイング:±3.9 V
- 低い消費電流:6.1mA
- 小さい無効化時電流:100µA
- 電源電圧範囲:5V～12V

2 アプリケーション

- 高速画像処理チャネル
- ADC バッファ
- 携帯型計測機器
- トランスインピーダンス アンプ
- アクティブ フィルタ
- ビデオ ライン ドライバ
- xDSL ライン ドライバ / レシーバ

3 概要

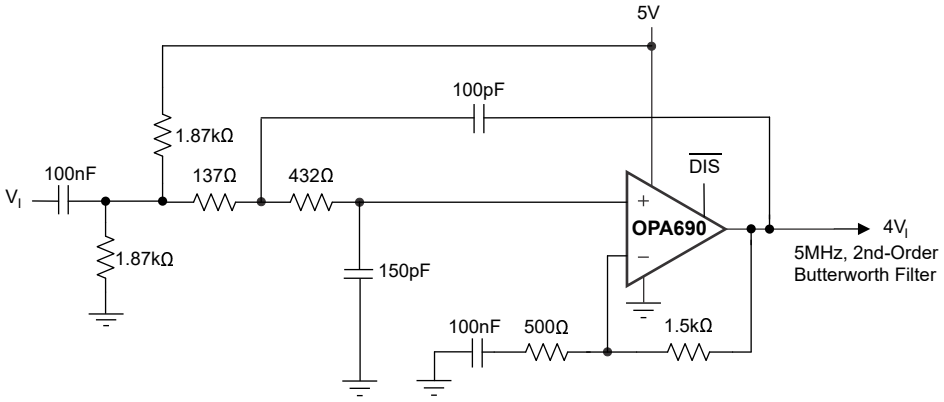
OPA690 デバイスは、ユニティ ゲイン安定、電圧帰還オペアンプの大きな進歩を示すものです。新しい入力アーキテクチャにより、従来は広帯域の電流帰還オペアンプにしか見られなかったスルーレートとフルパワー帯域幅が得られます。新しい出力段アーキテクチャにより、最小限のヘッドルーム要件で 215mA の電流を供給できます。これらの能力を組み合わせることで、100Ω 負荷に対して 1900V/µs という非常に優れたスルーレートを実現できます。13ns の非常に高速なセトリング タイムにより、OPA690 は、高速 ADC ドライバ、高速画像処理システム、電流 DAC トランスインピーダンス アンプなどの高速サンプリング システムに最適です。

静止電流が 6.1mA と小さいので、携帯型またはバッテリ駆動のアプリケーションに最適です。オプションのディセーブル制御ピン ($\overline{DIS}$) を使用すると、システム消費電力をさらに低減できます。$\overline{DIS}$ をオープンのままにするか、または $\overline{DIS}$ を High に保持すると、OPA690 は通常動作します。$\overline{DIS}$ を Low にすると、出力が高インピーダンス状態に移行するとともに、OPA690 の電源電流は 100µA 未満にまで低下します。

パッケージ情報

部品番号 (1)	パッケージ (2)	パッケージ サイズ(3)
OPA690	D (SOIC、8)	4.9mm × 6mm
	DBV (SOT-23、6)	3mm × 3mm

(1) セクション 4 を参照してください。
(2) 詳細については、セクション 11 を参照してください。
(3) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



単一電源、4V/V ゲイン、高周波数アクティブ フィルタ

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison Table

DEVICE	V_S (V)	GBW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	ARCHITECTURE
OPA814	±6.3	250	750	5.3	FET-input, voltage-feedback
OPA817	±6.3	400	1000	4.5	FET-input, voltage-feedback
OPA818	±6.5	2700	1400	2.2	FET-input, voltage-feedback
OPA690	±6	300	1900	4.6	Bipolar-input, voltage-feedback
OPA695	±6	N/A	4300	1.8	Bipolar-input, current-feedback

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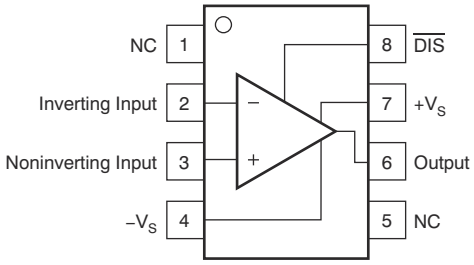
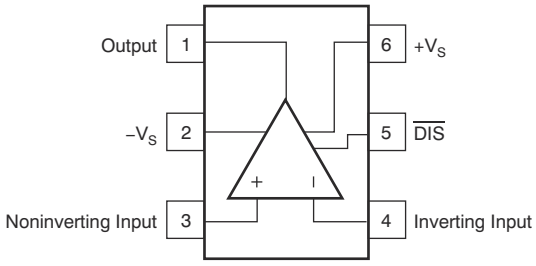
5 Pin Configuration and Functions



NOTE: NC = not connected.

図 5-1. D Package, 8-Pin SOIC (Top View)



Pin Orientation/Package Marking

図 5-2. DBV Package, 6-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	D (SOIC)	DBV (SOT-23)		
$\overline{DIS}$	8	5	I	Disable the op amp (low = disable, high = enable)
IN–	2	4	I	Inverting input
IN+	3	3	I	Noninverting input
NC	1, 5	—	—	No connection
Output	6	1	O	Output of amplifier
$–V_S$	4	2	P	Negative power supply
$+V_S$	7	6	P	Positive power supply

(1) I = input, O = output, P = power.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply		±6.5	V_{DC}
Internal power dissipation	See *Thermal Analysis*		
Differential input voltage		±1.2	V
Supply turn-on and turn-off rates(2)		±0.4	V/µs
Continuous input current(3)		±10	mA
Input voltage		$±V_S$	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Staying less than this specification keeps the edge-triggered ESD absorption devices across the supply pins off.
(3) Continuous input current limit for the ESD diodes to supply pins.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	5	10	12	V
T_A	Operating temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA690		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	6 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	125	171.6	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	70	110.6	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	65.3	85.1	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	25.6	53.9	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	64.8	84.9	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics OPA690IDBV, V_S = ±5 V

at T_A ≅ 25°C, R_F = 402 Ω, R_L = 100 Ω, G = 2 V/V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE (SEE 図 7-1)							
SSBW	Small-signal bandwidth	G = 1 V/V, V_O = 0.5 V_{PP}, R_F = 25 Ω			535		MHz
		G = 2 V/V, V_O = 0.5 V_{PP}			220		
		G = 10 V/V, V_O = 0.5 V_{PP}			30		
GBP	Gain bandwidth product	G ≥ 10 V/V			300		MHz
	Bandwidth for 0.1-dB gain flatness	V_O = 0.5 V_{PP}			25		MHz
	Peaking at a gain of 1 V/V	V_O = 0.5 V_{PP}			1		dB
	Large-signal bandwidth	V_O = 2 V_{PP}			225		MHz
	Slew rate	4-V step			1900		V/µs
	Rise-and-fall time	V_O = 0.5-V step			1.4		ns
		V_O = 4-V step			2.3		
	Settling time	0.02%, V_O = 2-V step			13		ns
		0.1%, V_O = 2-V step			8		
	Harmonic distortion	2nd-harmonic, f = 5 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–85		dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–85		
		3rd-harmonic, f = 5 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–75		
			V_O = 2 V_{PP}, R_L = 500 Ω		–90		
	Input voltage noise	f > 1 MHz			4.6		nV/√Hz
	Input current noise	f > 1 MHz			1.7		pA/√Hz
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	V_O = 0 V, R_L = 100 Ω		58	78		dB
			T_A = –40°C to +85°C	54			
V_{OS}	Input offset voltage	V_{CM} = 0 V			±0.3	±4	mV
			T_A = –40°C to +85°C			±4.7	
	Average offset voltage drift	V_{CM} = 0 V, T_A = –40°C to +85°C				±10	µV/°C
	Input bias current	V_{CM} = 0 V			±1	±10	µA
			T_A = –40°C to +85°C			±12	
	Average bias current drift	V_{CM} = 0 V, T_A = –40°C to +85°C				±40	nA/°C
	Input offset current	V_{CM} = 0 V			±0.05	±1	µA
			T_A = –40°C to +85°C			±1.6	
	Average offset current drift	V_{CM} = 0 V, T_A = –40°C to +85°C				±9	nA/°C
INPUT							
CMIR	Common-mode input voltage(1)			±3.4	±3.85		V
		T_A = –40°C to +85°C		±3.2			
CMRR	Common-mode rejection ratio	V_{CM} = ±1 V		60	80		dB
			T_A = –40°C to +85°C	56			
	Input impedance	Differential mode, V_{CM} = 0 V			6 || 0.1		MΩ || pF
		Common-mode, V_{CM} = 0 V			38 || 1		

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6.5 Electrical Characteristics OPA690IDBV, V_S = ±5 V (続き)

at T_A ≅ 25°C, R_F = 402 Ω, R_L = 100 Ω, G = 2 V/V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing	No load		±3.7	±3.9		V
			T_A = –40°C to +85°C	±3.6			
		R_L = 100 Ω		±3.7	±3.85		
			T_A = –40°C to +85°C	±3.3			
	Current output	Sourcing, V_O = 0 V		160	215		mA
			T_A = –40°C to +85°C	100			
		Sinking, V_O = 0 V		–160	–215		
			T_A = –40°C to +85°C	–100			
	Short-circuit current limit	V_O = 0 V			240		mA
	Closed-loop output impedance	G = 2, f = 100 kHz			0.01		Ω
DISABLE (DISABLED LOW)							
	Power-down supply current	$V_{\overline{DIS}}$ = 0 V			100	200	µA
			T_A = –40°C to +85°C			260	
	Disable time	V_{IN} = 1 V_{DC}			600		ns
	Enable time	V_{IN} = 1 V_{DC}			40		ns
	Off isolation	R_L = 150 Ω, V_{IN} = 0 V			73		dB
	Output capacitance in disable	G = 2, R_L = 150 Ω, V_{IN} = 0 V			8		pF
	Enable voltage				3.3	3.5	V
		T_A = –40°C to +85°C				3.7	
	Disable voltage			1.7	2.3		V
		T_A = –40°C to +85°C		1.5			
	Control-pin input bias current	$V_{\overline{DIS}}$ = 0 V			60	130	µA
			T_A = –40°C to +85°C			160	
POWER SUPPLY							
	Quiescent current			5.2	6.1	7	mA
		T_A = –40°C to +85°C		4.3		7	
PSRR	Power-supply rejection ratio	Input-referred		68	86		dB
			T_A = –40°C to +85°C	64			

(1) Tested < 3 dB below minimum specified CMRR at ±CMIR limits.

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6.6 Electrical Characteristics OPA690IDBV, V_S = 5 V

at T_A ≅ 25°C, R_F = 402 Ω, R_L = 100 Ω, G = 2 V/V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE (SEE 図 7-2)							
	Small-signal bandwidth	G = 1 V/V, V_O = 0.5 V_{PP}, R_F = 25 Ω			460		MHz
		G = 2 V/V, V_O = 0.5 V_{PP}			190		
		G = 10 V/V, V_O = 0.5 V_{PP}			30		
	Gain bandwidth product	G ≥ 10			300		MHz
	Bandwidth for 0.1-dB gain flatness	V_O = 0.5 V_{PP}			20		MHz
	Peaking at a gain of 1 V/V	V_O = 0.5 V_{PP}			1.3		dB
	Large-signal bandwidth	V_O = 2 V_{PP}			220		MHz
	Slew rate	2-V step			850		V/µs
	Rise-and-fall time	V_O = 0.5-V step			1.6		ns
		V_O = 2-V step			2		
	Settling time	0.02%, G = 2, V_O = 2-V step			19		ns
		0.1%, G = 2, V_O = 2-V step			16		
	Harmonic distortion	2nd-harmonic, f = 5 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–74		dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–75		
		3rd-harmonic, f = 5 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–75		
			V_O = 2 V_{PP}, R_L = 500 Ω		–77		
	Input voltage noise	f > 1 MHz			4.6		nV/√Hz
	Input current noise	f > 1 MHz			1.6		pA/√Hz
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	V_O = 2.5 V, R_L = 100 Ω to V_S/2		56	77		dB
			T_A = –40°C to +85°C	52			
	Input offset voltage	V_{CM} = 2.5 V			±0.3	±4	mV
			T_A = –40°C to +85°C			±4.7	
	Average offset voltage drift	V_{CM} = 2.5 V, T_A = –40°C to +85°C				±10	µV/°C
	Input bias current	V_{CM} = 2.5 V			±1	±10	µA
			T_A = –40°C to +85°C			±12	
	Average bias current drift	V_{CM} = 2.5 V, T_A = –40°C to +85°C				±40	nA/°C
	Input offset current	V_{CM} = 2.5 V			±0.05	±1	µA
			T_A = –40°C to +85°C			±1.6	
	Average offset current drift	V_{CM} = 2.5 V, T_A = –40°C to +85°C				±9	nA/°C
INPUT							
	Most-positive input voltage(1)			3.4	3.85		V
		T_A = –40°C to +85°C		3.2			
	Least-positive input voltage(1)			1.6	1.15		V
		T_A = –40°C to +85°C		1.8			
CMRR	Common-mode rejection ratio	V_{CM} = 2.5 V ±0.5 V		58	79		dB
			T_A = –40°C to +85°C	54			
	Input impedance	Differential mode, V_{CM} = 2.5 V			6 || 0.1		MΩ || pF
		Common-mode, V_{CM} = 2.5 V			27 || 1.1		

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6.6 Electrical Characteristics OPA690IDBV, V_S = 5 V (続き)

at T_A ≅ 25°C, R_F = 402 Ω, R_L = 100 Ω, G = 2 V/V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Most-positive output voltage	No load		3.7	3.9		V
			T_A = –40°C to +85°C	3.5			
		R_L = 100 Ω to 2.5 V		3.7	3.85		
			T_A = –40°C to +85°C	3.4			
	Least-positive output voltage	No load			1.1	1.3	V
			T_A = –40°C to +85°C			1.5	
		R_L = 100 Ω to 2.5 V			1.15	1.3	
			T_A = –40°C to +85°C			1.7	
	Current output	Sourcing			190	120	mA
			T_A = –40°C to +85°C			80	
		Sinking		–120	–190		
			T_A = –40°C to +85°C	–80			
	Short-circuit current				±250		mA
	Closed-loop output impedance	G = 2, f =100 kHz			0.01		Ω
DISABLE (DISABLED LOW)							
	Power-down supply current	$V_{\overline{DIS}}$ = 0 V			75	200	µA
			T_A = –40°C to +85°C			260	
	Off isolation	G = 2, 5 MHz			72		dB
	Output capacitance in disable				8		pF
	Enable voltage				3.3	3.5	V
			T_A = –40°C to +85°C			3.7	
	Disable voltage			1.7	2.4		V
			T_A = –40°C to +85°C	1.5			
$V_{\overline{DIS}}$	Control-pin input bias current	$V_{\overline{DIS}}$ = 0 V			60	130	µA
			T_A = –40°C to +85°C			160	
POWER SUPPLY							
	Quiescent current	V_S = +5 V		4.48	6.1	6.8	mA
			T_A = –40°C to +85°C	3.86		6.9	
+PSRR	Power-supply rejection ratio	Input-referred			85		dB

(1) Tested for CMRR = 69 dB at ±CMIR limits.

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6.7 Electrical Characteristics OPA690ID, V_S = ±5 V

at T_A ≅ 25°C, R_F = 402 Ω, R_L = 100 Ω, G = 2 V/V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE (SEE 図 7-1)							
SSBW	Small-signal bandwidth	G = 1 V/V, V_O = 0.5 V_{PP}, R_F = 25 Ω			500		MHz
		G = 2 V/V, V_O = 0.5 V_{PP}			220		
		G = 10 V/V, V_O = 0.5 V_{PP}			30		
GBP	Gain bandwidth product	G ≥ 10 V/V			300		MHz
	Bandwidth for 0.1-dB gain flatness	V_O < 0.5 V_{PP}			30		MHz
	Peaking at a gain of 1 V/V	V_O < 0.5 V_{PP}			4		dB
	Large-signal bandwidth	V_O = 5 V_{PP}			200		MHz
	Slew rate	4-V step			1800		V/µs
	Rise-and-fall time	V_O = 0.5-V step			1.4		ns
		V_O = 5-V step			2.8		
	Settling time	0.02%, V_O = 2-V step			12		ns
		0.1%, V_O = 2-V step			8		
	Harmonic distortion	2nd-harmonic, f = 5 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–68		dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–77		
		3rd-harmonic, f = 5 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–70		
			V_O = 2 V_{PP}, R_L = 500 Ω		–81		
	Input voltage noise	f > 1 MHz			5.5		nV/√Hz
	Input current noise	f > 1 MHz			3.1		pA/√Hz
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	V_O = 0 V, R_L = 100 Ω		58	69		dB
			T_A = –40°C to +85°C	54			
V_{OS}	Input offset voltage	V_{CM} = 0 V			±1	±4	mV
			T_A = –40°C to +85°C			±4.7	
	Average offset voltage drift	V_{CM} = 0 V, T_A = –40°C to +85°C				±10	µV/°C
	Input bias current	V_{CM} = 0 V			±3	±10	µA
			T_A = –40°C to +85°C			±12	
	Average bias current drift	V_{CM} = 0 V, T_A = –40°C to +85°C				±40	nA/°C
	Input offset current	V_{CM} = 0 V			±0.1	±1	µA
			T_A = –40°C to +85°C			±1.6	
	Average offset current drift	V_{CM} = 0 V, T_A = –40°C to +85°C				±9	nA/°C
INPUT							
CMIR	Common-mode input voltage(1)			±3.4	±3.5		V
		T_A = –40°C to +85°C		±3.2			
CMRR	Common-mode rejection ratio	V_{CM} = ±1 V		60	65		dB
			T_A = –40°C to +85°C	56			
	Input impedance	Differential mode, V_{CM} = 0 V			190 || 0.6		kΩ || pF
		Common-mode, V_{CM} = 0 V			3.2 || 0.9		MΩ || pF

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6.7 Electrical Characteristics OPA690ID, V_S = ±5 V (続き)

at T_A ≅ 25°C, R_F = 402 Ω, R_L = 100 Ω, G = 2 V/V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing	No load		±3.8	±4		V
			T_A = –40°C to +85°C	±3.6			
		R_L = 100 Ω		±3.7	±3.9		
			T_A = –40°C to +85°C	±3.3			
	Current output	Sourcing, V_O = 0 V		160	190		mA
			T_A = –40°C to +85°C	100			
		Sinking, V_O = 0 V		–160	–190		
			T_A = –40°C to +85°C	–100			
	Short-circuit current limit	V_O = 0 V			±250		mA
	Closed-loop output impedance	G = 2, f = 100 kHz			0.04		Ω
DISABLE (DISABLED LOW)							
	Power-down supply current	$V_{\overline{DIS}}$ = 0 V				–100	–200	μA
			T_A = –40°C to +85°C				–260	
	Disable time	V_{IN} = 1 V_{DC}			200		ns
	Enable time	V_{IN} = 1 V_{DC}			25		ns
	Off isolation	R_L = 150 Ω, V_{IN} = 0 V			70		dB
	Output capacitance in disable	G = 2, R_L = 150 Ω, V_{IN} = 0 V			4		pF
	Turn-on glitch				±50		mV
	Turn-off glitch				±20		mV
	Enable voltage			3.5	3.3		V
		T_A = –40°C to +85°C		3.7			
	Disable voltage				1.8	1.7	V
		T_A = –40°C to +85°C				1.5	
	Control-pin input bias current	$V_{\overline{DIS}}$ = 0 V			75	130	μA
			T_A = –40°C to +85°C			160	
POWER SUPPLY							
	Quiescent current			5.3	5.5	5.8	mA
		T_A = –40°C to +85°C		4.3		6.6	
PSRR	Power-supply rejection ratio	Input-referred		68	75		dB
			T_A = –40°C to +85°C	64			

(1) Tested < 3 dB below minimum specified CMRR at ±CMIR limits.

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6.8 Electrical Characteristics OPA690ID, V_S = 5 V

at T_A ≅ 25°C, R_F = 402 Ω, R_L = 100 Ω, G = 2 V/V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE (SEE 図 7-2)							
	Small-signal bandwidth	G = 1 V/V, V_O = 0.5 V_{PP}, R_F = 25 Ω			400		MHz
		G = 2 V/V, V_O = 0.5 V_{PP}			190		
		G = 10 V/V, V_O = 0.5 V_{PP}			25		
	Gain bandwidth product	G ≥ 10			250		MHz
	Bandwidth for 0.1-dB gain flatness	V_O < 0.5 V_{PP}			20		MHz
	Peaking at a gain of 1 V/V	V_O < 0.5 V_{PP}			5		dB
	Large-signal bandwidth	V_O = 2 V_{PP}			220		MHz
	Slew rate	2-V step			1000		V/µs
	Rise-and-fall time	V_O = 0.5-V step			1.6		ns
		V_O = 2-V step			2		
	Settling time	0.02%, G = 2, V_O = 2-V step			12		ns
		0.1%, G = 2, V_O = 2-V step			8		
	Harmonic distortion	2nd-harmonic, f = 5 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–65	–60	dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–75	–70	
		3rd-harmonic, f = 5 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–68	–64	
			V_O = 2 V_{PP}, R_L = 500 Ω		–77	–73	
	Input voltage noise	f > 1 MHz			5.6		nV/√Hz
	Input current noise	f > 1 MHz			3.2		pA/√Hz
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	V_O = 2.5 V, R_L = 100 Ω to V_S/2		56	63		dB
			T_A = –40°C to +85°C	52			
	Input offset voltage	V_{CM} = 2.5 V			±1	±4	mV
			T_A = –40°C to +85°C			±4.7	
	Average offset voltage drift	V_{CM} = 2.5 V, T_A = –40°C to +85°C				±10	µV/°C
	Input bias current	V_{CM} = 2.5 V			±3	±10	µA
			T_A = –40°C to +85°C			±12	
	Average bias current drift	V_{CM} = 2.5 V, T_A = –40°C to +85°C				±40	nA/°C
	Input offset current	V_{CM} = 2.5 V			±0.3	±1	µA
			T_A = –40°C to +85°C			±1.6	
	Average offset current drift	V_{CM} = 2.5 V, T_A = –40°C to +85°C				±9	nA/°C
INPUT							
	Most-positive input voltage(1)			3.4	3.5		V
		T_A = –40°C to +85°C		3.2			
	Least-positive input voltage(1)			1.6	1.5		V
		T_A = –40°C to +85°C		1.8			
CMRR	Common-mode rejection ratio	V_{CM} = 2.5 V ±0.5 V		58	63		dB
			T_A = –40°C to +85°C	54			
	Input impedance	Differential mode, V_{CM} = 2.5 V			92 || 1.4		kΩ || pF
		Common-mode, V_{CM} = 2.5 V			2.2 || 1.5		MΩ || pF

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6.8 Electrical Characteristics OPA690ID, V_S = 5 V (続き)

at T_A ≅ 25°C, R_F = 402 Ω, R_L = 100 Ω, G = 2 V/V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Most-positive output voltage	No load		3.8	4		V
			T_A = –40°C to +85°C	3.5			
		R_L = 100 Ω to 2.5 V		3.7	3.9		
			T_A = –40°C to +85°C	3.4			
	Least-positive output voltage	No load		1.2	1		V
			T_A = –40°C to +85°C	1.5			
		R_L = 100 Ω to 2.5 V			1.1	1.3	
			T_A = –40°C to +85°C			1.7	
	Current output	Sourcing			160	120	mA
			T_A = –40°C to +85°C			80	
		Sinking		–120	–160		
			T_A = –40°C to +85°C	–80			
	Short-circuit current				±250		mA
	Closed-loop output impedance	G = 2, f =100 kHz			0.04		Ω
DISABLE (DISABLED LOW)							
	Power-down supply current	$V_{\overline{DIS}}$ = 0 V			–100		µA
			T_A = –40°C to +85°C			–260	
	Off isolation	G = 2, 5 MHz			65		dB
	Output capacitance in disable				4		pF
	Turn-on glitch	G = 2, R_L = 150 Ω, V_{IN} = V_S/2			±50		mV
	Turn-off glitch	G = 2, R_L = 150 Ω, V_{IN} = V_S/2			±20		mV
	Enable voltage			3.5	3.3		V
		T_A = –40°C to +85°C		3.7			
	Disable voltage				1.8	1.7	V
		T_A = –40°C to +85°C				1.5	
$V_{\overline{DIS}}$	Control-pin input bias current	$V_{\overline{DIS}}$ = 0 V			75	130	µA
			T_A = –40°C to +85°C			160	
POWER SUPPLY							
	Quiescent current	V_S = +5 V		4.48	4.9	5.44	mA
			T_A = –40°C to +85°C	3.86		6.02	
+PSRR	Power-supply rejection ratio	Input-referred			72		dB

(1) Tested for CMRR = 69 dB at ±CMIR limits.

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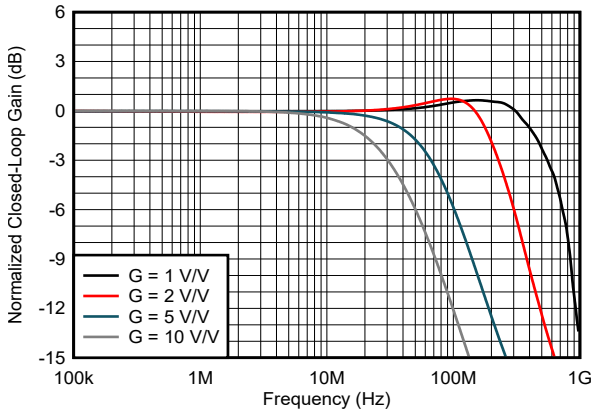
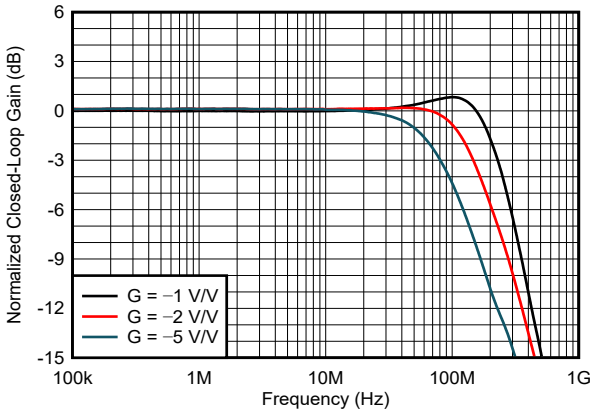
6.9 Typical Characteristics: OPA690IDBV, V_S = ±5V

at T_A ≅ 25°C, R_F = 402Ω, R_L = 100Ω, G = 2V/V, and input and output referenced to midsupply (unless otherwise noted)



V_{OUT} = 0.5V_{PP}

図 6-1. Noninverting Small-Signal Frequency Response



V_{OUT} = 0.5V_{PP}

図 6-2. Inverting Small-Signal Frequency Response

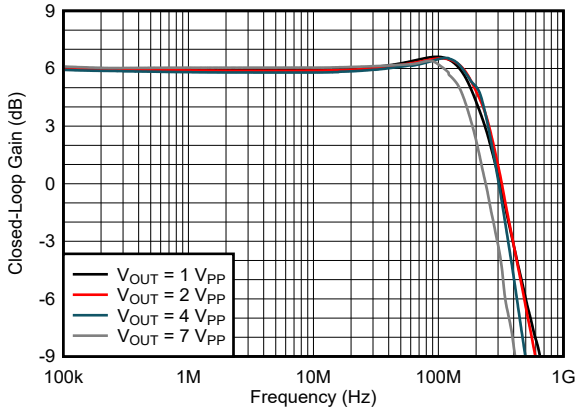


図 6-3. Noninverting Large-Signal Frequency Response

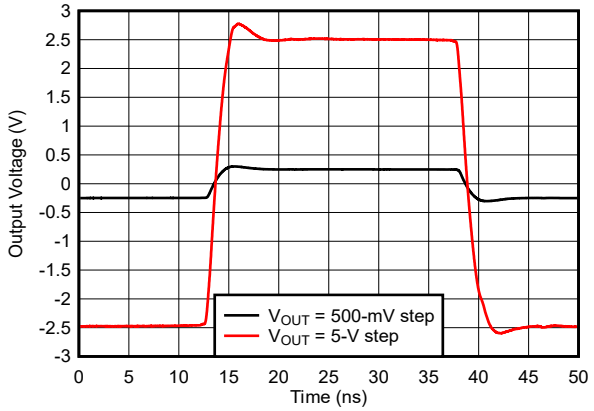
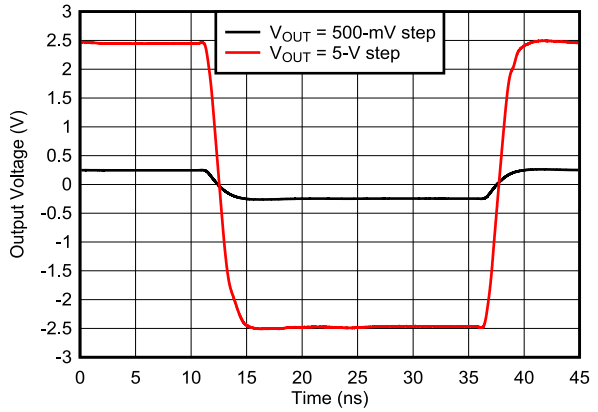
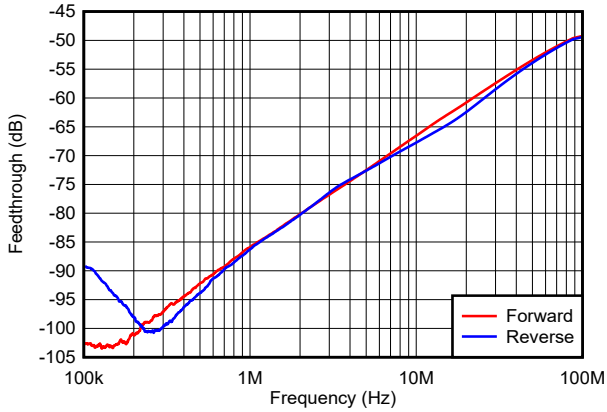


図 6-4. Noninverting Pulse Response



G = –2V/V

図 6-5. Inverting Pulse Response

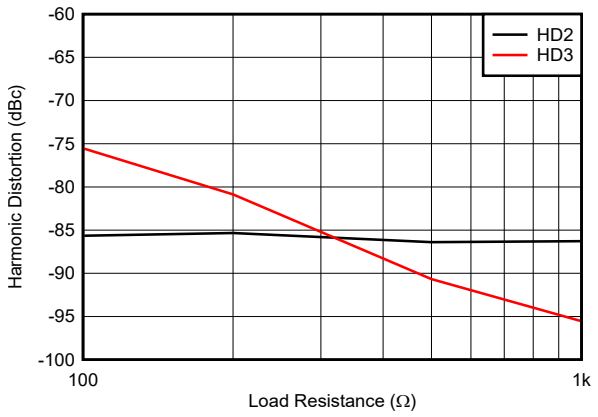


$V_{\overline{DIS}}$ = 0V

図 6-6. Disable Feedthrough vs Frequency

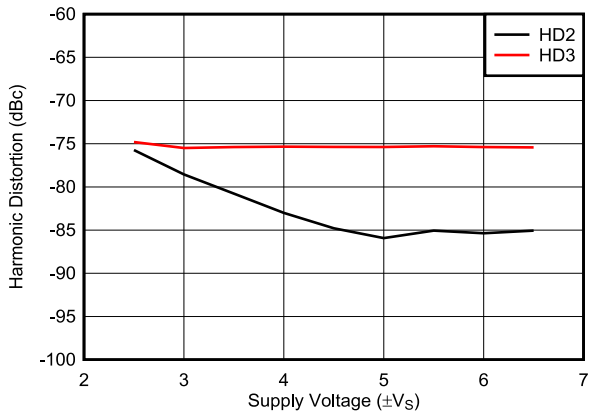
6.9 Typical Characteristics: OPA690IDBV, V_S = ±5V (continued)

at T_A ≅ 25°C, R_F = 402Ω, R_L = 100Ω, G = 2V/V, and input and output referenced to midsupply (unless otherwise noted)



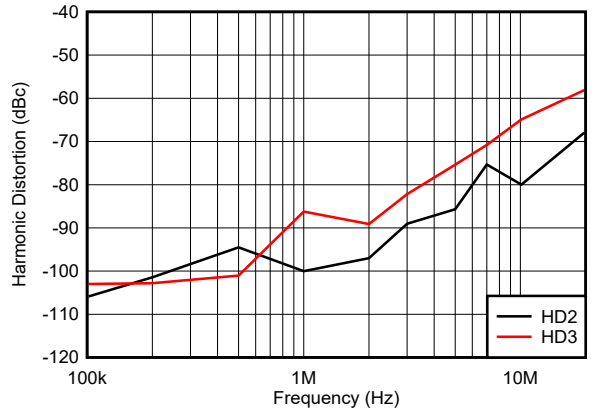
f = 5MHz V_{OUT} = 2V_{PP}

図 6-7. Harmonic Distortion vs Load Resistance



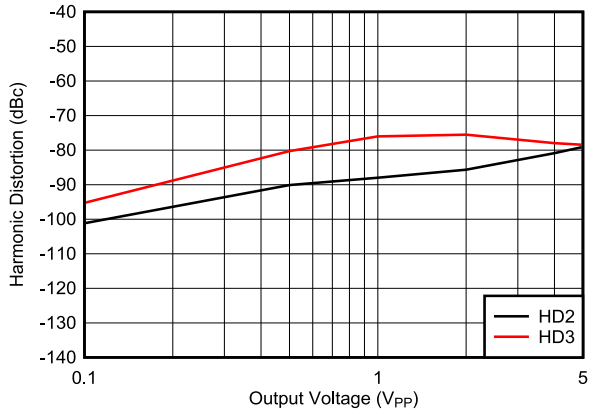
f = 5MHz V_{OUT} = 2V_{PP}

図 6-8. Harmonic Distortion vs Supply Voltage



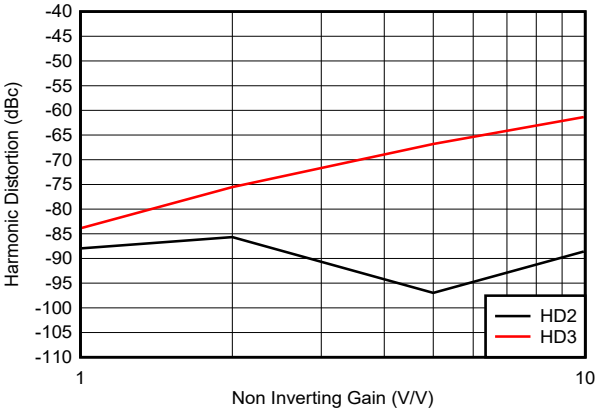
V_{OUT} = 2V_{PP}

図 6-9. Harmonic Distortion vs Frequency



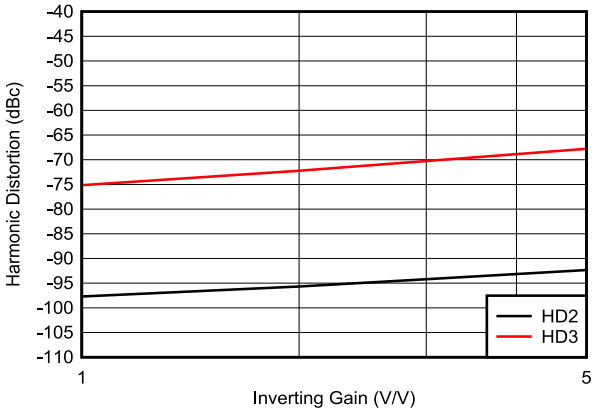
f = 5MHz

図 6-10. Harmonic Distortion vs Output Voltage



f = 5MHz V_{OUT} = 2V_{PP}

図 6-11. Harmonic Distortion vs Noninverting Gain



f =5 MHz V_{OUT} = 2V_{PP} R_F = 1kΩ

図 6-12. Harmonic Distortion vs Inverting Gain

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6.9 Typical Characteristics: OPA690IDBV, V_S = ±5V (continued)

at T_A ≅ 25°C, R_F = 402Ω, R_L = 100Ω, G = 2V/V, and input and output referenced to midsupply (unless otherwise noted)

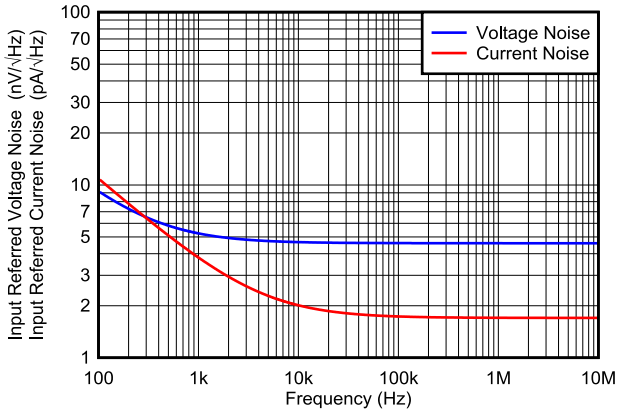


図 6-13. Voltage Noise Density vs Frequency

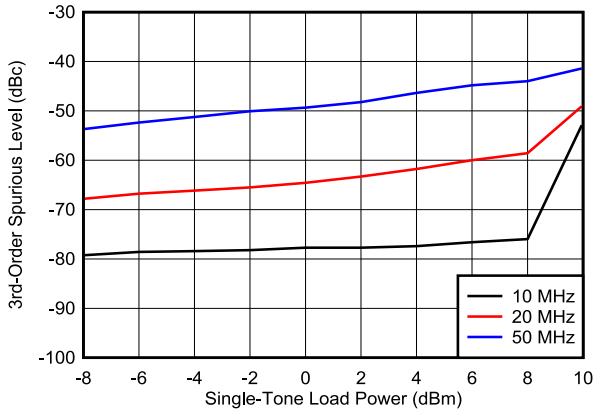


図 6-14. Intermodulation Distortion vs Load Power

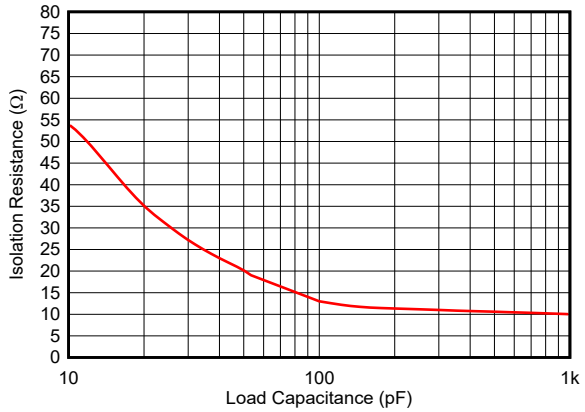
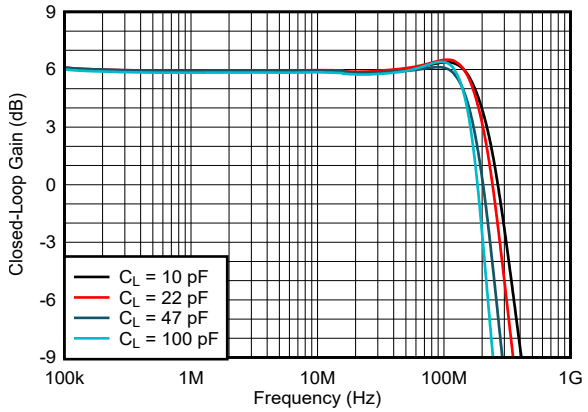
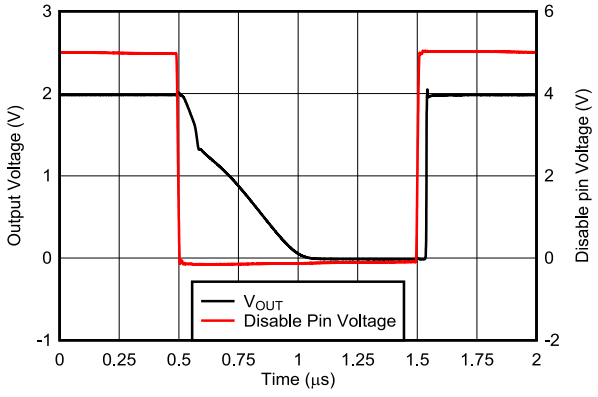


図 6-15. Recommended Isolation Resistor vs Capacitive Load



V_{OUT} = 0.5V_{PP}

図 6-16. Frequency Response vs Capacitive Load



V_{IN} = +1V

図 6-17. Enable and Disable Settling Response

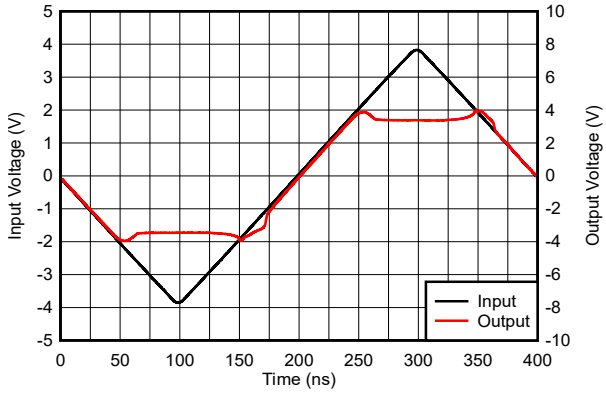


図 6-18. Noninverting Output Overdrive Recovery

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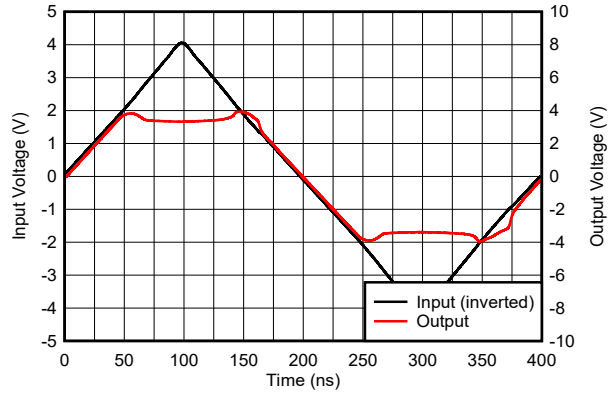
6.9 Typical Characteristics: OPA690IDBV, V_S = ±5V (continued)

at T_A ≅ 25°C, R_F = 402Ω, R_L = 100Ω, G = 2V/V, and input and output referenced to midsupply (unless otherwise noted)



G = −2V/V

図 6-19. Inverting Output Overdrive Recovery

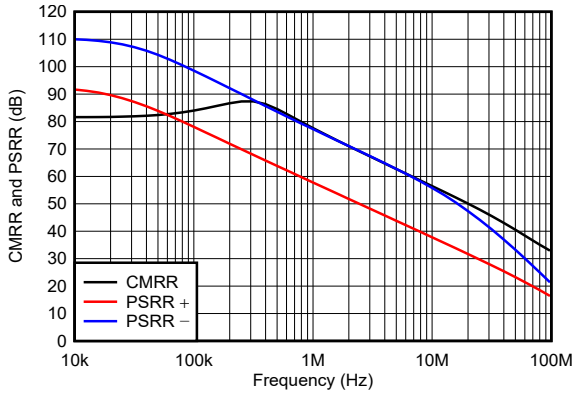
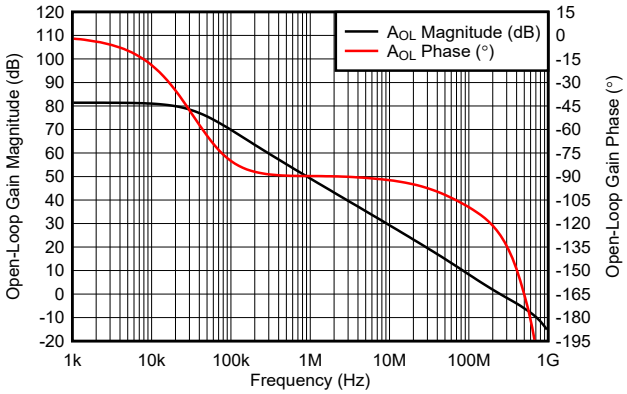


図 6-20. Common-Mode and Power-Supply Rejection Ratio vs Frequency



R_L = 1GΩ

図 6-21. Open-Loop Gain Magnitude and Phase vs Frequency

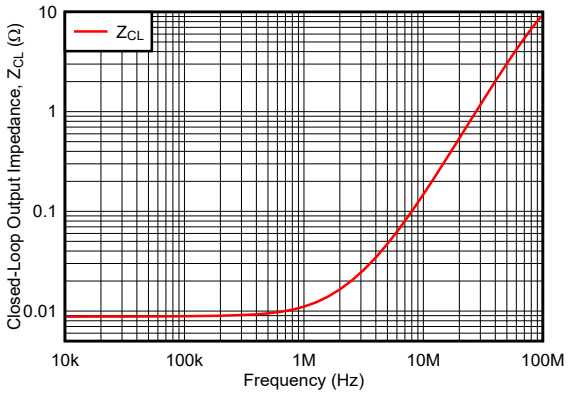


図 6-22. Closed-Loop Output Impedance vs Frequency

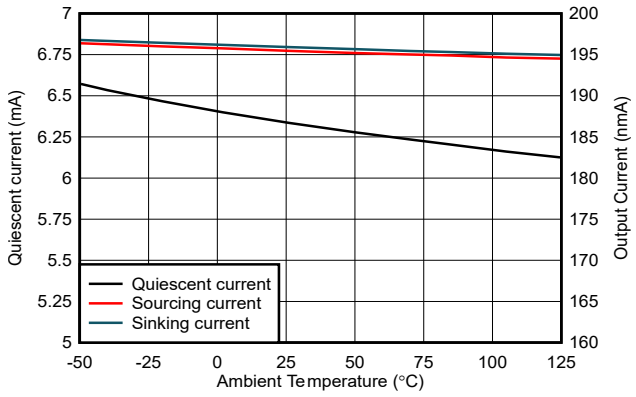


図 6-23. Supply and Current Over Temperature

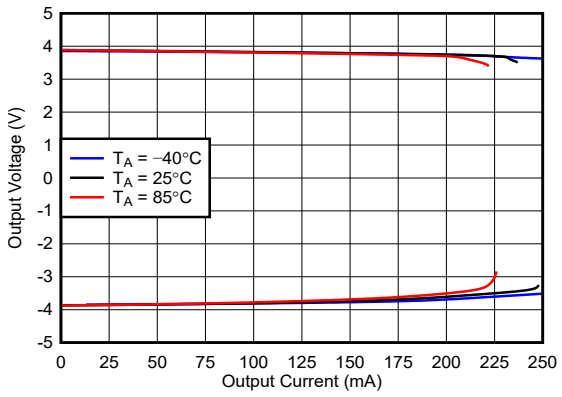


図 6-24. Output Voltage vs Output Current Over Temperature

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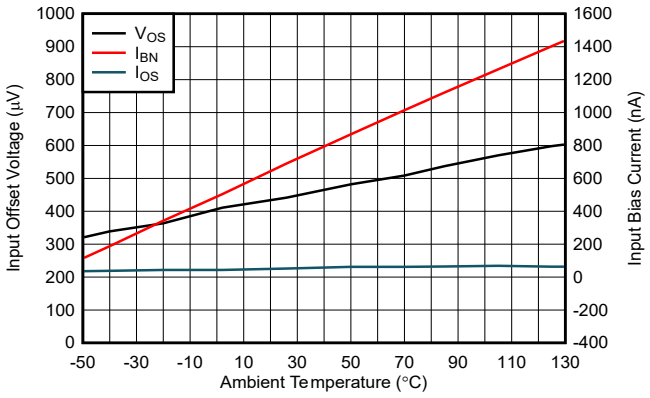
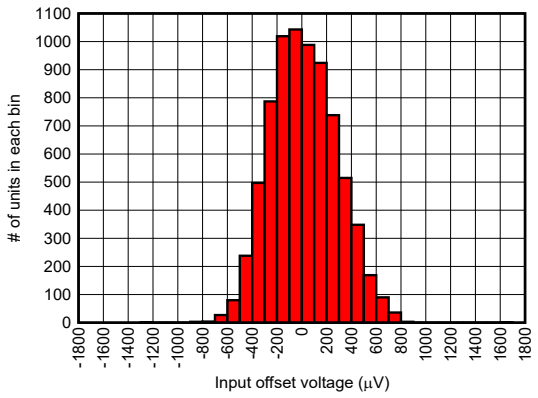
6.9 Typical Characteristics: OPA690IDBV, V_S = ±5V (continued)

at T_A ≅ 25°C, R_F = 402Ω, R_L = 100Ω, G = 2V/V, and input and output referenced to midsupply (unless otherwise noted)



33 units, delta from 25°C

図 6-25. Input Offset Voltage and Bias Current Over Temperature



7500 units, µ = 18µV, σ = 265µV

図 6-26. Input Offset Voltage Histogram

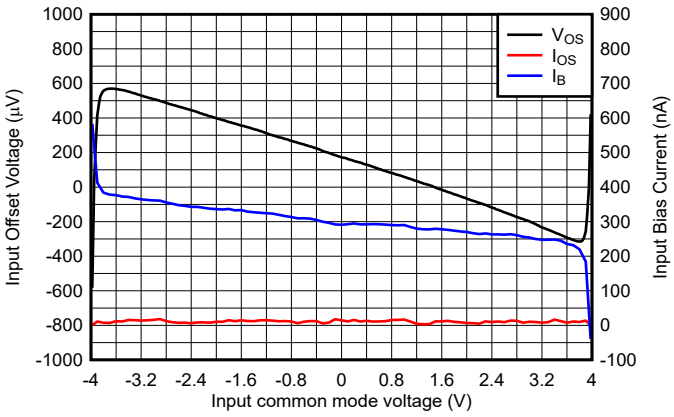


図 6-27. Input Offset Voltage and Bias Current vs Common-Mode Voltage

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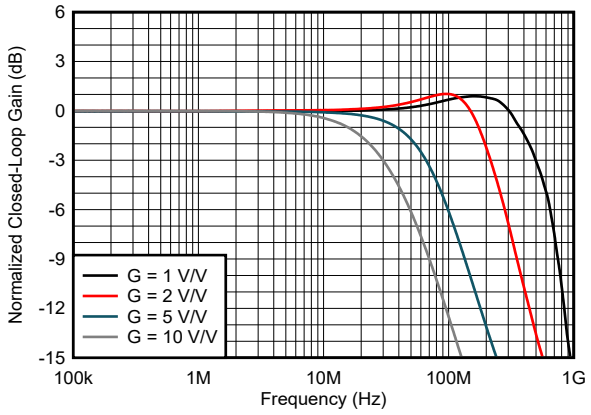
6.10 Typical Characteristics: OPA690IDBV, V_S = 5V

at T_A ≅ 25°C, R_F = 402Ω, R_L = 100Ω, G = 2V/V, and input and output referenced to midsupply (unless otherwise noted)



V_{OUT} = 0.5V_{PP}

図 6-28. Noninverting Small-Signal Frequency Response

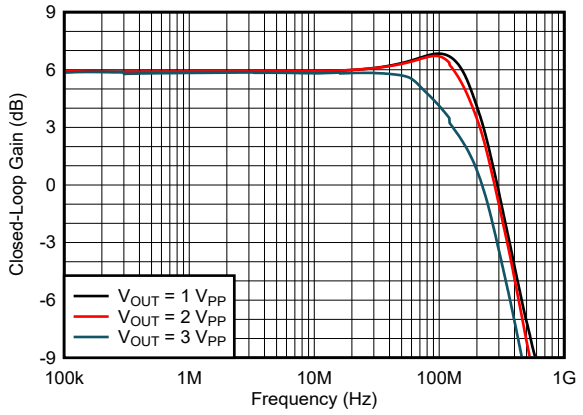


図 6-29. Noninverting Large-Signal Frequency Response

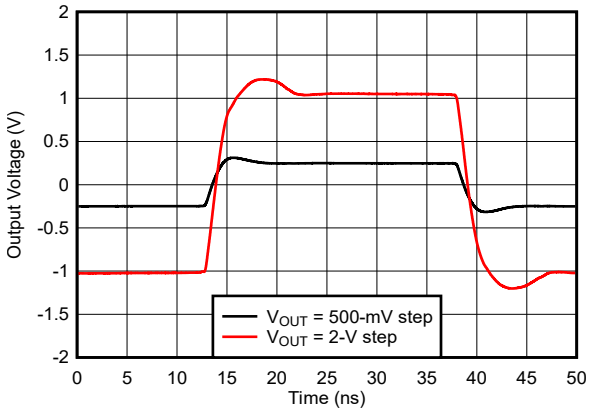
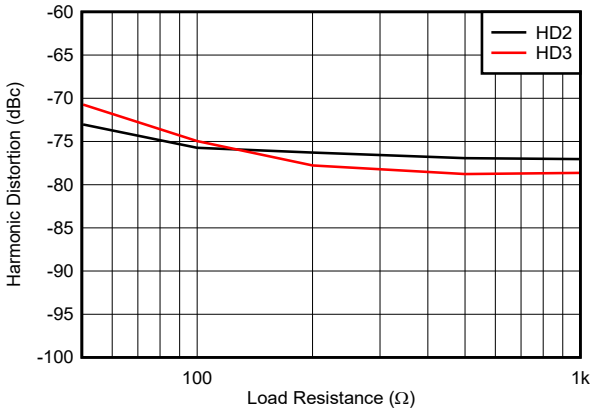
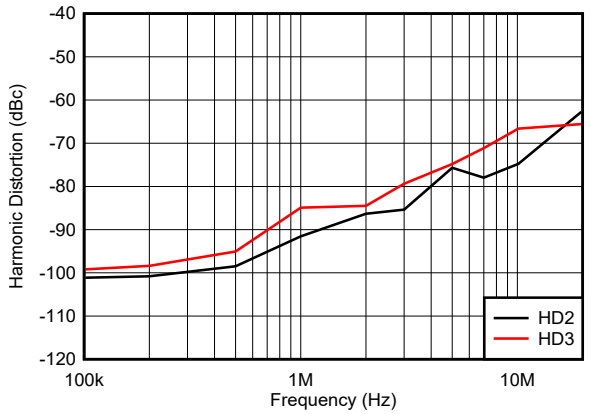


図 6-30. Noninverting Pulse Response



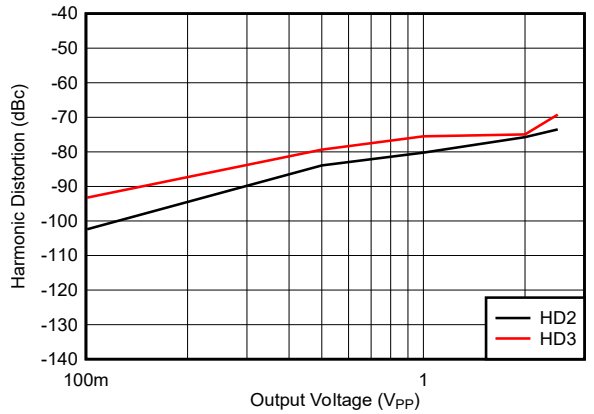
f = 5MHz V_{OUT} = 2V_{PP}

図 6-31. Harmonic Distortion vs Load Resistance



V_{OUT} = 2V_{PP}

図 6-32. Harmonic Distortion vs Frequency



f = 5MHz

図 6-33. Harmonic Distortion vs Output Voltage

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6.10 Typical Characteristics: OPA690IDBV, V_S = 5V (continued)

at T_A ≅ 25°C, R_F = 402Ω, R_L = 100Ω, G = 2V/V, and input and output referenced to midsupply (unless otherwise noted)

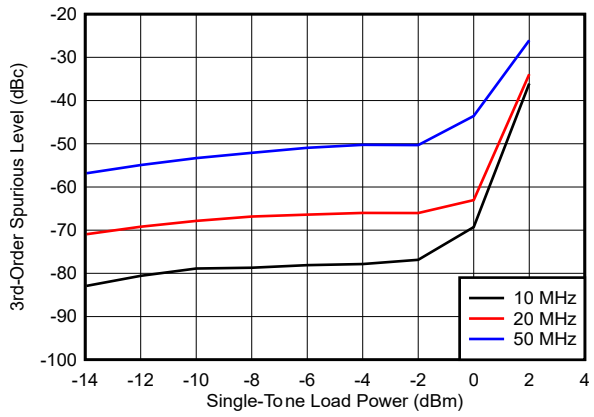


図 6-34. Intermodulation Distortion vs Load Power

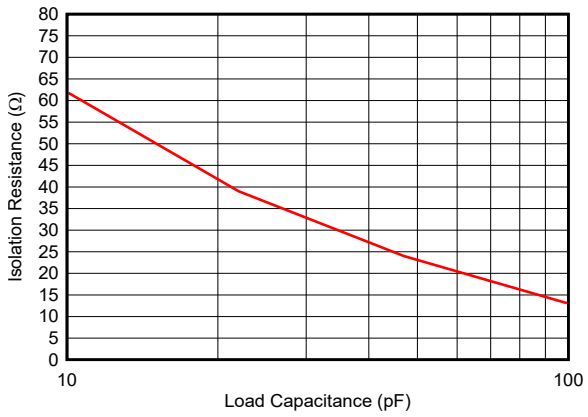
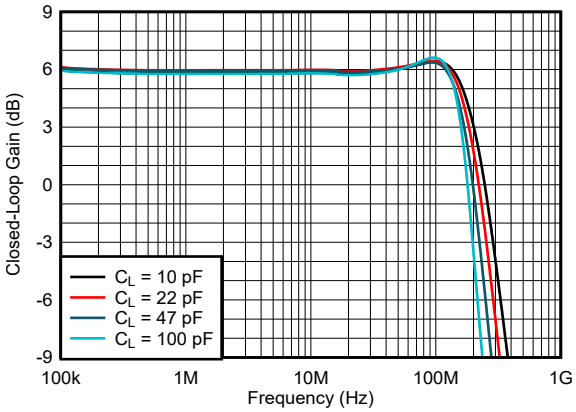


図 6-35. Recommended Isolation Resistor vs Capacitive Load



V_{OUT} = 0.5V_{PP}

図 6-36. Frequency Response vs Capacitive Load

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6.11 Typical Characteristics: OPA690ID, V_S = ±5V

at T_A = 25°C, G = 2, R_F = 402Ω, and R_L = 100Ω (unless otherwise noted); see 図 7-1 for ac performance only

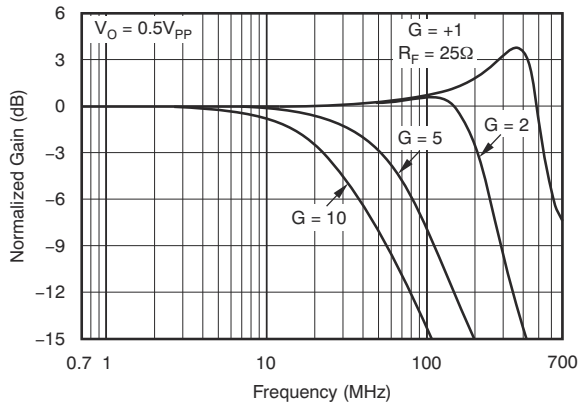

図 6-37. Small-Signal Frequency Response

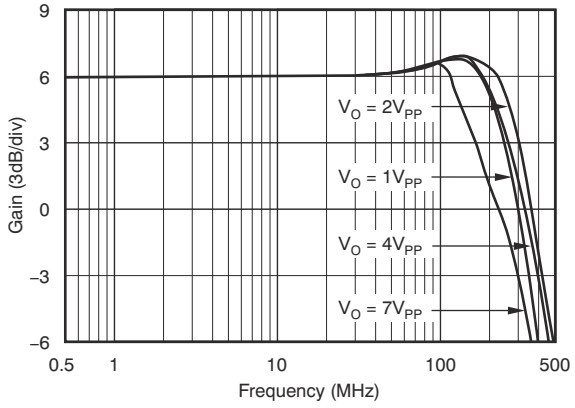

図 6-38. Large-Signal Frequency Response

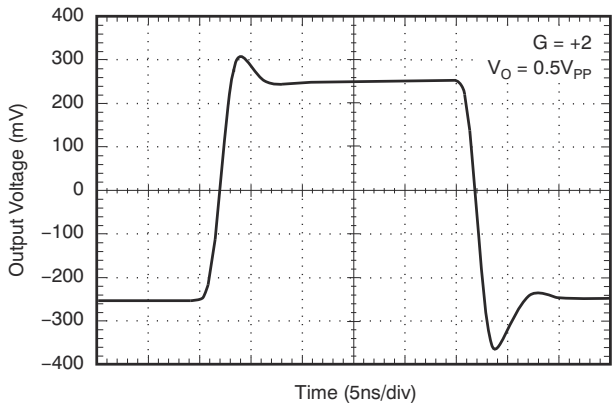

図 6-39. Small-Signal Pulse Response

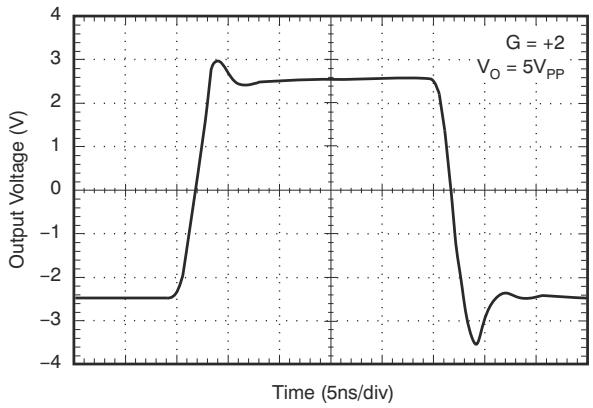

図 6-40. Large-Signal Pulse Response

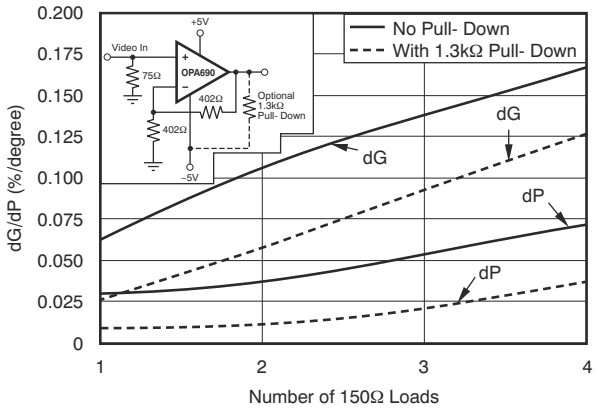

図 6-41. Composite Video dG/dP

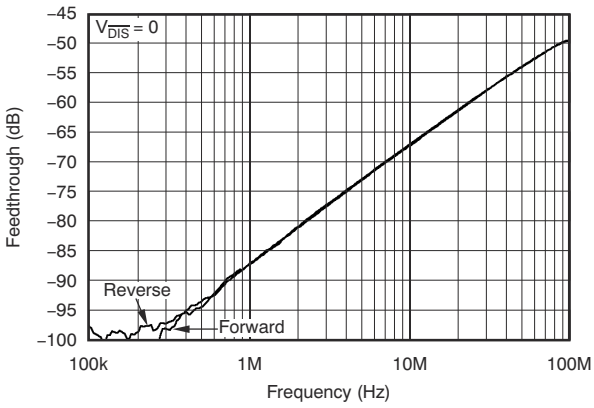

図 6-42. Disable Feedthrough vs Frequency

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6.11 Typical Characteristics: OPA690ID, V_S = ±5V (continued)

at T_A = 25°C, G = 2, R_F = 402Ω, and R_L = 100Ω (unless otherwise noted); see 図 7-1 for ac performance only

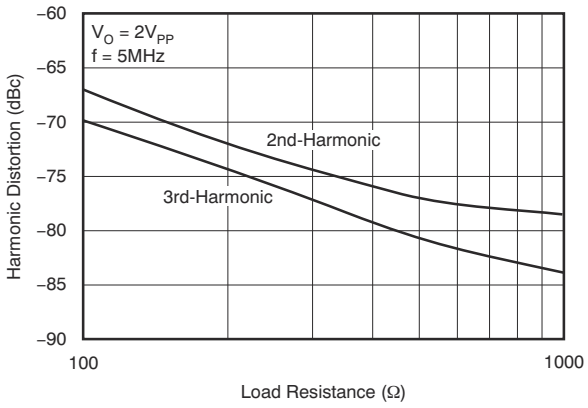

図 6-43. Harmonic Distortion vs Load Resistance

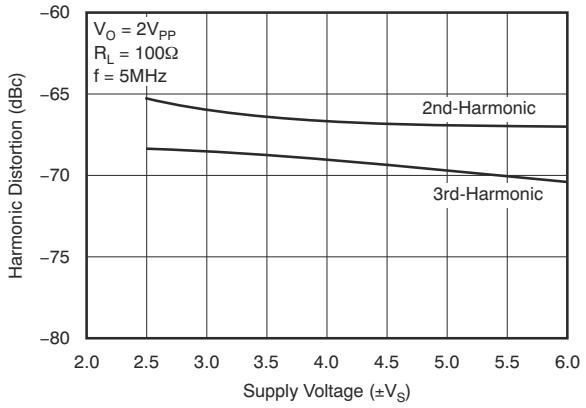

図 6-44. 5MHz Harmonic Distortion vs Supply Voltage

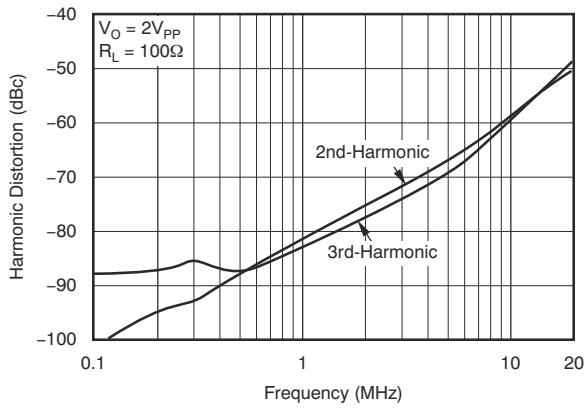

図 6-45. Harmonic Distortion vs Frequency

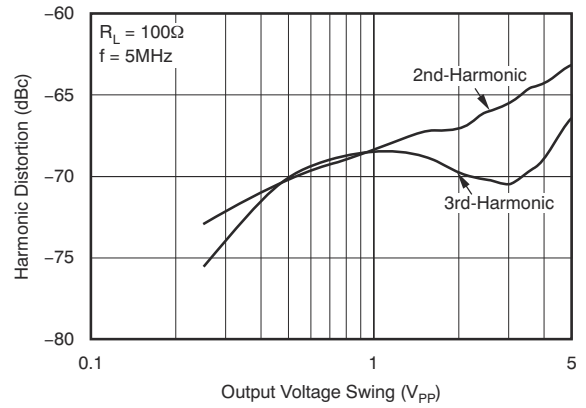

図 6-46. Harmonic Distortion vs Output Voltage

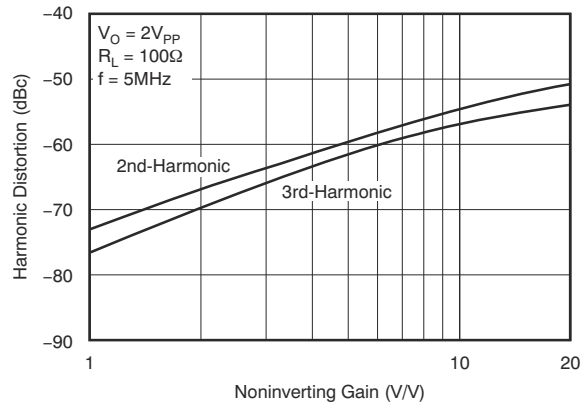

図 6-47. Harmonic Distortion vs Noninverting Gain

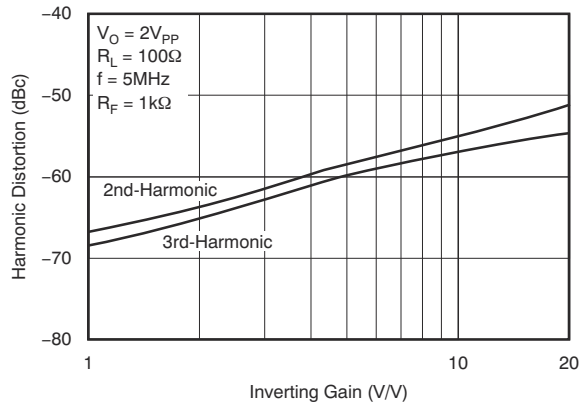

図 6-48. Harmonic Distortion vs Inverting Gain

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6.11 Typical Characteristics: OPA690ID, V_S = ±5V (continued)

at T_A = 25°C, G = 2, R_F = 402Ω, and R_L = 100Ω (unless otherwise noted); see 図 7-1 for ac performance only

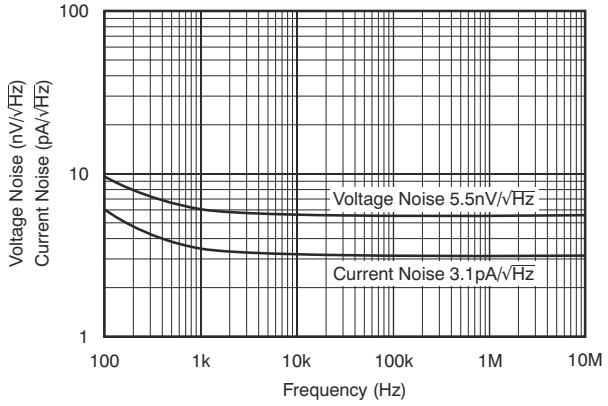

図 6-49. Input Voltage and Current Noise Density

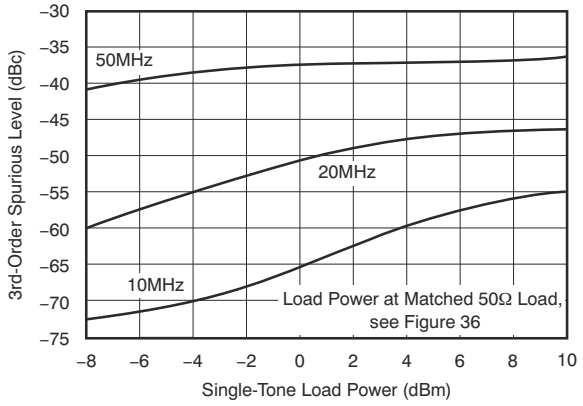

図 6-50. Two-Tone, 3rd-Order Intermodulation Spurious

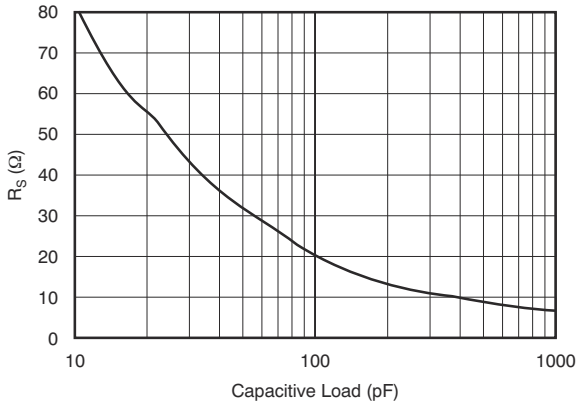

図 6-51. Recommended R_S vs Capacitive Load

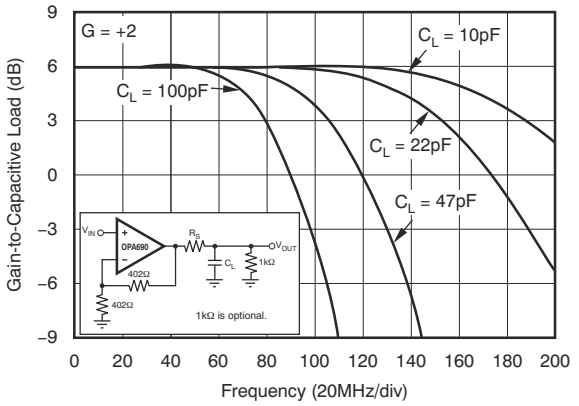

図 6-52. Frequency Response vs Capacitive Load

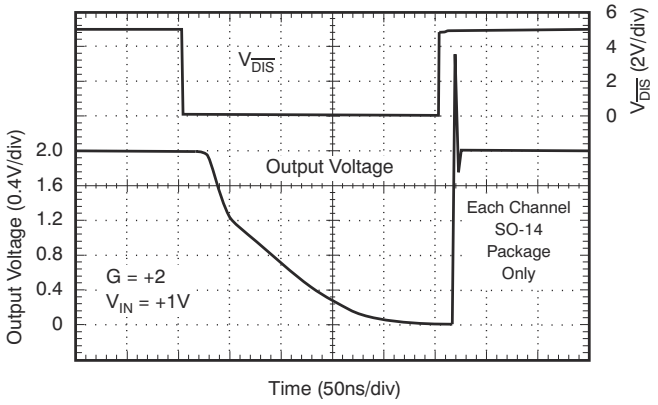

図 6-53. Large-Signal Enable or Disable Response

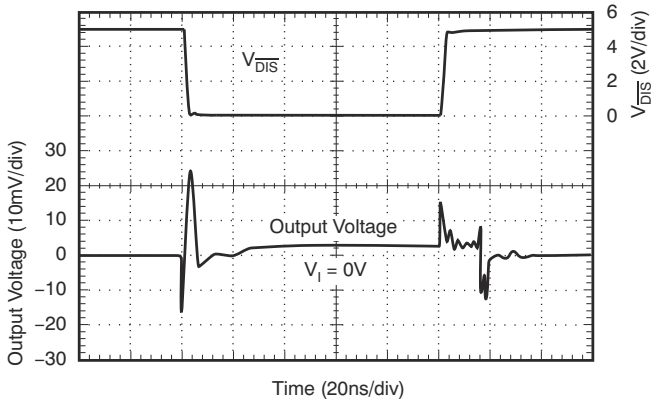

図 6-54. Enable or Disable Glitch

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6.11 Typical Characteristics: OPA690ID, V_S = ±5V (continued)

at T_A = 25°C, G = 2, R_F = 402Ω, and R_L = 100Ω (unless otherwise noted); see 図 7-1 for ac performance only

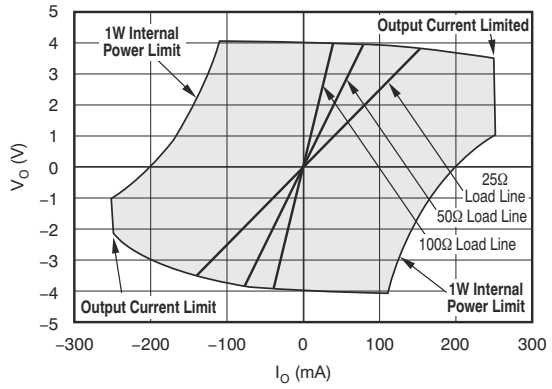

図 6-55. Output Voltage and Current Limitations

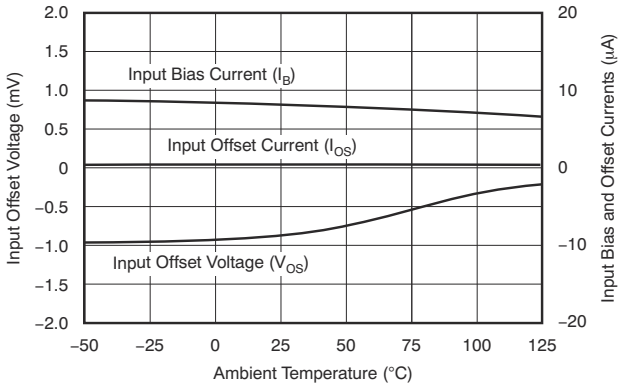

図 6-56. Typical DC Drift Over Temperature

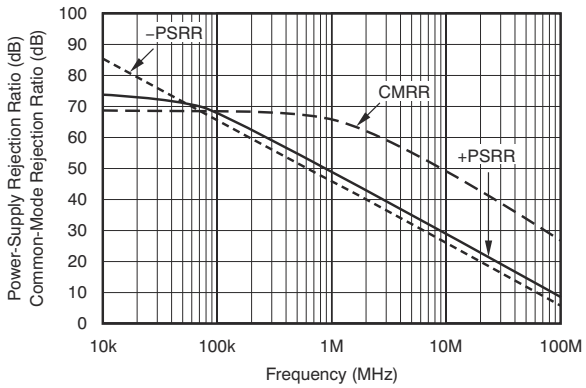

図 6-57. Common−Mode Rejection Ratio and Power−Supply Rejection Ratio vs Frequency

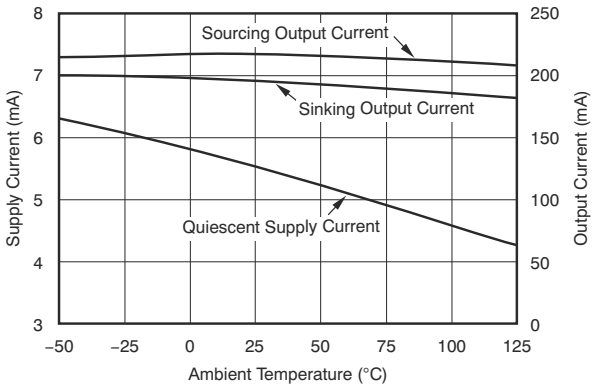

図 6-58. Supply and Output Currents vs Temperature

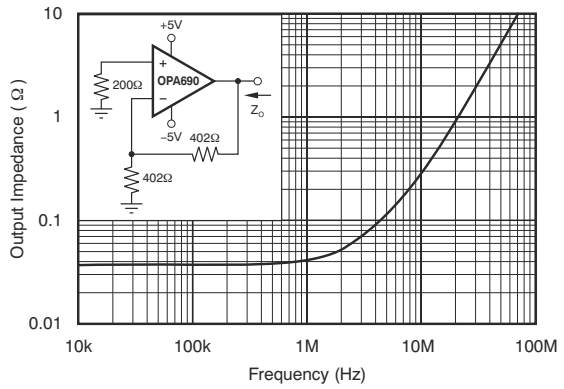

図 6-59. Closed-Loop Output Impedance vs Frequency

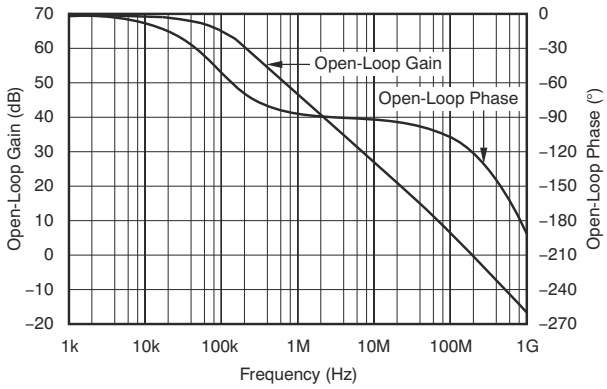

図 6-60. Open−Loop Gain and Phase

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6.11 Typical Characteristics: OPA690ID, V_S = ±5V (continued)

at T_A = 25°C, G = 2, R_F = 402Ω, and R_L = 100Ω (unless otherwise noted); see 図 7-1 for ac performance only

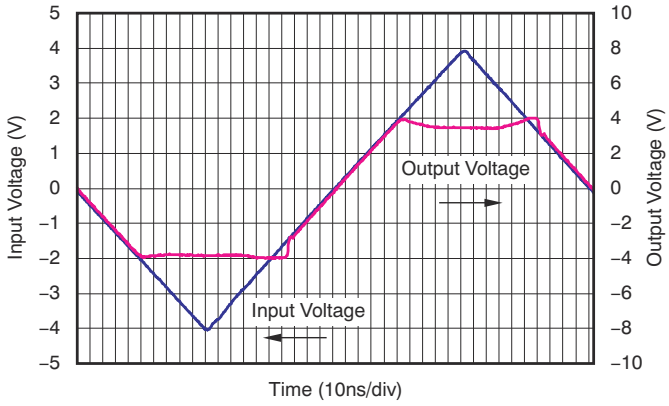

図 6-61. Noninverting Overdrive Recovery

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6.12 Typical Characteristics: OPA690ID, V_S = 5V

at T_A = 25°C, G = 2, R_F = 402Ω, and R_L = 100Ω (unless otherwise noted); see 図 7-2 for ac performance only

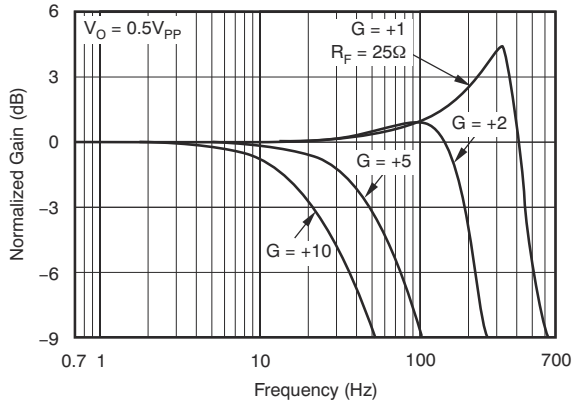

図 6-62. Small-Signal Frequency Response

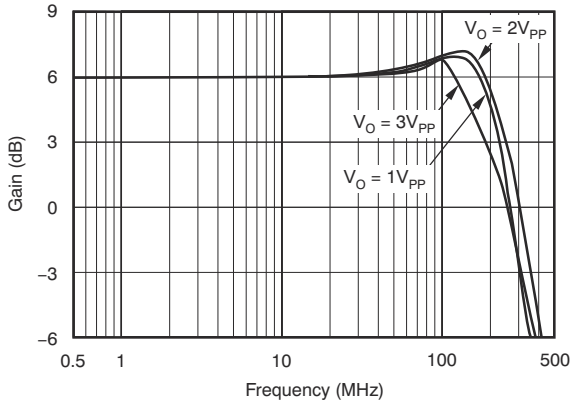

図 6-63. Large-Signal Frequency Response

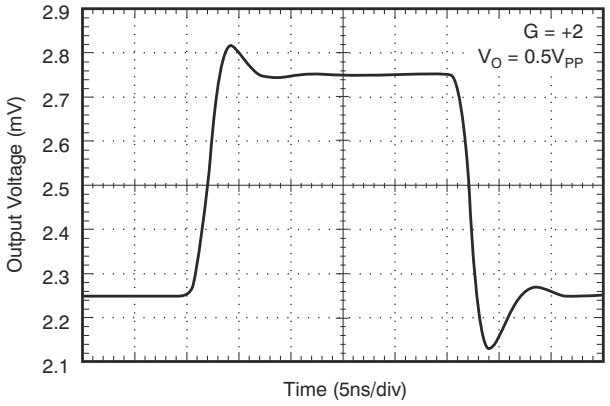

図 6-64. Small-Signal Pulse Response

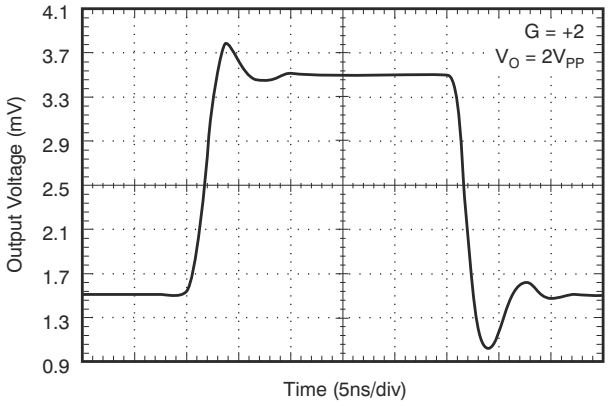

図 6-65. Large-Signal Pulse Response

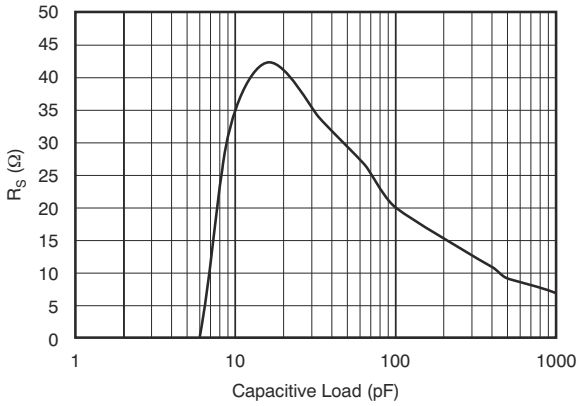

図 6-66. Recommended R_S vs Capacitive Load

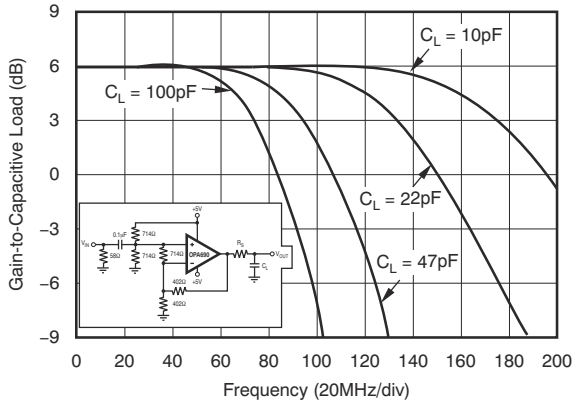

図 6-67. Frequency Response vs Capacitive Load

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6.12 Typical Characteristics: OPA690ID, V_S = 5V (continued)

at T_A = 25°C, G = 2, R_F = 402Ω, and R_L = 100Ω (unless otherwise noted); see 図 7-2 for ac performance only

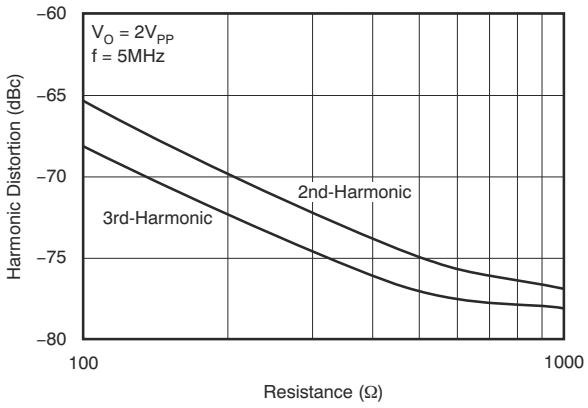

図 6-68. Harmonic Distortion vs Load Resistance

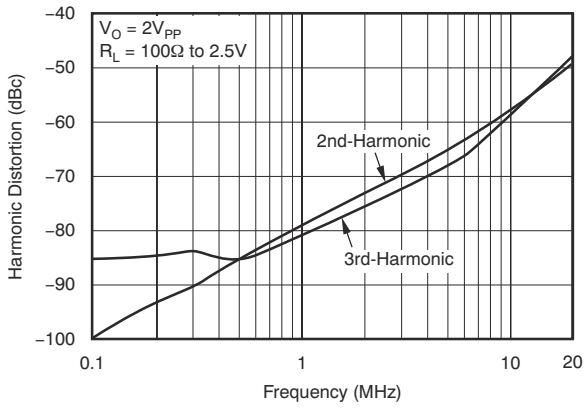

図 6-69. Harmonic Distortion vs Frequency

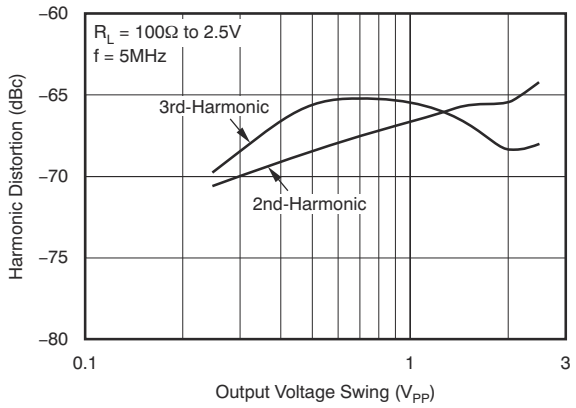

図 6-70. Harmonic Distortion vs Output Voltage

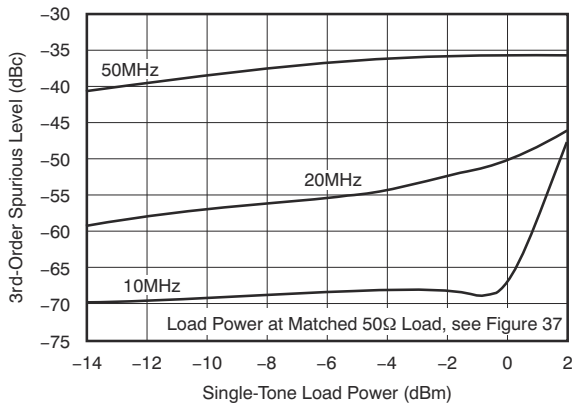

図 6-71. Two-Tone, 3rd-Order Intermodulation Spurious

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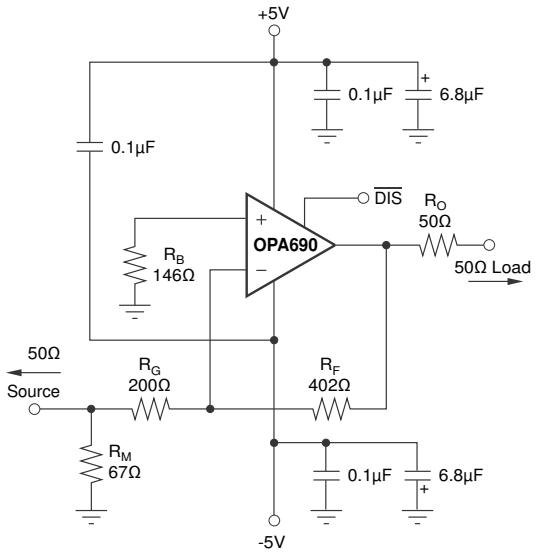
7 Detailed Description

7.1 Overview

The OPA690 provides an exceptional combination of high output power capability with a wideband, unity-gain stable voltage-feedback op amp using a new high slew-rate input stage. The input stage provides a very high slew rate (1900 V/µs) while consuming relatively low quiescent current (6.1 mA). This exceptional full-power performance comes at the price of a slightly higher input noise voltage than alternative architectures. The 4.6-nV/√Hz input voltage noise for the OPA690 is exceptionally low for this type of input stage.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Wideband Voltage-Feedback Operation

Typical differential input stages used for voltage-feedback op amps are designed to steer a fixed-bias current to the compensation capacitor, setting a limit to the achievable slew rate. The OPA690 uses a new input stage that places the transconductance element between two input buffers, using the output currents as the forward signal.

図 7-1 shows the dc-coupled, gain of 2 V/V, dual power-supply circuit configuration used as the basis of the *セクション 6.11*. For test purposes, the input impedance is set to 50 Ω with a resistor to ground and the output impedance is set to 50 Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins, while output powers (dBm) are at the matched 50-Ω load. For the circuit of 図 7-1, the total effective load is 100 Ω || 804 Ω. The disable control line is typically left open to maintain normal amplifier operation. An additional resistor (175 Ω) is included in series with the noninverting input. Combined with the 25-Ω DC source resistance looking back towards the signal generator, this gives an input bias current canceling resistance that matches the 200-Ω source resistance seen at the inverting input (see *セクション 8.1.8*). In addition to the usual power-supply decoupling capacitors to ground, a 0.1-µF capacitor is included between the two power-supply pins. In practical printed-circuit board (PCB) layouts, this optional-added capacitor typically improves the 2nd-harmonic distortion performance.

図 7-2 shows the AC-coupled, gain of 2, single-supply circuit configuration which is the basis of the 5 V and *セクション 6.12*. Although not a rail-to-rail design, the OPA690 requires minimal input and output voltage headroom compared to other very wideband voltage-feedback op amps. The device delivers a 3-V_{PP} output swing on a single 5-V supply with > 120-MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output. The circuit of 図 7-2 establishes an input midpoint bias using a simple resistive divider from the 5-V supply (two 698-

Ω resistors). The input signal is then ac-coupled into the midpoint voltage bias. The input voltage can swing to within 1.5 V of either supply pin, giving a 2-V_{PP} input signal range centered between the supply pins. The input impedance matching resistor (59 Ω) used for testing is adjusted to give a 50-Ω input load when the parallel combination of the biasing divider network is included.

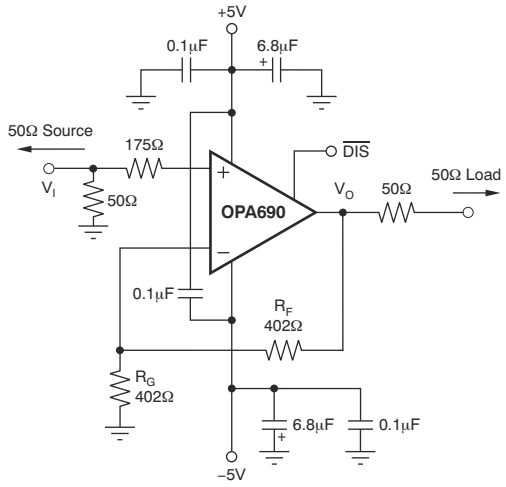

図 7-1. DC-Coupled, G = 2 V/V, Bipolar-Supply Specification and Test Circuit

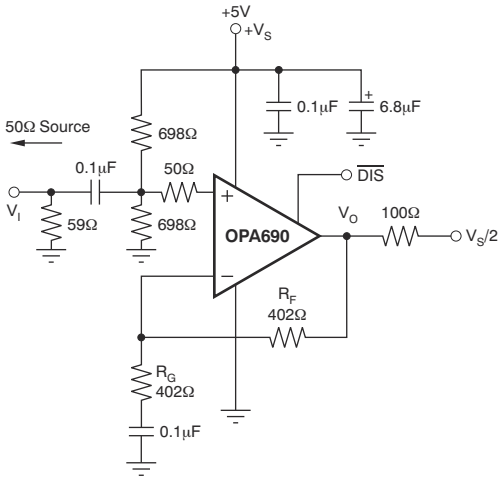

図 7-2. AC-Coupled, G = 2 V/V, Single-Supply Specification and Test Circuit

Again, an additional resistor (50 Ω in this case) is included directly in series with the noninverting input. This minimum recommended value provides part of the dc source resistance matching for the noninverting input bias current. The additional resistor is also used to form a simple parasitic pole to roll off the frequency response at very high frequencies (> 500 MHz) using the input parasitic capacitance to form a band-limiting pole. The gain resistor (R_G) is ac-coupled, giving the circuit a dc gain of 1, which puts the input dc bias voltage (2.5 V) at the output as well. The output voltage can swing to within 1 V of either supply pin while delivering > 100-mA output current. A demanding 100-Ω load to a midpoint bias is used in this characterization circuit. The new output stage circuit used in the OPA690 can deliver large output currents into this midpoint load with minimal crossover distortion .

7.3.2 Input and ESD Protection

The OPA690 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in セクション 6.1. All device pins are protected with internal ESD protection diodes to the power supplies. 図 7-3 shows the internal ESD protection.

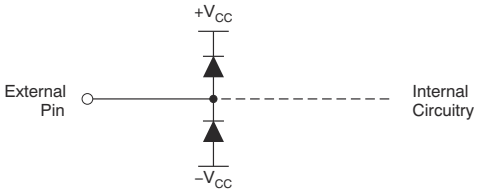

図 7-3. Internal ESD Protection

These diodes also provide moderate protection to input overdrive voltages greater than the supplies. The protection diodes can typically support 10 mA of continuous current. Where higher currents are possible (for example, in systems with ±15-V supply parts driving into the OPA690), add current-limiting series resistors into the two inputs. Keep these resistor values as low as possible, because high values degrade both noise performance and frequency response.

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7.4 Device Functional Modes

7.4.1 Disable Operation

The OPA690 provides an optional disable feature that can be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{DIS}$ control pin is unconnected, the OPA690 operates normally. To disable, assert the control pin low. 図 7-4 shows a simplified internal circuit for the disable control feature.

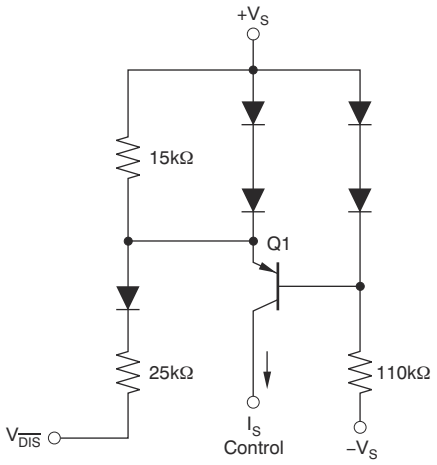

図 7-4. Simplified Disable Control Circuit

The supply current in the disable mode are only those required to operate the circuit of 図 7-4. Additional circuitry enables a faster turn-on time than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high-impedance state. If the OPA690 is operating at a gain of 1, the device shows a very high impedance at the output and exceptional signal isolation. If operating at a gain greater than 1, the total feedback network resistance (R_F + R_G) appears as the impedance looking back into the output, but the circuit still shows very high forward and reverse isolation. If configured as an inverting amplifier, the input and output is connected through the feedback network resistance (R_F + R_G) and the isolation is very poor as a result.

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8 Application and Implementation

注

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8.1 Application Information

8.1.1 Bandwidth Versus Gain: Noninverting Operation

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the gain bandwidth product (GBP) shown in セクション 6.5 and セクション 6.7. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) predicts the closed-loop bandwidth. In practice, this relationship only holds true when the phase margin approaches 90°, as in high-gain configurations. At low gains (increased feedback factors), most amplifiers exhibit a more complex response with lower phase margin. The OPA690 is compensated to give a slightly peaked response in a noninverting gain of 2 V/V (see 図 7-1). This compensation results in a typical gain of 2 bandwidth of 220 MHz, far exceeding that predicted by dividing the 300 MHz GBP by 2. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of 10, the 30-MHz bandwidth shown in the ±5-V *Electrical Characteristics* agrees with that predicted using the simple formula and the typical GBP of 300 MHz.

The frequency response in a gain of 2 V/V can be modified to achieve exceptional flatness by simply increasing the noise gain to 2.5. One method, without affecting the two signal gain, is to add an 804-Ω resistor across the two inputs in the circuit of 図 7-1. A similar technique can be used to reduce peaking in unity-gain (voltage-follower) applications. For example, by using a 402-Ω feedback resistor along with a 402-Ω resistor across the two op amp inputs, the voltage follower response is similar to the gain of 2 response of 図 7-2. Reduce the value of the resistor across the op amp inputs to further limit the frequency response due to increased noise gain.

8.1.2 Inverting Amplifier Operation

The OPA690 is a general-purpose, wideband voltage-feedback op amp; therefore, all of the familiar op amp application circuits are available to the designer. Inverting operation is one of the more common requirements and offers several performance benefits. 図 8-1 shows a typical inverting configuration where the I/O impedances and signal gain from 図 7-1 are retained in an inverting circuit configuration.

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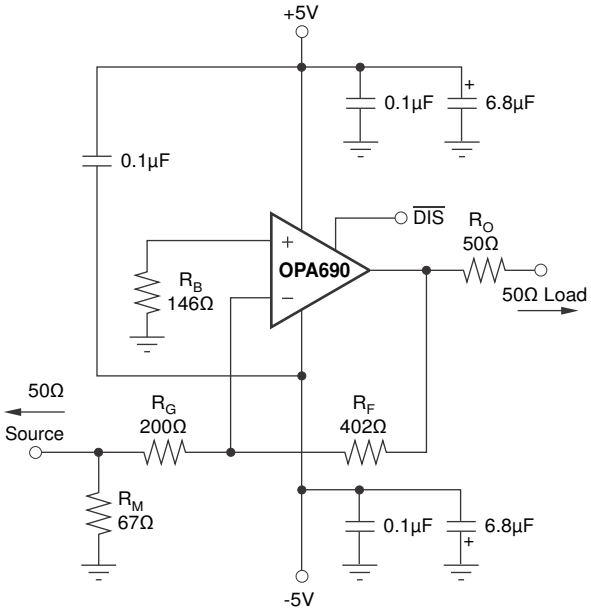

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図 8-1. Gain of –2 V/V Example Circuit

In the inverting configuration, be aware of three key design considerations. The first consideration is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted-pair, long PCB trace, or other transmission line conductor), R_G can be set equal to the required termination value and R_F adjusted to give the desired gain. This configuration is the simplest approach and results in optimized bandwidth and noise performance. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2 V/V, setting R_G to 50 Ω for input matching eliminates the requirement for R_M but requires a 100-Ω feedback resistor. This configuration has an interesting advantage: the noise gain becomes equal to 2 for a 50-Ω source impedance—the same as the noninverting circuits considered in the previous section. The amplifier output, however, now sees the 100-Ω feedback resistor in parallel with the external load. In general, limit the feedback resistor to the 200-Ω to 1.5-kΩ range. In this case, increase both the R_F and R_G values, as shown in 図 8-1, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and influences the bandwidth. For the example in 図 8-1, the R_M value combines in parallel with the external 50-Ω source impedance, yielding an effective driving impedance of 50 Ω || 67 Ω = 28.6 Ω. This impedance is added in series with R_G for calculating the noise gain (NG). The resultant NG is 2.8 for 図 8-1, as opposed to only 2 if R_M can be eliminated as discussed previously. Therefore, the bandwidth is slightly less for the circuit of 図 8-1 than for the gain of 2 circuit of 図 7-1.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input (R_B). If this resistor is set equal to the total dc resistance looking out of the inverting node, the output dc error, due to the input bias currents, is reduced to (Input Offset Current) × R_F. If the 50-Ω source impedance is dc-coupled in 図 8-1, the total resistance to ground on the inverting input is 228 Ω. Combining this in parallel with the feedback resistor gives the R_B = 146 Ω used in this example. To reduce the additional high-frequency noise introduced by this resistor, the resistor is sometimes bypassed with a capacitor. As long as R_B < 350 Ω, the capacitor is not required because the total noise contribution of all other terms is less than that of the op-amp input noise voltage. As a minimum, the OPA690 requires an R_B value of 50 Ω to damp out parasitic-induced peaking that is a direct short to ground on the noninverting input, and runs the risk of a very high-frequency instability in the input stage.

8.1.3 Optimizing Resistor Values

Because the OPA690 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values can be used for the feedback and gain-setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, make the feedback connection with a 25-Ω resistor, not a direct short. This connection isolates the inverting input capacitance from the output pin and improves the frequency response flatness. Usually, for G > 1 V/V applications, the feedback-resistor value must be between 200 Ω and 1.5 kΩ. For values less than 200 Ω, the feedback network presents additional output loading that can degrade the harmonic distortion performance of the OPA690.

A good practice is to target the parallel combination of R_F and R_G (see 図 7-1) to be less than approximately 300 Ω. The combined impedance R_F || R_G interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus, a zero in the forward response. Assuming a 2-pF total parasitic on the inverting node, holding R_F || R_G < 300 Ω keeps this pole greater than 250 MHz. Alone, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This result is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

8.1.4 Output Current and Voltage

The OPA690 provides output voltage and current capabilities that are unsurpassed in a low-cost monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1 V to either supply rail. Into a 15-Ω load (the minimum tested load), the device delivers more than ±160 mA.

The specifications described previously, though familiar in the industry, consider voltage and current limits separately. In many applications, the voltage × current, or V-I product is more relevant to circuit operation. See also 図 6-55, the output voltage and current limitations plot in セクション 6.11. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA690 output drive capabilities, noting that the graph is bounded by a safe operating area of 1-W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA690 can drive ±2.5 V into 25 Ω or ±3.5 V into 50 Ω without exceeding the output capabilities or the 1-W dissipation limit. A 100-Ω load line (the standard test circuit load) shows the full ±3.9-V output swing capability; see also セクション 6.11.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold start-up do the output current and voltage decrease to the numbers shown in セクション 6.5 and セクション 6.7. As the output transistors deliver power, the junction temperatures increase, decreasing the V_{BE}s (increasing the available output voltage swing) and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the overtemperature specifications because the output stage junction temperatures is greater than the minimum specified operating ambient.

To protect the output stage from accidental shorts to ground and the power supplies, output short-circuit protection is included in the OPA690. The circuit acts to limit the maximum source or sink current to approximately 250 mA.

8.1.5 Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that can be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA690 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series-isolation resistor between the amplifier output and the capacitive load. This configuration does not eliminate the pole from the loop response, but rather shifts the pole and adds a zero at a higher frequency.

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The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The typical characteristics show the recommended R_S versus capacitive load (図 6-51 for ±5 V and 図 6-66 for 5 V), and the resulting frequency response at the load. Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the OPA690. Long PCB traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA690 output pin (see *セクション 8.4.1*).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For the OPA690 operating in a gain of 2, the frequency response at the output pin is already slightly peaked without the capacitive load requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain reduces the peaking as described previously. The circuit of 図 8-2 demonstrates this technique, allowing lower values of R_S to be used for a given capacitive load.

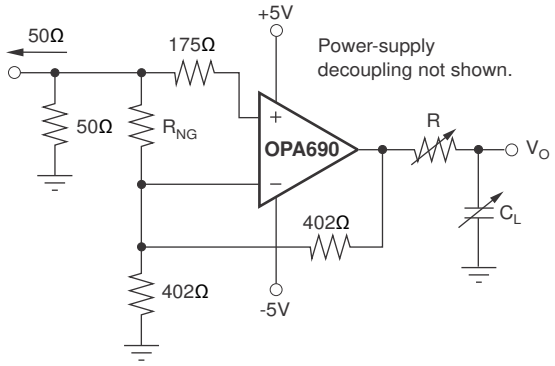

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図 8-2. Capacitive Load Driving With Noise Gain Tuning

This gain of 2 V/V circuit includes a noise gain tuning resistor across the two inputs to increase the noise gain, increasing the unloaded phase margin for the op amp. Although this technique reduces the required R_S resistor for a given capacitive load, this technique does increase the noise at the output. This technique also decreases the loop gain, slightly decreasing the distortion performance. If, however, the dominant distortion mechanism arises from a high R_S value, significant dynamic range improvement can be achieved using this technique. 図 8-3 shows the required R_S versus C_{LOAD} parametric on noise gain using this technique. This is the circuit of 図 8-2 with R_{NG} adjusted to increase the noise gain (increasing the phase margin) then sweeping C_{LOAD} and finding the required R_S to get a flat frequency response. This plot also gives the required R_S versus C_{LOAD} for the OPA690 operated at higher signal gains.

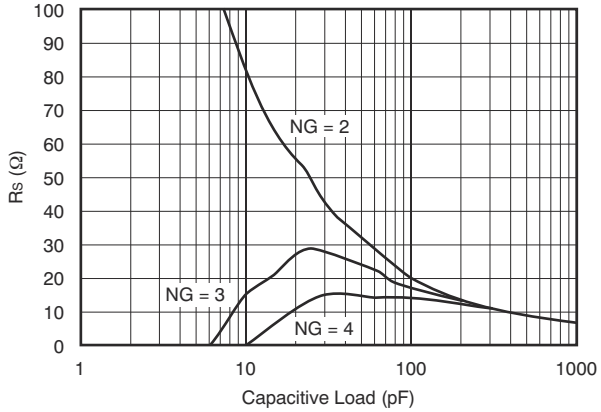

図 8-3. Required R_S vs Noise Gain

8.1.6 Distortion Performance

The OPA690 provides good distortion performance into a 100-Ω load on ±5-V supplies. Relative to alternative solutions, this device provides exceptional performance into lighter loads, while operating on a single 5-V supply. Increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see 図 7-1), this total load is sum of R_F + R_G, while in the inverting configuration the total load is just R_F. Also, providing an additional supply-decoupling capacitor (0.1 µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion.

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The new output stage used in the OPA690 actually holds the difference between fundamental power and the 2nd- and 3rd-harmonic powers relatively constant with increasing output power until very large output swings are required (> 4 V_{PP}). This feature also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are moderately low at low output power levels. The output stage continues to hold the distortion levels low even as the fundamental power reaches very high levels. セクション 6.11 shows that the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20 MHz, with 10 dBm/tone into a matched 50-Ω load (that is, 2 V_{PP} for each tone at the load, which requires 8 V_{PP} for the overall two-tone envelope at the output pin), 図 6-50 shows 47-dBc difference between the test tone powers and the 3rd-order intermodulation spurious powers. This performance improves further when operating at lower frequencies.

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8.1.7 Noise Performance

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve a slew rate at the expense of a higher input noise voltage. The 5.5-nV/√Hz input voltage noise for the OPA690 is, however, much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. 図 8-4 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

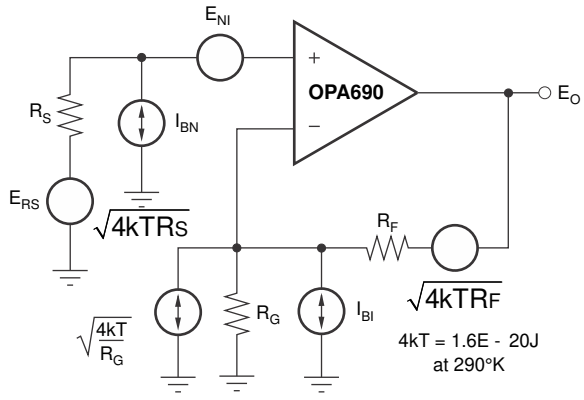

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図 8-4. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. 式 1 shows the general form for the output noise voltage using the terms shown in 図 8-4.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (1)$$

Dividing this expression by the noise gain [NG = (1 + R_F/R_G)] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in 式 2.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

Evaluating these two equations for the OPA690 circuit and component values (see 図 7-1) gives a total output spot noise voltage of 12.3 nV/√Hz and a total equivalent input spot noise voltage of 6.1 nV/√Hz. This is including the noise added by the bias current cancellation resistor (175 Ω) on the noninverting input. This total input-referred spot noise voltage is only slightly higher than the 5.5-nV/√Hz specification for the op amp voltage noise alone. This is the case as long as the impedances appearing at each op amp input are limited to the previously recommend maximum value of 300 Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 300 Ω satisfies both noise and frequency response flatness considerations. Because the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_B) for the inverting op amp configuration of 図 8-1 is not required.

8.1.8 DC Accuracy and Offset Control

The balanced input stage of a wideband voltage-feedback op amp allows good output dc accuracy in a wide variety of applications. Although the high-speed input stage does require relatively high input bias current (typically ±8 µA at each input terminal), the close matching can be used to reduce the output dc error caused by this current. The total output offset voltage can be considerably reduced by matching the dc source resistances appearing at the two inputs. This matching reduces the output dc error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of 図 7-1, and using worst-case 25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

–(NG = noninverting signal gain)

$\pm(NG \times V_{OS(MAX)}) \pm (R_F \times I_{OS(MAX)})$

$= \pm(2 \times 4\ mV) \pm (402\ \Omega \times 1\ \mu A)$

$= \pm 8.4\ mV$

A fine-scale output offset null, or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc offset control into an op-amp circuit. Most of these techniques eventually reduce to adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input can be considered. However, the dc offset voltage on the summing junction sets up a dc current back into the source that must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a dc-coupled inverting amplifier, see 図 8-5 for one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the dc offsetting current is brought into the inverting input node through resistor values that are much greater than the signal path resistors. This circuit configuration has minimal effect on the loop gain, and therefore, the frequency response.

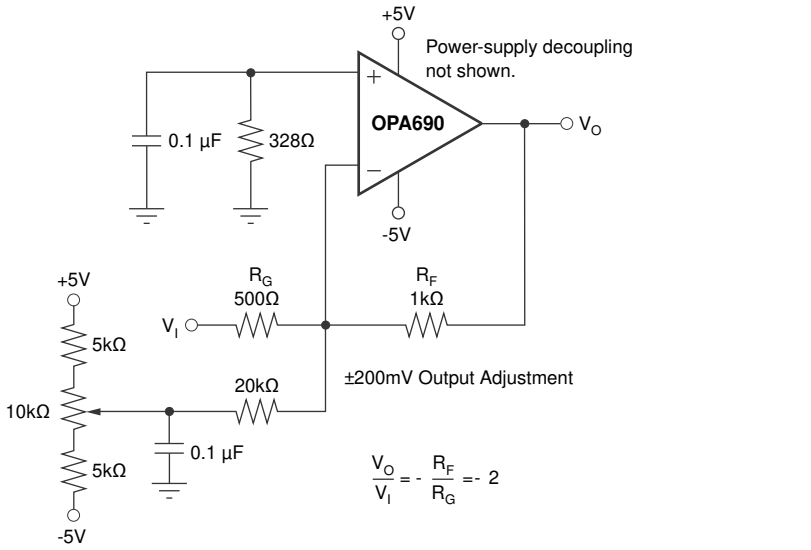

図 8-5. DC-Coupled, Inverting Gain of –2 V/V, With Offset Adjustment

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8.1.9 Thermal Analysis

As a result of the high output power capability of the OPA690, sinking heat or forced airflow can be required under extreme operating conditions. Maximum desired junction temperature sets the maximum allowed internal power dissipation. In no case can the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times R_{\theta JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies) under the condition in 式 3.

$$P_{DL} = V_S{}^2 / (4 \times R_L) \quad (3)$$

where

- R_L includes feedback network loading

注

The power in the output stage and not into the load determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA690-DBV (6-pin SOT-23 package) in the circuit of 図 7-1 operating at the maximum specified ambient temperature of 85°C and driving a grounded 20-Ω load.

$$P_D = 10\ V \times 6.2\ mA + 5^2 / (4 \times (20\ \Omega \parallel 804\ \Omega)) = 382\ mW \quad (4)$$

$$\text{Maximum } T_J = 85°C + (0.38\ W \times 150°C/W) = 142°C \quad (5)$$

Although this result is still much less than the specified maximum junction temperature, system reliability considerations can require lower tested junction temperatures. The highest possible internal dissipation occurs if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors. 図 6-55, the output V-I plot shown in *セクション 6.11*, include a boundary for 1-W maximum internal power dissipation under these conditions.

8.2 Typical Applications

8.2.1 High-Performance DAC Transimpedance Amplifier

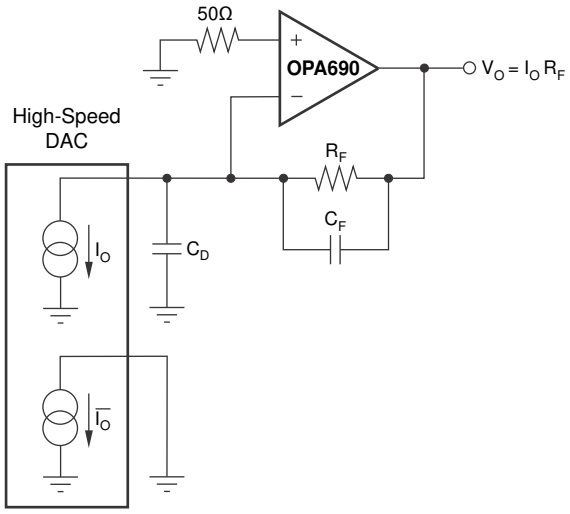

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図 8-6. DAC Transimpedance Amplifier

8.2.1.1 Design Requirements

High-frequency, direct digital synthesis (DDS) digital-to-analog converters (DACs) require a low-distortion output amplifier to retain SFDR performance into real-world loads. See 図 8-6 for a single-ended output drive implementation.

8.2.1.2 Detailed Design Procedure

In this circuit, only one side of the complementary output drive signal is used. 図 8-6 shows the signal output current connected into the virtual ground summing junction of the OPA690, which is set up as a transimpedance stage or *I-V converter*. The unused current output of the DAC is connected to ground. If the DAC requires that the outputs terminate to a compliance voltage other than ground for operation, the appropriate voltage level can be applied to the noninverting input of the OPA690. The dc gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance produces a zero in the noise gain for the OPA690 that can cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, set the pole in the feedback network to 式 6.

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \tag{6}$$

式 6 gives a closed-loop transimpedance bandwidth, f_{-3dB}, of approximately 式 7.

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \tag{7}$$

where

- GBP = gain bandwidth product (Hz) for the OPA690

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8.2.2 Single-Supply Active Filters

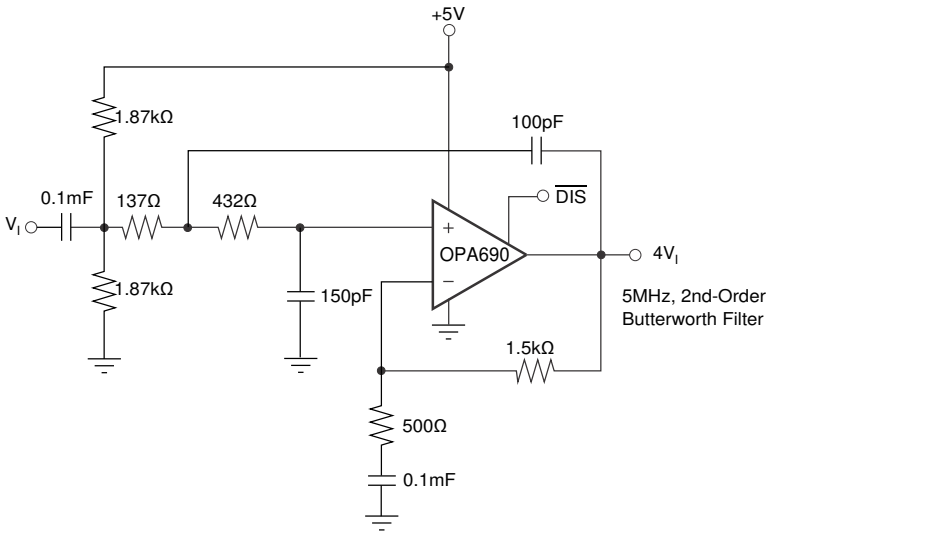

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図 8-7. Single-Supply, High-Frequency Active Filter

8.2.2.1 Design Requirements

The high bandwidth provided by the OPA690, while operating on a single 5-V supply, works well with high-frequency active filter designs. Again, the key additional requirement is to establish the dc operating point of the signal near the supply midpoint for highest dynamic range. See 図 8-7 for an example design of a 5-MHz low-pass Butterworth filter using the Sallen-Key topology.

Both the input signal and the gain setting resistor are ac-coupled using 0.1-µF blocking capacitors (actually giving band-pass response with the low-frequency pole set to 32 kHz for the component values shown). As discussed for 図 7-2, this allows the midpoint bias formed by the two 1.87-kΩ resistors to appear at both the input and output pins. The midband signal gain is set to 4 (12 dB) in this case. The capacitor to ground on the noninverting input is intentionally set larger to dominate input parasitic terms. At a gain of 4, the OPA690 on a single supply shows approximately 80-MHz small- and large-signal bandwidth. The resistor values are slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit show a precise 5-MHz, −3-dB point with a maximally flat pass band (greater than the 32-kHz ac-coupling corner), and a maximum stop-band attenuation of 36 dB at the −3-dB bandwidth of 80 MHz of the amplifier.

8.2.2.2 Application Curve

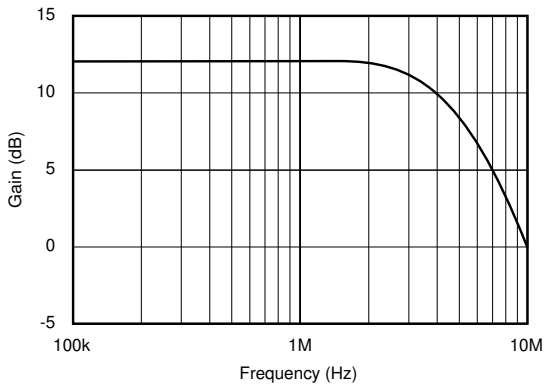

図 8-8. 5-MHz, 2nd-Order Butterworth Filter Response

8.2.3 High-Power Line Driver

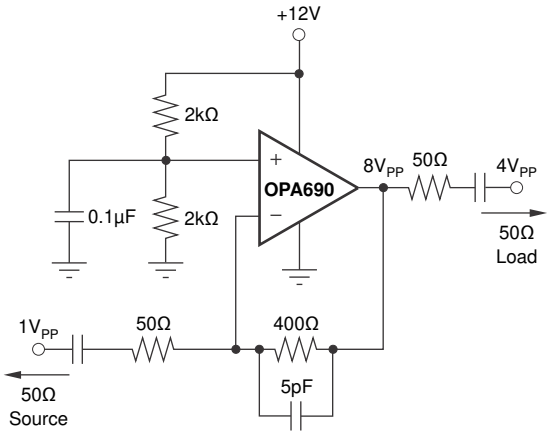

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図 8-9. High-Power Coax Line Driver

8.2.3.1 Design Requirements

The large output swing capability of the OPA690 and the high current capability allow the device to drive a 50-Ω line with a peak-to-peak signal up to 4 V_{PP} at the load, or 8 V_{PP} at the output of the amplifier using a single 12-V supply. 図 8-9 shows such a circuit set for a gain of 8 to the output or 4 to the load.

The 5-pF capacitor in the feedback loop provides added bandwidth control for the signal path.

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8.3 Power Supply Recommendations

The OPA690 is principally intended to work in a supply range of ±2.5 V to ±6 V. Good power-supply bypassing is required. Minimize the distance (< 0.1 inch) from the power-supply pins to high frequency, 0.1-µF decoupling capacitors. Often a larger capacitor (2.2 µF is typical) is used along with a high-frequency, 0.1-µF supply decoupling capacitor at the device supply pins.

For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors somewhat farther from the device and share these capacitors among several devices in the same area of the PCB.

Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second harmonic distortion performance.

8.4 Layout

8.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA690 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

1. Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance, open a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, ensure that the ground and power planes are unbroken elsewhere on the board.
2. Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1-µF decoupling capacitors. At the device pins, ensure that the ground and power-plane layout is not in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Always decouple the power-supply connections with these capacitors. An optional supply decoupling capacitor (0.1-µF) across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Also, use larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequencies, on the main supply pins. Place these decoupling capacitors somewhat farther from the device and share these capacitors among several devices in the same area of the PCB.
3. Careful selection and placement of external components preserve the high-frequency performance of the OPA690. Use very low reactance type resistors. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB traces as short as possible. Never use wire-wound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Place other network components, such as noninverting input termination resistors, close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 1.5 kΩ, this parasitic capacitance can add a pole or zero below 500 MHz that can affect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 402-Ω feedback is a good starting point for design. A 25-Ω feedback resistor, rather than a direct short, is suggested for the unity-gain follower application. This configuration effectively isolates the inverting input capacitance from the output pin that can otherwise cause an additional peaking in the gain of 1 frequency response.
4. Connections to other wideband devices on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils or 1.27 mm to 100 mils or 2.54 mm), preferably with ground and power planes opened up around the traces. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load* (図 6-51 for ±5 V and 図 6-66 for 5 V). Low parasitic capacitive loads (< 5 pF) do not always require an R_S because the OPA690 is nominally compensated to

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operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary on board, and in fact, a higher impedance environment improves distortion (see also the distortion versus load plots). With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA690 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; set this total effective impedance to match the trace impedance. The high output voltage and current capability of the OPA690 allows multiple destination devices to be handled as separate transmission lines, each with series and shunt terminations. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value (see also the *Recommended R_S vs Capacitive Load* plot (図 6-51 for ±5 V and 図 6-66 for 5 V). This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

5. Socketing a high-speed part like the OPA690 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the OPA690 onto the board.

8.4.2 Layout Example

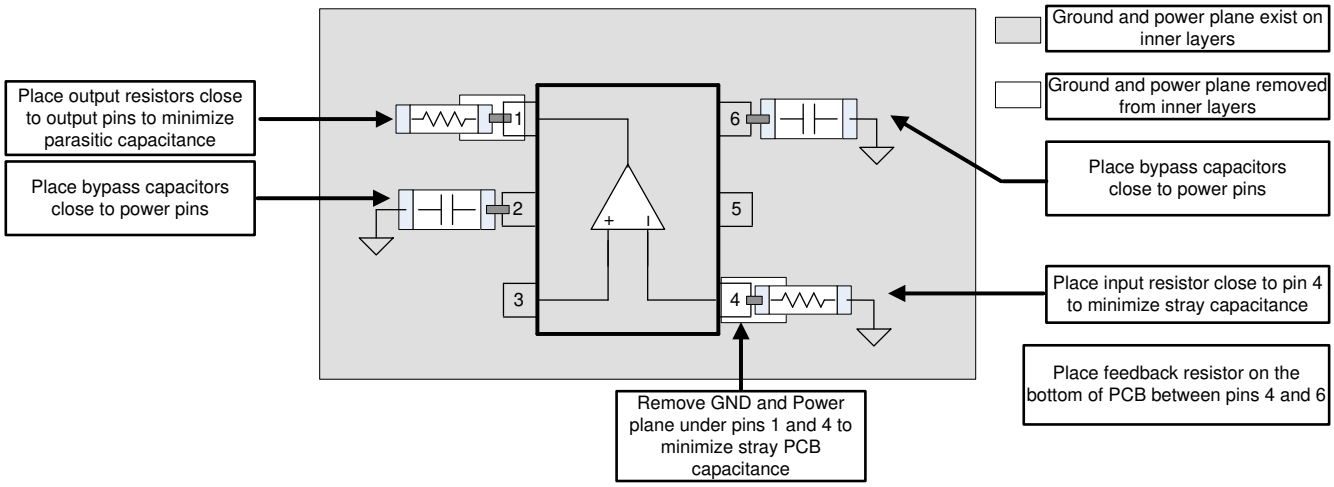

図 8-10. OPA690 Layout

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Macromodels and Applications Support

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. Spice is particularly helpful for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA690 is available through the OPA690 product folder under *Simulation Models*. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. The models do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types small-signal ac performance.

9.1.2 Demonstration Fixtures

Two printed-circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA690 in the two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in 表 9-1.

表 9-1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA690ID	8-pin SOIC	DEM-OPA-SO-1A	SBOU009
OPA690IDBV	6-pin SOT-23	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA690 product folder.

9.2 ドキュメントの更新通知を受け取る方法

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (August 2016) to Revision H (October 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「特長」を更新 ... 1
- 「*概要*」を更新 ... 1
- 表紙の図を更新 ... 1
- Updated *Device Comparison Table* ... 2
- Changed designator from DRB to DBV (typo) in Table 5-1, *Pin Functions* ... 3
- Added Supply turn-on and turn-off rate and continuous input current specifications to Absolute Maximum Ratings table ... 4
- Updated footnote on Absolute Maximum Ratings table to add additional clarification ... 4
- Changed Junction temperature specification from 175°C to 150°C in Absolute Maximum Ratings table ... 4
- Deleted Machine Model (MM) specification from ESD Ratings table ... 4
- Updated thermal specifications for DBV package in Thermal Information table ... 4
- Changed designator from DRB to DBV (typo) in Thermal Information ... 4
- Added new Electrical Characteristics tables for OPA690IDBV package ... 5
- Updated Electrical Characteristics: OPA690IDBV, ±5 V AC Performance section with improved typical small-signal bandwidth, large-signal bandwidth, slew rate, voltage noise, and distortion parameters ... 5
- Added T_A ≅ 25°C and input and output reference voltages to the default test conditions across all Electrical Characteristics sections ... 5
- Deleted 0°C to +70°C conditions across all Electrical Characteristics sections ... 5
- Deleted minimum specifications and over temperature specifications across all Electrical Characteristics: AC Performance sections ... 5
- Changed typical Bandwidth for 0.1-dB gain flatness typical value from 30 MHz to 25 MHz in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed Peaking at gain of 1 V/V from 4 dB to 1 dB in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical Large signal bandwidth condition from VO < 0.5 VPP to VO = 2 VPP in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical rise and fall time at 5 V-step from 2.8 ns to 2.3 ns at 4 V-step in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical 0.02% settling time from 12 ns to 13 ns Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical 2-nd harmonic distortion at 100 Ω from –68 dBc to –85 dBc in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical 2-nd harmonic distortion at 500 Ω from –77 dBc to –85 dBc in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical 3-nd harmonic distortion at 100 Ω from –70 dBc to –75 dBc in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical 3-nd harmonic distortion at 500 Ω from –81 dBc to –90 dBc in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical input voltage noise from 5.5 nV/√Hz to 4.6 nV/√Hz in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical input current noise from 3.1 pA/√Hz to 1.7 pA/√Hz in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical open-loop voltage gain from 69 dB to 78 dB in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical input offset voltage from ±1 mV to ±0.3 mV in Electrical Characteristics: OPA690IDBV, ±5 V 5
- Changed typical input bias current from ±3 µA to ±1 µA in Electrical Characteristics: OPA690IDBV, ±5 V ... 5
- Changed typical input offset current from ±0.1 µA to ±0.05 µA in Electrical Characteristics: OPA690IDBV, ±5 V ... 5

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- Changed typical Common-mode input voltage from ±3.5 V to ±3.85 V in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Common-mode rejection ratio from 65 dB to 80 dB in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Input impedance differential mode from 190 || 0.6 kΩ || pF to 6 || 0.1 MΩ || pF in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Input impedance differential mode from 3.2 || 0.9 MΩ || pF to 38 || 1 MΩ || pF in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed minimum Output voltage swing at no load from ±3.8 V to ±3.7 V in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Output voltage swing at No load from ±4 V to ±3.9 V in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Output voltage swing at 100 Ω load from ±3.9 V to ±3.85 V in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Current output sourcing from 190 mA to 215 mA in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Current output sinking from –190 mA to –215 mA in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Short circuit current limit from ±250 mA to ±240 mA in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Closed-loop output impedance from 0.04 Ω to 0.01 Ω in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Corrected the polarity of the power down supply current....5
- Changed typical disable time from 200 ns to 600 ns in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Enable time from 25 ns to 40 ns in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical output capacitance in disable from 4 pF to 8 pF in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Disable voltage from 1.8 V to 2.3 V in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed maximum Quiescent current from 5.8 mA to 7 mA in Electrical Characteristics: OPA690IDBV, ±5 V 5
- Changed typical Quiescent current from 5.5 mA to 6.1 mA in Electrical Characteristics: OPA690IDBV, ±5 V.. 5
- Changed minimum Quiescent current from 5.3 mA to 5.2 mA in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed maximum Quiescent current over temperature from 6.6 mA to 7 mA in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Changed typical Power-supply rejection ratio from 75 dB to 86 dB in Electrical Characteristics: OPA690IDBV, ±5 V....5
- Updated the Electrical Characteristics: OPA690IDBV, 5 V AC performance section with improved typical small-signal bandwidth, voltage noise, and distortion parameters....7
- Changed the Peaking at gain of 1 V/V from 5 dB to 1.3 dB in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical Slew rate from 1000 V/µs to 850 V/µs in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical 0.02% settling time from 12 ns to 19 ns Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical 0.1% settling time from 8 ns to 16 ns Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical input voltage noise from 5.6 nV/√Hz to 4.6 nV/√Hz in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical input current noise from 3.2 pA/√Hz to 1.6 pA/√Hz in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical open-loop voltage gain from 63 dB to 77 dB in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical input offset voltage from ±1 mV to ±0.3 mV in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical input bias current from ±3 µA to ±1 µA in Electrical Characteristics: OPA690IDBV, 5 V...7
- Changed the typical input offset current from ±0.3 µA to ±0.05 µA in Electrical Characteristics: OPA690IDBV, 5 V....7

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- Changed the typical Most positive input voltage from 3.5 V to 3.85 V in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical input bias current from ±3 µA to ±1 µA in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical Common-mode rejection ratio from 63 dB to 79 dB in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical Input impedance differential mode from 92 || 1.4 kΩ || pF to 6 || 0.1 MΩ || pF in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical Input impedance common-mode from 2.2 || 1.5 MΩ || pF to 27 || 1.1 MΩ || pF in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the minimum most positive output voltage at no load from 3.8 V to 3.7 V in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical most positive output voltage at no load from 4 V to 3.9 V in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical most positive output voltage at 100 Ω load from 3.9 V to 3.85 V in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the minimum most negative output voltage at no load from 1.2 V to 1.3 V in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical most negative output voltage at no load from 1 V to 1.1 V and at and 100 Ω load from 1.1 V to 1.15 V in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical current output sourcing from 160 mA to 190 mA in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical current output sinking from –160 mA to –190 mA in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical closed-loop output impedance from 0.04 Ω to 0.01 Ω in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical power-down supply current from –100 µA to 75 µA in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical off isolation from 65 dB to 72 dB in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical output capacitance in disable from 4 pF to 8 pF in Electrical Characteristics: OPA690IDBV, 5 V....7
- Deleted the turn-on and turnoff glitch specifications from Electrical Characteristics section....7
- Changed the typical disable voltage from 1.8 V to 2.4 V in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical disable pin input bias current from 75 µA to 60 µA in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the typical quiescent current from 4.9 mA to 6.1 mA in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the maximum quiescent current from 5.44 mA to 6.8 mA in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the maximum quiescent current over temperature from 6.02 mA to 6.9 mA in Electrical Characteristics: OPA690IDBV, 5 V....7
- Changed the power-supply rejection ratio from 72 dB to 85 dB in Electrical Characteristics: OPA690IDBV, 5 V....7
- Deleted *Single-Supply ADC Interface* from *Typical Applications*....38

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- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。....1
- Deleted *Ordering Information* table; see POA at the end of the data sheet....2

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Changes from Revision E (November 2008) to Revision F (February 2010)	Page
• データシート フォーマットを現行の基準に変更	1
• Added 図 6-61, Noninverting Overdrive Recovery plot	20

Changes from Revision D (August 2008) to Revision E (November 2008)	Page
• Deleted obsolete OPA680 from *Related Products* table	2

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA690ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 690
OPA690ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 690
OPA690IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	OAEI
OPA690IDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAEI
OPA690IDBVTG4	NRND	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
OPA690IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 690
OPA690IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 690
OPA690IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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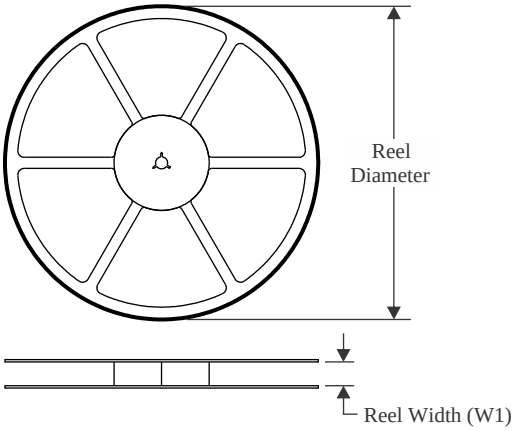
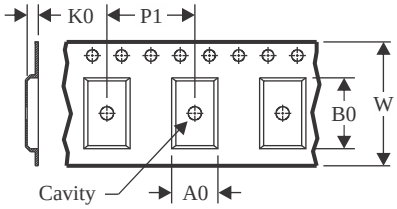
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

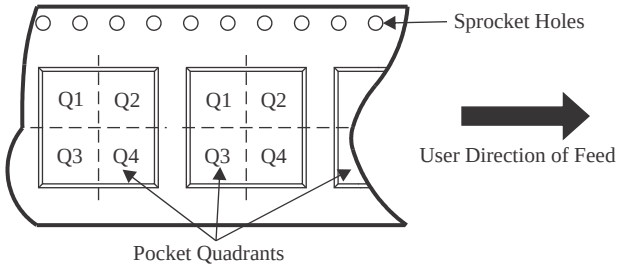


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

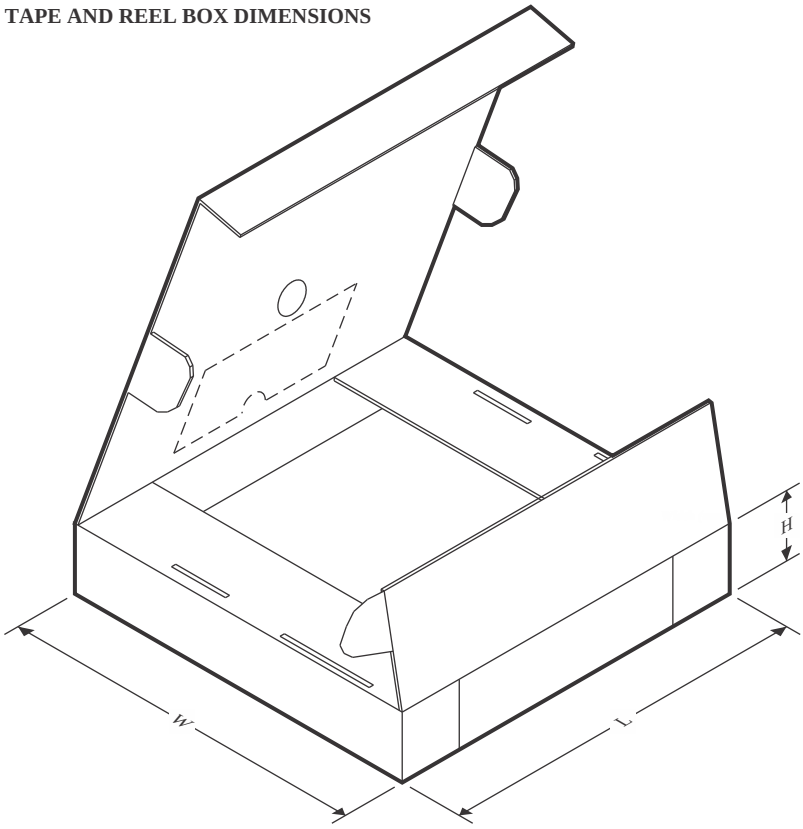
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA690IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA690IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

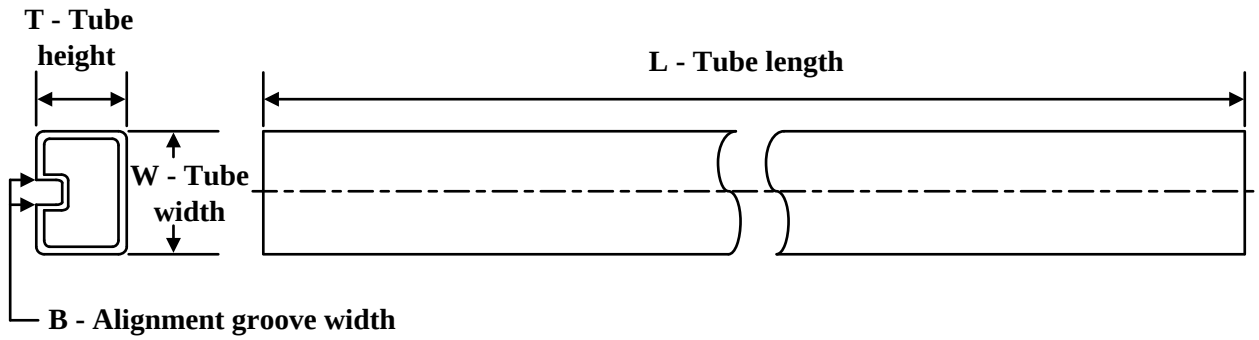
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

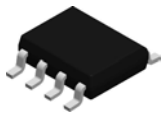
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA690IDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA690IDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA690ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA690ID.A	D	SOIC	8	75	506.6	8	3940	4.32

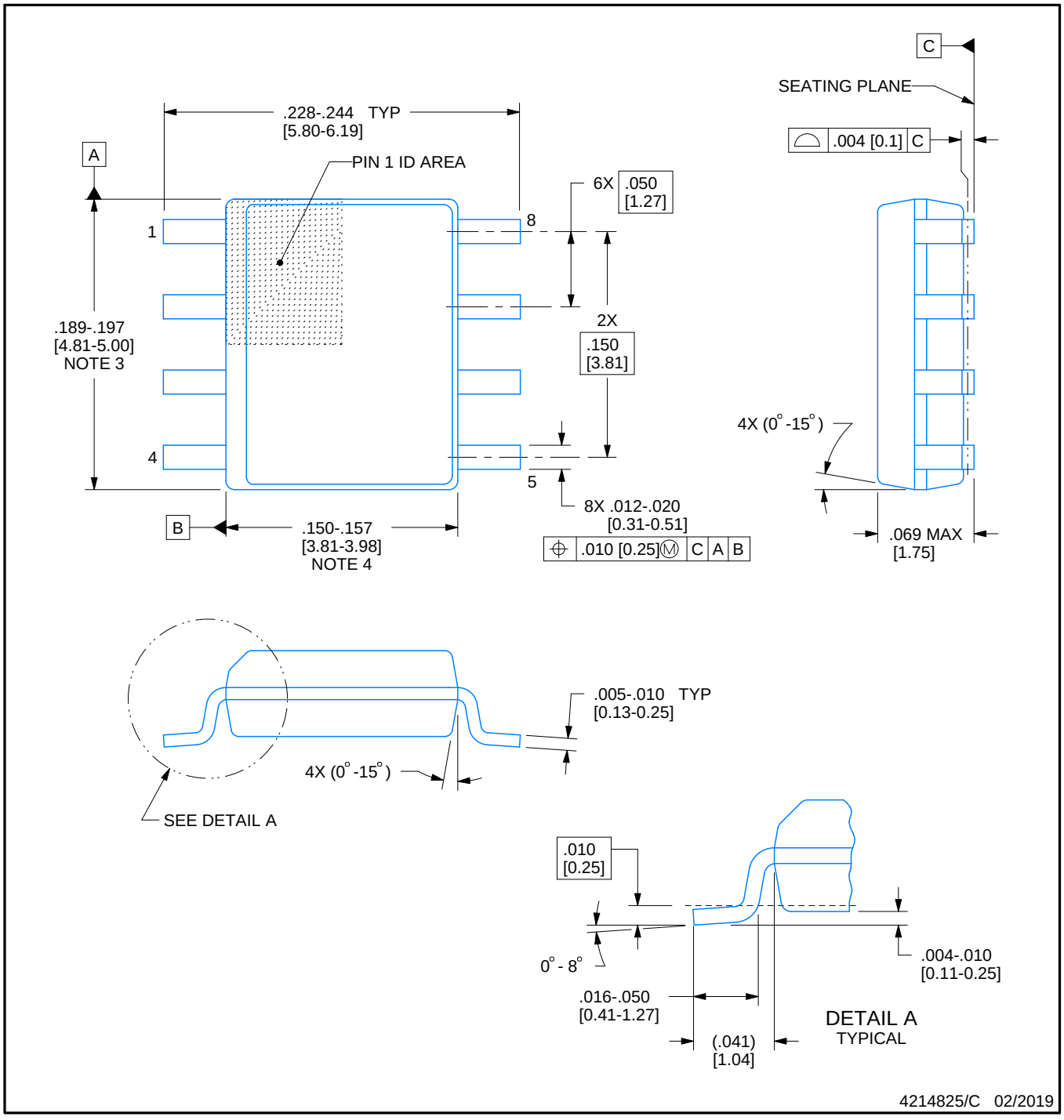


PACKAGE OUTLINE

D0008A

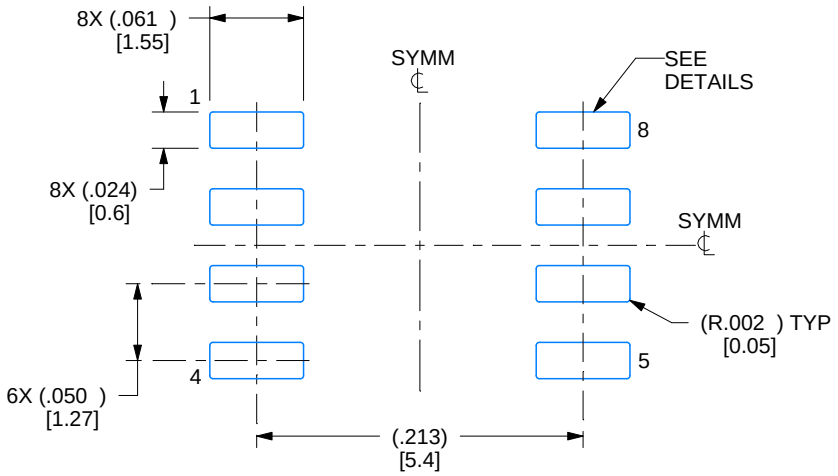
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

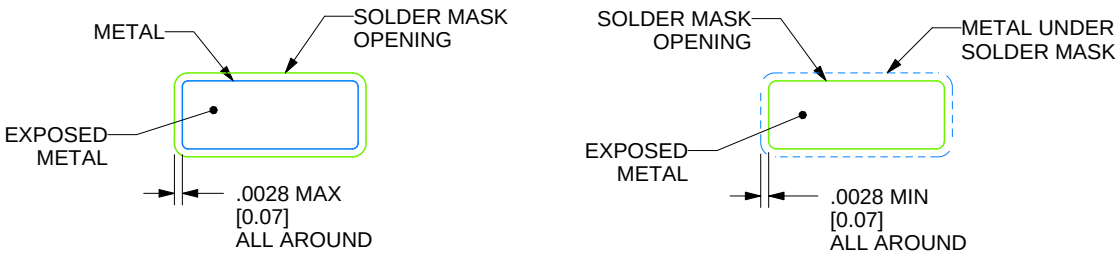


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

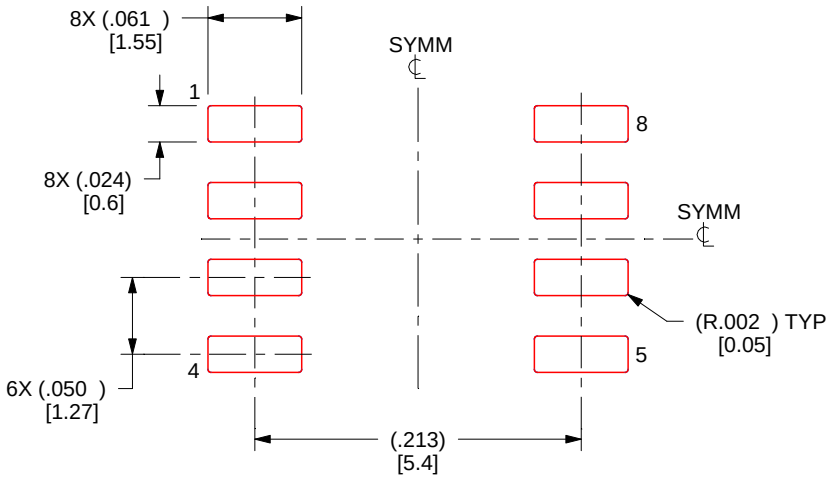
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

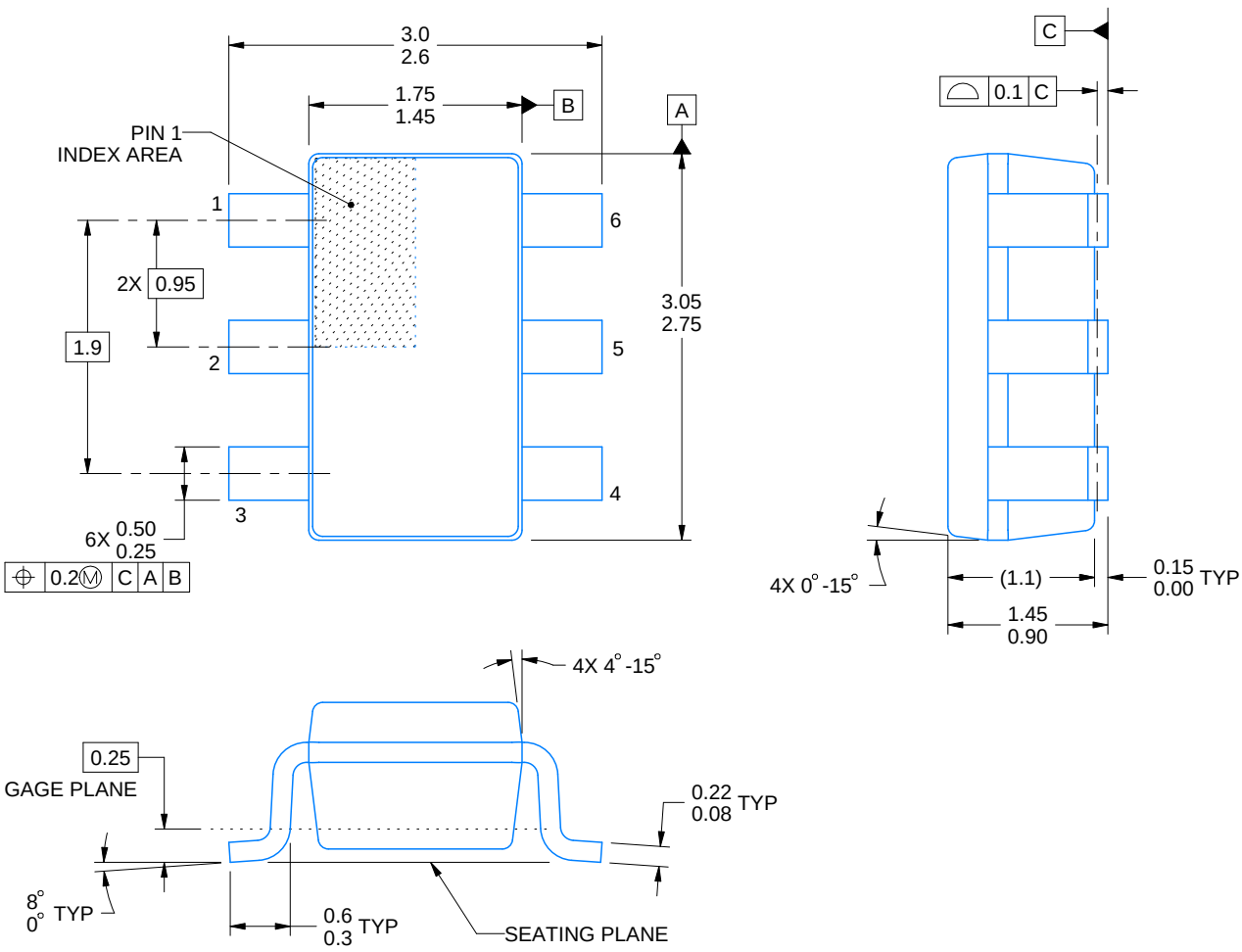
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

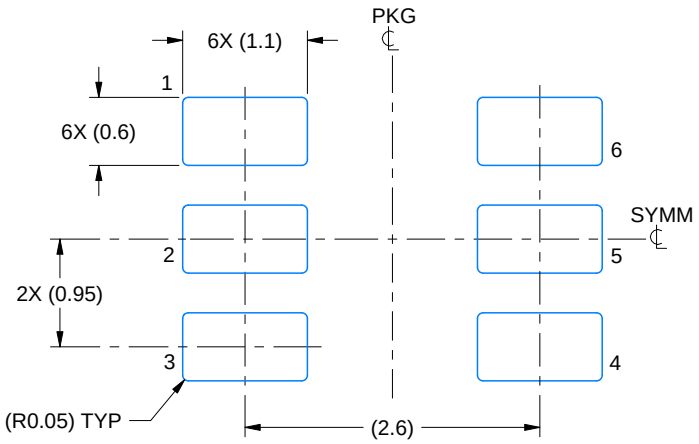
SMALL OUTLINE TRANSISTOR



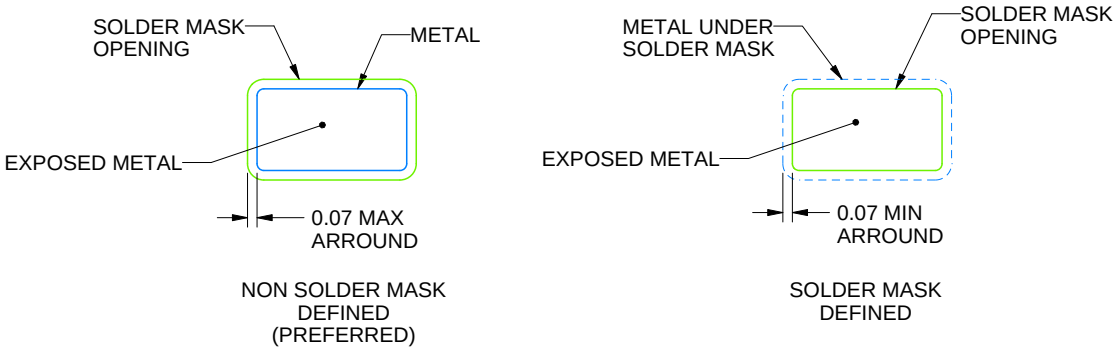
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

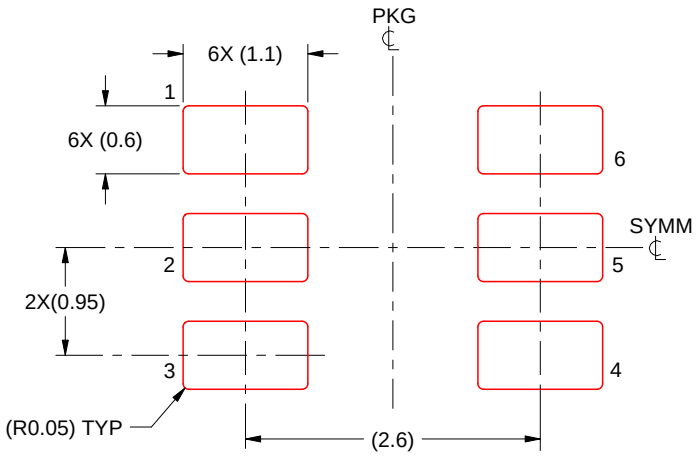


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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